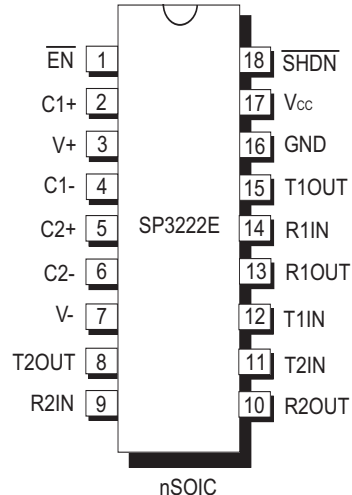


True +3.0V to +5.5V RS-232 Transceivers

FEATURES

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Minimum 120kbps Data Rate Under Full Load
- 1 μ A Low Power Shutdown with Receivers active (**SP3222E**)
- Interoperable with RS-232 down to a +2.7V power source
- Enhanced ESD Specifications:
 - +15kV Human Body Model
 - +15kV IEC61000-4-2 Air Discharge
 - +8kV IEC61000-4-2 Contact Discharge



nSOIC

Now Available in Lead Free Packaging

Note: See page 6 for other pinouts

DESCRIPTION

The **SP3222E/SP3232E** series is an RS-232 transceiver solution intended for portable or hand-held applications such as notebook or palmtop computers. The **SP3222E/SP3232E** series has a high-efficiency, charge-pump power supply that requires only 0.1 μ F capacitors in 3.3V operation. This charge pump allows the **SP3222E/SP3232E** series to deliver true RS-232 performance from a single power supply ranging from +3.0V to +5.5V. The **SP3222E/SP3232E** are 2-driver/2-receiver devices. This series is ideal for portable or hand-held applications such as notebook or palmtop computers. The ESD tolerance of the **SP3222E/SP3232E** devices are over +/-15kV for both Human Body Model and IEC61000-4-2 Air discharge test methods. The **SP3222E** device has a low-power shutdown mode where the devices' driver outputs and charge pumps are disabled. During shutdown, the supply current falls to less than 1 μ A.

SELECTION TABLE

MODEL	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	Shutdown	TTL 3-State	# of Pins
SP3222E	+3.0V to +5.5V	2	2	4 Capacitors	Yes	Yes	18, 20
SP3232E	+3.0V to +5.5V	2	2	4 Capacitors	No	No	16

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}-0.3V to +6.0V
 $V+$ (NOTE 1).....-0.3V to +7.0V
 $V-$ (NOTE 1).....+0.3V to -7.0V
 $V+ + |V-|$ (NOTE 1).....+13V
 I_{CC} (DC V_{CC} or GND current)..... ± 100 mA

Input Voltages

$TxIN$, \overline{EN} , \overline{SHDN}-0.3V to $V_{CC} + 0.3$ V
 $RxIN$ ± 15 V

Output Voltages

$TxOUT$ ± 13.2 V
 $RxOUT$,-0.3V to ($V_{CC} + 0.3$ V)

Short-Circuit Duration

$TxOUT$Continuous
Storage Temperature.....-65°C to +150°C

Power Dissipation per package

20-pin SSOP (derate 9.25mW/°C above +70°C).....750mW
18-pin SOIC (derate 15.7mW/°C above +70°C).....1260mW
20-pin TSSOP (derate 11.1mW/°C above +70°C).....890mW
16-pin SSOP (derate 9.69mW/°C above +70°C).....775mW
16-pin PDIP (derate 14.3mW/°C above +70°C).....1150mW
16-pin Wide SOIC (derate 11.2mW/°C above +70°C).....900mW
16-pin TSSOP (derate 10.5mW/°C above +70°C).....850mW
16-pin nSOIC (derate 13.57mW/°C above +70°C).....1086mW

NOTE 1: $V+$ and $V-$ can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for $V_{CC} = +3.0$ V to +5.5V with $T_{AMB} = T_{MIN}$ to T_{MAX} .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current		0.3	1.0	mA	no load, $V_{CC} = 3.3$ V, $T_{AMB} = 25^\circ\text{C}$, $TxIN = \text{GND}$ or V_{CC}
Shutdown Supply Current		1.0	10	μA	$\overline{SHDN} = \text{GND}$, $V_{CC} = 3.3$ V, $T_{AMB} = 25^\circ\text{C}$, $TxIN = V_{CC}$ or GND
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW			0.8	V	$TxIN$, \overline{EN} , \overline{SHDN} , Note 2
Input Logic Threshold HIGH	2.0		V_{CC}	V	$V_{CC} = 3.3$ V, Note 2
Input Logic Threshold HIGH	2.4		V_{CC}	V	$V_{CC} = 5.0$ V, Note 2
Input Leakage Current		± 0.01	± 1.0	μA	$TxIN$, \overline{EN} , \overline{SHDN} , $T_{AMB} = +25^\circ\text{C}$, $V_{IN} = 0$ V to V_{CC}
Output Leakage Current		± 0.05	± 10	μA	Receivers disabled, $V_{OUT} = 0$ V to V_{CC}
Output Voltage LOW			0.4	V	$I_{OUT} = 1.6$ mA
Output Voltage HIGH	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V	$I_{OUT} = -1.0$ mA
DRIVER OUTPUTS					
Output Voltage Swing	± 5.0	± 5.4		V	All driver outputs loaded with 3k Ω to GND, $T_{AMB} = +25^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for $V_{CC} = +3.0V$ to $+5.5V$ with $T_{AMB} = T_{MIN}$ to T_{MAX} . Typical values apply at $V_{CC} = +3.3V$ or $+5.0V$ and $T_{AMB} = 25^{\circ}C$.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER OUTPUTS (continued)					
Output Resistance	300			Ω	$V_{CC} = V+ = V- = 0V$, $T_{OUT} = \pm 2V$
Output Short-Circuit Current		± 35	± 60	mA	$V_{OUT} = 0V$
Output Leakage Current			± 25	μA	$V_{CC} = 0V$ or $3.0V$ to $5.5V$, $V_{OUT} = \pm 12V$, Drivers disabled
RECEIVER INPUTS					
Input Voltage Range	-15		+15	V	
Input Threshold LOW	0.6	1.2		V	$V_{CC} = 3.3V$
Input Threshold LOW	0.8	1.5		V	$V_{CC} = 5.0V$
Input Threshold HIGH		1.5	2.4	V	$V_{CC} = 3.3V$
Input Threshold HIGH		1.8	2.4	V	$V_{CC} = 5.0V$
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	k Ω	
TIMING CHARACTERISTICS					
Maximum Data Rate	120	235		kbps	$R_L = 3k\Omega$, $C_L = 1000pF$, one driver switching
Driver Propagation Delay, t_{PHL}		1.0		μs	$R_L = 3k\Omega$, $C_L = 1000pF$
Driver Propagation Delay, t_{PLH}		1.0		μs	$R_L = 3k\Omega$, $C_L = 1000pF$
Receiver Propagation Delay, t_{PHL}		0.3		μs	Receiver input to Receiver output, $C_L = 150pF$
Receiver Propagation Delay, t_{PLH}		0.3		μs	Receiver input to Receiver output, $C_L = 150pF$
Receiver Output Enable Time		200		ns	
Receiver Output Disable Time		200		ns	
Driver Skew		100	500	ns	$ t_{PHL} - t_{PLH} $, $T_{AMB} = 25^{\circ}C$
Receiver Skew		200	1000	ns	$ t_{PHL} - t_{PLH} $
Transition-Region Slew Rate			30	V/ μs	$V_{CC} = 3.3V$, $R_L = 3k\Omega$, $C_L = 1000pF$, $T_{AMB} = 25^{\circ}C$, measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$

NOTE 2: Driver input hysteresis is typically 250mV.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for $V_{CC} = +3.3V$, 120kbps data rate, all drivers loaded with 3k Ω , 0.1 μF charge pump capacitors, and $T_{AMB} = +25^{\circ}C$.

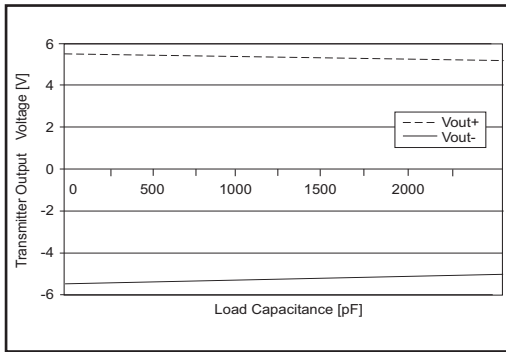


Figure 1. Transmitter Output Voltage vs Load Capacitance for the SP3222E and SP3232E

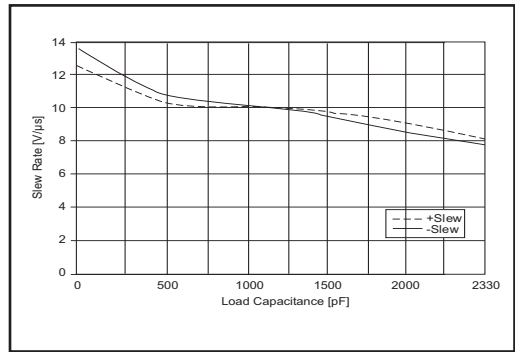


Figure 2. Slew Rate vs Load Capacitance for the SP3222E and SP3232E

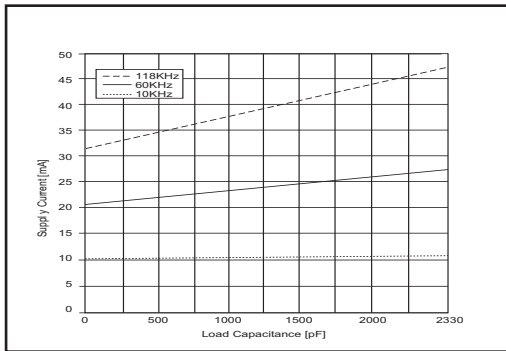


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data

NAME	FUNCTION	PIN NUMBER		
		SP3222E		SP3232E
		SOIC	SSOP TSSOP	
$\overline{\text{EN}}$	Receiver Enable. Apply Logic LOW for normal operation. Apply logic HIGH to disable the receiver outputs (high-Z state)	1	1	-
C1+	Positive terminal of the voltage doubler charge-pump capacitor	2	2	1
V+	+5.5V output generated by the charge pump	3	3	2
C1-	Negative terminal of the voltage doubler charge-pump capacitor	4	4	3
C2+	Positive terminal of the inverting charge-pump capacitor	5	5	4
C2-	Negative terminal of the inverting charge-pump capacitor	6	6	5
V-	-5.5V output generated by the charge pump	7	7	6
T ₁ OUT	RS-232 driver output.	15	17	14
T ₂ OUT	RS-232 driver output.	8	8	7
R ₁ IN	RS-232 receiver input	14	16	13
R ₂ IN	RS-232 receiver input	9	9	8
R ₁ OUT	TTL/CMOS receiver output	13	15	12
R ₂ OUT	TTL/CMOS receiver output	10	10	9
T ₁ IN	TTL/CMOS driver input	12	13	11
T ₂ IN	TTL/CMOS driver input	11	12	10
GND	Ground	16	18	15
V _{cc}	+3.0V to +5.5V supply voltage	17	19	16
$\overline{\text{SHDN}}$	Shutdown Control Input. Drive HIGH for normal device operation. Drive LOW to shutdown the drivers (high-Z output) and the on-board power supply	18	20	-
N.C.	No Connect	-	11, 14	-

Table 1. Device Pin Description

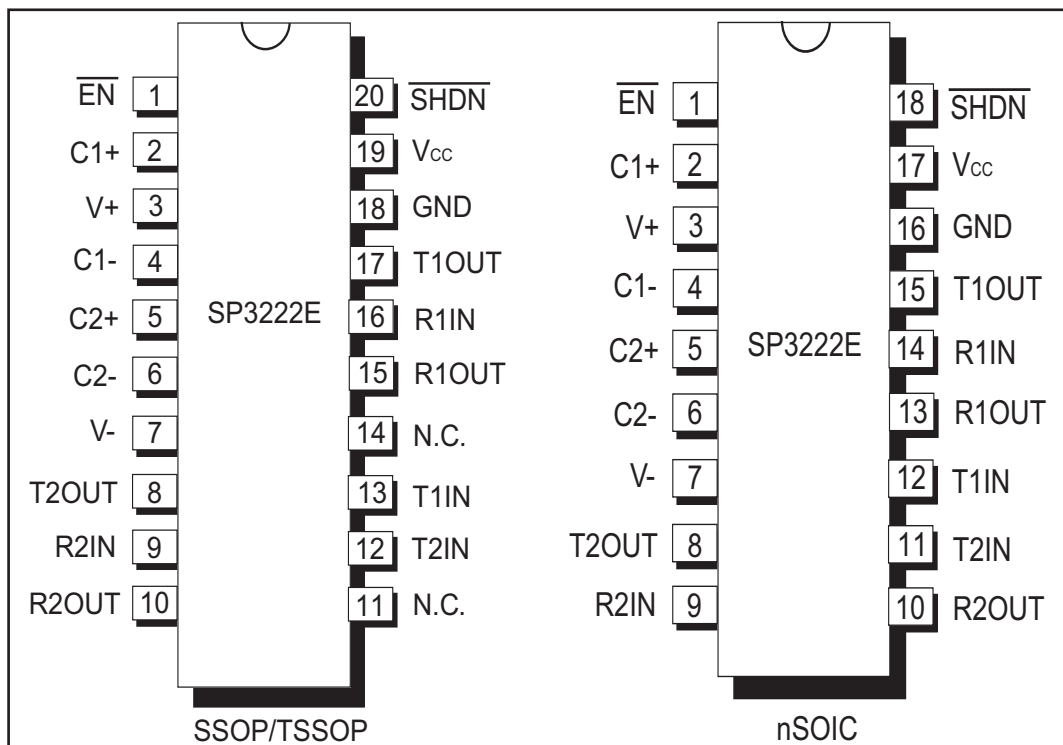


Figure 4. Pinout Configurations for the SP3222E

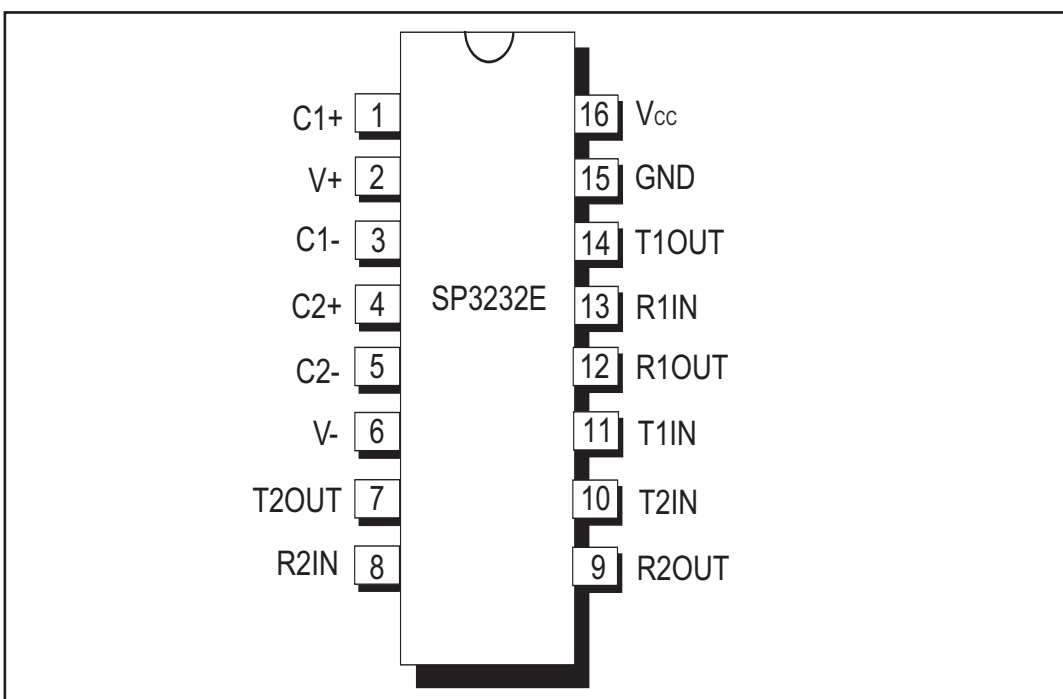


Figure 5. Pinout Configuration for the SP3232E

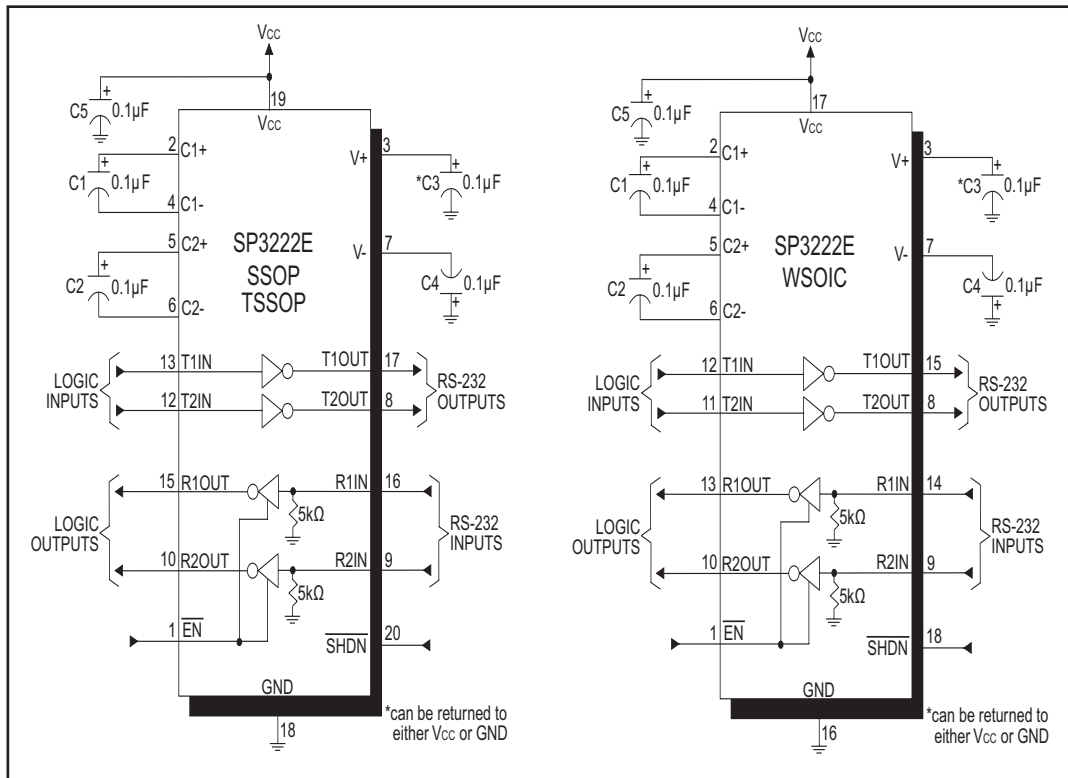


Figure 6. SP3222E Typical Operating Circuits

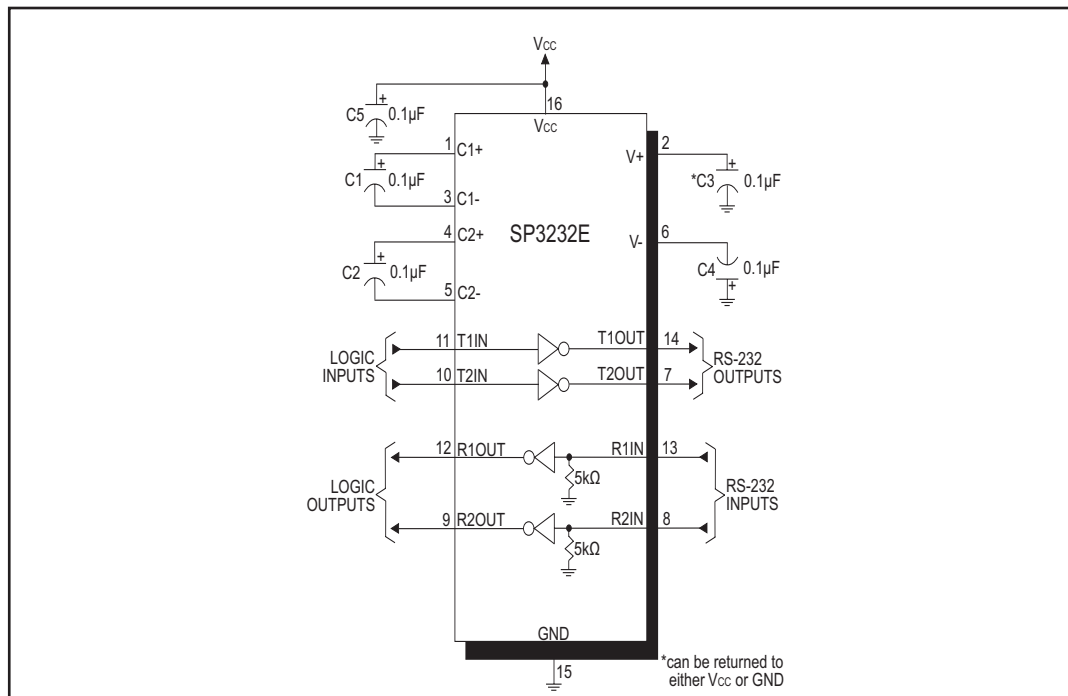


Figure 7. SP3232E Typical Operating Circuit

The **SP3222E/SP3232E** transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The **SP3222E/SP3232E** devices feature **Exar's** proprietary on-board charge pump circuitry that generates $\pm 5.5\text{V}$ for RS-232 voltage levels from a single $+3.0\text{V}$ to $+5.5\text{V}$ power supply. This series is ideal for $+3.3\text{V}$ -only systems, mixed $+3.3\text{V}$ to $+5.5\text{V}$ systems, or $+5.0\text{V}$ -only systems that require true RS-232 performance. The **SP3222E/SP3232E** devices can operate at a typical data rate of 235kbps when fully loaded.

The **SP3222E** and **SP3232E** are 2-driver/2-receiver devices ideal for portable or hand-held applications. The **SP3222E** features a $1\mu\text{A}$ shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only $1\mu\text{A}$ supply current.

THEORY OF OPERATION

The **SP3222E/SP3232E** series is made up of three basic circuit blocks:

1. Drivers
2. Receivers
3. The Exar proprietary charge pump

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to $\pm 5.0\text{V}$ EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is $\pm 5.4\text{V}$ with no load and $\pm 5\text{V}$ minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. Driver outputs will meet EIA/TIA-562 levels of $\pm 3.7\text{V}$ with supply voltages as low as 2.7V .

The drivers can guarantee a data rate of 120kbps fully loaded with $3\text{k}\Omega$ in parallel with 1000pF , ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver is internally limited to a maximum of $30\text{V}/\mu\text{s}$ in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meet the monotonicity requirements of the standard.

Figure 8 shows a loopback test circuit used to test the RS-232 Drivers. Figure 9 shows the test results of the loopback circuit with all drivers active at 120kbps with RS-232 loads in parallel with a 1000pF capacitor. Figure 10 shows the test results where one driver was active at 235kbps and all drivers loaded with an RS-232 receiver in parallel with 1000pF capacitors. A solid RS-232 data transmission rate of 120kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

The **SP3222E** driver's output stages are turned off (tri-state) when the device is in shutdown mode. When the power is off, the **SP3222E** device permits the outputs to be driven up to $\pm 12\text{V}$. The driver's inputs do not have pull-up resistors. Designers should connect unused inputs to V_{CC} or GND.

In the shutdown mode, the supply current falls to less than $1\mu\text{A}$, where $\overline{\text{SHDN}} = \text{LOW}$. When the **SP3222E** device is shut down, the device's driver outputs are disabled (tri-stated) and the charge pumps are turned off with V_{+} pulled down to V_{CC} and V_{-} pulled to GND. The time required to exit shutdown is typically $100\mu\text{s}$. Connect $\overline{\text{SHDN}}$ to V_{CC} if the shutdown mode is not used.

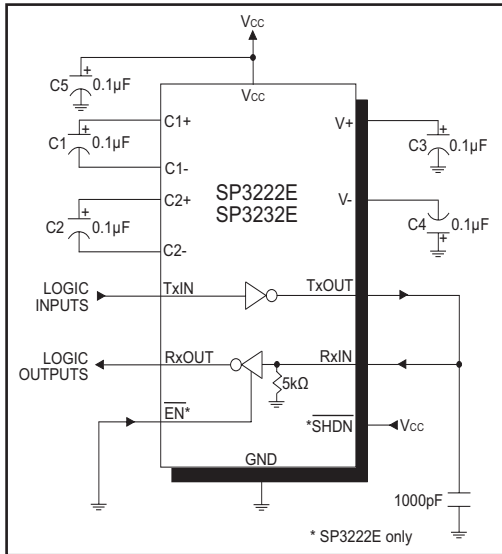


Figure 8. SP3222E/SP3232E Driver Loopback Test Circuit

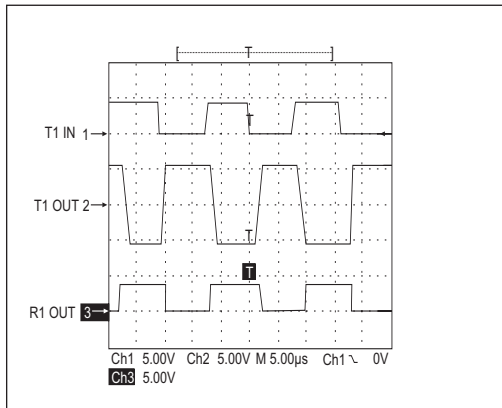


Figure 9. Loopback Test results at 120kbps

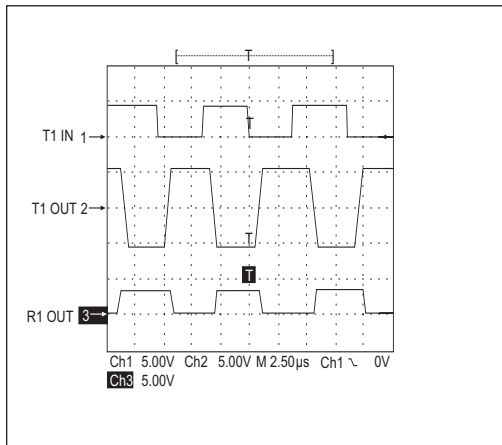


Figure 10. Loopback Test results at 235kbps

Receivers

The Receivers convert EIA/TIA-232 levels to TTL or CMOS logic output levels. The **SP3222E** receivers have an inverting tri-state output. These receiver outputs (RxOUT) are tri-stated when the enable control $\overline{\text{EN}}$ = HIGH. In the shutdown mode, the receivers can be active or inactive. $\overline{\text{EN}}$ has no effect on TxOUT. The truth table logic of the **SP3222E** driver and receiver outputs can be found in Table 2.

$\overline{\text{SHDN}}$	$\overline{\text{EN}}$	TxOUT	RxOUT
0	0	Tri-state	Active
0	1	Tri-state	Tri-state
1	0	Active	Active
1	1	Active	Tri-state

Table 2. SP3222E Truth Table Logic for Shutdown and Enable Control

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is an Exar-patented design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages of $\pm 5.5\text{V}$ regardless of the input voltage (V_{cc}) over the +3.0V to +5.5V range.

In most circumstances, decoupling the power supply can be achieved adequately using a 0.1 μ F bypass capacitor at C5 (refer to figures 6 and 7). In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as charge-pump capacitor C1. Physically connect bypass capacitors as close to the IC as possible.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C₁ and C₂ are initially charged to V_{CC}. C₁⁺ is then switched to GND and the charge in C₁⁻ is transferred to C₂⁻. Since C₂⁺ is connected to V_{CC}, the voltage potential across capacitor C₂ is now 2 times V_{CC}.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C₂ to the V_{SS} storage capacitor and the positive terminal of C₂ to GND. This transfers a negative generated voltage to C₃. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C₃, the positive side of capacitor C₁ is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C₁ produces -V_{CC} in the negative terminal of C₁, which is applied to the negative side of capacitor C₂. Since C₂⁺ is at V_{CC}, the voltage potential across C₂ is 2 times V_{CC}.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C₂ to GND, and transfers this positive generated voltage across C₂ to C₄, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C₄, the positive side of capacitor C₁ is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V⁺ and V⁻ are separately generated from V_{CC}, in a no-load condition V⁺ and V⁻ will be symmetrical. Older charge pump approaches that generate V⁻ from V⁺ will show a decrease in the magnitude of V⁻ compared to V⁺ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at greater than 250kHz. The external capacitors can be as low as 0.1 μ F with a 16V breakdown voltage rating.

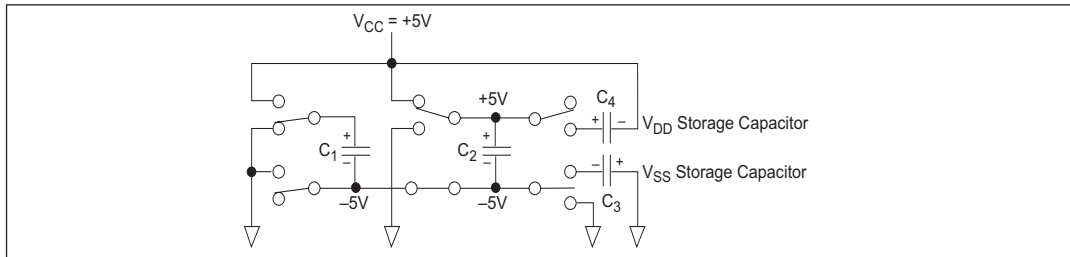


Figure 11. Charge Pump — Phase 1

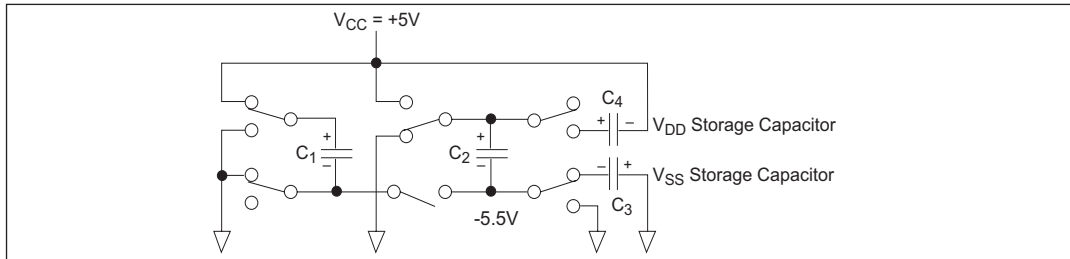


Figure 12. Charge Pump — Phase 2

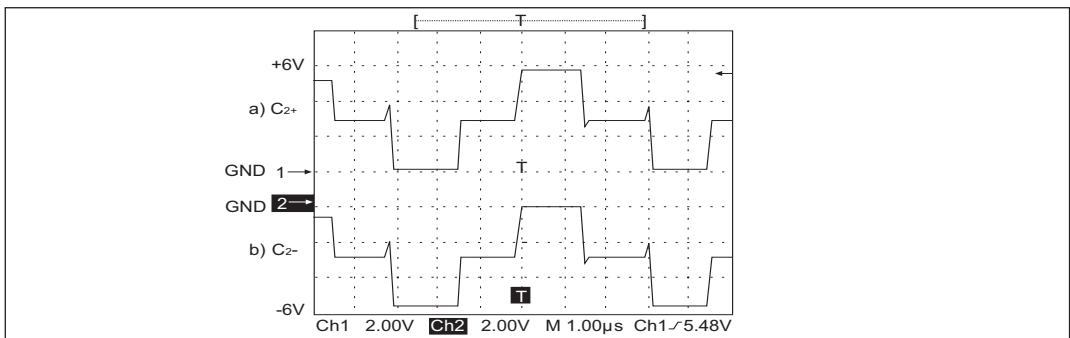


Figure 13. Charge Pump Waveforms

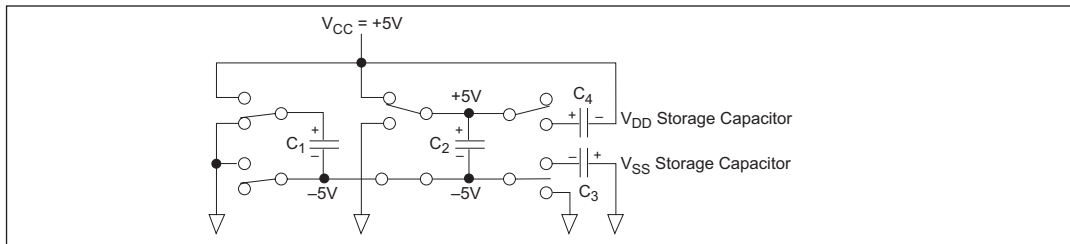


Figure 14. Charge Pump — Phase 3

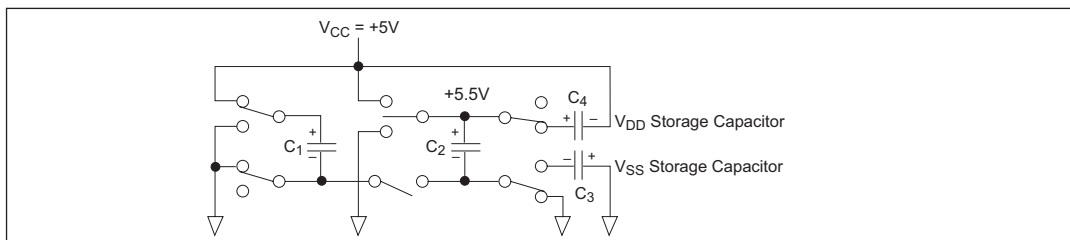


Figure 15. Charge Pump — Phase 4

ESD TOLERANCE

The **SP3222E/SP3232E** series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least $\pm 15\text{kV}$ without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC61000-4-2 Air-Discharge
- c) IEC61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semi-conductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 16. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC61000-4-2 is that

the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC61000-4-2 is shown on Figure 17. There are two methods within IEC61000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the

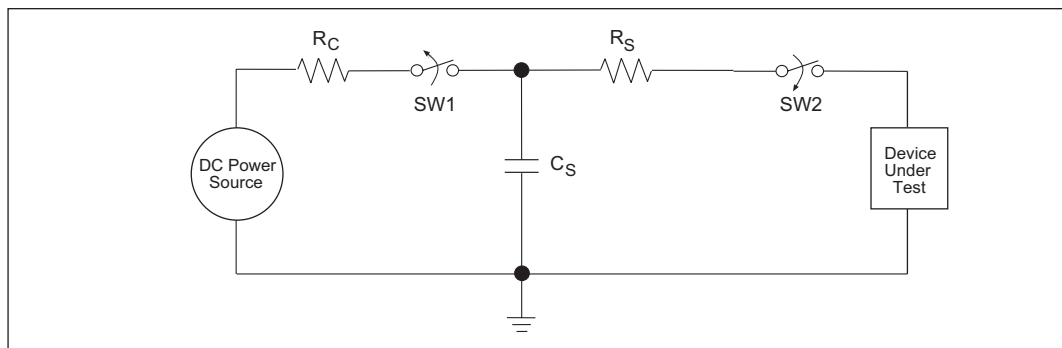


Figure 16. ESD Test Circuit for Human Body Model

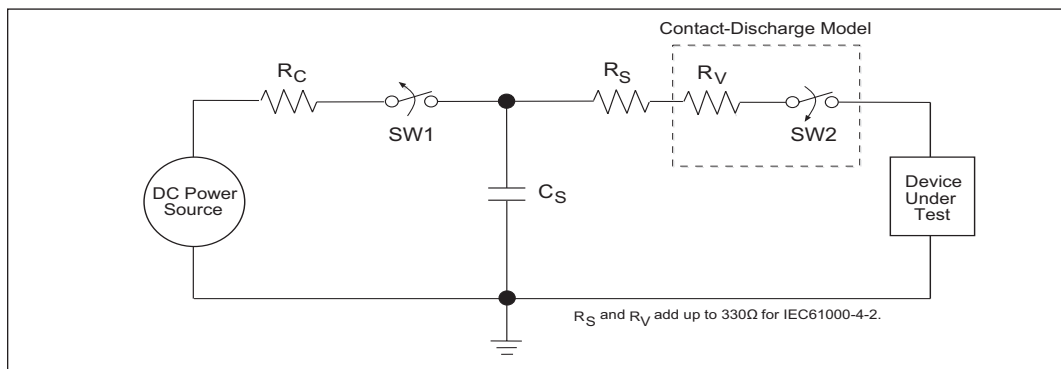


Figure 17. ESD Test Circuit for IEC61000-4-2

equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit models in Figures 16 and 17 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are $1.5k\Omega$ and $100pF$, respectively. For IEC-61000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω and $150pF$, respectively.

The higher C_S value and lower R_S value in the IEC61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

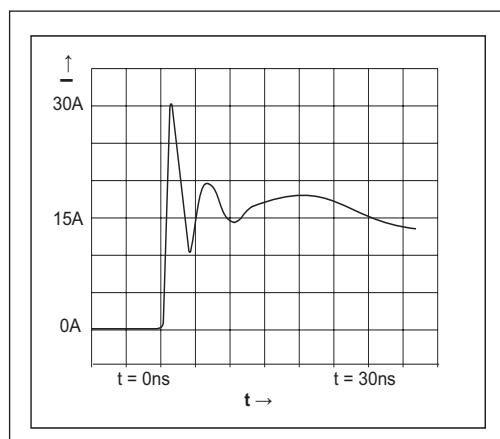
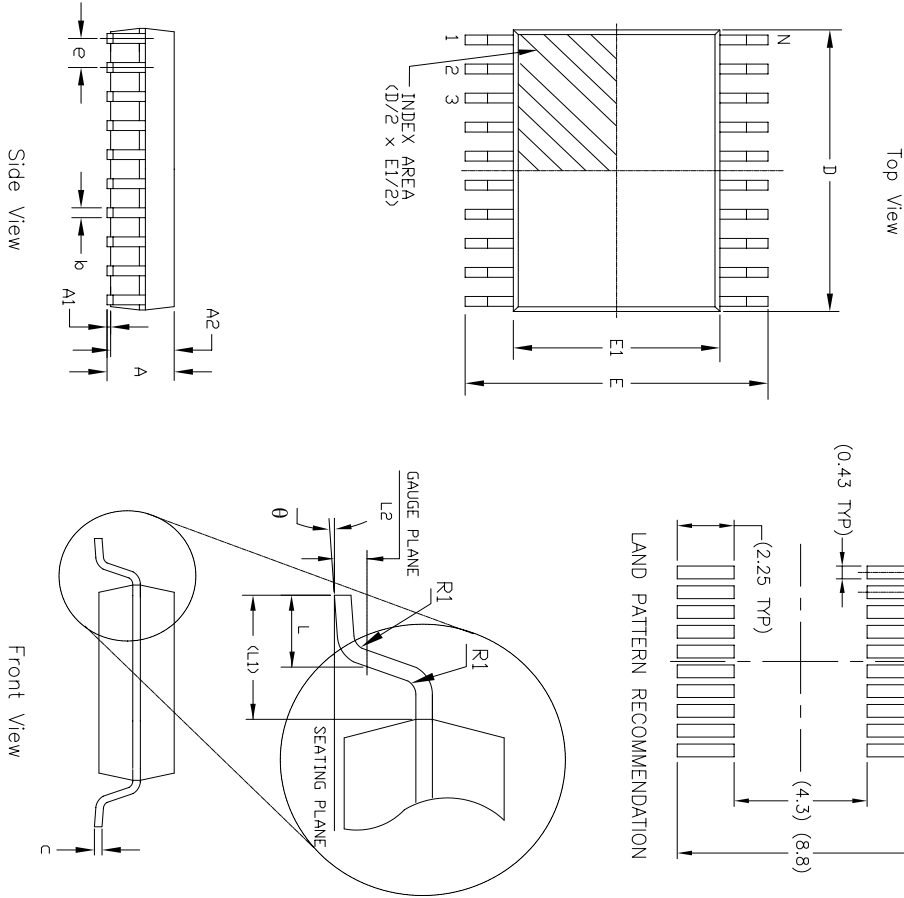


Figure 18. ESD Test Waveform for IEC61000-4-2


DEVICE PIN TESTED	HUMAN BODY MODEL	IEC61000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	$\pm 15kV$	$\pm 15kV$	$\pm 8kV$	4
Receiver Inputs	$\pm 15kV$	$\pm 15kV$	$\pm 8kV$	4

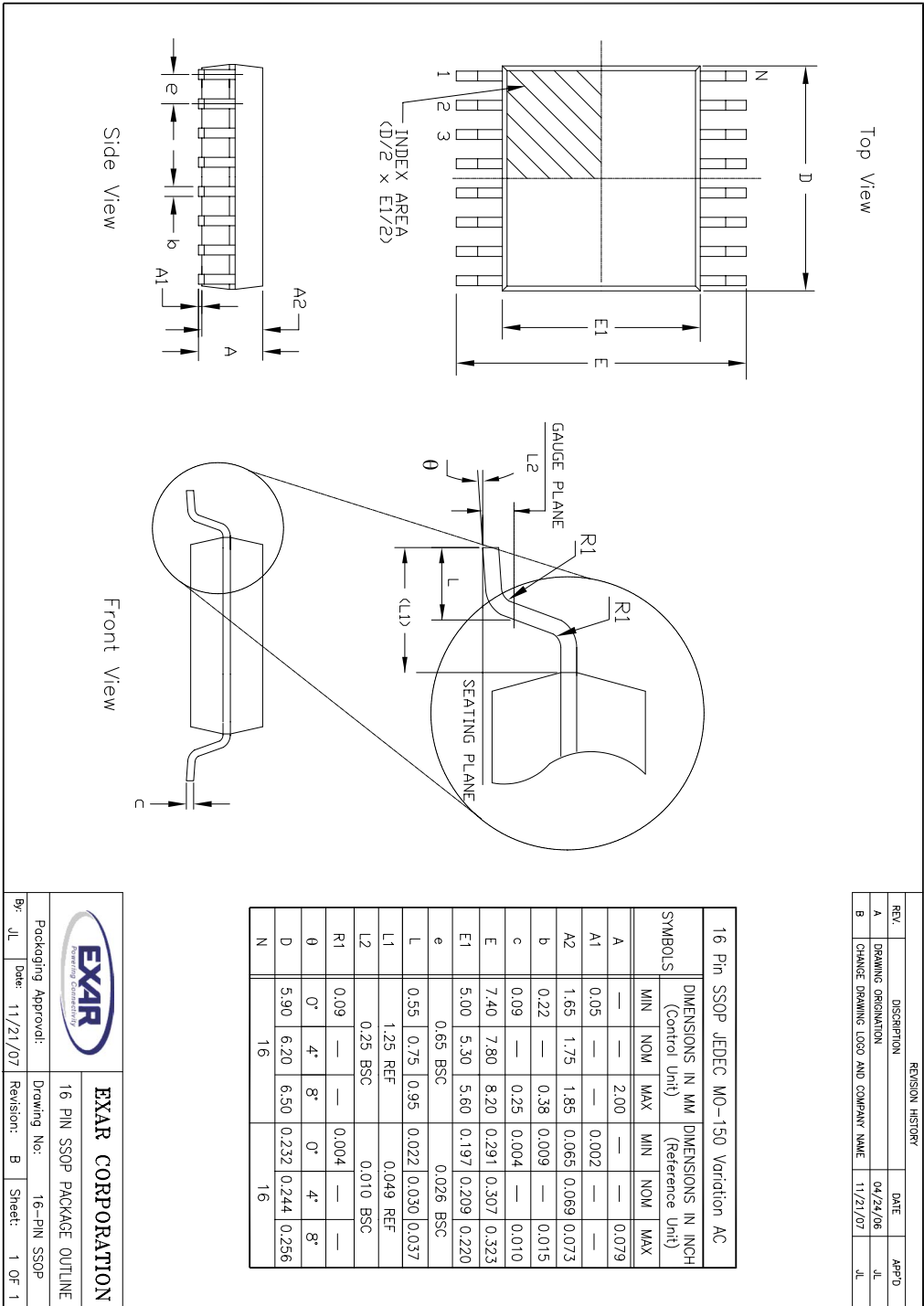
Table 3. Transceiver ESD Tolerance Levels

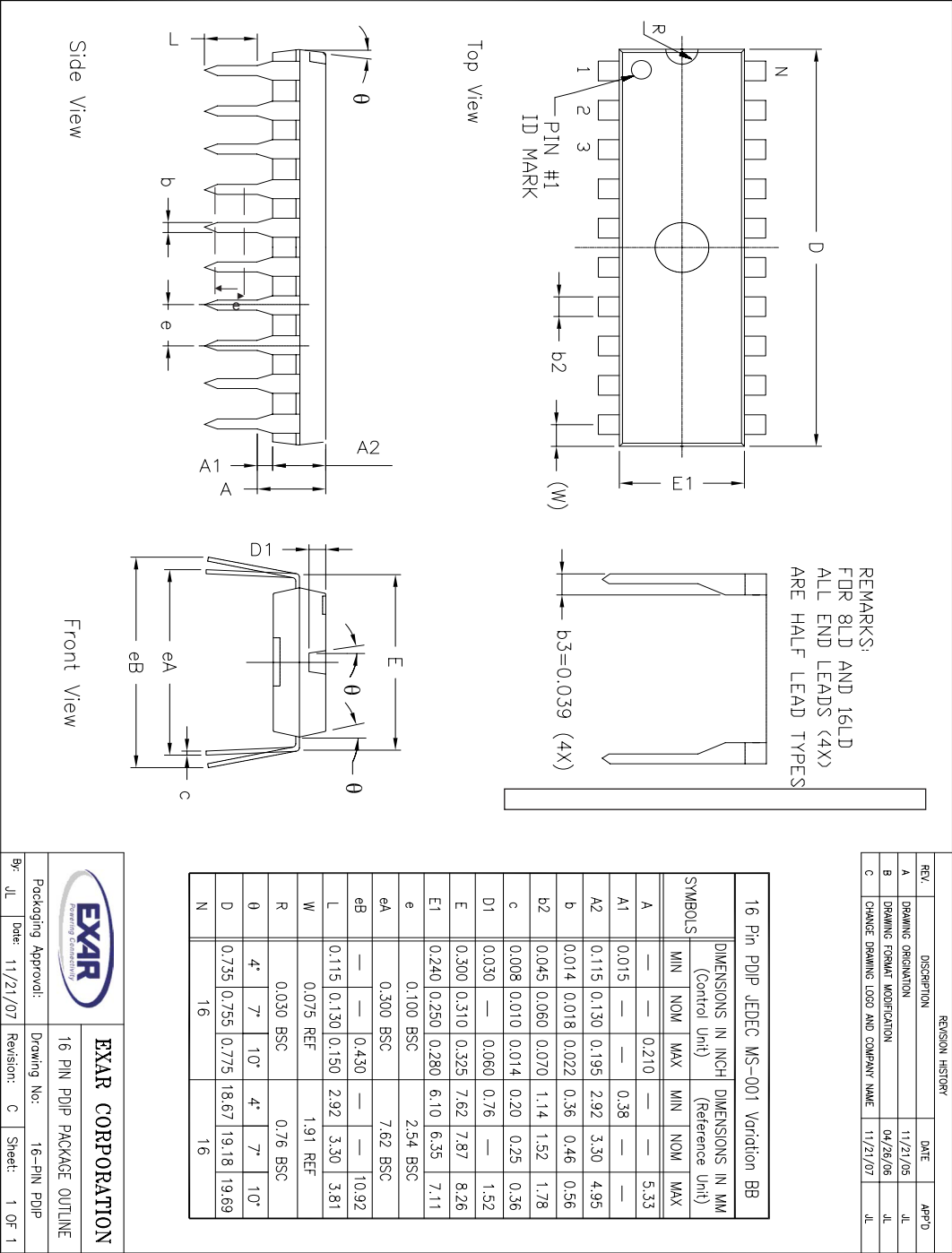


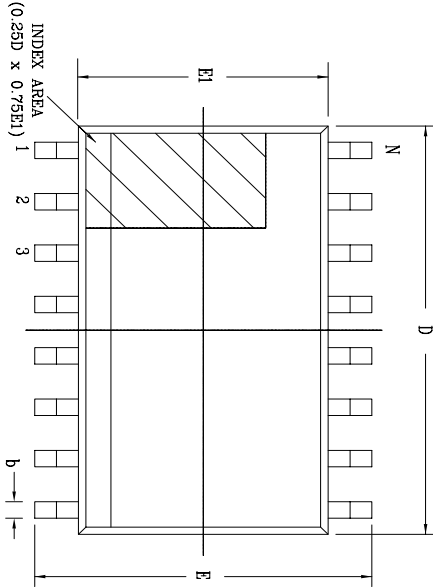
REVISION HISTORY				
REV.	DESCRIPTION	DATE	APP'D	
A	DRAWING ORIGINATOR	04/24/06	JL	
B	ADD LAND PATTERN RECOMMENDATION	07/25/07	JL	
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL	

20 Pin SSOP JEDEC MO-150 Variation AE									
SYMBOLS	DIMENSIONS IN MM (Control Unit)				DIMENSIONS IN INCH (Reference Unit)				
	MIN	NOM	MAX		MIN	NOM	MAX		
A	—	—	2.00	—	—	—	0.079	—	
A1	0.05	—	—	0.002	—	—	—	—	
A2	1.65	1.75	1.85	0.065	0.069	0.073	—	—	
b	0.22	—	0.38	0.009	—	0.015	—	—	
c	0.09	—	0.25	0.004	—	0.010	—	—	
E	7.40	7.80	8.20	0.291	0.307	0.323	—	—	
E1	5.00	5.30	5.60	0.197	0.209	0.220	—	—	
e	0.65 BSC				0.026 BSC				
L	0.55	0.75	0.95	0.022	0.030	0.037	—	—	
L1	1.25 REF				0.049 REF				
L2	0.25 BSC				0.010 BSC				
R1	0.09	—	—	0.004	—	—	—	—	
θ	0°	4°	8°	0°	4°	8°	—	—	
D	6.90	7.20	7.50	0.272	0.283	0.295	—	—	
N	20				20				

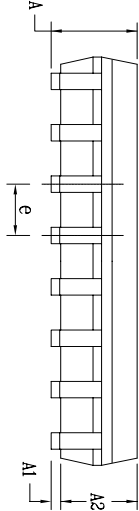
		EXAR CORPORATION	
		20 PIN SSOP PACKAGE OUTLINE	
Packaging Approval:	Drawing No:	20-PIN SSOP	
By: JL	Date: 11/21/07	Revision: C	Sheet: 1 OF 1



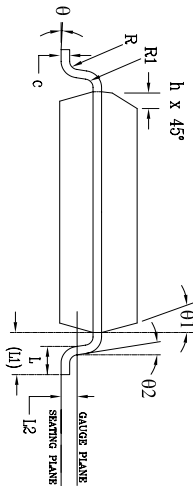




Top View




Side View



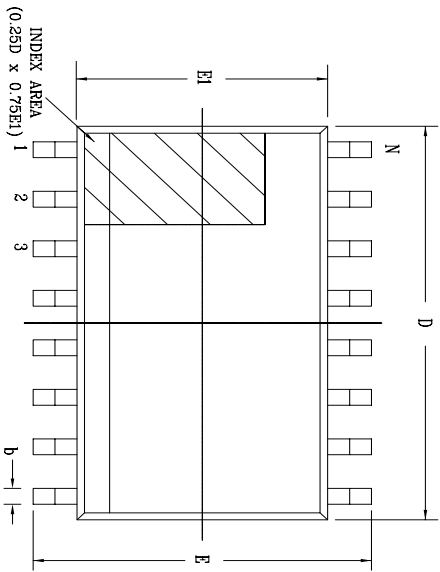
Front View

16 Pin SOICW		JEDEC MS-013		Variation AA		
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	—	2.65	0.093	—	0.104
A1	0.10	—	0.30	0.004	—	0.012
A2	2.05	—	2.55	0.081	—	0.100
b	0.31	—	0.51	0.012	—	0.020
c	0.20	—	0.33	0.008	—	0.013
E	10.30	BSC	—	0.406	BSC	—
E1	7.50	BSC	—	0.295	BSC	—
e	1.27	BSC	—	0.050	BSC	—
h	0.25	—	0.75	0.010	—	0.030
L	0.40	—	1.27	0.016	—	0.050
L1	1.40	REF	—	0.055	REF	—
L2	0.25	BSC	—	0.010	BSC	—
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	10.30	BSC	—	0.405	BSC	—
N	16	—	—	16	—	—

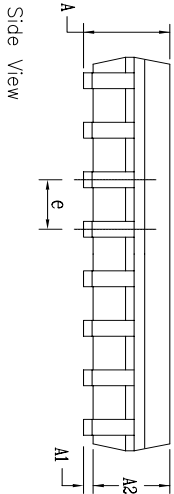
REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	11/05/05	JL
B	DRAWING FORMAT MODIFICATION	09/13/06	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

		EXAR CORPORATION	
Packaging Approval:		16 PIN SOICW PACKAGE OUTLINE	
By: JL	Date: 11/21/07	Drawing No: 16-PIN SOICW	Sheet: 1 OF 1

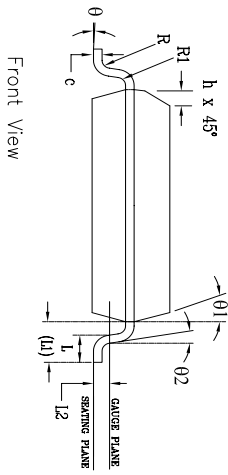
REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATOR	04/24/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL



Top View




Side View



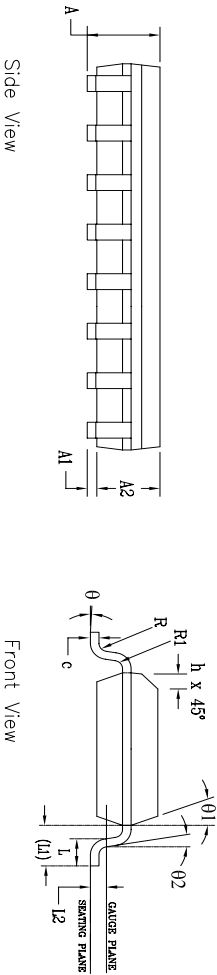
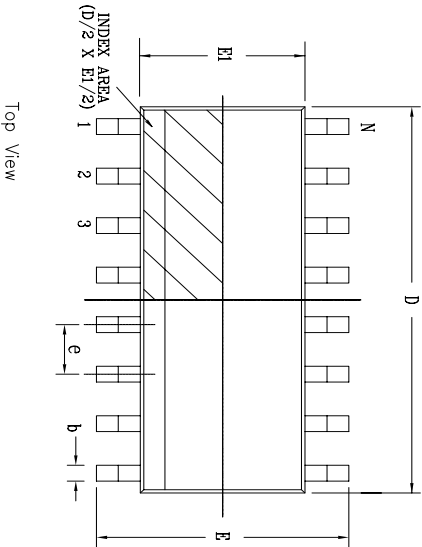
Front View


18 Pin SOICW JEDEC MS-013 Variation AB			
SYMBOLS	DIMENSIONS IN MM (Control Unit)		
	MIN	NOM	MAX
A	2.35	—	2.65
A1	0.10	—	0.30
A2	2.05	—	2.55
b	0.31	—	0.51
c	0.20	—	0.33
E	10.30	BSC	0.406 BSC
E1	7.50	BSC	0.295 BSC
e	1.27	BSC	0.050 BSC
h	0.25	—	0.75
L	0.40	—	1.27
L1	1.40	REF	0.055 REF
L2	0.25	BSC	0.010 BSC
R	0.07	—	0.003
R1	0.07	—	0.003
θ	0°	—	8°
θ1	5°	—	15°
θ2	0°	—	0°
D	11.55	BSC	0.455 BSC
N	18		18

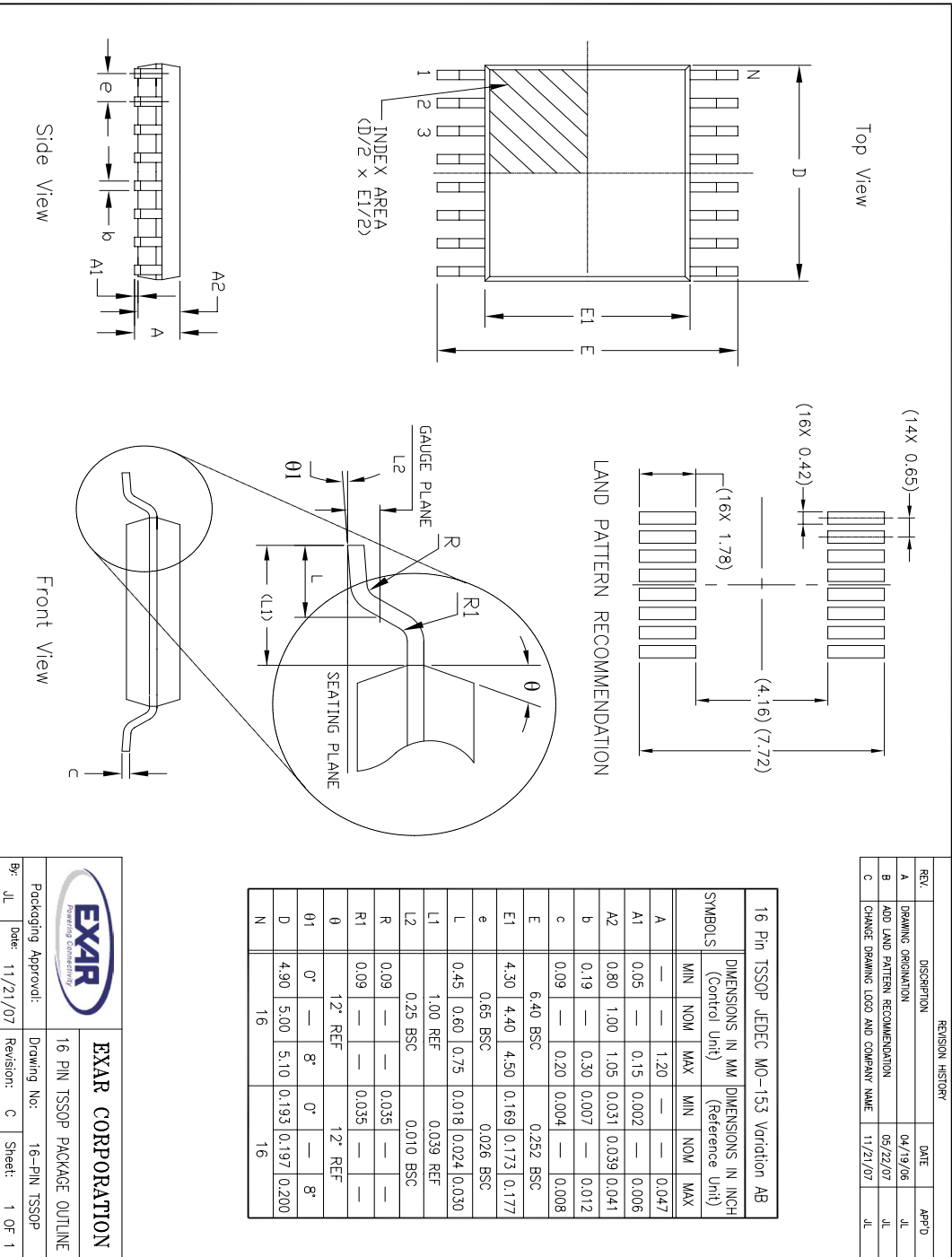
			
Packaging Approval:		Drawing No:	
By: JL		Date: 11/21/07	
Revision: B		Sheet: 1 OF 1	

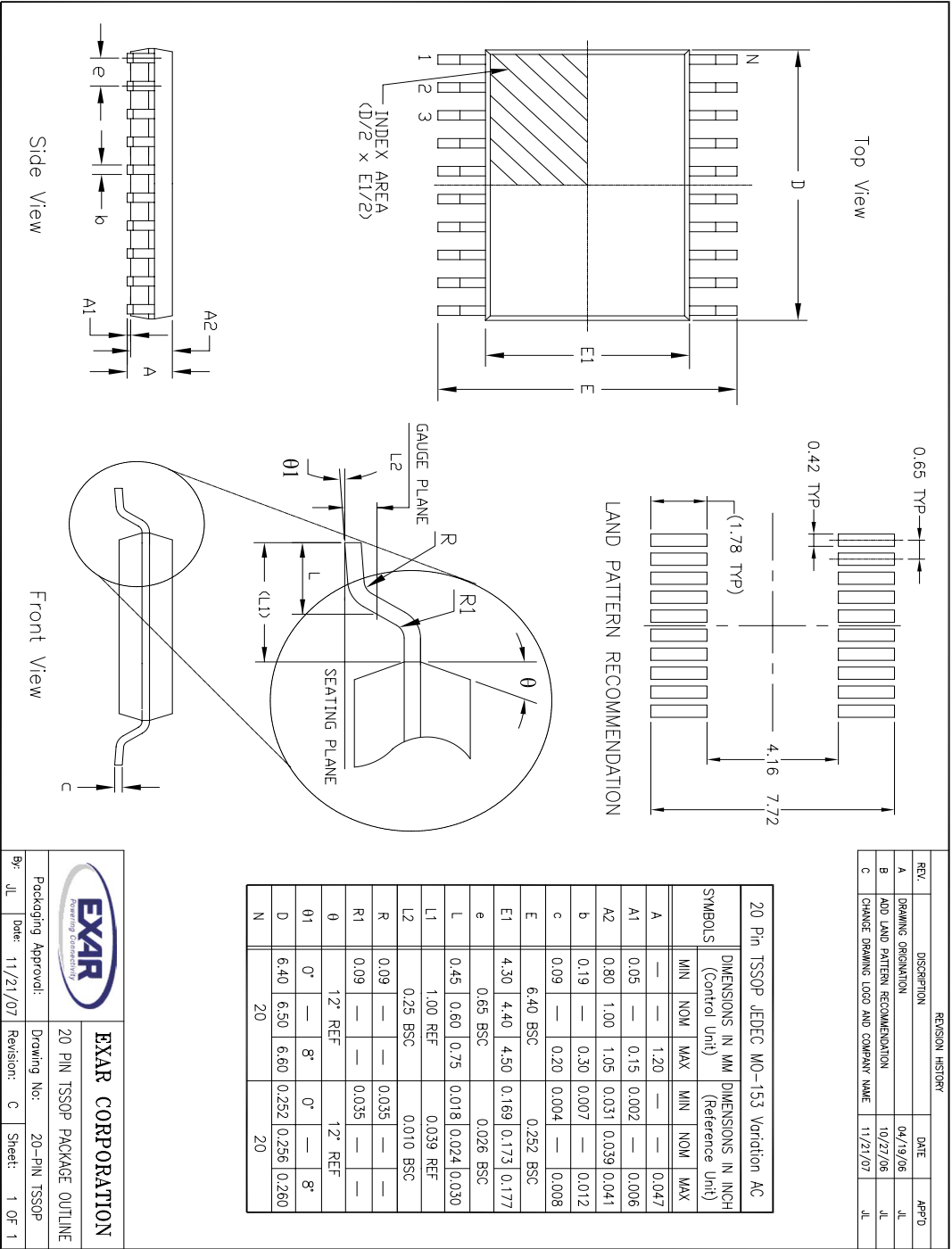
REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIENTATION	10/12/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

16 Pin SOICN		JEDEC MS-012		Variation AC	
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)	
	MIN	NOM	MAX	MIN	MAX
A	1.35	—	1.75	0.053	—
A1	0.10	—	0.25	0.004	—
A2	1.25	—	1.65	0.049	—
b	0.31	—	0.51	0.012	—
c	0.17	—	0.25	0.007	—
E	6.00 BSC			0.236 BSC	
E1	3.90 BSC			0.154 BSC	
e	1.27 BSC			0.050 BSC	
h	0.25	—	0.50	0.010	—
L	0.40	—	1.27	0.016	—
L1	1.04 REF			0.041 REF	
L2	0.25 BSC			0.010 BSC	
R	0.07	—	—	0.003	—
R1	0.07	—	—	0.003	—
θ	0°	—	8°	0°	—
θ1	5°	—	15°	5°	—
θ2	0°	—	—	0°	—
D	9.90 BSC			0.390 BSC	
N	16			16	



		EXAR CORPORATION	
Packaging Approval:		16 PIN SOICN PACKAGE OUTLINE	
By: JL	Date: 11/21/07	Drawing No: 16-PIN SOICN	Revision: C
		Sheet: 1 OF 1	





ORDERING INFORMATION

Part Number	Temp. Range	Package
SP3222ECA-L	0°C to +70°C	20 Pin SSOP
SP3222ECA-L/TR	0°C to +70°C	20 Pin SSOP
SP3222ECT-L	0°C to +70°C	18 Pin WSOIC
SP3222ECT-L/TR	0°C to +70°C	18 Pin WSOIC
SP3222ECY-L	0°C to +70°C	20 Pin TSSOP
SP3222ECY-L/TR	0°C to +70°C	20 Pin TSSOP
SP3222EEA-L	-40°C to +85°C	20 Pin SSOP
SP3222EEA-L/TR	-40°C to +85°C	20 Pin SSOP
SP3222EET-L	-40°C to +85°C	18 Pin WSOIC
SP3222EET-L/TR	-40°C to +85°C	18 Pin WSOIC
SP3222EEY-L	-40°C to +85°C	20 Pin TSSOP
SP3222EEY-L/TR	-40°C to +85°C	20 Pin TSSOP

Part Number	Temp. Range	Package
SP3232ECA-L	0°C to +70°C	16 Pin SSOP
SP3232ECA-L/TR	0°C to +70°C	16 Pin SSOP
SP3232ECN-L	0°C to +70°C	16 Pin NSOIC
SP3232ECN-L/TR	0°C to +70°C	16 Pin NSOIC
SP3232ECP-L	0°C to +70°C	16 Pin PDIP
SP3232ECT-L	0°C to +70°C	16 Pin WSOIC
SP3232ECT-L/TR	0°C to +70°C	16 Pin WSOIC
SP3232ECY-L	0°C to +70°C	16 Pin TSSOP
SP3232ECY-L/TR	0°C to +70°C	16 Pin TSSOP
SP3232EEA-L	-40°C to +85°C	16 Pin SSOP
SP3232EEA-L/TR	-40°C to +85°C	16 Pin SSOP
SP3232EEN-L	-40°C to +85°C	16 Pin NSOIC
SP3232EEN-L/TR	-40°C to +85°C	16 Pin NSOIC
SP3232EEP-L	-40°C to +85°C	16 Pin PDIP
SP3232EET-L	-40°C to +85°C	16 Pin WSOIC
SP3232EET-L/TR	-40°C to +85°C	16 Pin WSOIC
SP3232EEY-L	-40°C to +85°C	16 Pin TSSOP
SP3232EEY-L/TR	-40°C to +85°C	16 Pin TSSOP

Note: "/TR" is for tape and Reel option. "-L" is for lead free packaging

REVISION HISTORY

DATE	REVISION	DESCRIPTION
08/22/05	--	Legacy Sipex Datasheet
12/08/10	1.0.0	Convert to Exar Format and update ordering information.
03/14/13	1.0.1	Correct type error to driver Transition-Region Slew Rate conditions.

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