

## Transformer Driver for Isolated Power Supplies

Check for Samples: [SN6501](#)

### FEATURES

- Push-Pull Driver for Small Transformers
- Single 3.3 V or 5 V Supply
- High Primary-side Current Drive:
  - 5 V Supply: 350 mA (max)
  - 3.3 V Supply: 150 mA (max)
- Low Ripple on Rectified Output Permits Small Output Capacitors
- Small 5-pin SOT23 Package

### APPLICATIONS

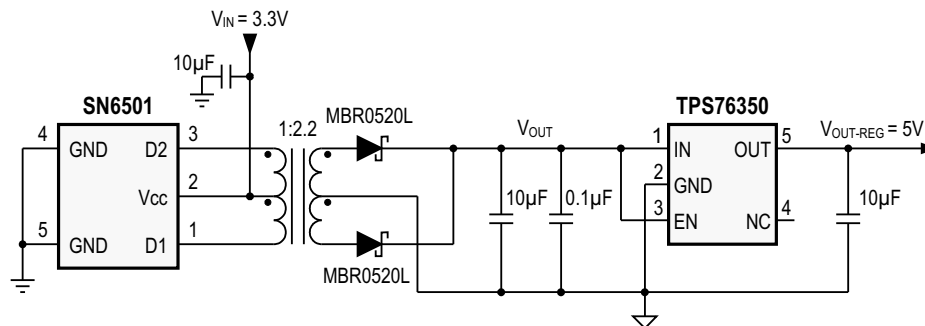
- Isolated Interface Power Supply for CAN, RS-485, RS-422, RS-232, SPI, I2C, Low-Power LAN
- Industrial Automation
- Process Control
- Medical Equipment

### DESCRIPTION

The SN6501 is a monolithic oscillator/power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. It drives a low-profile, center-tapped transformer primary from a 3.3 V or 5 V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio.

The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches.

The SN6501 is available in a small SOT23-5 package, and is specified for operation at temperatures from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .



**Figure 1. Typical Operating Circuit**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN6501

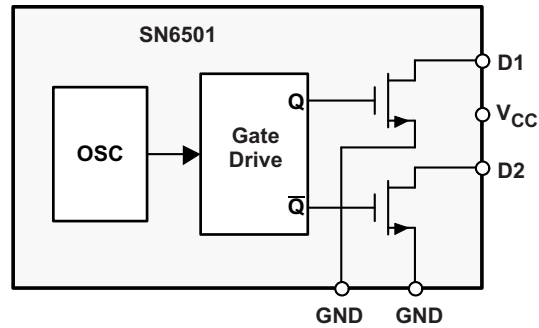
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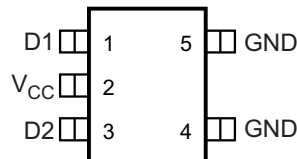


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## FUNCTIONAL BLOCK DIAGRAM

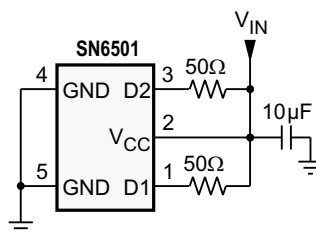


## PIN FUNCTIONS



PIN No.	NAME	DESCRIPTION
1	D1	Drain 1
2	Vcc	Supply voltage
3	D2	Drain 2
4,5	GND	Ground

## TEST CIRCUIT



**Figure 2. Test Circuit for  $R_{ON}$ ,  $f_{SW}$ ,  $f_{St}$ ,  $t_{r-D}$ ,  $t_{f-D}$ ,  $t_{BBM}$**

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

				VALUES
V <sub>CC</sub>	Supply voltage			–0.3 V to +6 V
V <sub>D1</sub> , V <sub>D2</sub>	Output switch voltage			14 V
I <sub>D1P</sub> , I <sub>D2P</sub>	Peak output switch current			500 mA
P <sub>TOT</sub>	Continuous power dissipation			250 mW
ESD	Human Body Model	ESDA/JEDEC JS-001-2012	All Pins	±4 kV
	Charged Device Model	JEDEC JESD22-C101E		±1.5 kV
	Machine Model	JEDEC JESD22-A115-A		±200 V
T <sub>STG</sub>	Storage temperature range			–65°C to 150°C
T <sub>J</sub>	Junction temperature			170°C

- (1) Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute-maximum-rated conditions for extended periods affects device reliability.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		SN6501	UNITS
		DBV 5-PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	208.3	°C/W
θ <sub>JCTop</sub>	Junction-to-case (top) thermal resistance	87.1	
θ <sub>JB</sub>	Junction-to-board thermal resistance	40.4	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	5.2	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	39.7	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## RECOMMENDED OPERATING CONDITIONS

				MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage			3		5.5	V
V <sub>D1</sub> , V <sub>D2</sub>	Output switch voltage	V <sub>CC</sub> = 5 V ± 10%,	When connected to Transformer with primary winding Center-tapped	0		11	V
		V <sub>CC</sub> = 3.3 V ± 10%		0		7.2	
I <sub>D1</sub> , I <sub>D2</sub>	D1 and D2 output switch current – Primary-side	V <sub>CC</sub> = 5 V ± 10%	V <sub>D1</sub> , V <sub>D2</sub> Swing ≥ 3.8 V, see <a href="#">Figure 42</a> for typical characteristics			350	mA
		V <sub>CC</sub> = 3.3 V ± 10%	V <sub>D1</sub> , V <sub>D2</sub> Swing ≥ 2.5 V, see <a href="#">Figure 41</a> for typical characteristics			150	
T <sub>A</sub>	Ambient temperature			–40		125	°C

# SN6501

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## ELECTRICAL CHARACTERISTICS

Over full-range of recommended operating conditions, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>ON</sub>	Switch-on resistance	V <sub>CC</sub> = 3.3 V ± 10%, See <a href="#">Figure 2</a>		1	3	Ω
		V <sub>CC</sub> = 5 V ± 10%, See <a href="#">Figure 2</a>		0.6	2	
I <sub>CC</sub>	Average supply current <sup>(1)</sup>	V <sub>CC</sub> = 3.3 V ± 10%, no load		150	400	uA
		V <sub>CC</sub> = 5 V ± 10%, no load		300	700	
f <sub>ST</sub>	Startup frequency	V <sub>CC</sub> = 2.4 V, See <a href="#">Figure 2</a>		300		kHz
f <sub>SW</sub>	D1, D2 Switching frequency	V <sub>CC</sub> = 3.3 V ± 10%, See <a href="#">Figure 2</a>	250	360	550	kHz
		V <sub>CC</sub> = 5 V ± 10%, See <a href="#">Figure 2</a>	300	410	620	
t <sub>r-D</sub>	D1, D2 output rise time	V <sub>CC</sub> = 3.3 V ± 10%, See <a href="#">Figure 2</a>		70		ns
		V <sub>CC</sub> = 5 V ± 10%, See <a href="#">Figure 2</a>		80		
t <sub>f-D</sub>	D1, D2 output fall time	V <sub>CC</sub> = 3.3 V ± 10%, See <a href="#">Figure 2</a>		110		ns
		V <sub>CC</sub> = 5 V ± 10%, See <a href="#">Figure 2</a>		60		
t <sub>BBM</sub>	Break-before-make time	V <sub>CC</sub> = 3.3 V ± 10%, See <a href="#">Figure 2</a>		150		ns
		V <sub>CC</sub> = 5 V ± 10%, See <a href="#">Figure 2</a>		50		

(1) Average supply current is the current used by SN6501 only. It does not include load current.

## TYPICAL OPERATING CHARACTERISTICS

Typical Curves in Figure 3 through Figure 8 are measured with Circuit in Figure 51 at TP1; whereas, Typical Curves in Figure 9 through Figure 38 are measured with Circuit in Figure 52 at TP1 and TP2 ( $T_A = 25^\circ\text{C}$  unless otherwise noted). See Table 2 and Table 3 for Transformer Specifications.

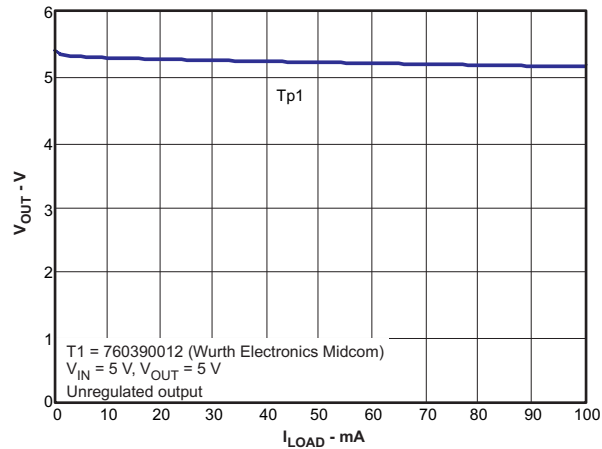


Figure 3. Output Voltage vs. Load Current

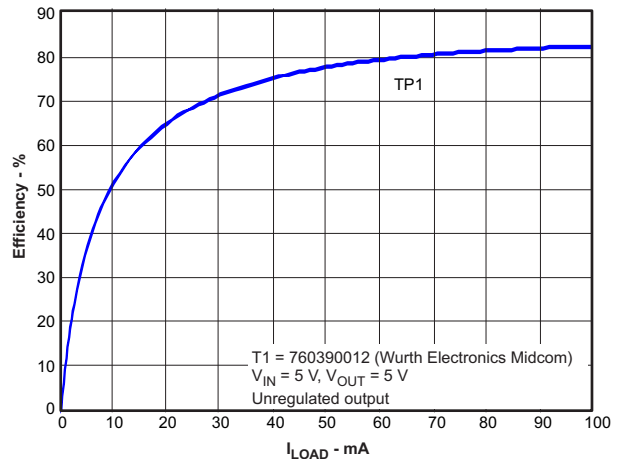


Figure 4. Efficiency vs. Load Current

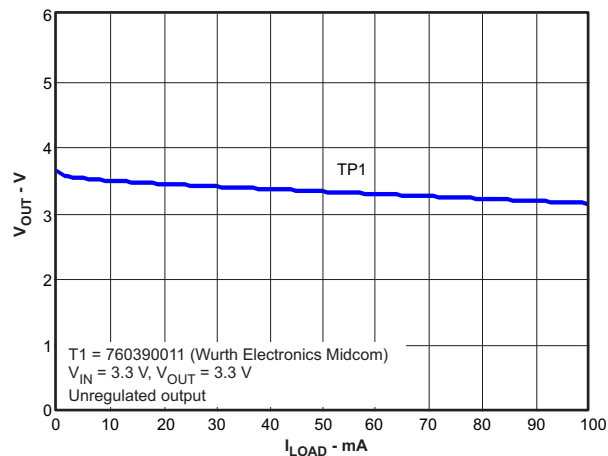


Figure 5. Output Voltage vs. Load Current

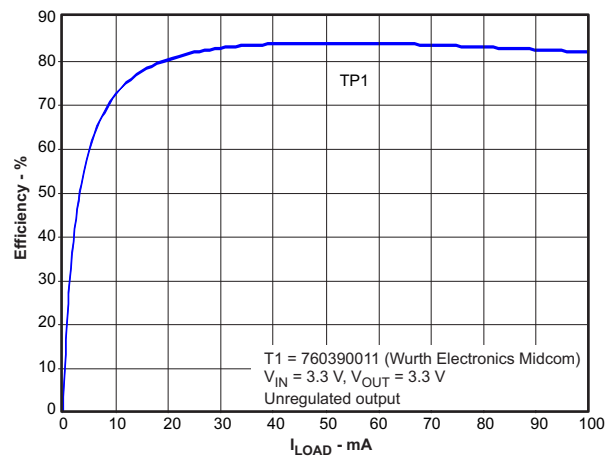


Figure 6. Efficiency vs. Load Current

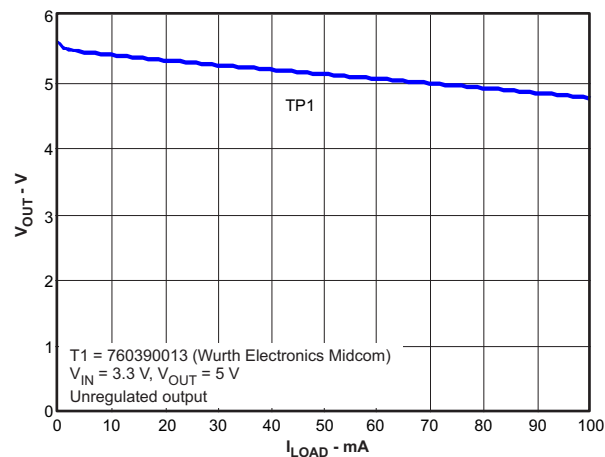


Figure 7. Output Voltage vs. Load Current

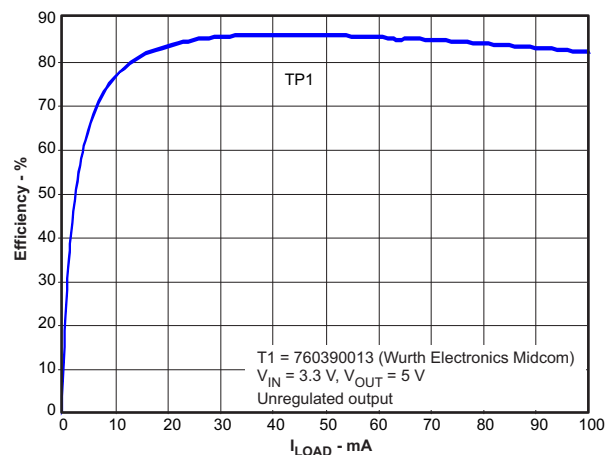


Figure 8. Efficiency vs. Load Current

## TYPICAL OPERATING CHARACTERISTICS (continued)

Typical Curves in Figure 3 through Figure 8 are measured with Circuit in Figure 51 at TP1; whereas, Typical Curves in Figure 9 through Figure 38 are measured with Circuit in Figure 52 at TP1 and TP2 ( $T_A = 25^\circ\text{C}$  unless otherwise noted).

See Table 2 and Table 3 for Transformer Specifications.

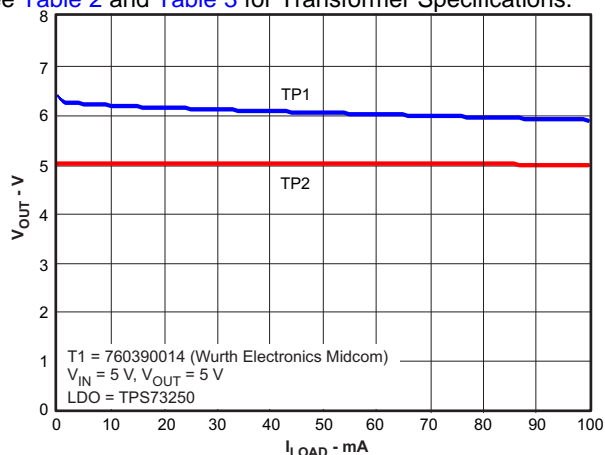


Figure 9. Output Voltage vs Load Current

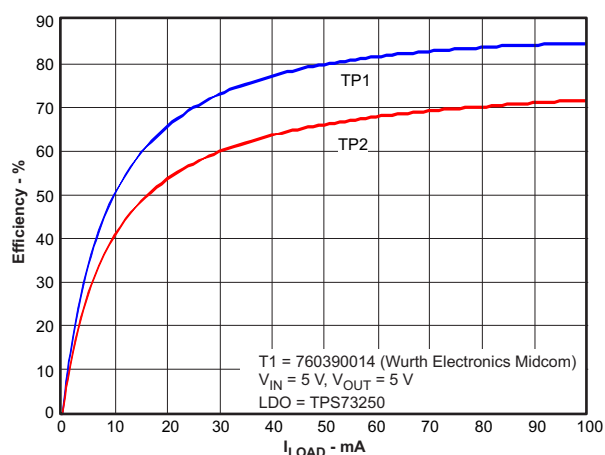


Figure 10. Efficiency vs Load Current

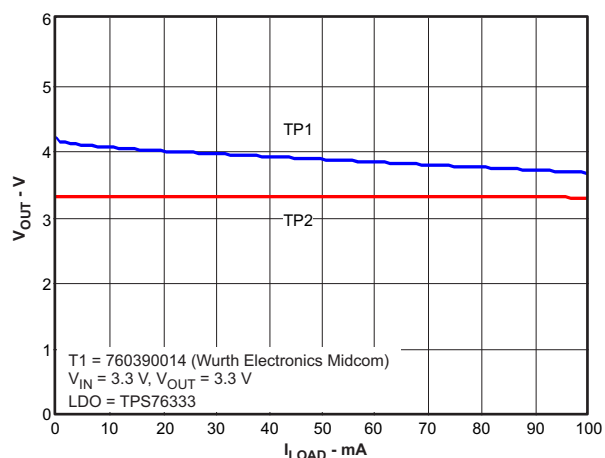


Figure 11. Output Voltage vs Load Current

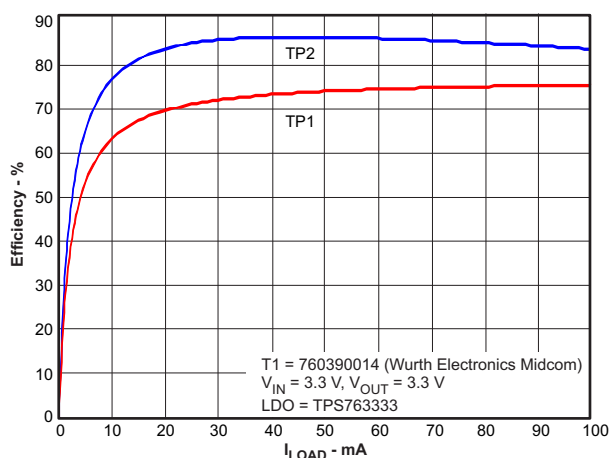


Figure 12. Efficiency vs Load Current

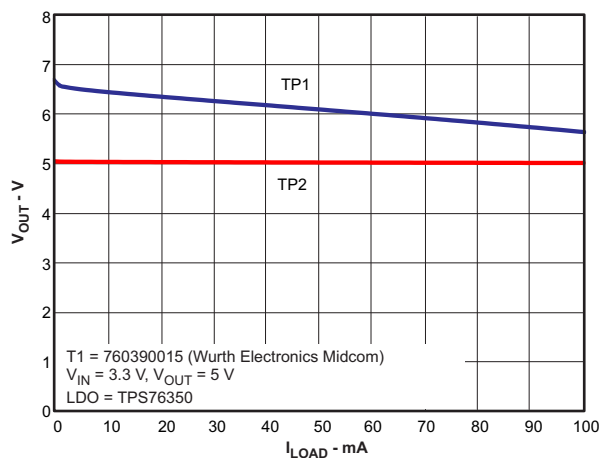


Figure 13. Output Voltage vs Load Current

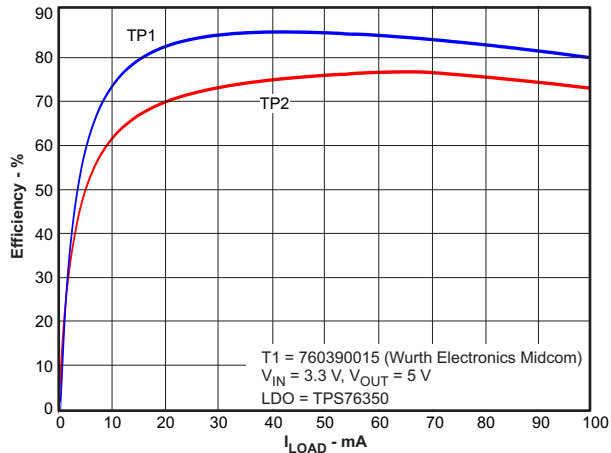


Figure 14. Efficiency vs Load Current

## TYPICAL OPERATING CHARACTERISTICS (continued)

Typical Curves in Figure 3 through Figure 8 are measured with Circuit in Figure 51 at TP1; whereas, Typical Curves in Figure 9 through Figure 38 are measured with Circuit in Figure 52 at TP1 and TP2 ( $T_A = 25^\circ\text{C}$  unless otherwise noted).

See Table 2 and Table 3 for Transformer Specifications.

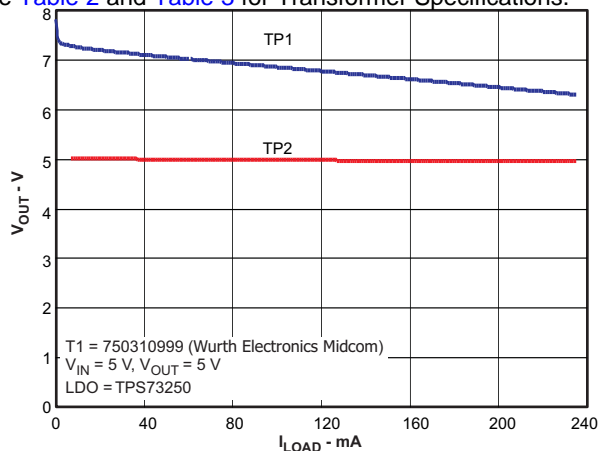


Figure 15.

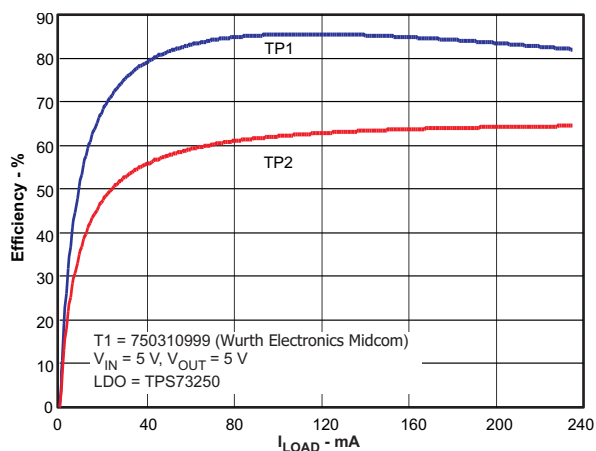


Figure 16.

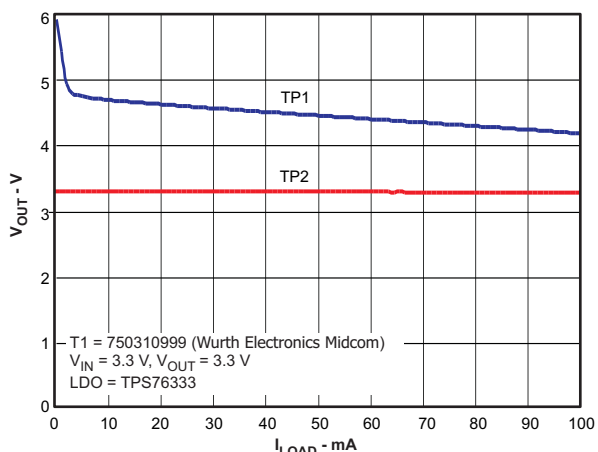


Figure 17.

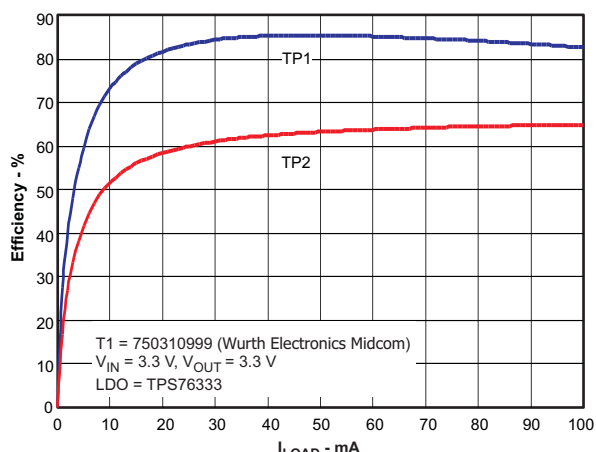


Figure 18.

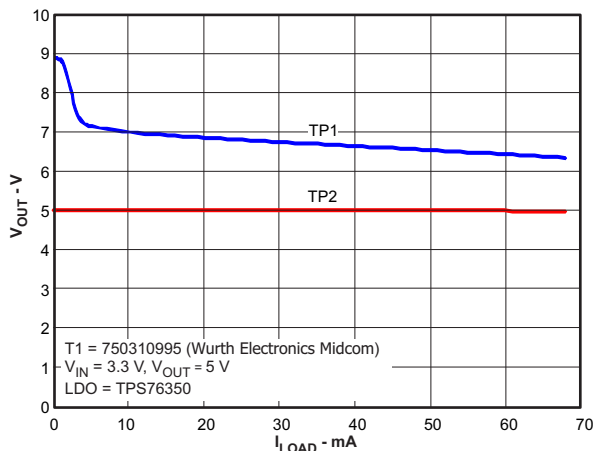


Figure 19. Output Voltage vs Load Current

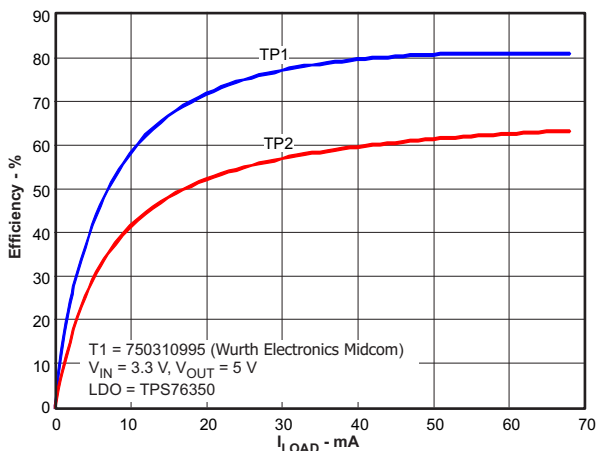


Figure 20. Efficiency vs Load Current

## TYPICAL OPERATING CHARACTERISTICS (continued)

Typical Curves in Figure 3 through Figure 8 are measured with Circuit in Figure 51 at TP1; whereas, Typical Curves in Figure 9 through Figure 38 are measured with Circuit in Figure 52 at TP1 and TP2 ( $T_A = 25^\circ\text{C}$  unless otherwise noted).

See Table 2 and Table 3 for Transformer Specifications.

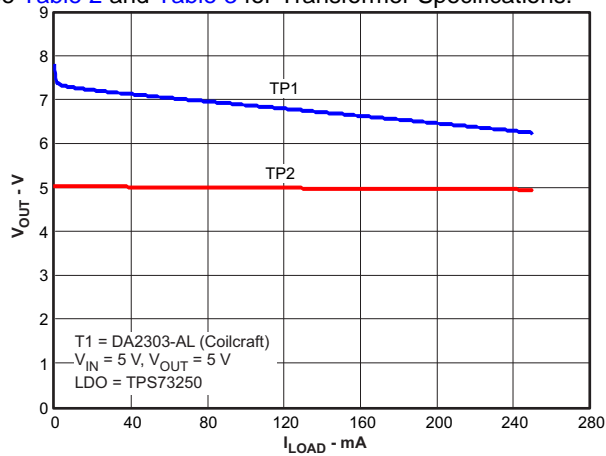


Figure 21. Output Voltage vs Load Current

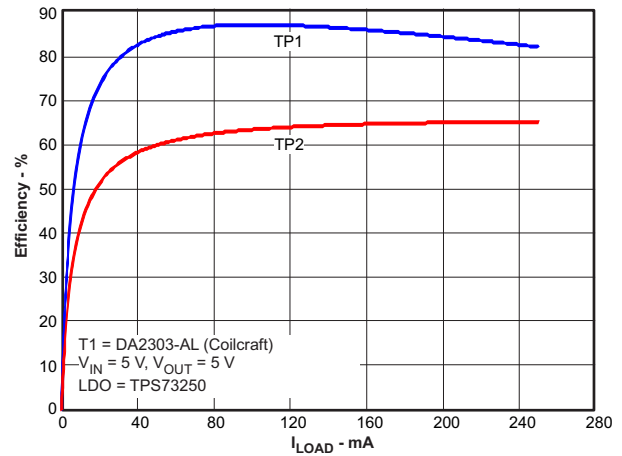


Figure 22. Efficiency vs Load Current

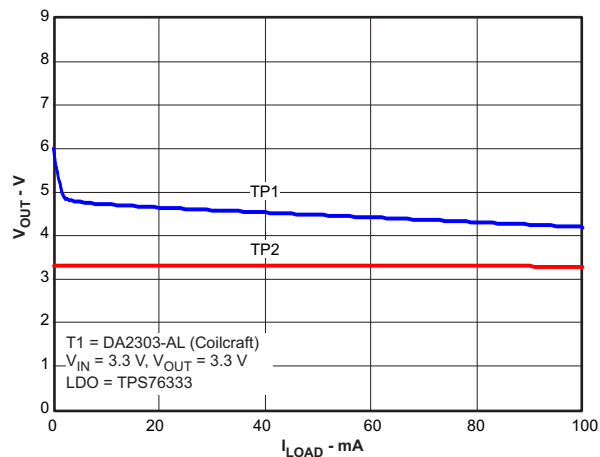


Figure 23. Output Voltage vs Load Current

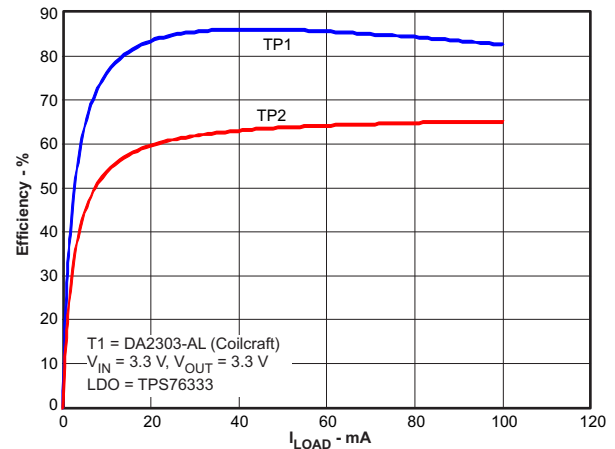


Figure 24. Efficiency vs Load Current

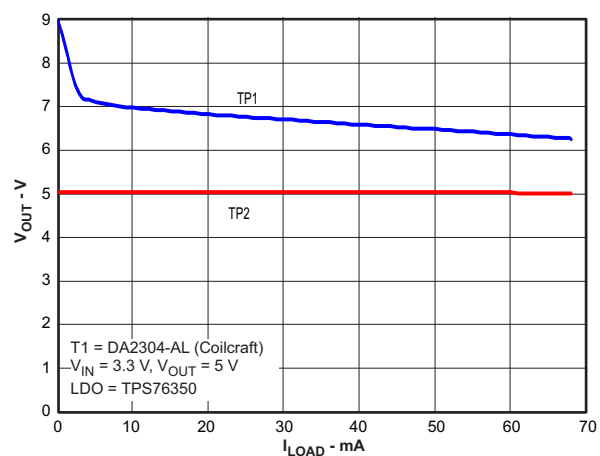


Figure 25. Output Voltage vs Load Current

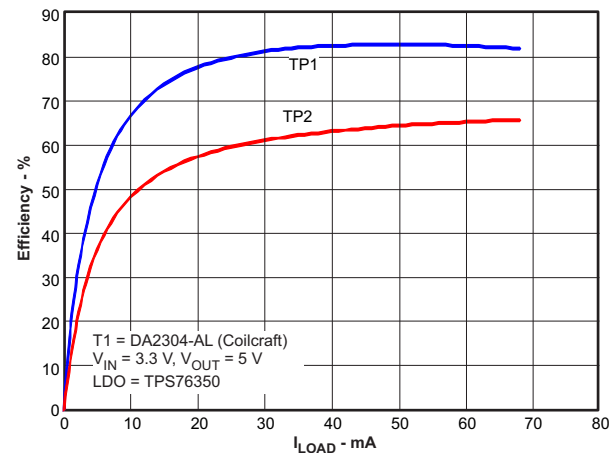


Figure 26. Efficiency vs Load Current



## TYPICAL OPERATING CHARACTERISTICS (continued)

Typical Curves in Figure 3 through Figure 8 are measured with Circuit in Figure 51 at TP1; whereas, Typical Curves in Figure 9 through Figure 38 are measured with Circuit in Figure 52 at TP1 and TP2 ( $T_A = 25^\circ\text{C}$  unless otherwise noted).

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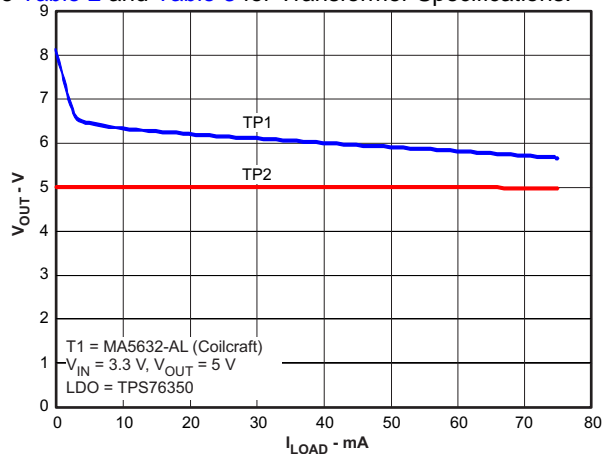


Figure 27. Output Voltage vs Load Current

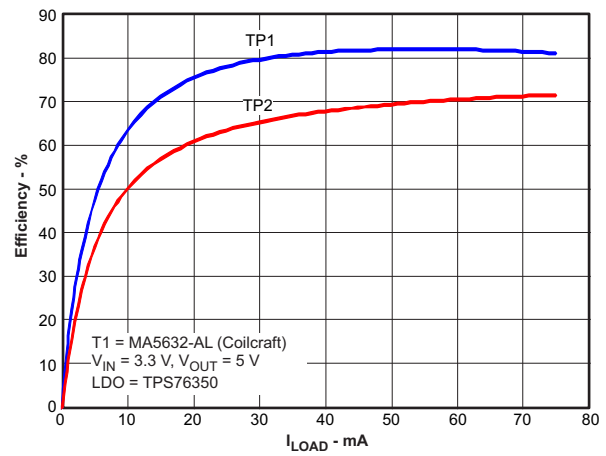


Figure 28. Efficiency vs Load Current

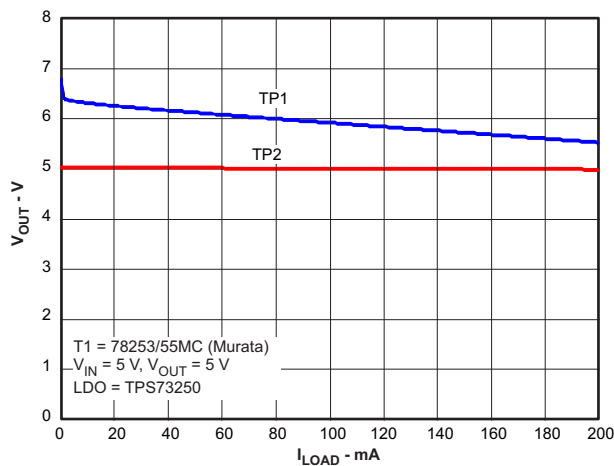


Figure 29. Output Voltage vs Load Current

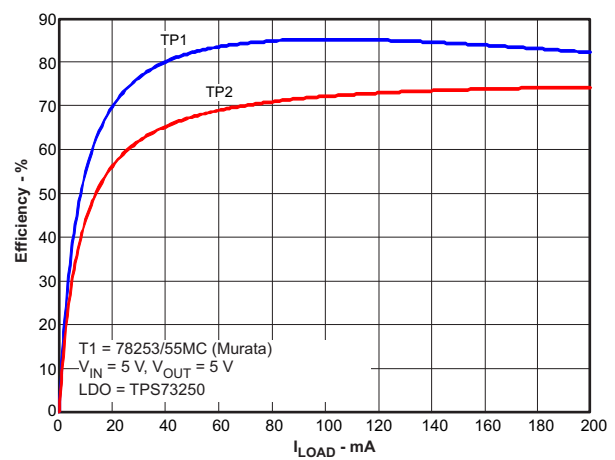


Figure 30. Efficiency vs Load Current

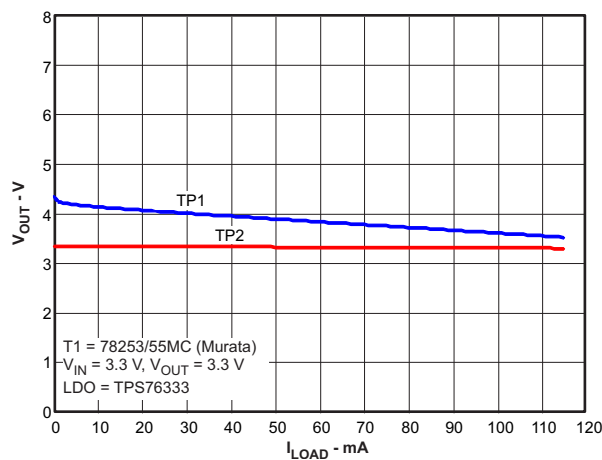


Figure 31. Output Voltage vs Load Current

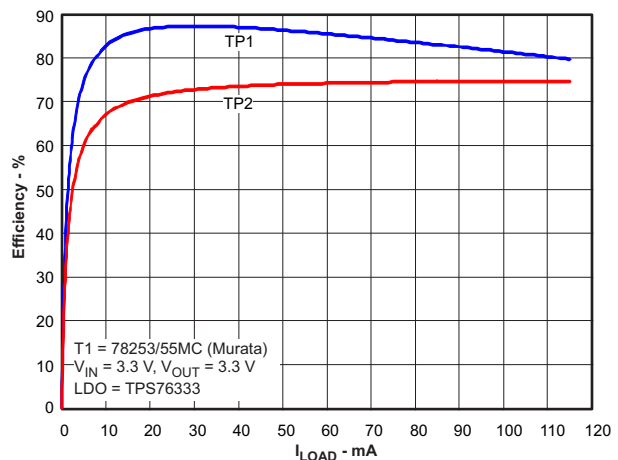


Figure 32. Efficiency vs Load Current

## TYPICAL OPERATING CHARACTERISTICS (continued)

Typical Curves in [Figure 3](#) through [Figure 8](#) are measured with Circuit in [Figure 51](#) at TP1; whereas, Typical Curves in [Figure 9](#) through [Figure 38](#) are measured with Circuit in [Figure 52](#) at TP1 and TP2 ( $T_A = 25^\circ\text{C}$  unless otherwise noted).

See [Table 2](#) and [Table 3](#) for Transformer Specifications.

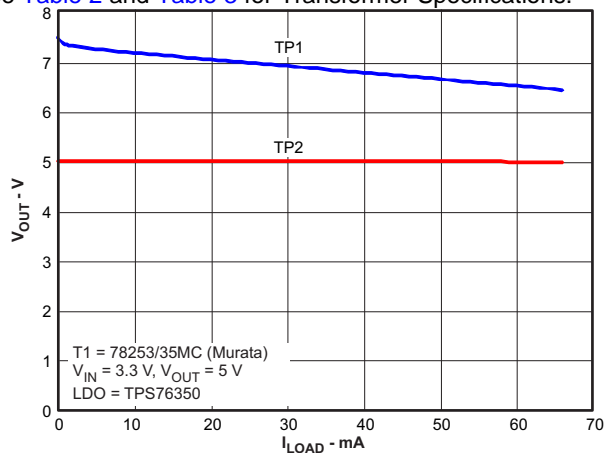


Figure 33. Output Voltage vs Load Current

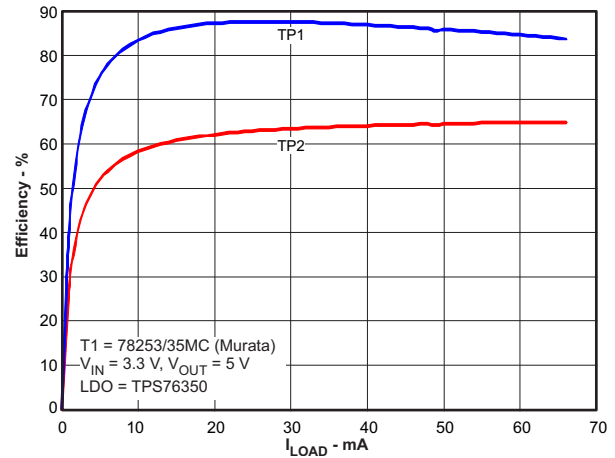


Figure 34. Efficiency vs Load Current

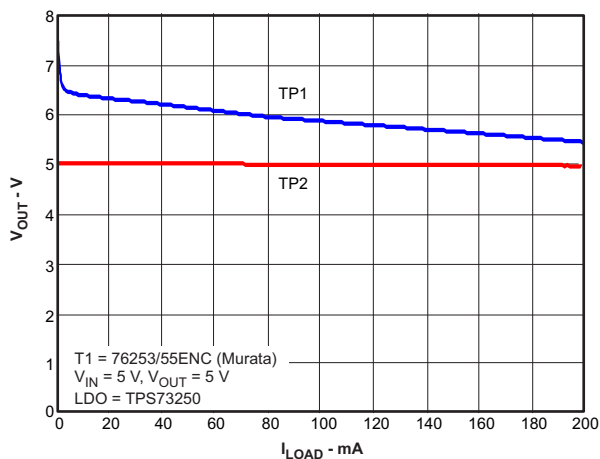


Figure 35. Output Voltage vs Load Current

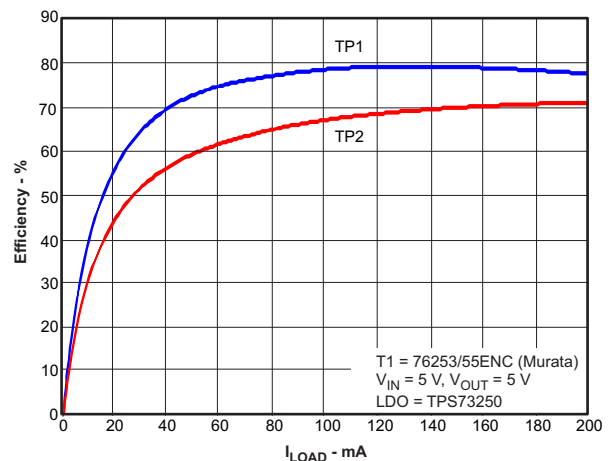


Figure 36. Efficiency vs Load Current

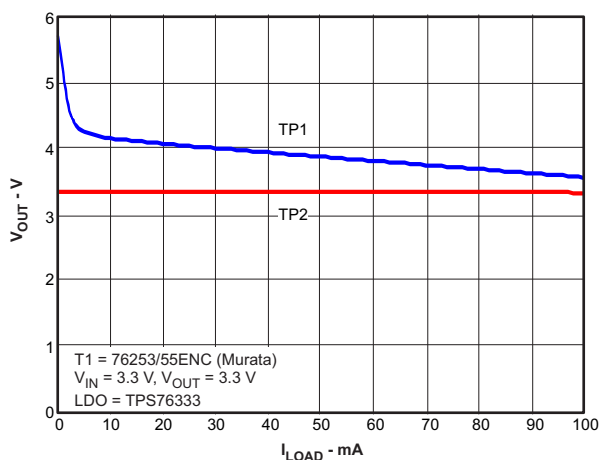


Figure 37. Output Voltage vs Load Current

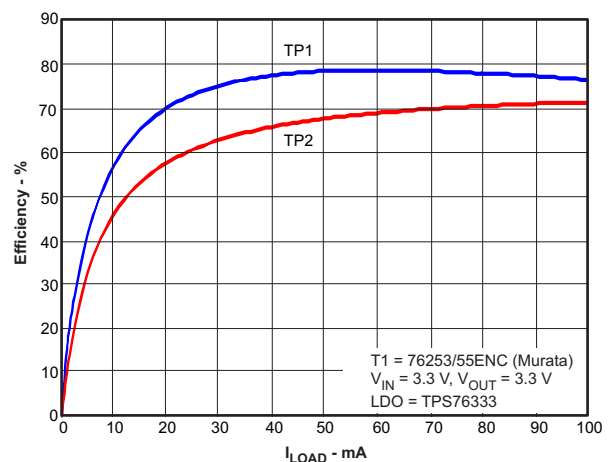


Figure 38. Efficiency vs Load Current

## TYPICAL OPERATING CHARACTERISTICS (continued)

Typical Curves in Figure 3 through Figure 8 are measured with Circuit in Figure 51 at TP1; whereas, Typical Curves in Figure 9 through Figure 38 are measured with Circuit in Figure 52 at TP1 and TP2 ( $T_A = 25^\circ\text{C}$  unless otherwise noted).

See Table 2 and Table 3 for Transformer Specifications.

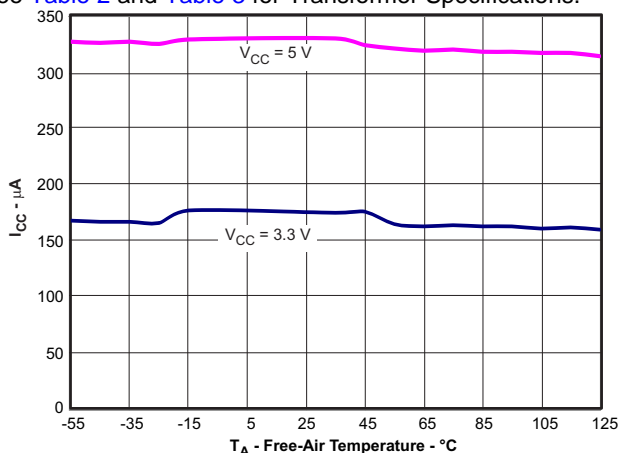


Figure 39. Average Supply Current vs Free-Air Temperature

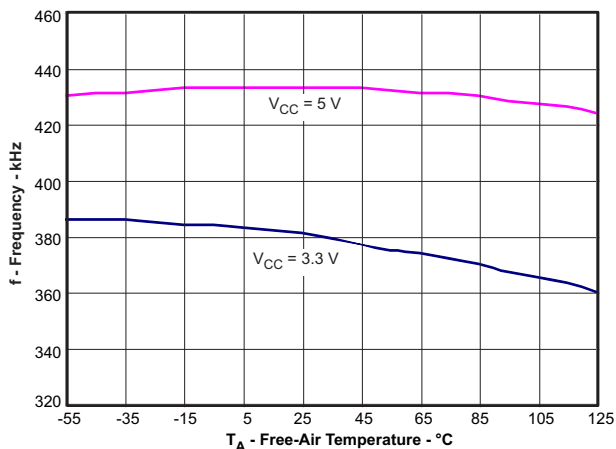


Figure 40. D1, D2 Switching Frequency vs Free-Air Temperature

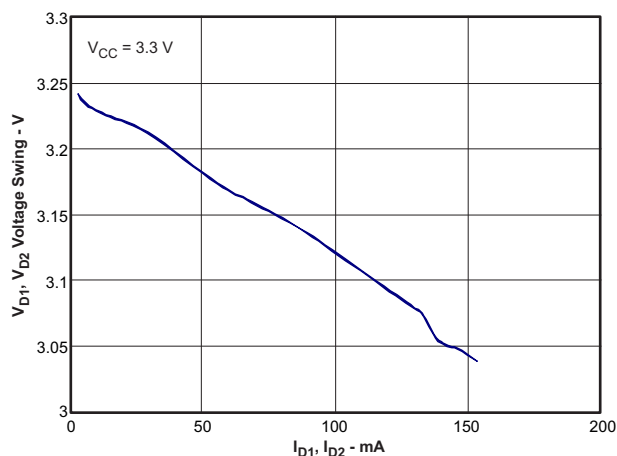


Figure 41. D1, D2 Primary-side Output Switch Voltage Swing vs Current

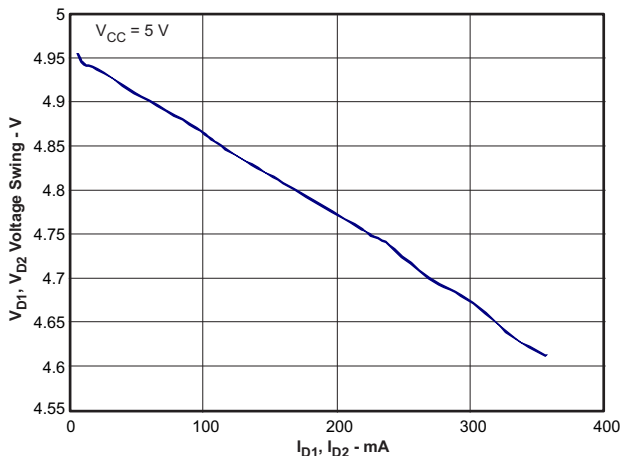


Figure 42. D1, D2 Primary-side Output Switch Voltage Swing vs Current

## TYPICAL OPERATING CHARACTERISTICS (continued)

Typical Curves in [Figure 3](#) through [Figure 8](#) are measured with Circuit in [Figure 51](#) at TP1; whereas, Typical Curves in [Figure 9](#) through [Figure 38](#) are measured with Circuit in [Figure 52](#) at TP1 and TP2 ( $T_A = 25^\circ\text{C}$  unless otherwise noted).

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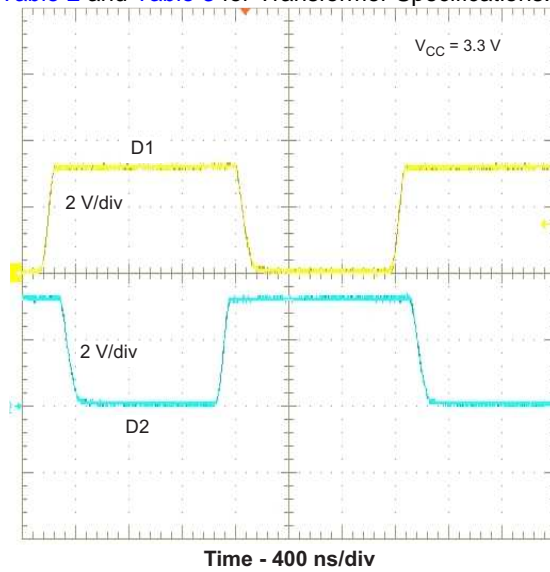


Figure 43. D1, D2 Switching Waveforms

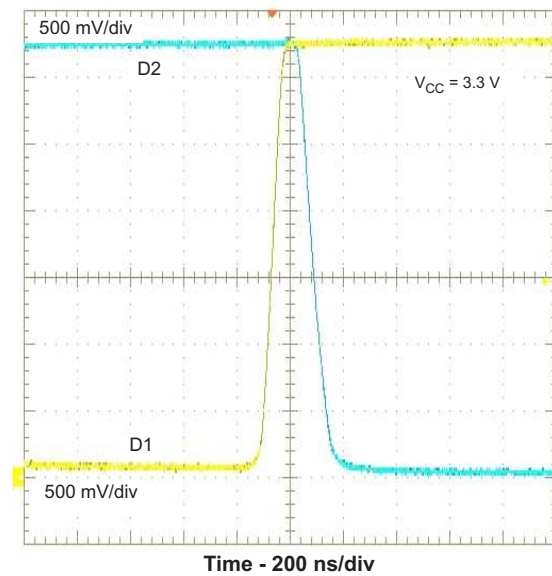
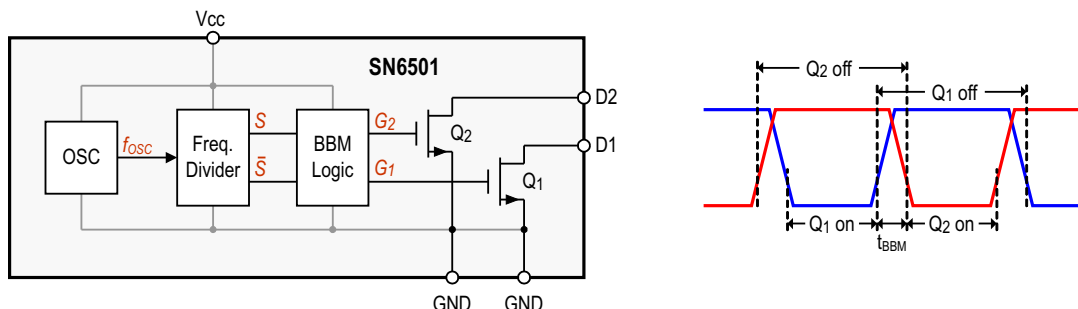


Figure 44. D1, D2 Break-Before-Make Waveform

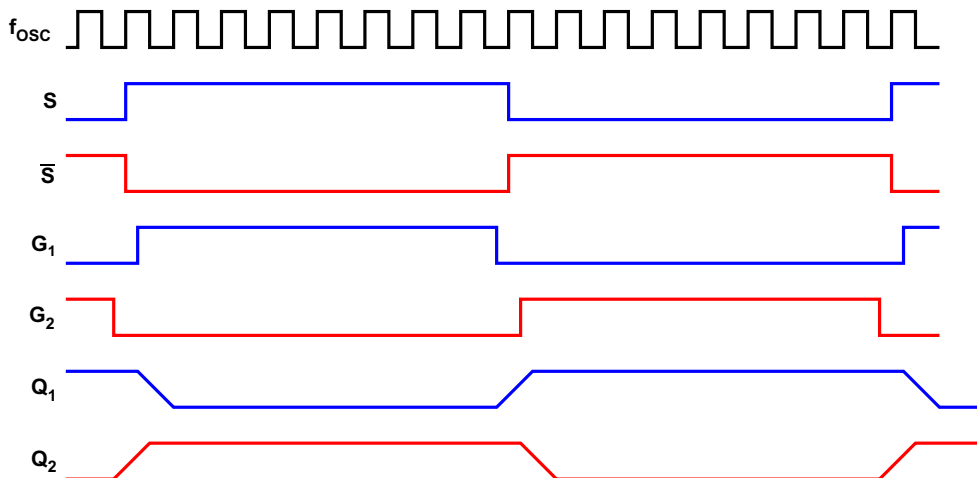
## APPLICATION INFORMATION

The SN6501 is a transformer driver designed for low-cost, small form-factor, **isolated DC-DC converters utilizing the push-pull topology**. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off.



**Figure 45. SN6501 Block Diagram and Output Timing with Break-Before-Make Action**

The output frequency of the oscillator is divided down by an asynchronous divider that provides two complementary output signals, S and  $\bar{S}$ , with a 50% duty cycle. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. The resulting output signals, G<sub>1</sub> and G<sub>2</sub>, present the gate-drive signals for the output transistors Q<sub>1</sub> and Q<sub>2</sub>. As shown in [Figure 46](#), before either one of the gates can assume logic high, there must be a short time period during which both signals are low and both transistors are high-impedance. This short period, known as break-before-make time, is required to avoid shorting out both ends of the primary.



**Figure 46. Detailed Output Signal Waveforms**

## PUSH-PULL CONVERTER

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary (see [Figure 47](#)).

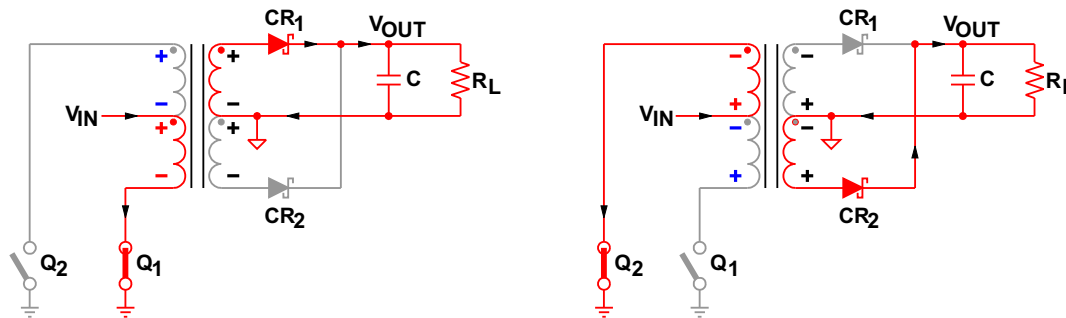


Figure 47. Switching Cycles of a Push-Pull Converter

When Q1 conducts, VIN drives a current through the lower half of the primary to ground, thus creating a negative voltage potential at the lower primary end with regards to the VIN potential at the center-tap.

At the same time the voltage across the upper half of the primary is such that the upper primary end is positive with regards to the center-tap in order to maintain the previously established current flow through Q2, which now has turned high-impedance. The two voltage sources, each of which equaling VIN, appear in series and cause a voltage potential at the open end of the primary of  $2 \times V_{IN}$  with regards to ground.

Per dot convention the same voltage polarities that occur at the primary also occur at the secondary. The positive potential of the upper secondary end therefore forward biases diode CR1. The secondary current starting from the upper secondary end flows through CR1, charges capacitor C, and returns through the load impedance RL back to the center-tap.

When Q2 conducts, Q1 goes high-impedance and the voltage polarities at the primary and secondary reverse. Now the lower end of the primary presents the open end with a  $2 \times V_{IN}$  potential against ground. In this case CR2 is forward biased while CR1 is reverse biased and current flows from the lower secondary end through CR2, charging the capacitor and returning through the load to the center-tap.

## CORE MAGNETIZATION

Figure 48 shows the ideal magnetizing curve for a push-pull converter with B as the magnetic flux density and H as the magnetic field strength. When Q1 conducts the magnetic flux is pushed from A to A', and when Q2 conducts the flux is pulled back from A' to A. The difference in flux and thus in flux density is proportional to the product of the primary voltage, VP, and the time, tON, it is applied to the primary:  $B \approx V_P \times t_{ON}$ .

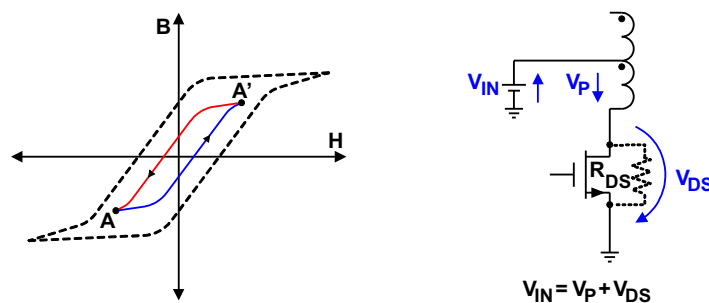


Figure 48. Core Magnetization and Self-Regulation Through Positive Temperature Coefficient of  $R_{DS(on)}$

This volt-seconds (V-t) product is important as it determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results with an offset from the origin of the B-H curve. If balance is not restored, the offset increases with each following cycle and the transformer slowly creeps toward the saturation region.

Fortunately, due to the positive temperature coefficient of a MOSFET's on-resistance, the output FETs of the SN6501 have a self-correcting effect on V-t imbalance. In the case of a slightly longer on-time, the prolonged current flow through a FET gradually heats the transistor which leads to an increase in  $R_{DS-on}$ . The higher resistance then causes the drain-source voltage,  $V_{DS}$ , to rise. Because the voltage at the primary is the difference between the constant input voltage,  $V_{IN}$ , and the voltage drop across the MOSFET,  $V_P = V_{IN} - V_{DS}$ ,  $V_P$  is gradually reduced and V-t balance restored.

## CONVERTER DESIGN

The following recommendations on components selection focus on the design of an efficient push-pull converter with high current drive capability. Contrary to popular belief, **the output voltage of the unregulated converter output drops significantly over a wide range in load current**. The characteristic curve in [Figure 25](#) for example shows that the difference between  $V_{OUT}$  at minimum load and  $V_{OUT}$  at maximum load exceeds a transceiver's supply range. Therefore, in order to provide a stable, load independent supply while maintaining maximum possible efficiency the implementation of a low dropout regulator (LDO) is strongly advised.

The final converter circuit is shown in [Figure 52](#). The measured  $V_{OUT}$  and efficiency characteristics for the regulated and unregulated outputs are shown in [Figure 21](#) to [Figure 20](#).

## SN6501 DRIVE CAPABILITY

The SN6501 transformer driver is designed for low-power push-pull converters with input and output voltages in the range of 3 V to 5.5 V. While converter designs with higher output voltages are possible, care must be taken that higher turns ratios don't lead to primary currents that exceed the SN6501 specified current limits.

## LDO SELECTION

The minimum requirements for a suitable low dropout regulator are:

- Its current drive capability should slightly exceed the specified load current of the application to prevent the LDO from dropping out of regulation. **Therefore for a load current of 100 mA, choose a 100 mA to 150 mA LDO.** While regulators with higher drive capabilities are acceptable, they also usually possess higher dropout voltages that will reduce overall converter efficiency.
- The internal dropout voltage,  $V_{DO}$ , at the specified load current should be as low as possible to maintain efficiency. For a low-cost 150 mA LDO, a  $V_{DO}$  of 150 mV at 100 mA is common. Be aware however, that this lower value is usually specified at room temperature and can increase by a factor of 2 over temperature, which in turn will raise the required minimum input voltage.
- The required minimum input voltage preventing the regulator from dropping out of line regulation is given with:

$$V_{I-min} = V_{DO-max} + V_{O-max}$$

This means in order to determine  $V_I$  for worst-case condition, the user must take the maximum values for  $V_{DO}$  and  $V_O$  specified in the LDO data sheet for rated output current (i.e., 100 mA) and add them together. Also specify that the output voltage of the push-pull rectifier at the specified load current is equal or higher than  $V_{I-min}$ . If it is not, the LDO will lose line-regulation and any variations at the input will pass straight through to the output. Hence below  $V_{I-min}$  the output voltage will follow the input and the regulator behaves like a simple conductor.

- The maximum regulator input voltage must be higher than the rectifier output under no-load. Under this condition there is no secondary current reflected back to the primary, thus making the voltage drop across  $R_{DS-on}$  negligible and allowing the entire converter input voltage to drop across the primary. At this point the secondary reaches its maximum voltage of

$$V_{S-max} = V_{IN-max} \times n$$

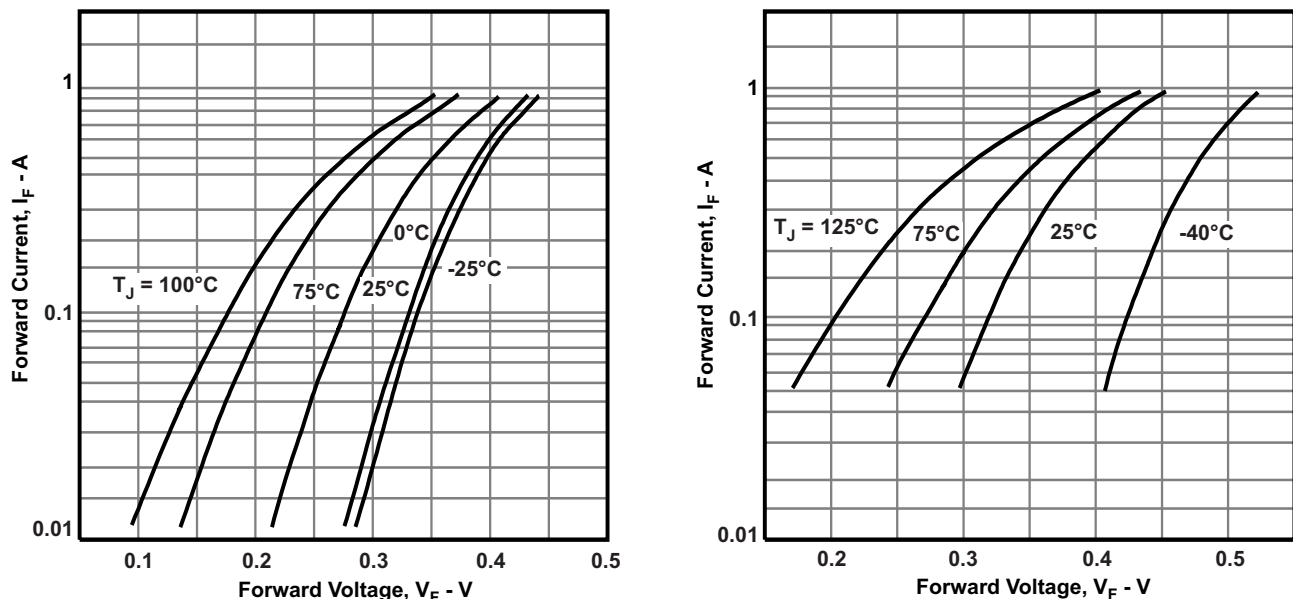
with  $V_{IN-max}$  as the maximum converter input voltage and  $n$  as the transformer turns ratio. Thus to prevent the LDO from damage the maximum regulator input voltage must be higher than  $V_{S-max}$ . [Table 1](#) lists the maximum secondary voltages for various turns ratios commonly applied in push-pull converters with 100 mA output drive.

**Table 1. Required maximum LDO Input Voltages for Various Push-pull Configurations**

PUSH-PULL CONVERTER				LDO
CONFIGURATION	$V_{IN-max}$ [V]	TURNS-RATIO	$V_{S-max}$ [V]	$V_{I-max}$ [V]
3.3 $V_{IN}$ to 3.3 $V_{OUT}$	3.6	$1.5 \pm 3\%$	5.6	6 to 10
3.3 $V_{IN}$ to 5 $V_{OUT}$	3.6	$2.2 \pm 3\%$	8.2	10
5 $V_{IN}$ to 5 $V_{OUT}$	5.5	$1.5 \pm 3\%$	8.5	10

## DIODE SELECTION

A rectifier diode should always possess **low-forward voltage to provide as much voltage to the converter output as possible**. When used in high-frequency switching applications, such as the SN6501 however, the diode must also possess **a short recovery time**. Schottky diodes meet both requirements and are therefore strongly recommended in push-pull converter designs. An excellent choice for low-volt applications is the **MBR0520L** with a typical forward voltage of 275 mV at 100 mA forward current. For higher output voltages such as  $\pm 10$  V and above use the MBR0530 which provides a higher DC blocking voltage of 30 V.


**Figure 49. Diode Forward Characteristics for MBR0520L (left) and MBR0530 (right)**

## CAPACITOR SELECTION

The capacitors in the converter circuit in [Figure 52](#) are **multi-layer ceramic chip (MLCC) capacitors**.

As with all high speed CMOS ICs, the SN6501 requires a **bypass capacitor in the range of 10 nF to 100 nF**.

The input bulk capacitor at the center-tap of the primary supports large currents into the primary during the fast switching transients. For minimum ripple make this capacitor **10  $\mu$ F to 22  $\mu$ F**. In a 2-layer PCB design with a dedicated ground plane, place this capacitor close to the primary center-tap to minimize trace inductance. In a 4-layer board design with low-inductance reference planes for ground and  $V_{IN}$ , the capacitor can be placed at the supply entrance of the board. To ensure low-inductance paths use two vias in parallel for each connection to a reference plane or to the primary center-tap.

The bulk capacitor at the rectifier output smoothes the output voltage. Make this capacitor 10  $\mu$ F to 22  $\mu$ F.

The small capacitor at the regulator input is not necessarily required. However, good analog design practice suggests, using a small value of 47 nF to 100 nF improves the regulator's transient response and noise rejection.

The LDO output capacitor buffers the regulated output for the subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements specified in the data sheet. However, in most cases, a low-ESR ceramic capacitor in the range of 4.7  $\mu$ F to 10  $\mu$ F will satisfy these requirements.





# SN6501

SLLSEA0E –FEBRUARY 2012–REVISED JANUARY 2013

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Then calculating the available minimum primary voltage,  $V_{P-min}$ , involves subtracting the maximum possible drain-source voltage of the SN6501,  $V_{DS-max}$ , from the minimum converter input voltage  $V_{IN-min}$ :

$$V_{P-min} = V_{IN-min} - V_{DS-max} \quad (5)$$

$V_{DS-max}$  however, is the product of the maximum  $R_{DS(on)}$  and  $I_D$  values for a given supply specified in the SN6501 data sheet:

$$V_{DS-max} = R_{DS-max} \times I_{Dmax} \quad (6)$$

Then inserting Equation 6 into Equation 5 yields:

$$V_{P-min} = V_{IN-min} - R_{DS-max} \times I_{Dmax} \quad (7)$$

and inserting Equation 7 and Equation 4 into Equation 3 provides the minimum turns ration with:

$$n_{min} = 1.031 \times \frac{V_{F-max} + V_{DO-max} + V_{O-max}}{V_{IN-min} - R_{DS-max} \times I_{D-max}} \quad (8)$$

## Example:

For a 3.3  $V_{IN}$  to 5  $V_{OUT}$  converter using the rectifier diode MBR0520L and the 5 V LDO TPS76350, the data sheet values taken for a load current of 100 mA and a maximum temperature of 85°C are  $V_{F-max} = 0.2$  V,  $V_{DO-max} = 0.2$  V, and  $V_{O-max} = 5.175$  V.

Then assuming that the converter input voltage is taken from a 3.3 V controller supply with a maximum  $\pm 2\%$  accuracy makes  $V_{IN-min} = 3.234$  V. Finally the maximum values for drain-source resistance and drain current at 3.3 V are taken from the SN6501 data sheet with  $R_{DS-max} = 3 \Omega$  and  $I_{D-max} = 150$  mA.

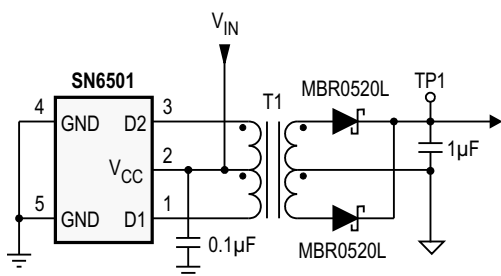
Inserting the values above into Equation 8 yields a minimum turns ratio of:

$$n_{min} = 1.031 \times \frac{0.2V + 0.2V + 5.175 V}{3.234 V - 3 \Omega \times 150 \text{ mA}} = 2 \quad (9)$$

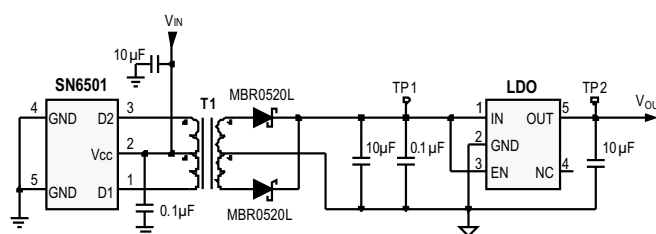
Most commercially available transformers for 3-to-5 V push-pull converters offer turns ratios between 2.0 and 2.3 with a common tolerance of  $\pm 3\%$ .

## Recommended Transformers

Depending on the application, use the minimum configuration in Figure 51 or standard configuration in Figure 52.



**Figure 51. Unregulated Output for Low-Current Loads with Wide Supply Range**



**Figure 52. Regulated Output for Stable Supplies and High Current Loads**

The Würth Electronics Midcom isolation transformers in Table 2 are optimized designs for the SN6501, providing high efficiency and small form factor at low-cost.

The 1:1.1 and 1:1.7 turns-ratios are designed for logic applications with wide supply rails and low load currents. These applications operate without LDO, thus achieving further cost-reduction.

**Table 2. Recommended Isolation Transformers Optimized for SN6501**

Turns Ratio	V x T (Vμs)	Isolation (V <sub>RMS</sub> )	Dimensions (mm)	Application	LDO	Figures	Order No.	Manufacturer
1:1.1	11	2500	6.73 x 7.14 x 4.06	5V → 5V	No	<a href="#">Figure 3</a> <a href="#">Figure 4</a>	760390012	Würth Electronics Midcom
1:1.1	7	2500	6.73 x 7.14 x 4.06	3.3V → 3.3V	No	<a href="#">Figure 5</a> <a href="#">Figure 6</a>	760390011	
1:1.7	11	2500	6.73 x 7.14 x 4.06	3.3V → 5V	No	<a href="#">Figure 7</a> <a href="#">Figure 8</a>	760390013	
1:1.3	11	2500	6.73 x 7.14 x 4.06	5V → 5V 3.3V → 3.3V	Yes	<a href="#">Figure 9</a> <a href="#">Figure 10</a> <a href="#">Figure 11</a> <a href="#">Figure 12</a>	760390014	
1:2.0	11	2500	6.73 x 7.14 x 4.06	3.3V → 5V	Yes	<a href="#">Figure 13</a> <a href="#">Figure 14</a>	760390015	

Other isolation transformers that have been tested with SN6501 are listed in [Table 3](#).

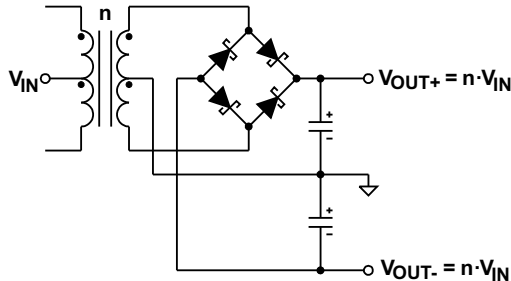
**Table 3. Standard Isolation Transformers Tested With SN6501**

Turns Ratio	V x T (Vμs)	Isolation (V) <sup>(1)</sup>	Dimensions (mm)	Application	LDO	Figures	Order No.	Manufacturer
1:1.5	11	2500	10 x 12.07 x 5.97	5V → 5V 3.3V → 3.3V	Yes	<a href="#">Figure 15</a> <a href="#">Figure 16</a> <a href="#">Figure 17</a> <a href="#">Figure 18</a>	750310999	Würth Electronics Midcom
1:2.2	11	2500	10 x 12.07 x 5.97	3.3V → 5V	Yes	<a href="#">Figure 19</a> <a href="#">Figure 20</a>	750310995	
1:1.5	34.4	2500	10 x 12.7 x 5.97	5V → 5V 3.3V → 3.3V	Yes	<a href="#">Figure 21</a> <a href="#">Figure 22</a> <a href="#">Figure 23</a> <a href="#">Figure 24</a>	DA2303-AL	Coilcraft
1:2.2	21.5	2500	10 x 12.7 x 5.97	3.3V → 5V	Yes	<a href="#">Figure 25</a> <a href="#">Figure 26</a>	DA2304-AL	
1:2.0	10.2	2500	10 x 12.7 x 5.97	3.3V → 5V	Yes	<a href="#">Figure 27</a> <a href="#">Figure 28</a>	MA5632-AL	
1:1.31	50	1500	9 x 12.7 x 6.35	5V → 5V 3.3V → 3.3V	Yes	<a href="#">Figure 29</a> <a href="#">Figure 30</a> <a href="#">Figure 31</a> <a href="#">Figure 32</a>	78253/55MC	Murata
1:2.27	35	1500	9 x 12.7 x 6.35	3.3V → 5V	Yes	<a href="#">Figure 33</a> <a href="#">Figure 34</a>	78253/35MC	
1:1.33	50	6000	15 x 15.0 x 12.5	5V → 5V 3.3V → 3.3V	Yes	<a href="#">Figure 35</a> <a href="#">Figure 36</a> <a href="#">Figure 37</a> <a href="#">Figure 38</a>	76253/55ENC	

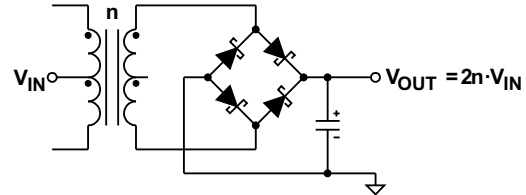
(1) Würth Electronics Midcom and Coilcraft Transformer Isolation ratings are specified in V<sub>RMS</sub> while Murata Transformers ratings are given in V<sub>DC</sub>.

## HIGHER OUTPUT VOLTAGE DESIGNS

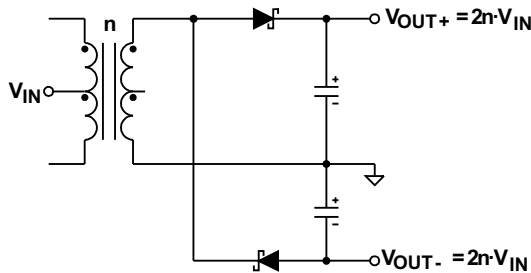
The SN6501 can drive push-pull converters that provide high output voltages of up to 30 V, or bipolar outputs of up to  $\pm 15$  V. Using commercially available center-tapped transformers, with their rather low turns ratios of 0.8 to 5, requires different rectifier topologies to achieve high output voltages. Figure 53 to Figure 56 show some of these topologies together with their respective open-circuit output voltages.



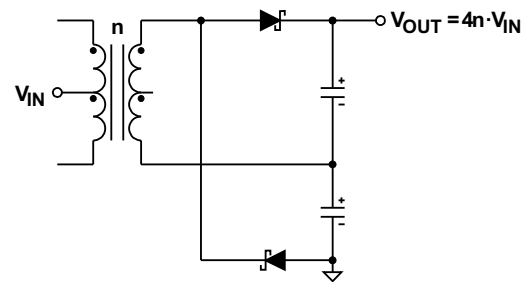
**Figure 53. Bridge Rectifier with Center-Tapped Secondary Enables Bipolar Outputs**



**Figure 54. Bridge Rectifier Without Center-Tapped Secondary Performs Voltage Doubling**



**Figure 55. Half-wave Rectifier Without Center-tapped Secondary Performs Voltage Doubling, Centered Ground provides Bipolar Outputs**



**Figure 56. Half-wave Rectifier Without Centered Ground and Center-tapped Secondary Performs Voltage Doubling Twice, Hence Quadrupling  $V_{IN}$**

## APPLICATION CIRCUITS

The following application circuits are shown for a 3.3 V input supply commonly taken from the local, regulated micro-controller supply. For 5 V input voltages requiring different turn ratios refer to the transformer manufacturers and their websites listed in Table 4.

**Table 4. Transformer Manufacturers**

Coilcraft Inc.	<a href="http://www.coilcraft.com">http://www.coilcraft.com</a>
Halo-Electronics Inc.	<a href="http://www.haloelectronics.com">http://www.haloelectronics.com</a>
Murata Power Solutions	<a href="http://www.murata-ps.com">http://www.murata-ps.com</a>
Würth Electronics Midcom Inc	<a href="http://www.midcom-inc.com">http://www.midcom-inc.com</a>



# SN6501

SLLSEA0E – FEBRUARY 2012 – REVISED JANUARY 2013

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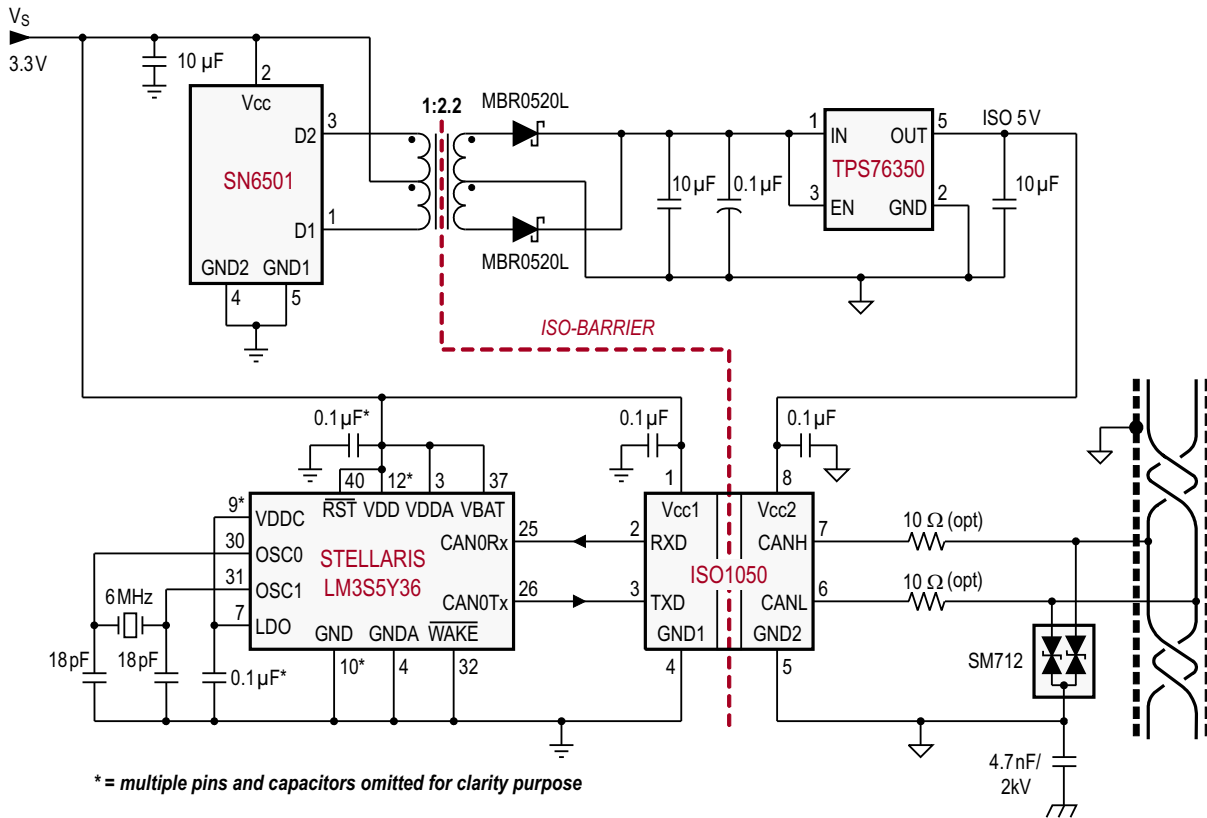


Figure 58. Isolated CAN Interface

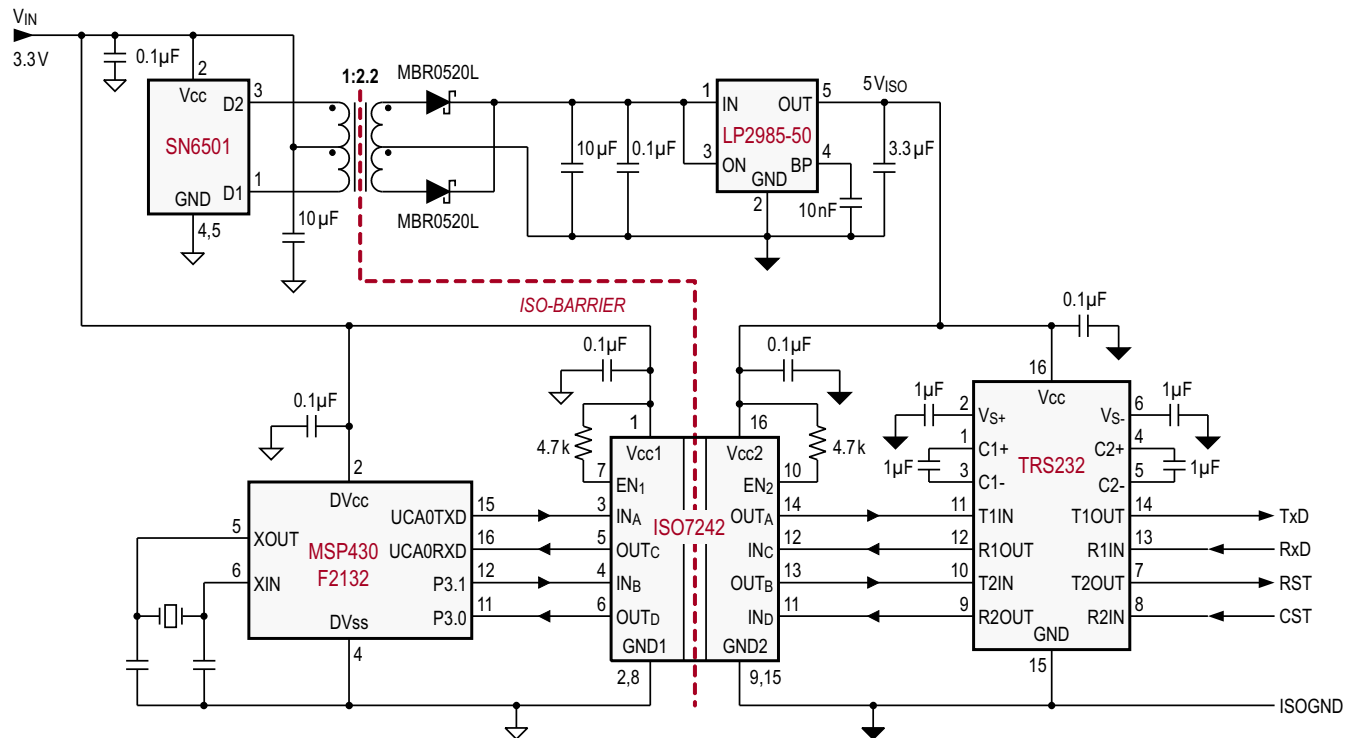


Figure 59. Isolated RS-232 Interface

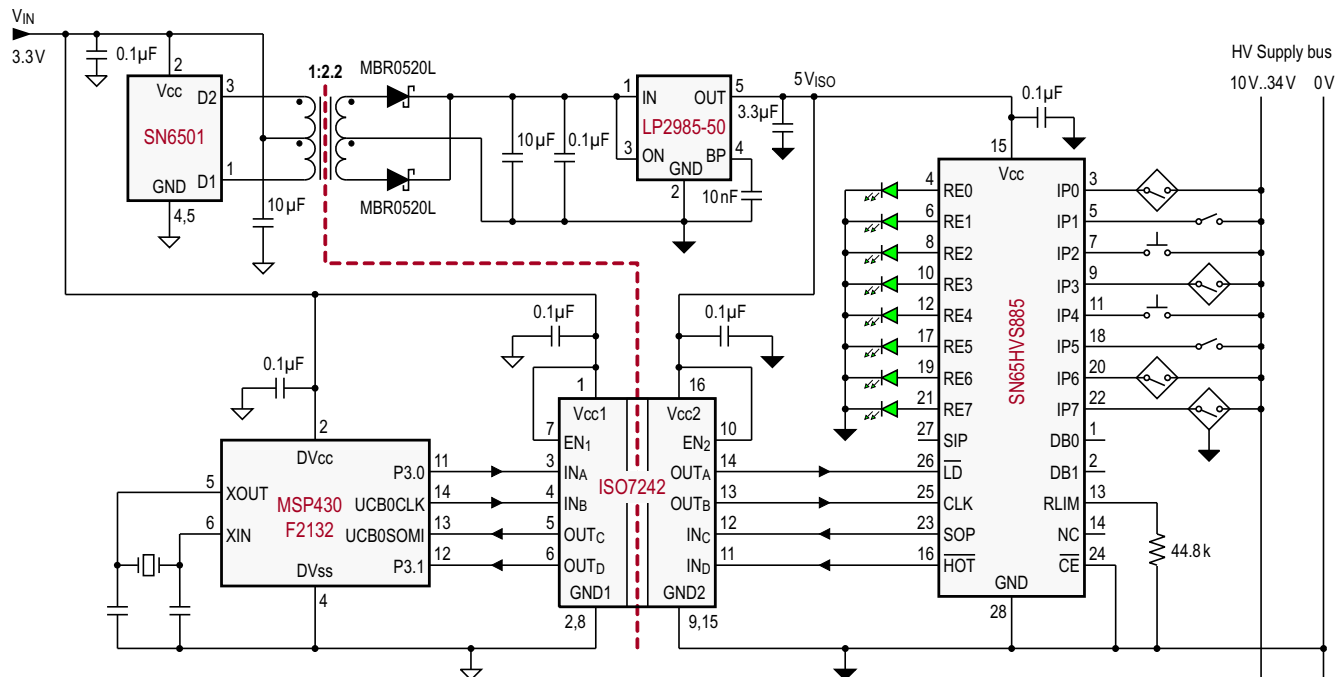


Figure 60. Isolated Digital Input Module

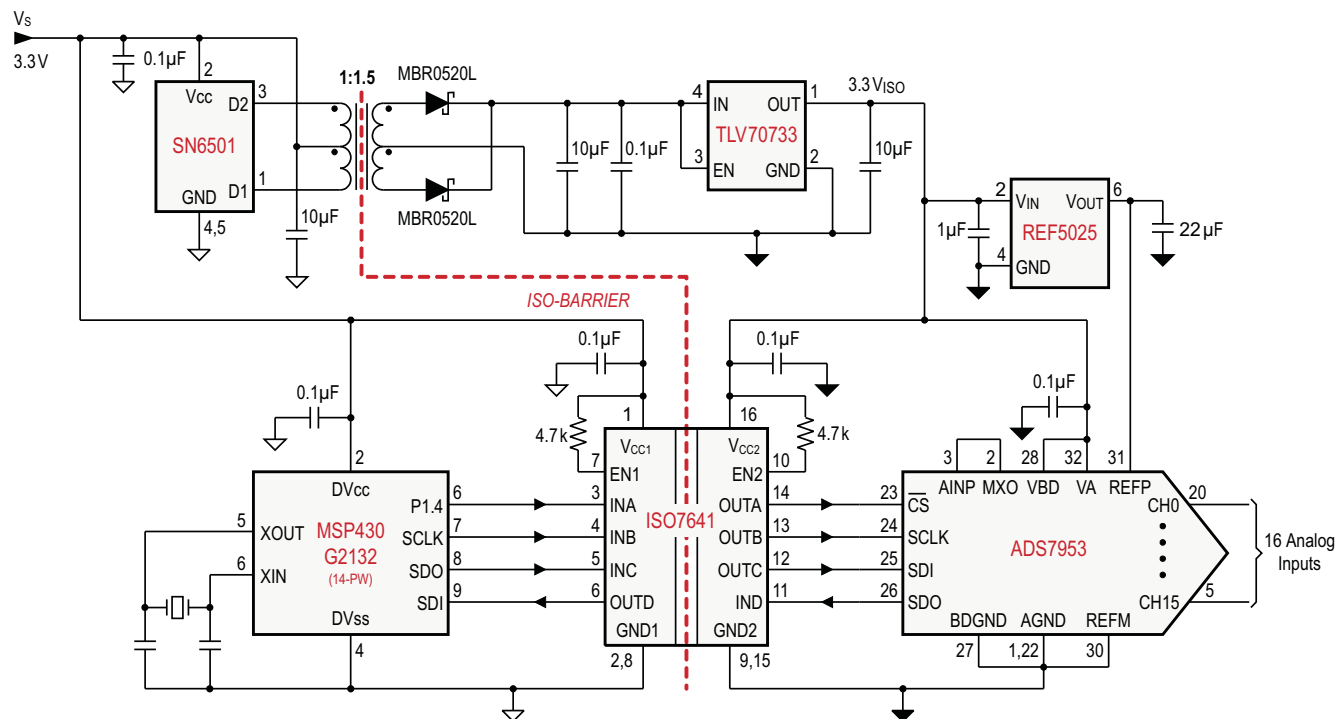
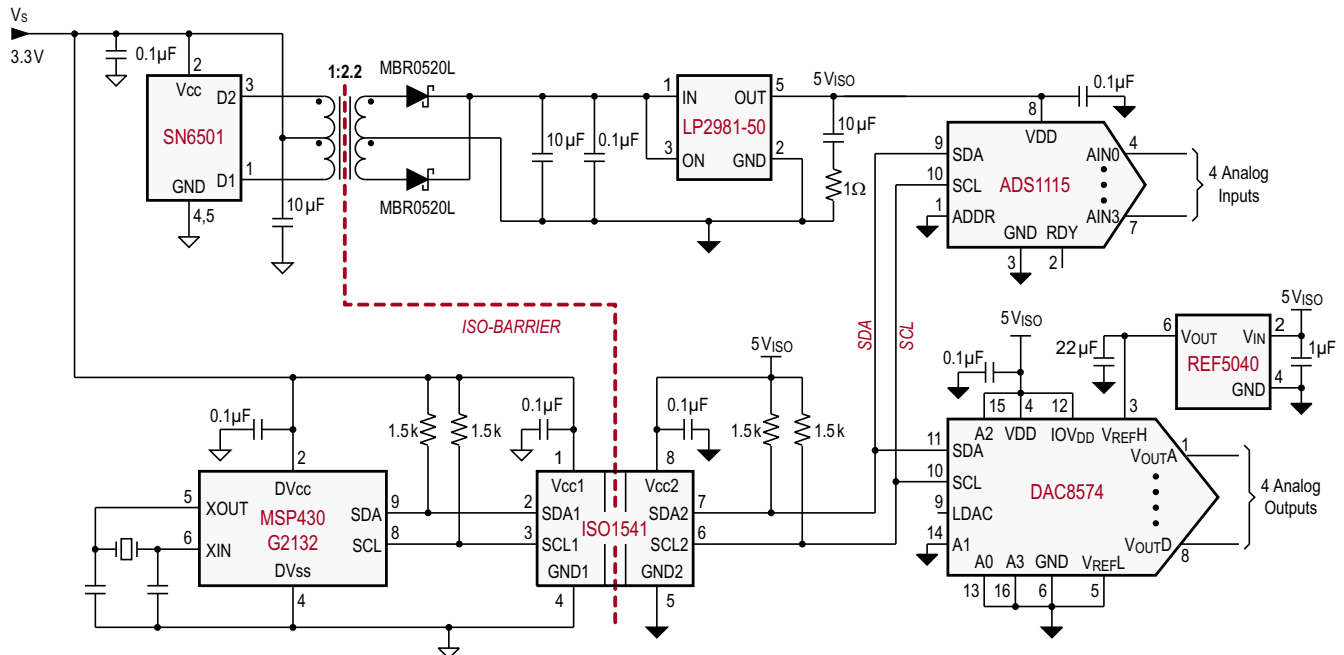


Figure 61. Isolated SPI Interface for an Analog Input Module with 16 Inputs

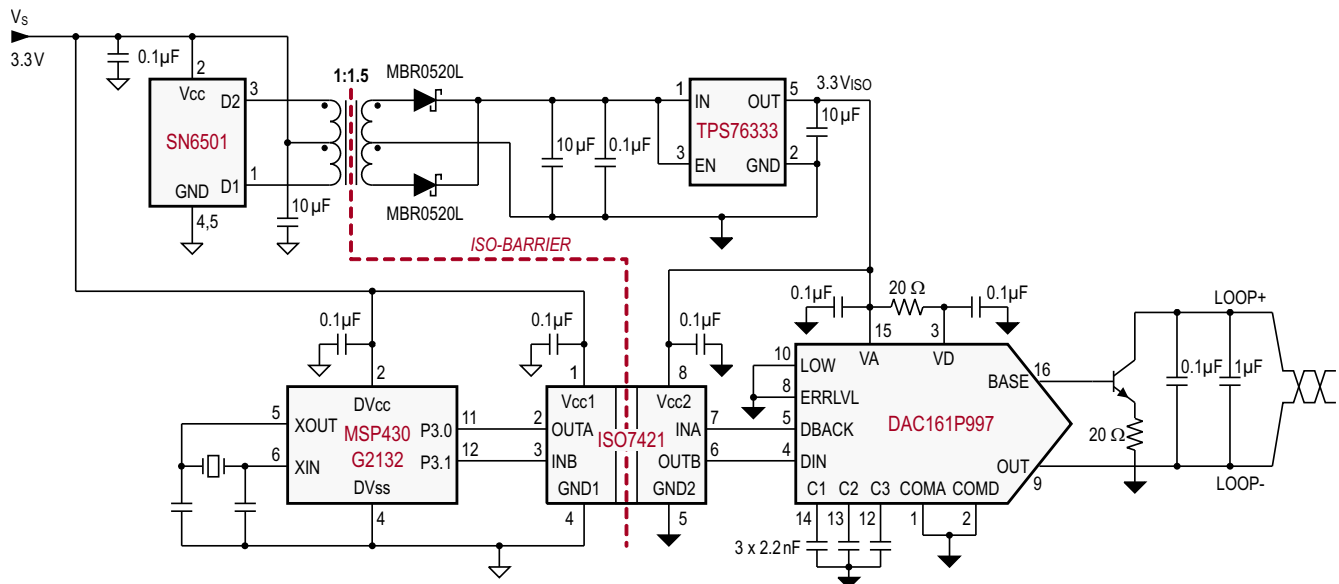
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**Figure 62. Isolated I2C Interface for an Analog Data Acquisition System with 4 Inputs and 4 Outputs**



**Figure 63. Isolated 4-20mA Current Loop**



## REVISION HISTORY

Changes from Original (February 2012) to Revision A	Page
• Changed the device From: Product Preview To: Production .....	1
• Added <a href="#">Figure 15</a> through <a href="#">Figure 18</a> .....	6
• Changed <a href="#">Equation 8</a> .....	18
• Changed <a href="#">Equation 9</a> .....	18
• Changed <a href="#">Table 4</a> , From: Wuerth-Elektronik / Midcom To: Wurth Electronics Midcom Inc .....	20
• Changed <a href="#">Figure 61</a> .....	23

Changes from Revision A (March 2012) to Revision B	Page
• Changed Feature From: Small 5-pin DBV Package To: Small 5-pin SOT23 Package .....	1
• Changed <a href="#">Figure 52</a> title .....	18

Changes from Revision B (March 2012) to Revision C	Page
• Changed the $f_{OSC}$ Oscillator frequency values .....	4
• Changed <a href="#">Equation 2</a> .....	17

Changes from Revision C (March 2012) to Revision D	Page
• Changed $f_{OSC}$ , Oscillator frequency To: $f_{SW}$ , D1, D2 Switching frequency .....	4
• Added graphs <a href="#">Figure 3</a> through <a href="#">Figure 8</a> .....	5
• Added <a href="#">Figure 35</a> through <a href="#">Figure 38</a> .....	10
• Changed the title of <a href="#">Figure 40</a> From: D1, D2 Oscillator Frequency vs Free-Air Temperature To: D1, D2 Switching Frequency vs Free-Air Temperature .....	10
• Added section: Recommended Transformers .....	18
• Changed the location and title of <a href="#">Figure 52</a> .....	18

Changes from Revision D (September 2012) to Revision E	Page
• Replaced <a href="#">Figure 14</a> .....	6

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN6501DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN6501DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

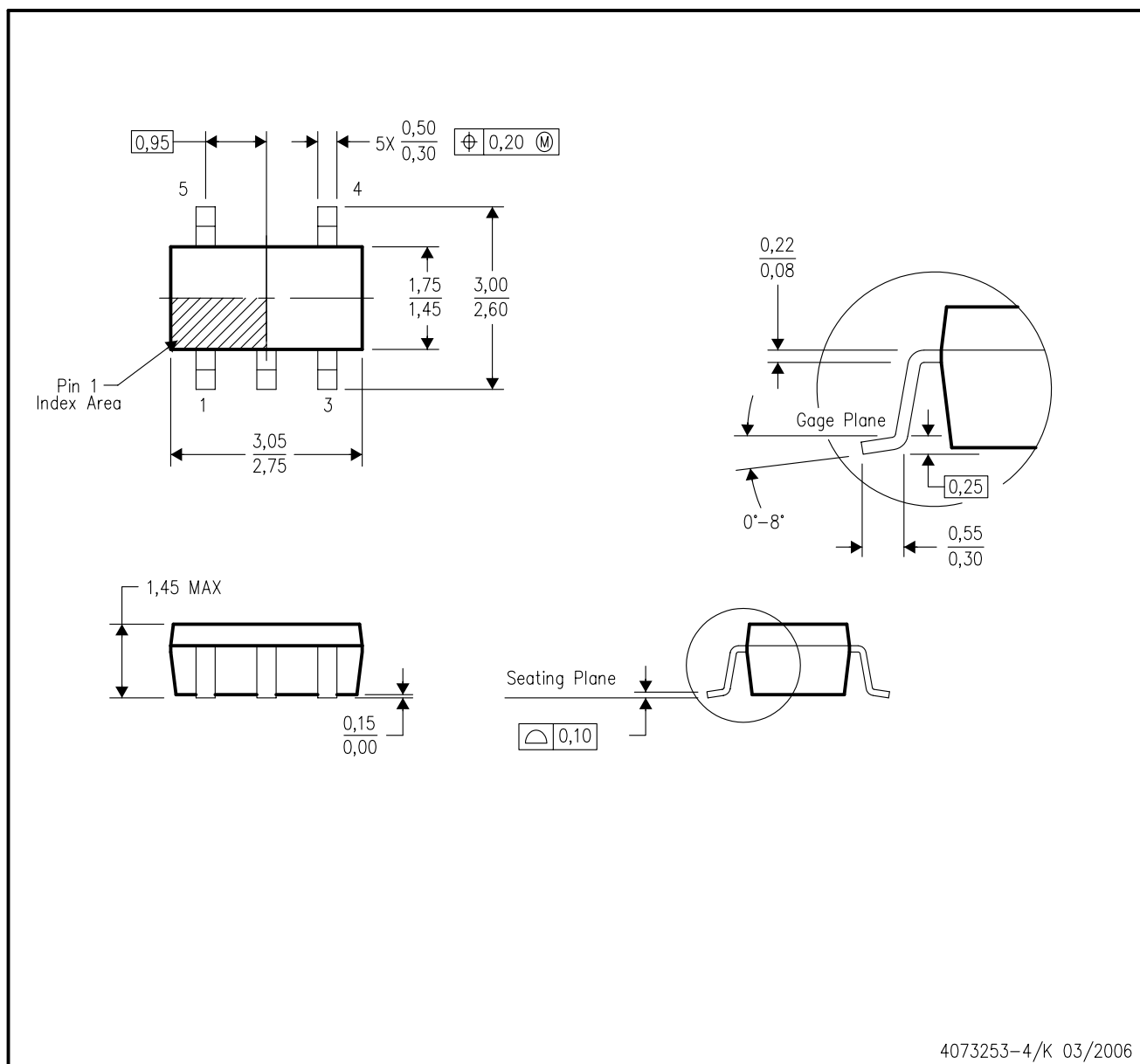
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## DBV (R-PDSO-G5)

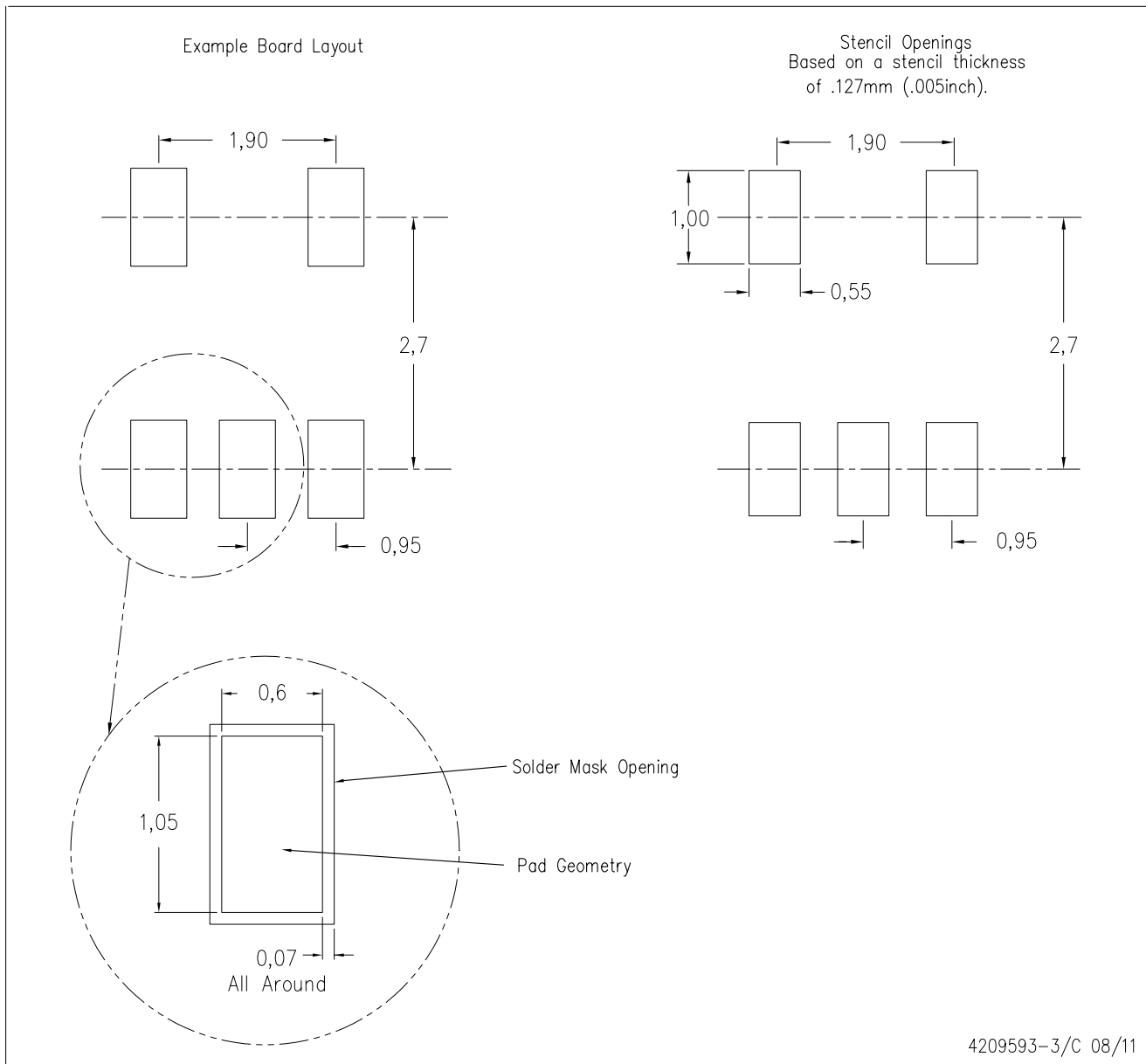
## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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