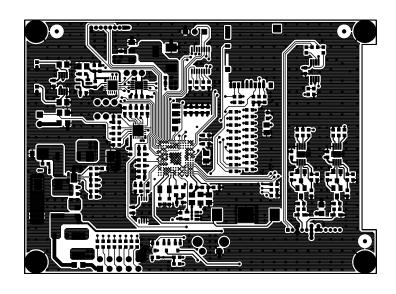
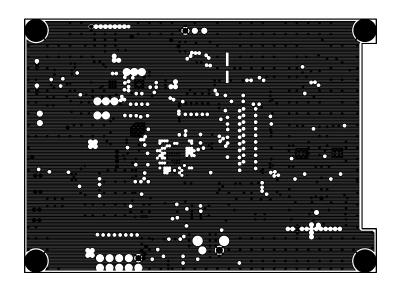
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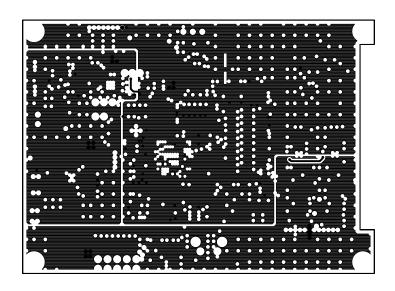
			* REVISION HISTORY *					
	 ∕\RT	IINE	REV	DATE	Designer			
•	- 1111					R 1.0	20. 03. 04	Jeong Sook, Kim
	,	,		,		R 2.0	20. 05. 08	Jeong Sook, Kim
B/D	CONDUCTTIVE_TFT	B/D Size	93 X 67 mm	4 LAYE	R			
Rev	2.0	Layer	Component Side	Design Unit	mil			
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			

CAM350/DFMSTREAM V 12.2 : Fri May 08 12:08:25 2020 - (Untitled) : art02.pho



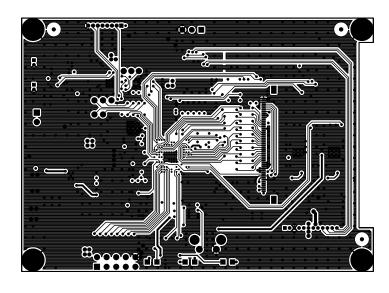
			* REVISION HISTORY *					
,	 ∕\RT	IIN	REV	DATE	Designer			
"	- ····					R 1.0	20. 03. 04	Jeong Sook, Kim
l <u> </u>						R 2.0	20. 05. 08	Jeong Sook, Kim
B/D	CONDUCTTIVE_TFT	B/D Size	93 X 67 mm	4 LAYE	R			
Rev	2.0	Layer	Layer 2 (gnd)	Design Unit	mil			
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			

CAM350/DFMSTREAM V 12.2 : Fri May 08 12:08:25 2020 - (Untitled) : art03.pho



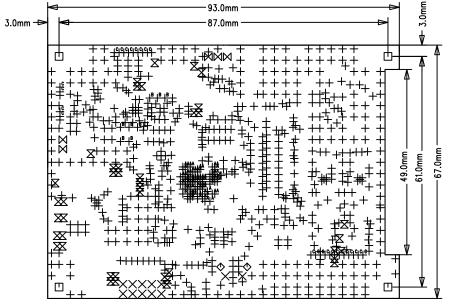
	Ant		REV	* REVISION	HISTORY *			
(∕\RT	LIN		20. 03. 04	•			
D /D		n /n o:	07 V C7	4 LAYE	n	R 2.0	20. 05. 08	Jeong Sook, Kim
B/U	CONDUCTTIVE_TFT	B/D Size	93 X 67 mm	4 LATE	K			
Rev	2.0	Layer	Layer 3 (power)	Design Unit	mil			
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			

CAM350/DFMSTREAM V 12.2 : Fri May 08 12:08:26 2020 - (Untitled) : art04.pho



	∕ RT	LINE		REV	REVISION DATE	HISTORY * Designer		
"			R 1.0	20. 03. 04	Jeong Sook, Kim			
R/n	CONDUCTTIVE_TFT	D /D C:	93 X 67 mm	4 LAYE	D	R 2.0	20. 05. 08	Jeong Sook, Kim
10,0	CONDUCTIVE_IFT	D/U SIZE	33 X 07 IIIIII	TEATE	<u>`</u>			
Rev	2.0	Layer	Solder Side	Design Unit	mil			
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			

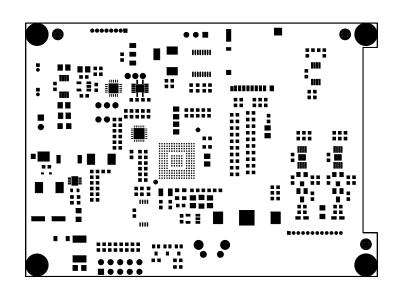
CAM350/DFMSTREAM V 12.2 : Fri May 08 12:08:26 2020 - (Untitled) : dd0124.pho



					* REVISION	HISTORY *		
	 ∕\RT	IINI	REV	DATE	Designer			
						R 1.0	20. 03. 04	Jeong Sook, Kim
D /D	I	- /	07 V 07	4 1 4 4 7 5		R 2.0	20. 05. 08	Jeong Sook, Kim
R/D	CONDUCTTIVE_TFT	B/D Size	93 X 67 mm	4 LAYE	K			
Rev	2.0	Layer	Drill Drawing	Design Unit	mil			
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			

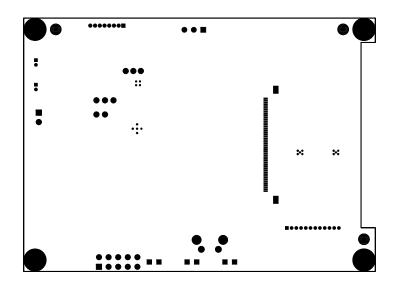
SIZE	QTY	SYM	PLATED	TOL
11.81	718	+	YES	+/-0.0
39.37	12	×	YES	+/-0.0
125.98	4		YES	+/-0.0
51.18	2	\Diamond	YES	+/-0.0
23.62	41	X	YES	+/-0.0
35	5	\boxtimes	YES	+/-0.0
7.87	80	+	YES	+/-0.0
40	8	+B	YES	+/-0.0
19.69	24	4	YES	+/-0.0

CAM350/DFMSTREAM V 12.2 : Fri May 08 12:08:26 2020 - (Untitled) : sm0121.pho



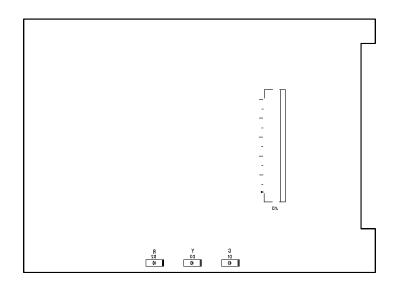
ſ											
I		_					* REVISION HISTORY *				
l		 ∕\RT	IIN				REV	DATE	Designer		
l							R 1.0	20. 03. 04	Jeong Sook, Kim		
ı							R 2.0	20. 05. 08	Jeong Sook, Kim		
l	B/D	CONDUCTTIVE_TFT	B/D Size	93 X 67 mm	4 LAYE	R			, .		
l	Rev	2.0	Layer	Solder Mask Top	Design Unit	mil					
l	Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T					

CAM350/DFMSTREAM V 12.2 : Fri May 08 12:08:26 2020 - (Untitled) : sm0428.pho



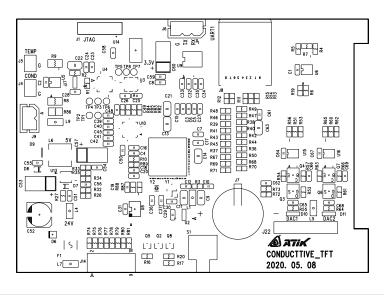
	A n t	1 1811	•			REV	* REVISION	HISTORY *
	/\ RT	LINI				R 1.0	20. 03. 04	
B/D	CONDUCTTIVE_TFT	B/D Size	93 X 67 mm	4 LAYE	R	R 2.0	20. 05. 08	Jeong Sook, Kim
Rev	2.0	Layer		Design Unit	mil			
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			

CAM350/DFMSTREAM V 12.2 : Fri May 08 12:08:26 2020 - (Untitled) : ssb0429.pho



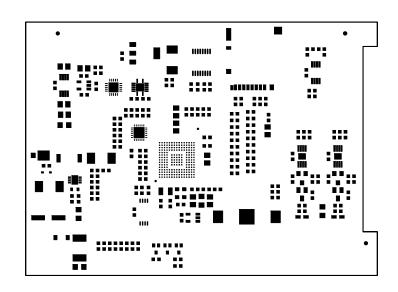
	_∕\RT	LINI		REV	REVISION DATE	HISTORY * Designer		
"				20. 03. 04	_ ,			
B/D	CONDUCTTIVE_TFT	B/D Size	93 X 67 mm	4 LAYE	R	R 2.0	20. 05. 08	Jeong Sook, Kim
Rev	2.0	Layer	Silk Screen Bottom	Design Unit	mil			
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			

CAM350/DFMSTREAM V 12.2 : Fri May 08 12:08:26 2020 - (Untitled) : sst0126.pho



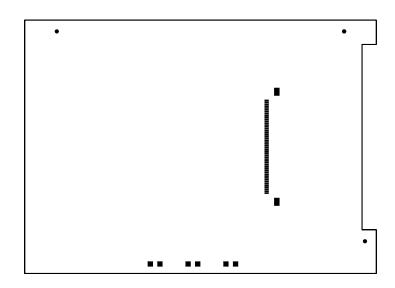
	∕ RT	IINI		REV	* REVISION DATE	HISTORY *		
(\\\.	LIIV		R 1.0	20. 03. 04	Jeong Sook, Kim		
B/D	CONDUCTTIVE_TFT	B/D Size	93 X 67 mm	4 LAYE	R	R 2.0	20. 05. 08	Jeong Sook, Kim
Rev	2.0	Layer	Silk Screen Top	Design Unit	mil			
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			

CAM350/DFMSTREAM V 12.2 : Fri May 08 12:08:26 2020 - (Untitled) : smd001023.pho



			* REVISION HISTORY *					
,	 ∕\RT	IIN	REV	DATE	Designer			
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l						R 2.0	20. 05. 08	Jeong Sook, Kim
B/D	CONDUCTTIVE_TFT	B/D Size	93 X 67 mm	4 LAYE	R			
Rev	2.0	Layer		Design Unit	mil			
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			

CAM350/DFMSTREAM V 12.2 : Fri May 08 12:08:26 2020 - (Untitled) : smd004022.pho



	▲ ART LINE							HISTORY * Designer
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D /D		- /	07 4 07	4 LAYE		R 2.0	20. 05. 08	Jeong Sook, Kim
B/D	CONDUCTTIVE_TFT	B/D Size	93 X 67 mm	4 LATE	K			
Rev	2.0	Layer		Design Unit	mil			
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			