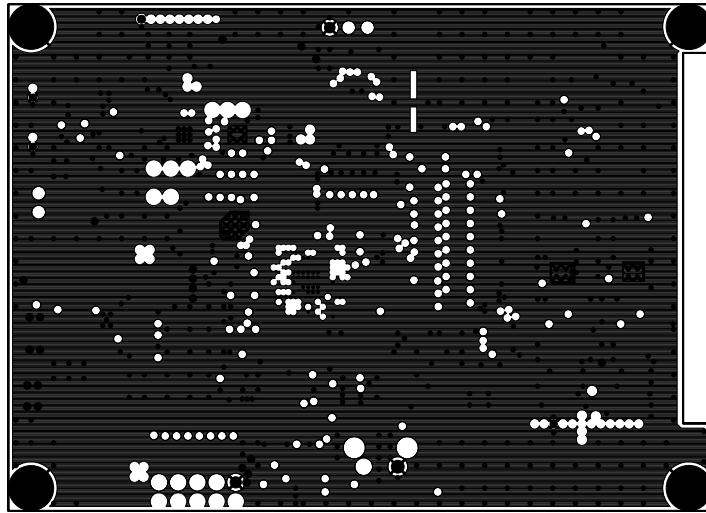

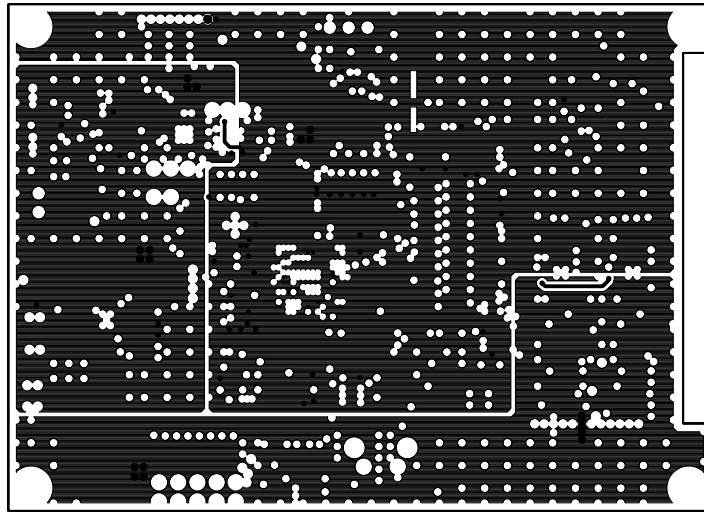

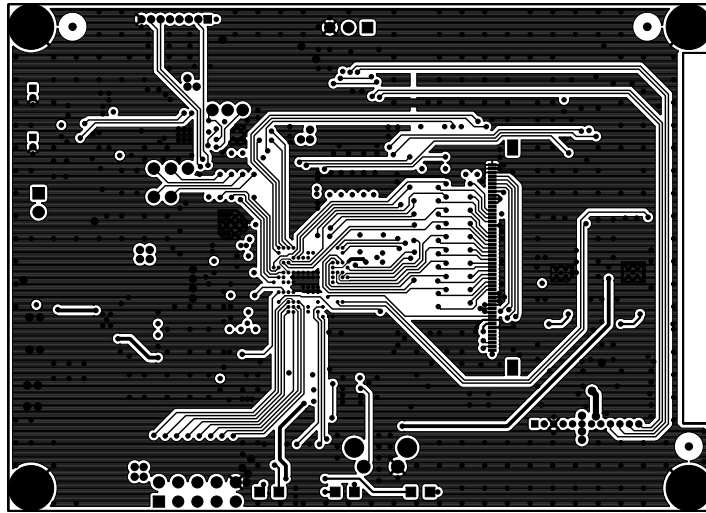
						* REVISION HISTORY *			
						REV	DATE	Designer	
B/D	CONDUCTIVE_TFT	B/D Size	93 X 67 mm	4 LAYER			R 1.0	20. 03. 04	Jeong Sook, Kim
Rev	2.0	Layer	Component Side	Design Unit	mil		R 2.0	20. 05. 08	Jeong Sook, Kim
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T				




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B/D	CONDUCTIVE_TFT	B/D Size	93 X 67 mm	4 LAYER		REV	DATE	Designer
Rev	2.0	Layer	Layer 2 (gnd)	Design Unit	mil	R 1.0	20. 03. 04	Jeong Sook, Kim
						R 2.0	20. 05. 08	Jeong Sook, Kim
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			

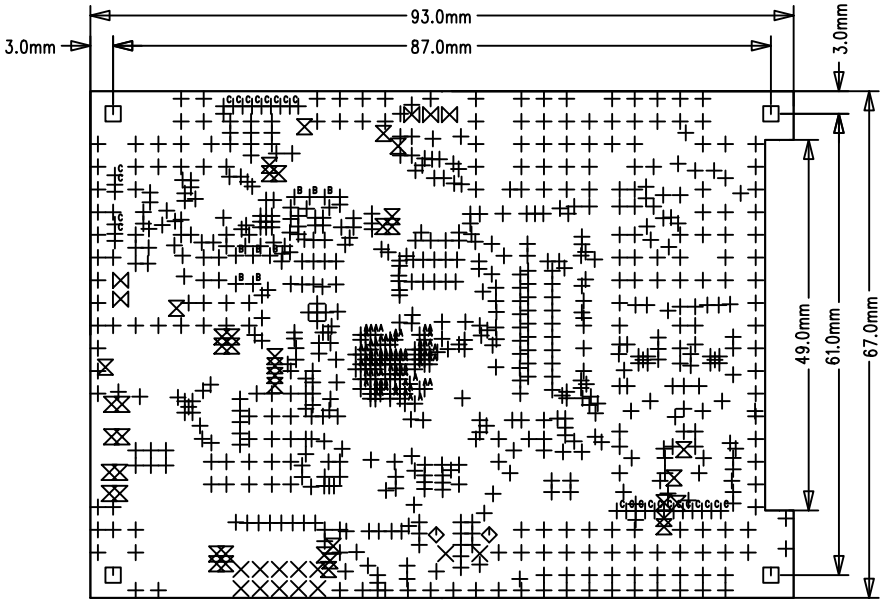


						* REVISION HISTORY *		
REV		DATE		Designer				
R 1.0		20. 03. 04		Jeong Sook, Kim				
R 2.0		20. 05. 08		Jeong Sook, Kim				




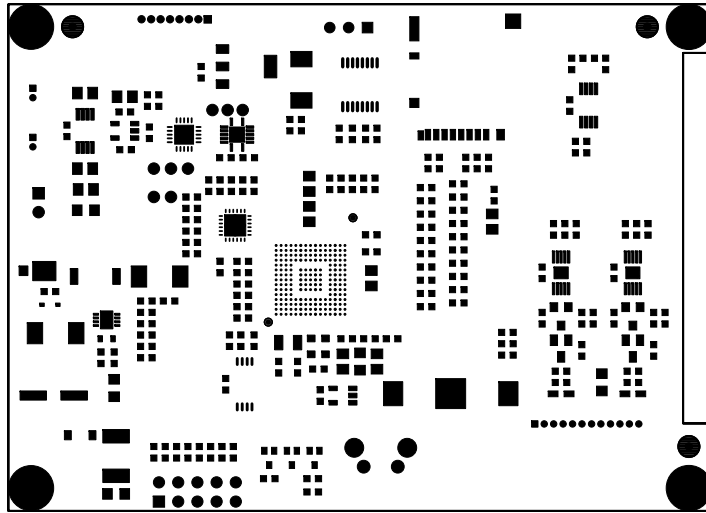
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REV		DATE		Designer			
R 1.0		20. 03. 04		Jeong Sook, Kim			
R 2.0		20. 05. 08		Jeong Sook, Kim			


B/D	CONDUCTIVE_TFT	B/D Size	93 X 67 mm	4 LAYER	
Rev	2.0	Layer	Solder Side	Design Unit	mil
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T



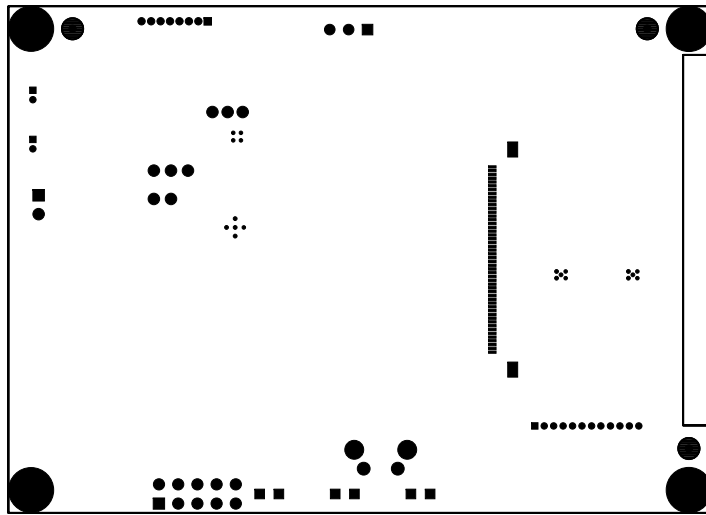
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39.37	12	×	YES	+/-0.0
125.98	4	□	YES	+/-0.0
51.18	2	◇	YES	+/-0.0
23.62	41	⊗	YES	+/-0.0
35	5	⊗	YES	+/-0.0
7.87	80	+ ^A	YES	+/-0.0
40	8	+ ^B	YES	+/-0.0
19.69	24	+ ^C	YES	+/-0.0


						* REVISION HISTORY *		
B/D		CONDUCTIVE_TFT	B/D Size	93 X 67 mm	4 LAYER			
Rev	2.0	Layer	Drill Drawing	Design Unit	mil			
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			
REV		DATE		Designer				
R 1.0		20. 03. 04		Jeong Sook, Kim				
R 2.0		20. 05. 08		Jeong Sook, Kim				

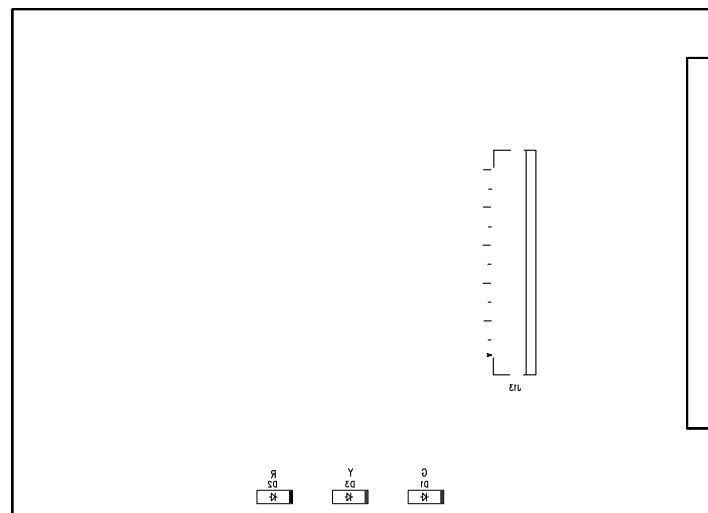


						* REVISION HISTORY *		
REV		DATE		Designer				
R 1.0		20. 03. 04		Jeong Sook, Kim				
R 2.0		20. 05. 08		Jeong Sook, Kim				


B/D	CONDUCTIVE_TFT	B/D Size	93 X 67 mm	4 LAYER	
Rev	2.0	Layer	Solder Mask Top	Design Unit	mil
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T



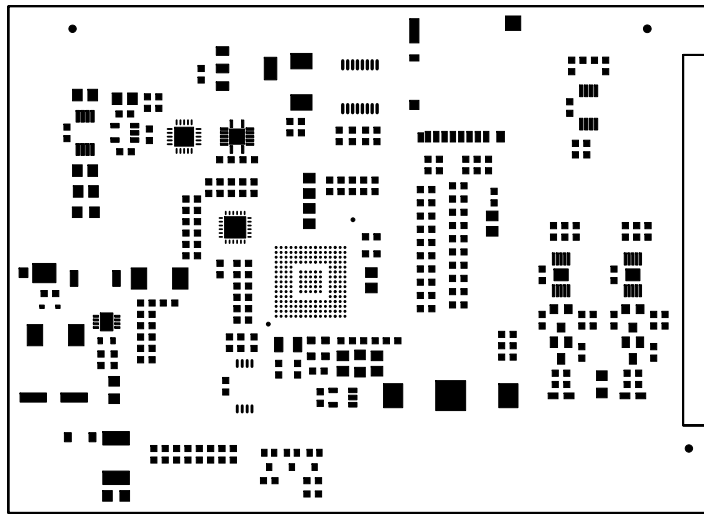
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B/D	CONDUCTIVE_TFT	B/D Size	93 X 67 mm	4 LAYER		REV	DATE	Designer
Rev	2.0	Layer		Design Unit	mil	R 1.0	20. 03. 04	Jeong Sook, Kim
						R 2.0	20. 05. 08	Jeong Sook, Kim
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T			




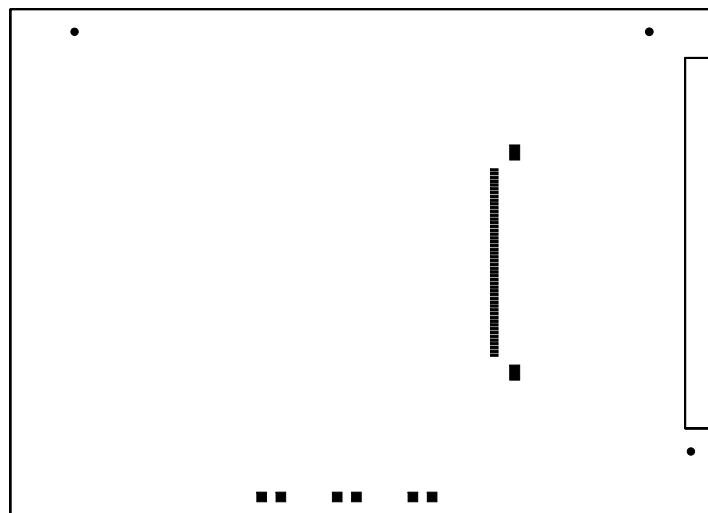
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B/D	CONDUCTIVE_TFT	B/D Size	93 X 67 mm	4 LAYER		REV	DATE	Designer
Rev	2.0	Layer	Silk Screen Bottom	Design Unit	mil	R 1.0	20. 03. 04	Jeong Sook, Kim
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T	R 2.0	20. 05. 08	Jeong Sook, Kim


						* REVISION HISTORY *		
REV		DATE		Designer				
R 1.0		20. 03. 04		Jeong Sook, Kim				
R 2.0		20. 05. 08		Jeong Sook, Kim				

B/D	CONDUCTIVE_TFT	B/D	Size	93 X 67 mm	4 LAYER	
Rev	2.0	Layer	Silk Screen Top	Design Unit	mil	
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T	



					* REVISION HISTORY *		
REV	DATE	Designer					
R 1.0	20. 03. 04	Jeong Sook, Kim					
R 2.0	20. 05. 08	Jeong Sook, Kim					
B/D	CONDUCTIVE_TFT	B/D Size	93 X 67 mm	4 LAYER			
Rev	2.0	Layer		Design Unit	mil		
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T		



						* REVISION HISTORY *		
B/D	CONDUCTIVE_TFT	B/D Size	93 X 67 mm	4 LAYER		REV	DATE	Designer
Rev	2.0	Layer		Design Unit	mil	R 1.0	20. 03. 04	Jeong Sook, Kim
Data	2020. 05. 08	Designer	Jeong Sook, Kim	Pcb Thickness	T	R 2.0	20. 05. 08	Jeong Sook, Kim