Design and analysis of Low power hybrid full adder for array multiplier in 90nm technology

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***Abstract*— The majority of full adder (FA) circuits are constructed using three distinct modules and a hybrid logic design. A key advantage of hybrid FA cells is that each module can be individually optimized to enhance circuit performance. This work proposes a high-performance 1-bit hybrid FA cell designed using transmission gate logic (TG) and pass transistor logic (PTL). The proposed FA circuit is optimized with 20 transistors to achieve low power consumption and minimal delay. The design is implemented in 90nm CMOS technology using Cadence Virtuoso, and its performance metrics are evaluated against existing FA architectures. Comparative analysis demonstrates that the proposed FA achieves superior efficiency in Power Delay Product (PDP), propagation delay, and power consumption. The FA is further integrated into 4-bit and 8-bit array multipliers, showcasing significant performance improvements for arithmetic circuits. Additionally, Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification validate the correctness of the proposed designs.**

Keywords*— *Full voltage swing XOR–XNOR Full adder Transmission gate Pass transistor logic

I. INTRODUCTION

One of the key characteristics of electronic devices, such as Internet of Things (IoT) devices, cellular phones, and personal digital assistants (PDAs), is high performance. To handle the high operating frequency and intricate designs, high-speed circuits are required for optimal operation. Digital signal processors and microprocessors use the Arithmetic and Logic Unit (ALU) as a primary block in application-specific electronic devices. The key component of the ALU circuit is the adder module. FA is also the basic component of many arithmetic circuit functions, such as comparators, multipliers, and compressors. Therefore, one of the main topics of study for VLSI researchers to increase the performance of the digital system is the performance of the adder circuits. Different static logic styles are used, and these logic styles are generally divided into two groups: conventional logic and hybrid logic styles.

The entire FA concept is implemented using just one logic in the traditional style-based full adder. The classical method, which uses pull-up (PMOS) and pull-down (NMOS) networks, is given an example by the complementary metal-oxide-semiconductor (CMOS) based FA. This method realizes the entire adder using 28 transistors. This circuit is resilient against transistor sizing and voltage scaling, and it delivers complete voltage swing at all internal and external nodes. However, the main disadvantage of this FA design is the presence of PMOS block, which degrades performance because of PMOS's limited mobility. To boost performance, PMOS transistors are scaled up.

The complementary pass-transistor logic style (CPL) is another traditional method for implementing the FA architecture. The FA design is implemented using a twin rail structure with 32 transistors in this CPL logic architecture. This construction provides good driving capability, high speed, and a full voltage swing at the output node. However, this circuit's primary drawback is its high-power dissipation, which is caused by the cell's numerous internal nodes. The complex layout caused by the uneven transistor arrangement is another issue with this FA design.

The FA design can also be realized by the classical method of pass transistor logic (PTL). However, when logic "1" and logic "0" travel via NMOS and PMOS transistors, respectively, the threshold loss issue occurs. Consequently, a new logic style—the transmission gate (TG) logic style—is employed to address the threshold problem. Twenty transistors are used to implement the FA utilizing the TG logic type. The primary drawback of this kind of adder is its poor driving capabilities, despite its low power consumption.

To overcome the limitations of conventional FA architectures, researchers have developed hybrid logic-based FA designs, which combine multiple logic styles to achieve an optimal balance between speed, power, and area. By integrating different logic techniques, these designs aim to enhance power efficiency, delay performance, and overall circuit compactness.

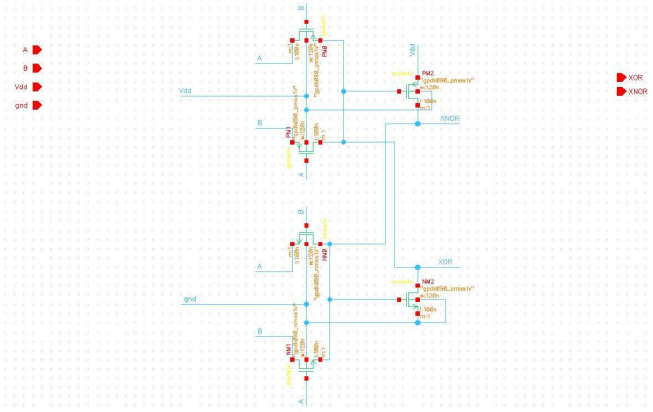
Hybrid FA structures consist of three distinct modules: an XOR-XNOR generation module, a SUM module, and a CARRY module. The XOR-XNOR module generates full-swing XOR and XNOR signals, ensuring glitch-free operations. The SUM module is designed to minimize delay and power consumption, while the CARRY module optimizes transistor arrangements to reduce switching delay and power dissipation.

Hybrid FA architectures allow individual module optimization for flexible performance tuning. However, cascading multiple stages can degrade driving capability, impacting signal transmission and timing. Despite this, they offer improved power efficiency, speed, and area utilization, making them ideal for VLSI applications like multipliers, DSPs, and low-power computing.

This paper presents a high-performance hybrid FA design using transmission gate (TG) and pass transistor logic (PTL) for low power, reduced delay, and improved area efficiency. Implemented in 90nm CMOS technology and analyzed in Cadence Virtuoso, the proposed FA is integrated into 4-bit and 8-bit array multipliers, demonstrating superior efficiency and performance. DRC and LVS verification ensure design correctness.

II. REVIEW XOR - XNOR CIRCUITS

The XOR-XNOR circuit can be designed in two main ways, according to the literature. The initial method generates the XOR function first, followed by using an inverter to produce the XNOR function. The output of the second and third modules has glitches and false switching because of the XOR and XNOR signals being provided independently. The delay variance among XOR-XNOR signals could be reduced in different designs by using a different technique that generates XOR-XNOR signals simultaneously at the output.



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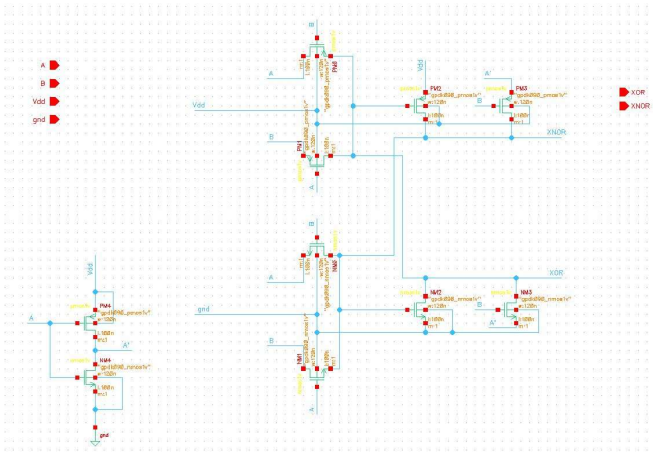

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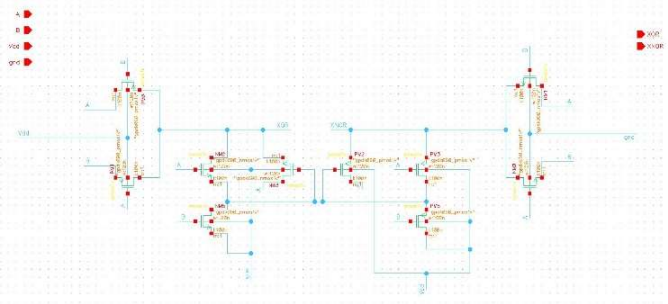


(c)

Fig. 1. XOR/XNOR circuit (a). Test1 (b). Test2 (c). Test3.

In Fig. 1. (a), an XOR-XNOR circuit that Test1 proposed is modified by different researchers to enhance its functionality. The CPL and feedback restorer transistors are employed in this setup, and just six transistors are needed to provide full swing at the XOR-XNOR outputs. The two-step process in this design causes a delayed response issue when the inputs AB = 00 and AB equals 11 are applied. Test2 presents an additional implementation of the XOR-XNOR circuit. As shown in Fig. 1(b), this design adds one NMOS and one PMOS transistor at the output node (XOR and XNOR), which have an inverted input at the source site. Additionally, this design reported a larger delay issue because of the two-step transition. Test 3 suggested an XOR-XNOR circuit based on ten transistors. As shown in Fig. 1(c), they used the CPL and restorer circuit to resolve a higher delay in their design. Furthermore, a separate generation of XOR and XNOR designs was made to enhance the performance of the XOR-XNOR circuit. Ten transistors are used to implement the XOR-XNOR approach, as shown in Fig. 2.

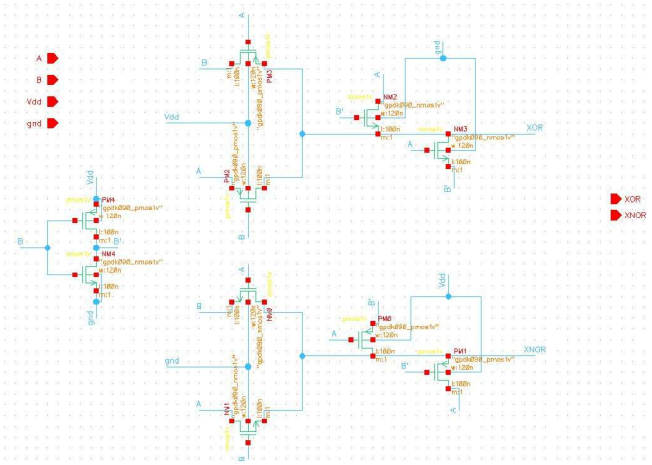


Fig. 2. XOR-XNOR full swing logic generation.

The suggested XOR-XNOR design is implemented with a single static inverter and CPL logic. Both XOR and XNOR outputs are separately realized in the suggested circuit. The XOR architecture makes use of two PMOS (PM2 & PM3) and two NMOS (NM2 & NM3). Similarly, the XNOR design uses two PMOS (PM0 & PM1) and two NMOS (NM0 & NM1). Transistors PM2 and PM3 are linked in parallel to form PTL logic at the XOR design. Furthermore, NM2 and NM3 transistors are also created using pass transistors, in which the gate and source are connected to inverted input B, respectively. However, transistors NM0 and NM1 are connected in parallel as PTL on the XNOR side, while transistors PM0 and PM1 are also implemented using pass transistors; the source and gate are connected to inverted input B, respectively. The next part provides a summary of the various input combinations to help understand how the suggested design works.

The PM3, NM1, PM0, and PM1 transistors turn "ON" when the input AB equals "01." The logic "1" and logic "0" are thus provided at the output node (XOR-XNOR) by PM3 and NM1 transistor. Transistors PM0 and PM1 simultaneously turn "ON" and send weak logic (-Vthp) to the XNOR output. Accordingly, PM2, NM2, NM3, and NM0 transistors receive "ON" when the input AB equals "10," and PM2 and NM0 transistors separately pass logic "1" and logic "0" at the output node (XOR-XNOR). When transistors NM2 and NM3 simultaneously turn "ON," they pass the VDD-Vthn (weak logic) on the XOR node. Since the outputs can use the entire swing path, the weak logic outputs have no effect on the output swing when the input AB equals "01" and "10".

Transistors PM3, PM2, PM0, and NM2 become "ON" when input AB equals "00". While NM2 provides a complete logic "1" on the XOR node and simultaneously causes the

PM0 transistor to switch "ON," PM3 and PM2 pass -Vthp (weak logic) at the XOR output. Likewise, transistors NM3, NM0, NM1, and PM1 turn "ON" when input AB equals "11". On the XNOR node, the NM0 and NM1 transistors transmit weak logic, VDD-Vthn. On the other hand, transistor PM1 passes the full logic "1" to the XNOR node while transistor (NM3) concurrently becomes "ON," causing the logic "1" to be passed at the XNOR node. With full output swing and strong driving power at every node, this circuit enables reduced power consumption, increased speed, and a reduced number of transistors.

III. PROPOSED FULL ADDER DESIGN

Three distinct modules are used to implement the suggested FA circuit as shown. The sum and carry outputs are first produced by the second and third modules, respectively. Second, each module is constructed separately to maximize the circuit's performance in terms of area, latency, and power consumption. The next section discusses these modules.

A. Module II

The equation below illustrates how the input carry signal and the intermediate signals (XOR and XNOR) are used to build the second module (SUM circuit) of FA. This unit's primary function is to supply the following modules with sufficient driving power.

$$SUM = X \oplus CIN = XOR.CIN' + XNOR.CIN \quad (1)$$

Two transmission gates (TG) are used in Module II (SUM circuit), where the PM0 and NM0 transistor gates are coupled to the XNOR and XOR signals produced by the first module. These transistors' source and drain nodes (PM0 and NM0) are connected to the SUM output and CIN′, respectively. On the other hand, XOR and XNOR signals are used to gate the second TG gate (PM1 & NM1). These PM1 and NM1 transistors source and drain nodes are coupled by the input carry signal (CIN) and SUM, respectively.

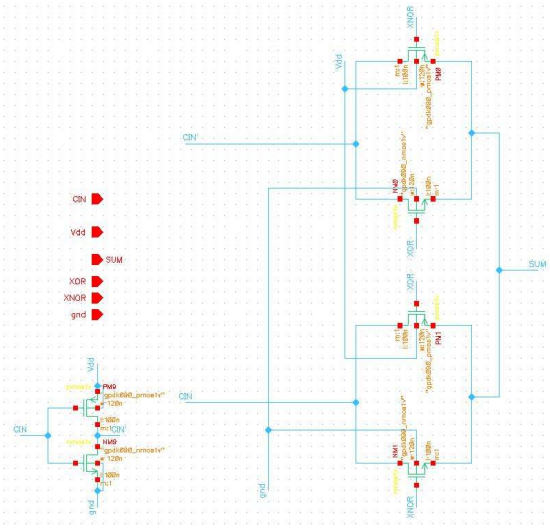


Fig. 3. Module II (SUM).

B. Module III

The carry module (COUT) is the third module in the suggested FA circuit. The TG logic and MUX circuits are used to realize this module. When A = B, COUT = B; otherwise, COUT = CIN.

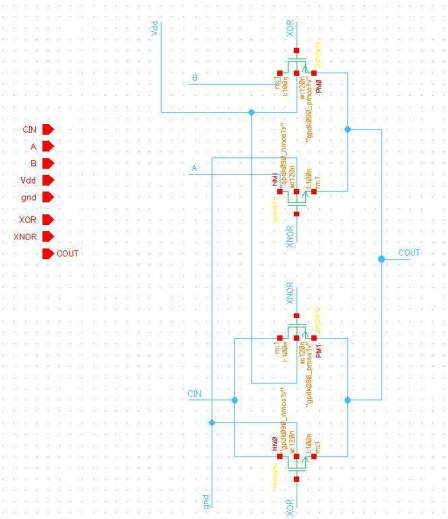
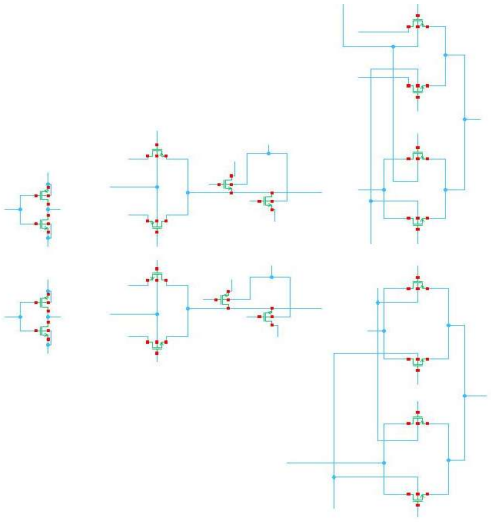


Fig. 4. Module III (COUT).

C. Full adder cell

Using 20 transistors, a novel one-bit FA circuit was created, as shown in Fig. 5. Figs. 2–4 show how the suggested adder is implemented using the XOR-XNOR circuit, SUM module, and CARRY module, respectively. Figure 1(c) shows how these three modules are connected to one another. Two TG gates are used in this circuit to implement the SUM module. The XNOR and XOR signals from the first module are used to gate the PM0, PM1, NM0, and NM1 transistors. Both the PM0 and NM0 transistors turn "ON" when XOR is on logic "1" (XNOR is at logic "0"), and the SUM output is directly connected to the inverted input carry signal (CIN′). If CIN is in logic "0," then CIN′ is in logic "1," and this logic travels to the output via transistors PM0 and NM0. Both the PM1 and NM1 transistors turn "ON," however, when XOR receives logic "0" and XNOR receives logic "1," and the SUM output is linked to the input carry signal (CIN). TG and MUX are used to implement the CARRY module in the suggested FA circuit. Both the PM0 and NM1 transistors switch "ON" and send the values of B and A to the output node (COUT) when the XOR signal reaches logic "0" at that moment and the XNOR signal reaches logic "1." In another case, the PM1 and NM0 transistors become "ON" and send the input carry signal (CIN) to the output node simultaneously when the XOR node is at logic "1" and the XNOR is at logic "0." The schematic of 1-bit FA designs is displayed in Fig. 5.



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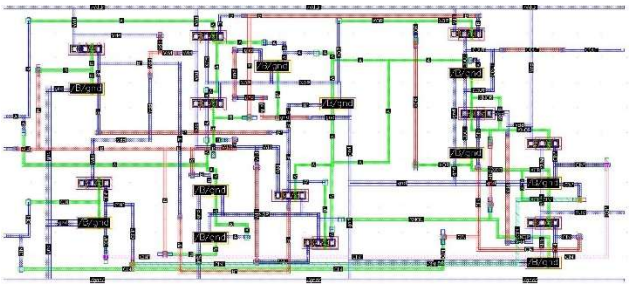


(b)

Fig. 5.a) Proposed 1-bit hybrid Full adder. b) Layout of FA

IV. 4-Bit and 8-Bit Array Multiplier Design

The 4-bit array multiplier is implemented using four 1-bit hybrid FA cells arranged in an array, optimizing area and power while maintaining high-speed operation. The design consists of four rows of FA cells, efficiently handling bit-wise multiplication and addition.

Similarly, the 8-bit array multiplier is constructed using the same hybrid FA cells but requires additional stages and carry propagation paths to accommodate the increased bit width. The primary difference lies in the increased number of rows and columns needed for higher-bit multiplication.

Both the FA and the multipliers underwent DRC and LVS verification in Cadence Virtuoso, ensuring design correctness and manufacturability. The integration of the hybrid FA enhances power efficiency, reduces delay, and optimizes area, making it suitable for arithmetic-intensive applications.

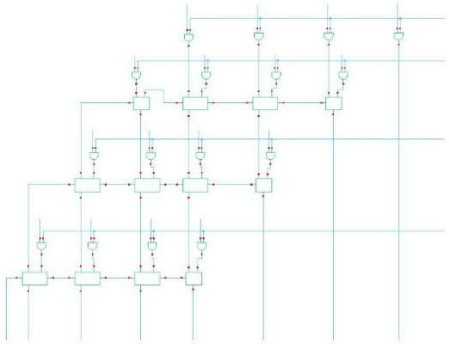
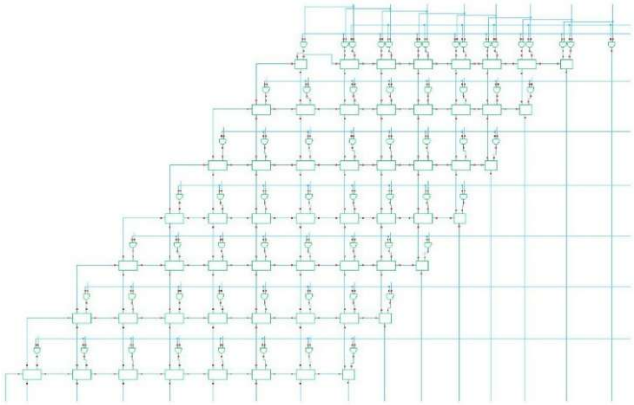


Fig. 6. Proposed 4-bit Array multiplier design



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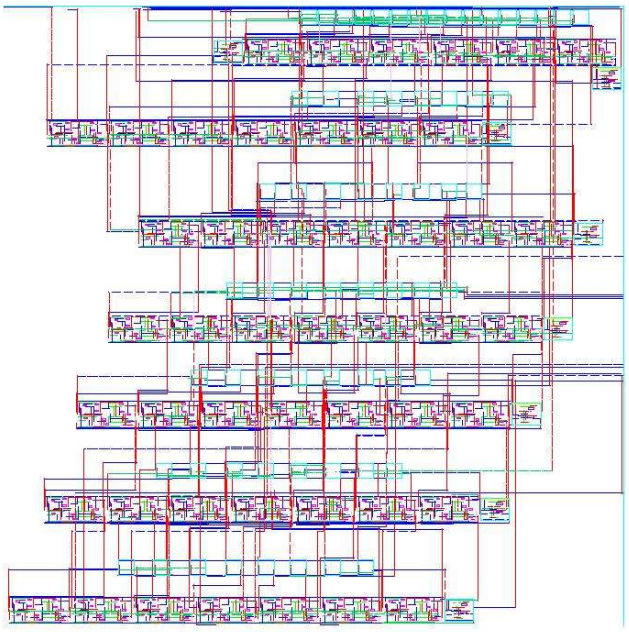


(b)

Fig. 7. a) Proposed 8-bit Array multiplier design b) Layout of 8 Bit Array multiplier

To evaluate the post-layout performance of the 8-bit array multiplier, RC parasitic extraction was performed using standard EDA tools. The layout was processed to extract parasitic resistance and capacitance values associated with the interconnects and device junctions. This extraction results in a detailed netlist containing resistive and capacitive elements that significantly influence the timing, power, and signal integrity of the circuit.

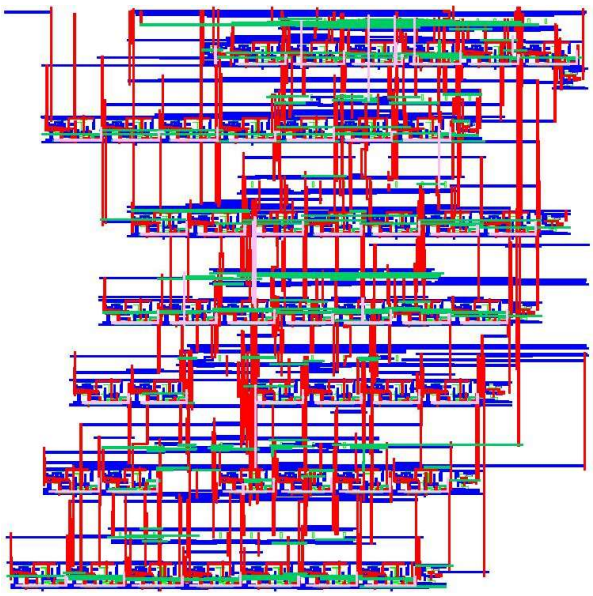


Fig. 8. RC parasitic extraction view of 8-bit array multiplier layout

Fig. 8 illustrates the extracted parasitic network, where multiple metal layers are visible. The vertical and horizontal routing layers are highlighted with distinct colors. The dense red and blue traces indicate the presence of parasitic components introduced due to interconnect routing and via

structures. This extraction is crucial for accurate post-layout simulations, as it helps in timing analysis, delay optimization, and verification against design constraints.

These parasitics are accounted for in Static Timing Analysis (STA) and can have a significant impact on critical path delay. Incorporating this step ensures that the synthesized and placed-and-routed design will meet the timing requirements under real-world operating conditions.

V. COMPARATIVE STUDY OF THE PROPOSED DESIGN

This section discusses the comparison findings of several FA designs, 4 Bit Array multiplier and 8 Bit Array multiplier designs. The outcomes are displayed in the performance metrics portion that follows.

A. Simulation setup

Cadence software has been used to test all the suggested circuits utilizing 90 nm CMOS GPDK process technology for the transient analysis in this work. All the simulations are run on a 2V power supply. The transient analysis of the suggested FA circuit, 4-bit Array multiplier and 8-bit Array multiplier is shown in Figures below.

B. Simulation results

The performance of the proposed hybrid full adder (FA), 4-bit array multiplier and 8-bit array multiplier is compared against existing designs. The Power Delay Product (PDP), power consumption, and delay are considered for analysis.

i) Comparative Analysis of the Full Adder

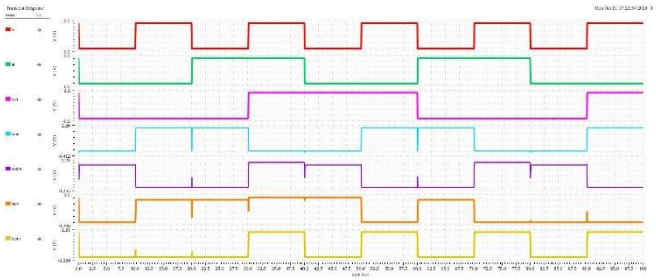


Fig. 9. Waveform of proposed 1-bit hybrid Full adder

TABLE I: Performance of different FA cells in 90 nm CMOS technology at 2V supply voltage.

Design	No. of Transistor	Propagation delay(ps)	Power consumption (µW)	PDP(aJ)
Test1	16	34.15	4.43	151.42
Test2	18	37.77	5.38	203.42
Test3	20	19.92	5.42	108.04
Proposed Design	20	19.92	5.42	108.04

The proposed hybrid full adder demonstrates competitive performance in terms of low PDP and power consumption, making it suitable for high-performance arithmetic circuits.

ii) Analysis of the 4-bit and 8-bit Array multiplier

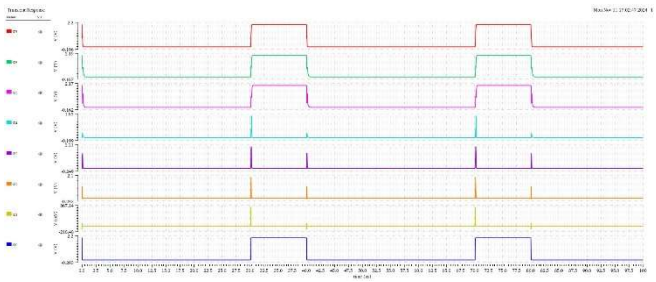
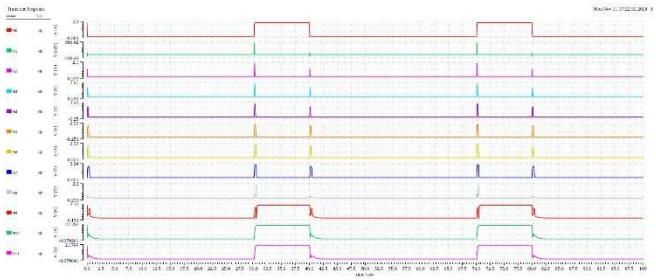


Fig. 10. Waveform of proposed 4-bit Array multiplier



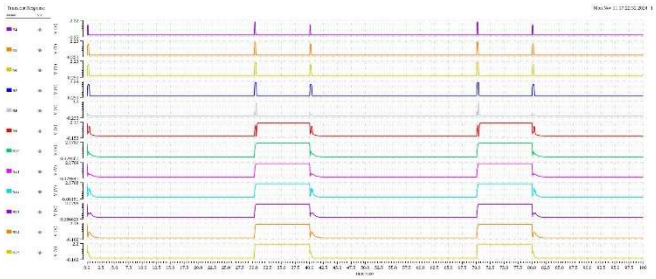


Fig. 11. Waveform of proposed 8-bit Array multiplier

TABLE II: Performance of 4-bit and 8-bit Array multiplier in 90 nm CMOS technology at 2V supply voltage.

Design	No. of Transistor	Propagation delay(ns)	Power consumption (mW)	PDP(pJ)
4-bit Array multiplier	304	0.01964	1.25	0.02455
8-bit Array multiplier	1440	19.65	5.37	105.52

VI. CONCLUSION

This work presents the design of a hybrid full adder (FA) circuit that combines transmission gate and pass transistor logic to achieve better power efficiency, reduced delay, and optimized area compared to conventional designs. The proposed design was developed using 90nm CMOS technology and integrated into both 4-bit and 8-bit array multipliers. The complete design flow was carried out using Cadence tools.

Design Rule Check (DRC) and Layout Versus Schematic (LVS) verifications were successfully performed to ensure layout correctness and rule compliance. Additionally, parasitic extraction was carried out on the 8-bit array

multiplier layout to account for resistance and capacitance effects introduced during the physical design stage.

Post-layout simulation using the extracted parasitic netlist was conducted to analyze the timing and power characteristics of the final layout. These simulations helped in evaluating the real-world performance of the circuit, confirming that it meets the expected specifications.

The successful completion of these steps confirms that post-layout verification was thoroughly carried out and validated. The proposed hybrid full adder and its implementation in array multipliers demonstrated reliable performance and can be effectively used in low-power, high-speed VLSI applications.

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