



Design and implementation of 20-T hybrid full adder for high-performance arithmetic applications

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ABSTRACT

Most of the full adder (FA) circuits are implemented through a hybrid logic style using three different modules. The principal peculiarity of these hybrid logic style-based FA cells is that each module could be optimized individually to improve the circuit performance. A high-performance 1-bit hybrid FA cell is proposed with pass transistor logic and transmission gate logic in the present work. The proposed FA circuit is implemented using 20-transistors to achieve optimum performance. The proposed circuit is simulated in Cadence virtuoso tool by using 90-nm process CMOS technology. Comparison of the design matrices for the proposed 1-bit hybrid FA cell against the five different reported FA circuits is also carried out. The present study reported 13.01–54.93 % and 13.01–59.20 % improvement in terms of delay and power delay product (PDP), respectively, compared to other FA designs. The proposed circuit is also investigated in different supply voltages (0.6–1.5V). Furthermore, the FA circuit is verified in different process corner conditions to check the robustness.

1. Introduction

High performance is one of the essential features in electronic devices, like personal digital assistants (PDAs), cellular phones, and Internet of Things (IoT) devices [1]. High-speed circuits are needed for high performance to cope with the high operating frequency and complex designs. In the application-specific electronic devices, digital signal processors or microprocessors have Arithmetic and Logic Unit (ALU) as a primary block. The adder module is the core element of the ALU circuit. FA is also the fundamental building block for several arithmetic circuit operations, for example, multipliers, compressors, and comparators. Hence, improvement in the performance of the adder circuits is one of the leading research areas of the VLSI researchers to enhance the performance of the digital system. Different static logic styles are used, and these logic styles are generally divided into two groups: conventional logic and hybrid logic styles [2–6].

In the conventional style-based full adder, only one logic is used to implement the whole FA design. The complementary metal-oxide-semiconductor (CMOS) based FA is an example of the classical approach, which is implemented using pull-up (PMOS) and pull-down (NMOS) network. In this approach, 28-transistors are used to realize the full adder. This circuit offers full voltage swing at all the external and internal nodes and provides robustness against the transistor sizing and

voltage scaling. However, the major drawback of this FA design is the presence of PMOS block, and due to the low mobility of PMOS, performance is degraded; therefore, to improve the performance, PMOS transistors are sized up [2].

Another classical approach to implement the FA design is the complementary pass-transistor logic style (CPL). This CPL logic style uses a dual rail structure with 32-transistors to implement the FA design. This structure offers a full voltage swing at the output node, high speed, and good driving capabilities. However, the main demerit of this circuit is high power dissipation owing to a large number of internal nodes in the cell. Another problem with this FA design is that the layout is complex because of the irregular transistor arrangement [3].

Pass transistor logic (PTL) is also a classical approach that can be used to realize the FA design. However, the threshold loss problem arises when logic "1" and logic "0" pass-through NMOS and PMOS transistors, respectively. Therefore, to resolve the issue of the threshold problem, a new logic style is used, which is the transmission gate (TG) logic style. To implement the FA using the TG logic style, 20-transistors are used. This type of adder has low power consumption; however, the main demerit of this type of adder is the weak driving capability [2,3].

Subsequently, FA is realized using a hybrid style to overcome the problem of conventional style-based FA circuits. In the hybrid style, multiple classical styles optimize the circuit's performance [5,6].

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In a hybrid FA structure, three different modules are used. In the first module, the two input signals (A& B) are applied that deliver full swing signals (XOR & XNOR) at the output. These XOR-XNOR signals should have good driving proficiency to drive the SUM and CARRY circuits. The second and third modules generate the sum and carry output correspondingly using the outputs of the first module and the third carry input signal (CIN). This type of FA design offers the full voltage swing at the output node and good driving capability to transmit the signals further [6–10].

Furthermore, hybrid FA is classified based on its internal structures. Aguirre [9] presented the internal logic architecture of the FA, which is shown in Fig. 1 (a). This first module (XOR/XNOR) of FA is realized using double pass transistor logic (DPL). Module second and module third are implemented using XOR/XNOR and AND/OR gate, respectively. Another internal configuration of the FA proposed by Kumar [12] is presented in Fig. 1(b). The first module (XOR/XNOR) of this FA configuration is realized through swing restored complementary pass transistor logic (SR-CPL). The second and third modules are implemented using XOR/XNOR and NAND/NOR gates, respectively. One more internal architecture of the hybrid FA design given by Valashani [13] is displayed in Fig. 1(c). In this design, the XOR- XNOR functions are produced through the first module, and these generated signals show good driving capability and provide the full output swing concurrently. The second and third modules are the SUM and CARRY circuits realized using the TG and MUX circuits.

The main advantage of these hybrid logic styles is that one can mend each module individually and improve performance through good interfacing among different modules. On the other hand, the performance of this type of hybrid logic is degraded if it is implemented through different cascading stages due to reducing in the driving capability.

A high-performance XOR-XNOR design is used in this paper, proposed by Kandpal et al., 2018 [14]. The Proposed XOR-XNOR is realized using CPL logic with one static inverter and has a symmetrical structure without cross-coupling. Further, XOR-XNOR provides simultaneous XOR-XNOR logic, balanced output, and exhibits full voltage swing in all internal and external nodes. The designed XOR-XNOR is used as the first module of the hybrid FA design. Module II and III are used to implement sum and carry logic in a FA and can be implemented using different topologies in CMOS. Therefore, the performance evaluation of the proposed XOR-XNOR module is to be checked in FA. In this paper, the XOR-XNOR design is used in the FA, which is used to resolve compatibility issues and improve the Full adder's performance. In the proposed FA design, module II and module III are implemented using the TG and multiplexer (MUX). It uses only 20-transistors and reported low power consumption with lesser delay. In the present study, the FA circuit is simulated using the Cadence Virtuoso tool in 90 nm CMOS technology at 1.2 VDD.

The rest of this work is organized as follows. Section II gives a brief introduction to the proposed XOR-XNOR circuits. The hybrid FA design with module II and Module III is discussed in section III. Section IV explains the simulation results and analytical comparisons, and Section V gives the conclusion.

2. XOR-XNOR design

There are primarily two methods for designing the XOR-XNOR circuit in the literature. The XOR function is generated at first in the foremost method, and then the XNOR function is produced by using an inverter [2,11,20]. XOR and XNOR signals are delivered separately, due to which false switching and glitches arise in the output of the second and third modules. In another method, XOR-XNOR signals are generated simultaneously at the output; therefore, the delay variation among XOR-XNOR signals could be minimized in various designs [13–19].

An XOR-XNOR circuit presented by Radhakrishnan [4] is shown in Fig. 2. (a), which various researchers modify to improve its

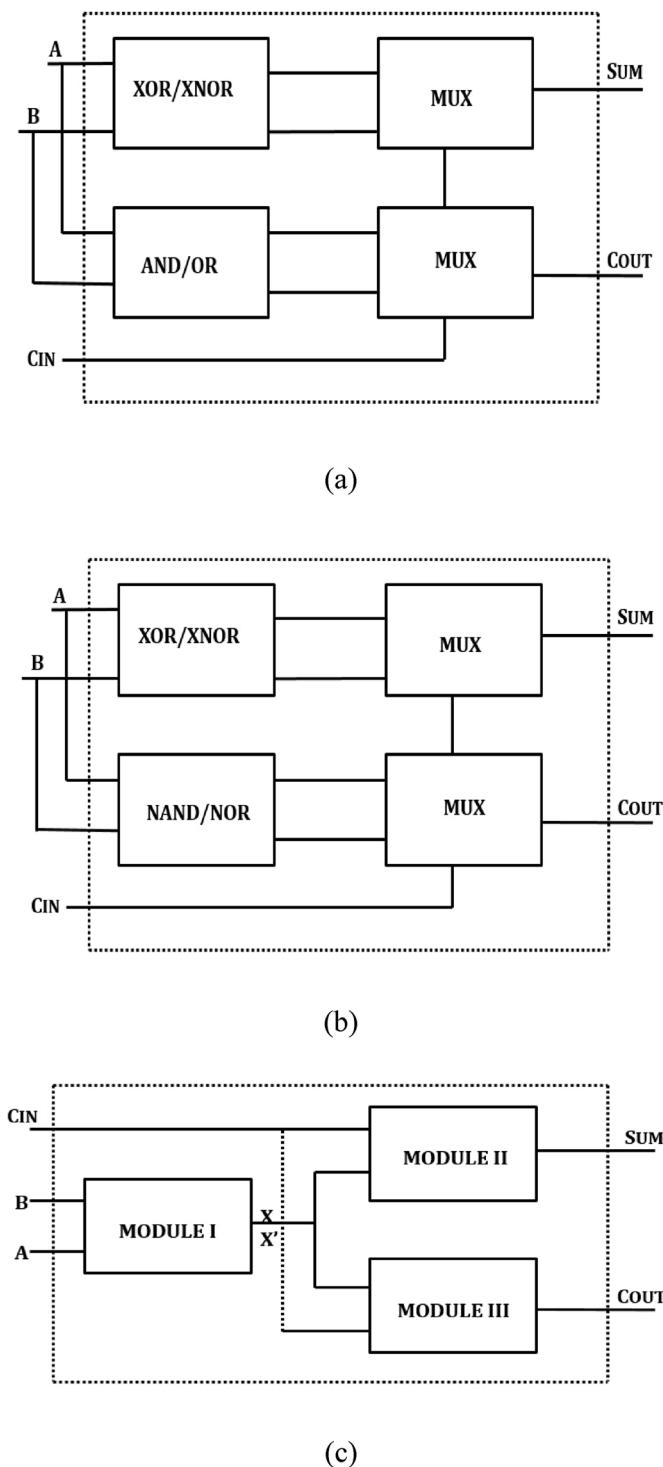


Fig. 1. Three internal configurations of hybrid FA cell (a). Aguirre's logic structure [9] (b). Kumar's logic structure [12] (c). Valashani's logic structure [13].

performance. This configuration is implemented using the CPL and feedback restorer transistors, and only six transistors are used to provide full swing at XOR-XNOR outputs. In this design, the slow response problem arises when the AB equals 00 and AB equals 11 inputs are applied due to the two-step process. Another implementation of the XOR-XNOR circuit is presented by Valashani [13]. In this design, one NMOS and one PMOS transistor are added at the output node (XOR and XNOR), which have inverted input at the source site, as presented in

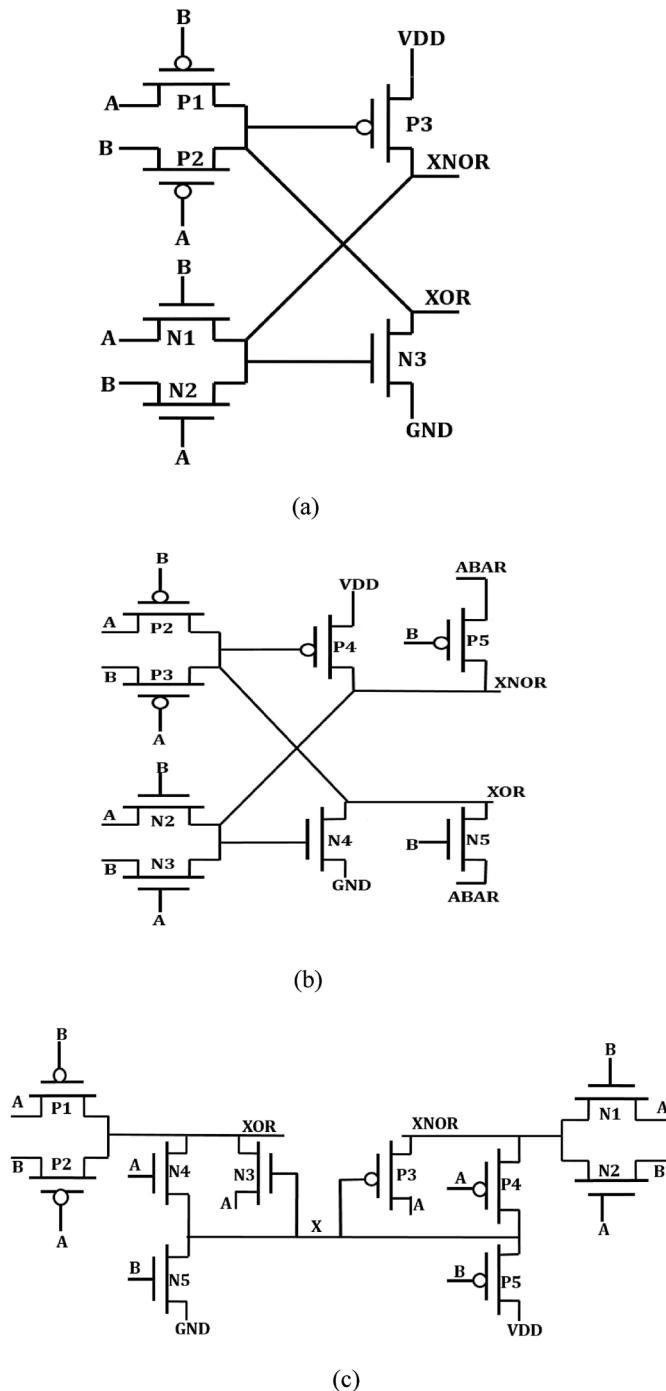


Fig. 2. XOR/XNOR circuit (a). Radhakrishnan [4] (b). Valashani [13] (c). Kandpal [15].

Fig. 2(b). This design also reported a higher delay problem due to the two-step transition. Kandpal [15] proposed a 10-transistor based XOR-XNOR circuit. A higher delay was resolved in their design by using the CPL and restorer circuit, as presented in Fig. 2(c). Furthermore, to improve the performance of the XOR-XNOR circuit, an independent generation of XOR and XNOR designs was done. The method of XOR-XNOR is realized with 10-transistors, as depicted in Fig. 3.

The proposed XOR-XNOR design is realized using the CPL logic with one static inverter. In the proposed circuit, XOR and XNOR output are independently realized. Two PMOS (P2 & P3) and two NMOS (N2 & N3) are used in the XOR design. Similarly, two NMOS (N4 & N5) and two PMOS (P4 & P5) are used in the XNOR design. At the XOR design,

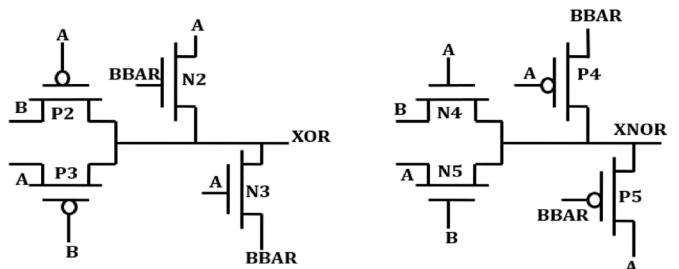


Fig. 3. XOR-XNOR full swing logic generation.

transistors (P2 & P3) are connected in parallel as PTL logic. In addition, transistors (N2 & N3) are also implemented with pass transistors where the source and gate relate inverted input B, respectively. On the other hand, on the XNOR side, transistors (N4 & N5) are linked in parallel as PTL, and transistors (P4 & P5) are also implemented with pass transistors the source and gate are connected with inverted input B, respectively. To understand the operation of the proposed design, the upcoming section presents an overview of the different input combinations.

When the input AB equals "01", then P2, N5, P4, and P5 transistors turn "ON." As a result, P2 and N5 transistors give the logic "1" and logic "0" at the outputs node (XOR-XNOR). Simultaneously, transistors P4 and P5 get "ON" and pass -V_{thp} (weak logic) at the XNOR output. Correspondingly, when the input AB equals "10", P3, N2, N3, and N4 transistors get "ON" and P3, and N4 transistors pass logic "1" and logic "0" at the output node (XOR-XNOR), individually. At the same time, transistors N2 and N3 turn "ON," these transistors (N2 and N3) pass the VDD-V_{thn} (weak logic) on the XOR node. Thus, the input AB equals "01" and "10", the weak logic outputs do not affect the output swing as the full swing path is available for outputs.

The input AB equals "00", P2, P3, P4, and N2 transistors get "ON". P2 and P3 pass -V_{thp} (weak logic) at the XOR output, whereas N2 gives full logic "1" on the XOR node, and at the same time P4 transistor turns "ON," and it passes the logic "1" at the XNOR output. Similarly, when input AB equals "11", N3, N4, N5, and P5 transistors get "ON." The N4 and N5 transistors pass VDD-V_{thn} (weak logic) on the XNOR node. In contrast, transistor P5 gives the complete logic "1" on the XNOR node, and simultaneously transistor (N3) gets "ON," and thereby, the logic "1" is passed at the XNOR node. This circuit facilitates low power consumption, higher speed, and a smaller transistor count with full output swing and good driving power at all the nodes.

3. Proposed full adder design

The proposed FA circuit is realized as presented in Fig. 1(c) using three different modules. First, the second and third module generates the sum and carry output, respectively. Second, each module is implemented independently to optimized the circuit performance in terms of power consumption, delay, and area. These modules are discussed in the following section.

3.1. Module II

The second module (SUM circuit) of FA is implemented using the input carry signal and the intermediate signals (XOR and XNOR), as shown in the equation below. The essential feature of this unit is to provide adequate driving power to the subsequent modules.

$$\text{SUM} = \text{X} \oplus \text{CIN} = \text{XOR.CIN}' + \text{XNOR.CIN} \quad (1)$$

Module II (SUM circuit) uses two transmission gates (TG), where the P7 & N7 transistor gate is connected with XNOR and XOR signal generated from the first module. Source and Drain nodes of these transistors (P7 & N7) are associated with CIN' and the SUM output,

respectively. On the other hand, the second TG gate (P8 & N8) is gated with XOR and XNOR signals. Source and Drain nodes of these P8 & N8 transistors are connected through input carry signal (CIN) and SUM, respectively.

3.2. Module III

In the proposed FA circuit, the third module is the carry module (COUT). This module is realized with the TG logic and MUX circuits. When the A = B, then the COUT = B; if not, COUT = CIN.

3.3. Full adder cell

A new one-bit FA circuit was realized using 20-transistors, as presented in Fig. 6. The proposed adder is implemented using the XOR-XNOR circuit, SUM module, and CARRY module, respectively, as depicted in Figs. 3–5. These three modules are interconnected with each other (Fig. 1(c)). In this circuit, the SUM module is implemented using two TG gates. The P7, P8, N7, and N8 transistors are gated with the first module's XNOR and XOR signals. When XOR is on logic "1" (XNOR is at logic "0"), then both the P7 and N7 transistors turn "ON," and SUM output is directly linked to the inverted input carry signal (CIN'). When CIN is in logic "0," then CIN' will be on logic "1," and this logic pass through the transistor P7 and N7 to the output. On the other hand, when XOR gets logic "0" and XNOR is at logic "1," then both P8 and N8 transistors turn "ON," and SUM output is connected to the input carry signal (CIN).

In the proposed FA circuit, the CARRY module is implemented using TG and MUX. When XOR gets logic "0" at that time, XNOR signal attain logic "1," then both the P9 & N9 transistors turn "ON," and they pass the value of B and A to the output node (COUT). In another case, when the XOR node is at the logic "1," then XNOR is at the logic "0" at the same time the P10 and N10 transistors turn "ON" and pass the input carry signal (CIN) to the output node.

Fig. 6 shows the schematic and layout of 1-bit FA designs. The proposed FA design uses fewer intermediate nodes than Aguirre's [9] and Kumar's [12] structure; therefore, it reduces the switching power component. Furthermore, for high performance, the proposed FA design uses independent XOR-XNOR design as module I. In the next section, the performance of the proposed FA circuit through different simulation conditions is investigated.

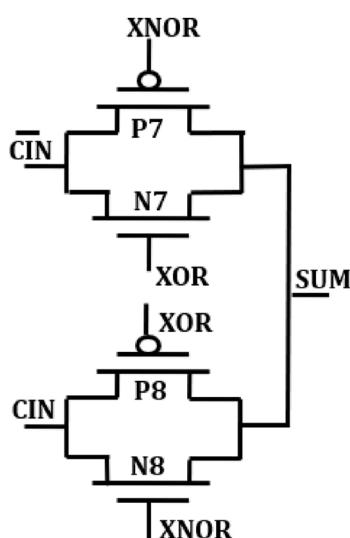


Fig. 4. Module II (SUM).

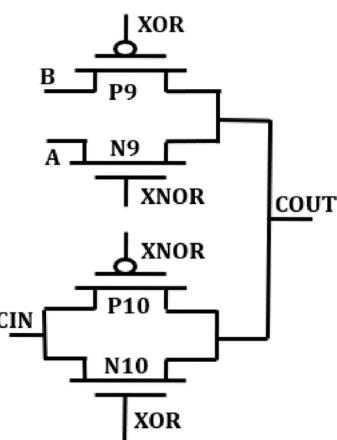


Fig. 5. Module III (COUT).

4. Comparative study of the proposed design

In this section, comparison results of different designs of XOR-XNOR and FA are discussed. The results are shown in the upcoming subsection for the performance metrics.

4.1. Simulation setup

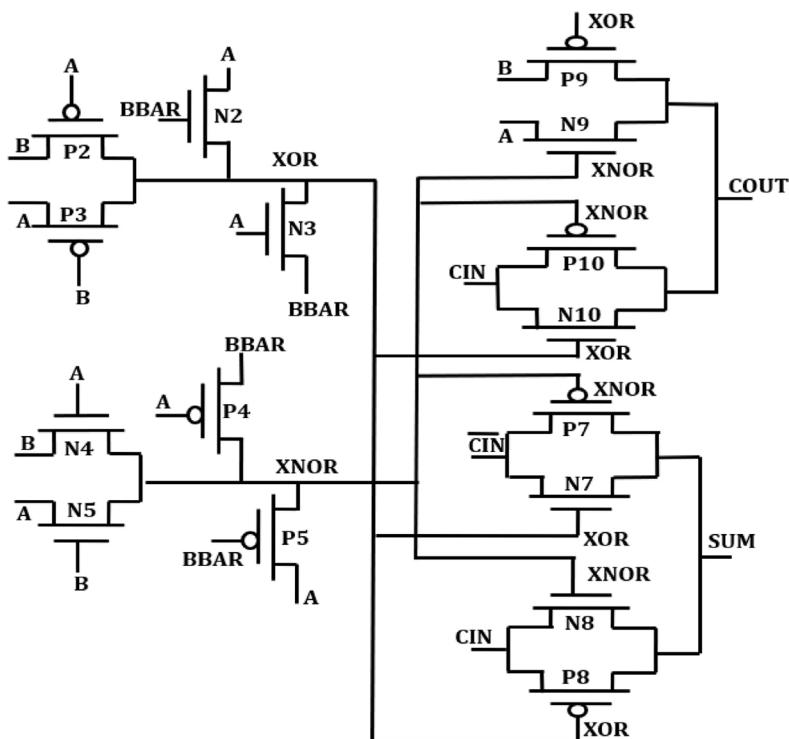
All the proposed circuits have been tested in Cadence software using 90 nm CMOS GPDK process technology for the transient analysis in the present work. A 1.2V power supply carries out all the simulations. For simulating the circuit in the physical environment, two inverters are used at the input of the test circuit. The size of these inverters is selected so that there is enough distortion in the real environment, and the minimum output load of four inverters is used to evaluate the performance [7]. The generic testbed is presented in Fig. 7 for the simulation of different types of circuits.

Fig. 8 presents the transient analysis of the XOR-XNOR and proposed FA circuit by utilizing the test bench (Fig. 7).

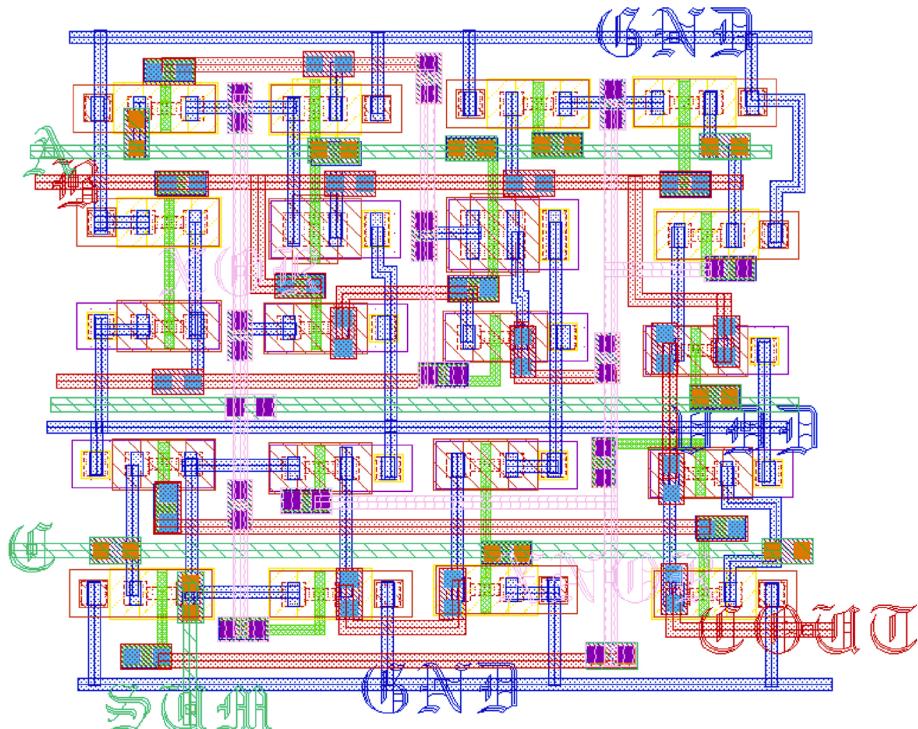
4.2. Simulation results

- 1) XOR-XNOR Circuit: To check the functionality of the XOR-XNOR circuit, a piecewise linear (pwl) input signal (A & B) is used. Fig. 8(a) shows the applied input pattern and corresponding XOR-XNOR outputs. Table 1 compares the result of the proposed design with the prior art in terms of worst-case delay, power consumption, and power delay product (PDP). For the calculation of PDP, the worst-case delay of XOR/XNOR output is taken. The XOR-XNOR circuit, presented in Ref. [4], uses the least number of transistors. However, it has a higher worst-case delay. The proposed XOR-XNOR circuit has the smaller worst-case delay among all the circuits.
- 2) FA design: An input wave pattern is shown in Fig. 8(b), in which three inputs A, B, and C are applied to the inputs of the proposed FA through the test bench, and SUM and COUT are the output of the signal. Table 2 represents the simulation result of FA structure comparing the result of different types of the adder in terms of delay (input carry to carry output), power consumption, and PDP. By optimizing transistors' size, there is a significant reduction in delay without much increase in power consumption. In addition, minimum PDP is also achieved by optimization. The following section displayed the performance of the FA circuit.

The worst-case delay of carrying signal in different FA designs is shown in Table 2. It is apparent from the table that the proposed FA design gives the lowest delay among all reviewed circuits. The proposed



(a)



(b)

Fig. 6. (a). Proposed 1-bit hybrid Full adder, and (b). Layout of FA.

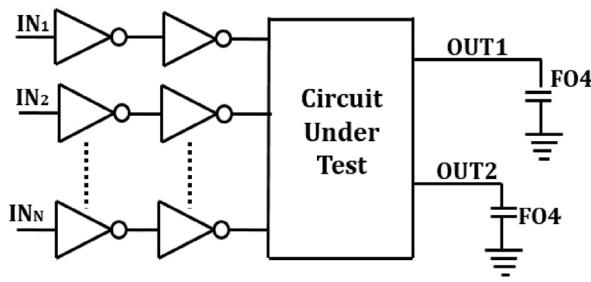


Fig. 7. Test bench.

design offers a 13.01–54.93% improvement in delay when compared to existing structures.

From the comparison done in Table 2, it is apparent that Valashani's design [13] consumed minimal power in their proposed design due to

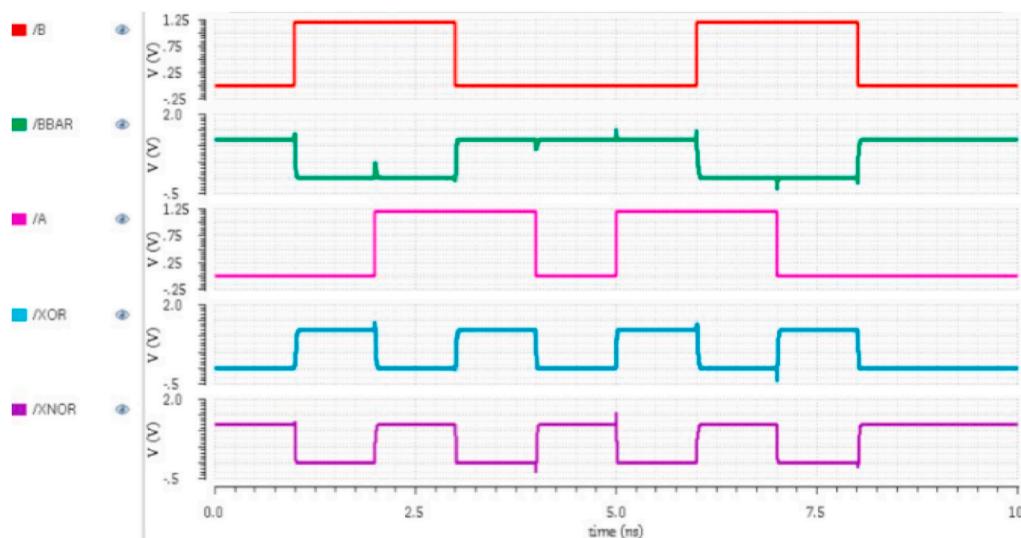
Table 1

Performance of different XOR-XNOR cells in 90 nm CMOS technology at 1.2V supply voltage.

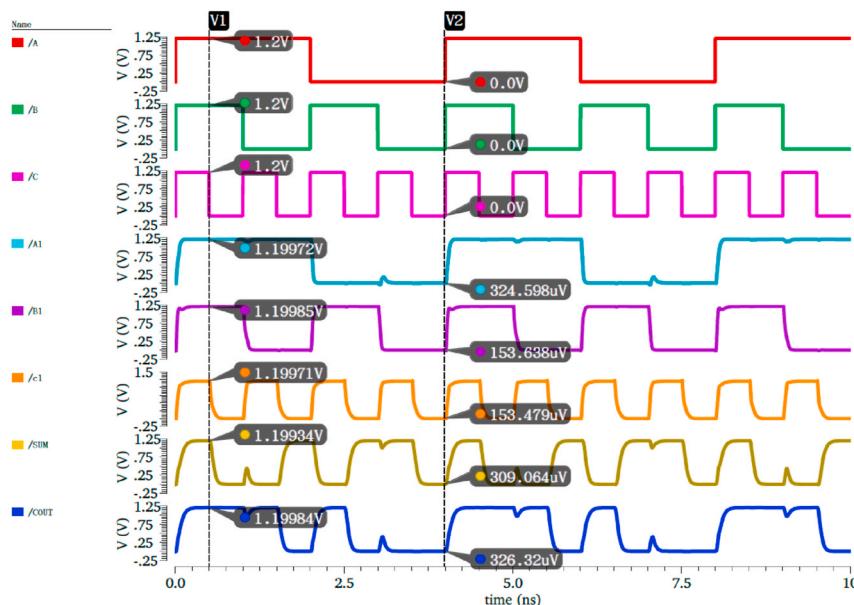
Design	No of Transistor	Propagation Delay(ps)		Power Consumption (uW)	PDP (aJ)
		XOR	XNOR		
Radhakrishnan [4]	6	106	96.5	10.9	1155.4
Valashani [13]	10	73.7	52.2	10.7	788.59
Kandpal [15]	10	48.3	49.4	8.89	439.16
Proposed Design	10	47.3	48.4	8.52	412.36

fewer transistors. Therefore, the proposed FA design consumes moderate power when compared to its best counterparts.

Power delay product is a quantitative measure of efficiency, which provides 13.01–59.20% improvement in the proposed design compared



(a)



(b)

Fig. 8. Time-domain simulation result (waveform) of (a). XOR-XNOR and (b). Proposed FA circuit.

Table 2

Performance of different FA cells in 90 nm CMOS technology at 1.2V supply voltage.

Design	No of Transistor	Propagation Delay(ps)	Power Consumption (uW)	PDP (aJ)
Aguirre_1 [9]	28	80.1	28.5	2282.85
Aguirre_2 [9]	28	69.2	29.5	2041.40
Kumar [12]	27	68.1	26.7	1818.27
Valashani [13]	18	71.3	25	1782.50
Kandpal [15]	20	41.5	25.8	1070.70
Proposed Design	20	36.1	25.8	931.38

to the reviewed circuits.

The robustness of the proposed FA circuit is tested by altering the supply voltage from 0.6V to 1.5V and compared with the existing architecture as described in Fig. 9. The performance of various FA circuits is compared in terms of delay, power, and PDP, as shown in Fig. 9 (a to c).

In Fig. 9(a), the proposed FA design is compared with the reviewed FA circuits based on their delay, and it is found that the proposed FA cell exhibited the best performance amongst available FA cells.

At varying power supply, power consumption of different FA cells is tested and displayed in Fig. 9(b). Valashani's design [13] consumes the lowest power amongst all the other circuits. Moreover, the PDP of the proposed FA design showed the best results for different supply voltages, as shown in Fig. 9(c).

4.3. Process corner analysis

The performance of the proposed FA cell is also evaluated in varying process corners viz. Slow-slow (SS), slow-fast (SF), nominal-nominal (NN), fast-slow (FS), and fast-fast (FF). Fig. 10 (a, b & c) shows the performance evaluation of available FA at different process corners. It is observed that the proposed design operates properly when it is simulated in different process corner conditions and shows the best results in terms of Delay and PDP.

From Fig. 10(a and b), it is observed that the delay and power consumption are highest on SS and FF corners and lowest on FF and SS process corners, respectively, in the proposed FA design.

Fig. 10(c) showed minimum PDP in FF and maximum PDP in SS corner, respectively.

5. Conclusion

The present study mainly focuses on the circuit design level, choosing a proper logic style for implementing the FA circuit. A hybrid style gives liberty to VLSI designers to select different modules to implement the circuit as per their prerequisites. In the present work, a new design of a 1-bit FA is presented on the hybrid design scheme using the 20-transistors. The proposed method alleviates the threshold voltage problem and enhances the driving capability. A comprehensive comparison is conducted in the Cadence virtuoso tool at 90 nm technology. The present study reported 13.01–54.93% and 13.01–59.20% improvement in delay and PDP, respectively, compared to the best counterpart circuits. The performance is also tested at different supply voltage and process corner conditions. From the results, it is revealed that the proposed design is highly robust in all states. Therefore, the proposed method is suitable for high-performance VLSI applications.

Author statement

Jyoti Kandpal: Conceptualization; Methodology; Investigation; Formal analysis; Writing – original draft. Abhishek Tomar: Conceptualization; Supervision; Validation; Writing – review & editing. Mayur

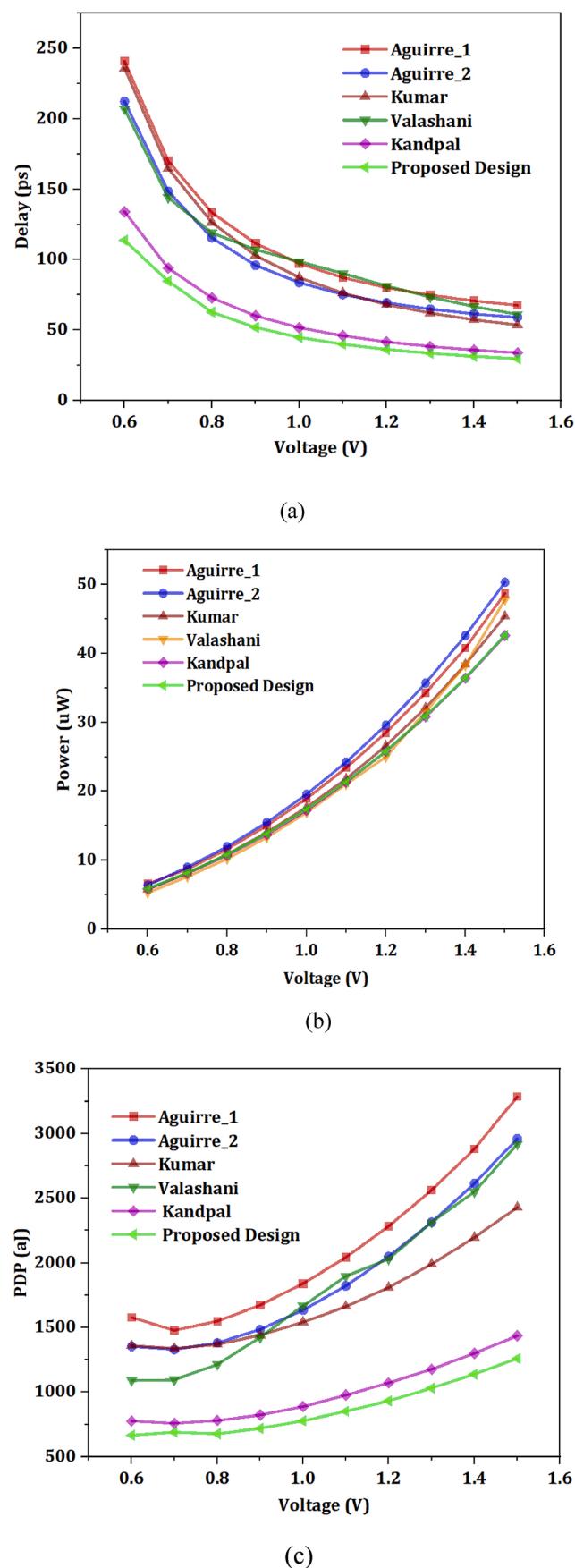


Fig. 9. (a). Delay (COUT) (b) Power (c) PDP results under varying supply voltage.

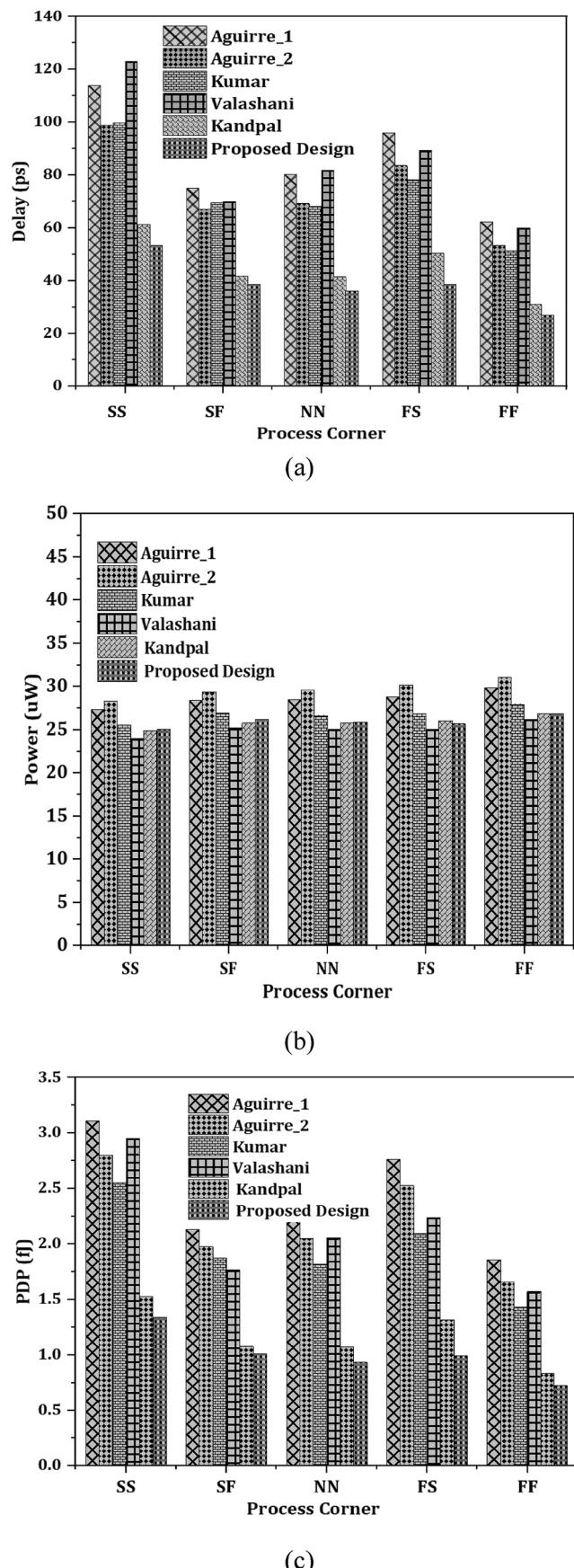


Fig. 10. (a) Delay, (b) Power, and (c) PDP under the different process corner conditions.

Agarwal: Methodology; Supervision; Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this manuscript.

No conflict of interest exists in the submission of this manuscript.

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References

- [1] A.P. Chandrakasan, S. Sheng, R.W. Brodersen, Low-power CMOS digital design, *IEEE J. Solid State Circ.* 27 (1992) 473–483.
- [2] N. Zhuang, H. Hu, A new design of the CMOS full adder, *IEEE J. Solid State Circ.* 27 (5) (1992) 840–844, <https://doi.org/10.1109/4.133177>.
- [3] R. Zimmermann, W. Fichtner, Low-power logic styles: CMOS versus pass-transistor logic, *IEEE J. Solid State Circ.* 32 (7) (1997) 1079–1090, <https://doi.org/10.1109/4.597298>.
- [4] D. Radhakrishnan, Low-voltage low-power CMOS full adder, *Proc. IEEE Circuits, Devices and Systems* 148 (1) (2001) 19–24, <https://doi.org/10.1049/proc-20010170>.
- [5] A.M. Shams, T.K. Darwish, M.A. Bayoumi, Performance analysis of low-power 1-bit CMOS full adder cells, *IEEE Trans. Very Large Scale Integr. Syst.* 10 (1) (2002) 20–29, <https://doi.org/10.1109/92.988727>.
- [6] M. Zhang, J. Gu, C.H. Chang, A novel hybrid pass logic with static CMOS output drive full-adder cell Proc., *IEEE Int. Symp. Circuits Syst.* (2003) 317–320, <https://doi.org/10.1109/ISCAS.2003.1206266>.
- [7] S. Goel, A. Kumar, M. Bayoumi, Design of robust, energy-efficient full adders for deep-sub micrometre design using hybrid-CMOS logic style, *IEEE Transaction Very Large-Scale Integration, Off. Syst.* 14 (12) (2006) 1309–1321, <https://doi.org/10.1109/TVLSI.2006.887807>.
- [8] M. Alioto, G. Di Cataldo, G. Palumbo, Mixed full adder topologies for high-performance low-power arithmetic circuits, *Microelectron. J.* 38 (1) (2007) 130–139, <https://doi.org/10.1016/j.mejo.2006.09.001>.
- [9] M. Aguirre-Hernandez, M. Linares-Aranda, CMOS full-adders for energy-efficient arithmetic applications, *IEEE Trans. Very Large Scale Integr. Syst.* 19 (4) (2011) 718–721, <https://doi.org/10.1109/TVLSI.2009.2038166>.
- [10] C. K Tung, S.H. Sheih, C.H. Cheng, Low-power high-speed full adder for portable electronic applications, *Electron. Lett.* 49 (17) (2013) 1063–1064, <https://doi.org/10.1049/el.2013.0893>.
- [11] P. Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar, A. Dandapat, Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit, *IEEE Trans. Very Large Scale Integr. Syst.* 23 (10) (2015) 2001–2008, <https://doi.org/10.1109/TVLSI.2014.2357057>.
- [12] P. Kumar, R.K. Sharma, Low voltage high-performance hybrid full adder, *Engineering Science and Technology, an International Journal* 19 (1) (2015) 559–565, <https://doi.org/10.1142/S0218126617500840>.
- [13] M. Amini-Valashani, Majid, Mehdi Ayat, Sattar Mirzakuchaki, Design and analysis of a novel low-power and energy-efficient 18T hybrid full adder, *Microelectron. J.* 74 (2018) 49–59, <https://doi.org/10.1016/j.mejo.2018.01.018>.
- [14] J. Kandpal, A. Tomar, S. Adhikari, V. Joshi, Design of Low Power and High-Speed XOR/XNOR Circuit Using 90 nm CMOS Technology, 2nd International Conference on Innovations in Electronics, Signal Processing, and Communication, IESC, 2019, pp. 221–225, <https://doi.org/10.1109/IESPC.2019.8902392>.
- [15] J. Kandpal, A. Tomar, M. Agarwal, K.K. Sharma, High-speed hybrid-logic full adder using high- performance 10-T XOR-XNOR cell, *IEEE Trans. Very Large Scale Integr. Syst.* 28 (6) (2020) 1413–1422, <https://doi.org/10.1109/TVLSI.2020.2983850>.
- [16] M. Agarwal, N. Agrawal, M.A. Alam, A new design of low power high speed hybrid CMOS full adder, in: 2014 International Conference on Signal Processing and Integrated Networks (SPIN), 2014, pp. 448–452, <https://doi.org/10.1109/SPIN.2014.6776995>.
- [17] J. Kandpal, A. Tomar, K. Pandey, M. Agarwal, High performance 20-T based hybrid full adder using 90nm CMOS technology, in: 2019 Women Institute of Technology Conference on Electrical and Computer Engineering (WITCON ECE), 2019, pp. 192–195, <https://doi.org/10.1109/WITCONECE48374.2019.9092897>.
- [18] V. Foroutan, M.R. Taheri, K. Navi, A. Azizi, Design of two Low- Power full-adder cells using GDI structure and hybrid CMOS logic style, *Integrat. VLSI J.* 47 (1) (2014) 48–61, <https://doi.org/10.1016/j.vlsi.2013.05.001>.
- [19] V.R. Tirumalasetty, M.R. Machupalli, Design and analysis of low power high-speed 1-bit full adder cells for VLSI applications, *Int. J. Electron.* 106 (4) (2019) 521–536, <https://doi.org/10.1080/00207217.2018.1545256>.
- [20] M.C. Parameshwara, H.C. Srinivasiah, Low-power hybrid 1-bit full-adder circuit for energy efficient arithmetic applications, *J. Circ. Syst. Comput.* 26 (1) (2017) 1750014, <https://doi.org/10.1142/S0218126617500141>.