Developing an Ultra-low Power RISC-V Processor for Anomaly Detection

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***Abstract*—This paper aims to develop an ultra-low power processor for wearable devices for anomaly detection. To this end, this paper proposes a processor architecture that divides the architecture into a part for general applications running on wearable devices (*day* part) and a part that performs anomaly detection by analyzing sensor data (*night* parts), and each part operates completely independently. This *day-night* architecture allows the day part, which contains the power-hungry main-CPU and system interconnect, to be turned off most of the time except for intermittent work, and the night part, which consists only of the sub-CPU and minimal IPs, can run all the time with low power. By developing a processor based on the proposed processor architecture, the design verification of the proposed technology and the superiority of power saving are demonstrated.**

I. Introduction

Wearable devices have been developing to support more features for anomaly detection, focusing on how much more diverse physiological data can be collected and how much more accurate anomaly judgment can be made, as well as how more convenient wearable devices provide users. To find answers to these questions, low power is essential because wearable devices must collect various sensor data always-on and determine anomalies in real time, while allowing users not experiencing inconvenience due to frequent charging requests.

In this paper, we aim to develop ultra-low power (ULP) processors for anomaly detection. To this end, we first developed a baseline processor that reflects the latest processor technology for wearable devices. The baseline processor architecture is configured to include two types of heterogeneous CPUs (i.e., the main-CPU and sub-CPU). The main-CPU is a CPU for general apps running on wearable devices, and it consumes high power and provides high performance. We applied dynamic power mangement (DPM) technology to this main-CPU for low power, which enters the *standby* mode and is power-gated if there is no task to process. On the other hand, the sub-CPU is a CPU that is used only to collect data from wearable sensors and detect anomalies, which is a CPU with low performance but low power consumption. We used the RISC-V Rocket core [1] as the main-CPU and the RISC-V Orca core [2] as the sub-CPU. In the developed baseline processor, the anomaly detection app operates always on the sub-CPU, and when anomalies are detected, the sub-CPU wakes up the main-CPU, and the main CPU gives the user an alarm and contacts the external medical institution.

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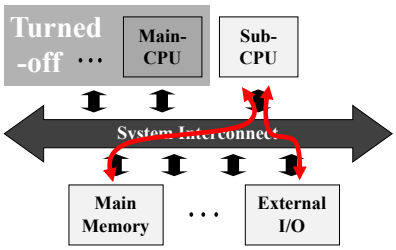

Fig. 1. Problem of the conventional processor arch. when accessing sensors.

As a result of analyzing the power consumption in standby mode of the developed baseline processor, we found that one important thing has been overlooked in the existing low-power processor for wearable device: the power consumption of system interconnect that reaches 41% of the total processor power consumption in standby mode. Furthermore, the existing processor architectures for wearable device require that the system interconnect be turned on at all times along with the sub-CPU, so there is no way to put it into standby mode.

Motivated by this, we come up with a new processor architecture that puts the system interconnect into standby mode and allows only the sub-CPU to process independently. We develop a prototype processor based on the proposed architecture to demonstrate the power-saving superiority of the proposed architecture.

II. Day-Night Architecture

The processor architecture of the wearable device for the abnormal detection is illustrated in Fig. 1. In this architecture, the system interconnect is responsible for communicating with CPUs, memory, and other IPs, so that the sub-CPU also runs through the system interconnect when performing the anomaly detection app. More specifically, the sub-CPUs must communicate with external I/O through the system interconnect to read sensing data and also communicate with memory through the system interconnect to read and write data. In other words, just like the sub-CPU, the system interconnect must be always-on. This means that the power consumption due to the system interconnect cannot be avoided, and a problem arises that power consumption of the system interconnect accounts for a significant proportion in a situation where only the anomaly detection app operates and IPs for the general apps are all

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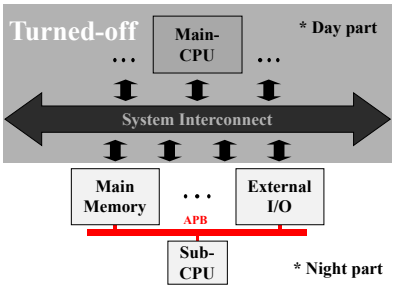

Fig. 2. Operation in standby mode of the proposed processor architecture.

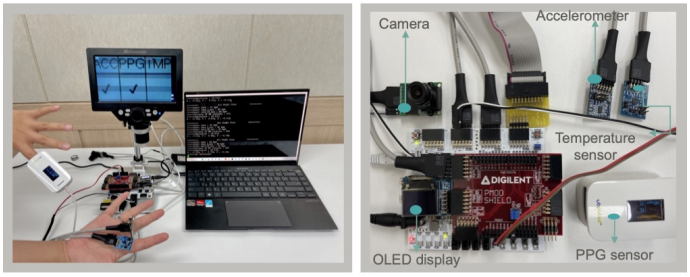

Fig. 3. Complete demonstration of running the anomaly detection app on the processor FPGA prototype.

turned off. Moreover, the fact that most of the time only the anomaly detection app operates in general wearable device usage patterns makes us expect that, when addressing this problem, the expected power saving effect may be significant.

To address the problem, we propose the *day-night* processor architecture that consists of a day part to drive the general apps and a night part to perform the anomaly detection, and each part operates independently. As shown in Fig. 2, the system interconnect with the main-CPU belongs to the day part, so both can be turned off when the night part operates. For the night part to perform anomaly detection app, the sub-CPU must access memory containing CPU code and data, and a peripheral device to read sensor values.

To optimally implement the proposed architecture, we devised a technical solution that allows day and night parts to share existing main memory and external peripheral modules, and night parts to access them. To this end, a dual port memory controller is introduced in the existing main memory, and a separate port is attached to the peripheral device to connect it to the sub-CPU. Since high performance is not required between the sub-CPU and the main memory and external peripherals, all of them configure the advanced peripheral bus (APB) interface and use the APB bus as a communication structure. We also add arbiters that sequentially give priority to prevent data collisions between day and night parts.

III. Prototype Processor

For evaluation of the proposed processor, we implemented both conventional and proposed processor prototypes. For both processros, we used Rocket core as the main-CPU and the four stage pipelined ORCA core as the sub-CPU of the baseline processor. The system interconnect used the micro-NoC developed specifically for low-power SoCs [3], and the power manager is a controller that converts the day part into a standby mode and performs power gating. As with most processor designs [4], both CPUs are typically connected to the Advanced Extensible Interface (AXI) as they require high bandwidth and low latency data transfer. SRAM is the same. On the other hand, SPI, UART, I2C, IROM, JTAG, and FLASH are all configured with APB interfaces because high performance is not required. In particular. for the independent operation of the night part, we designed a dual port (AXI for the main-CPU and APB for the sub-CPU) memory controller to the existing main memory. These two ports do not work at the same time, but operate mutually exclusive. In addition, we designed the external I/O to communicate with the sub-CPU without going through the system interconnect, and made it possible for the sub-CPU to send interrupts directly to the main-CPU.

TABLE I
Energy saving results of the proposed processor.

	Conv. processor	Prop. processor
Resource consumption (LUTs, FFs)	27832, 23436	27891 23530
Power (mW)	27	17
Energy (μJ)	723.6	433.2
Energy saving (%)	–	40.1

We synthesized the processors using Xiliinx Vivado and completed functional verification by prototyping them using Arty-A7 FPGA boards. We connected the PPG, accelerometer, and temperature sensor to the FPGA board as shown in Fig. 3 to execute an anomaly detection app on the processor prototypes. In addition, we mounted a buzzer and OLED display on the board for emergency alarm messages, and used a bluetooth module to transmit the message to the server. To communicate with the processor, we set the PPG and monitor with UART, accelerometer and temperature sensor with I2C, camera and OLED display with SPI, and buzzer with GPIO.

Finally, Table I provides FPGA prototyping results for the conventional and proposed processors. The table shows the resource, power, and energy consumption of the two processors, indicating that the proposed processor achieved about 40% energy savings, although there was a very small increase in resource consumption compared to the conventional processor.

IV. Conclusion

We introduced a new low-power processor architecture, day-night, specific for anomaly detection apps on wearable devices. The day-night architecture allows not only the main-CPU but also the system interconnect, another heavy power consumer, to be turned off in standby mode. Running an anomaly detection app on the implemented processor prototype demonstrates that the proposed solution can achieve energy savings of about 40%.

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