# Rakesh K M

E-mail: kmrakesh23@gmail.com
Phone no.: +91 90252 53871
Linkedin: linkedin.com/in/kmrakesh
Github: github.com/Rakesh-2306

## CAREER OBJECTIVE

A dedicated learner and aspiring professional in Electronics and Communication Engineering, currently pursuing a Master's in VLSI Design. Passionate about acquiring comprehensive knowledge and excelling as a versatile engineer across hardware design, performance verification, and problem-solving. Skilled in collaboration, leadership, and translating complex requirements into effective solutions.

## EDUCATION

**Vellore Institute of Technology, Chennai**
M.Tech. in VLSI Design 2024 – Present

**Sri Sairam Engineering College, Chennai**
B.E. in ECE 2019 – 2023

## TECHNICAL SKILLS

**HDLs:** Verilog, SystemVerilog, TCL
**Programming:** Perl, Python, C, Java, MySQL, scripting
**Tools:** Cadence Virtuoso, Innovus, Intel Quartus, Mentor Graphics,
ModelSim, Synopsys, Ubuntu, PSpice, MATLAB
**Others:** Object Oriented Programming, DRC/LVS, System-level testing, Debugging, Automation

## PROFESSIONAL EXPERIENCE

**ITC Infotech**
Associate IT Consultant Jul 2023 – Jul 2024

- Server Administration, Microsoft Azure, Databases, Power BI, MATLAB Server, ServiceNow
- Automation and scripting for data analysis and system administration

**Cisco Networking Academy**
Cyber Security Intern Apr 2021 – Jul 2021

- Cybersecurity, IP Networking, Network Security
- Hands-on network configuration and security experience

## PROJECTS

**Implementation of Ultra-Lightweight RISC-V Architecture for Anomaly Detection in Healthcare Applications** Present (Ongoing)
Currently developing a custom Day–Night RISC-V processor architecture in ASIC flow featuring an always-on low-power core, shared memory with dual-port controller, and APB-based interconnect optimized for real-time anomaly detection in wearable healthcare applications.

**Design and Analysis of Low Power Hybrid Full Adder for Array Multiplier** Mar 2025
Designed a hybrid full adder (FA)-based 4-bit and 8-bit array multiplier using 90nm CMOS technology with transmission gate and pass transistor logic for power and performance optimization. Performed DRC, LVS, functional verification using Cadence Virtuoso, ensuring design integrity.

**Design and Analysis of 4-bit and 8-bit Kogge Stone Adder Using Memristor Technology** Nov 2024
Designed and simulated memristor-based Kogge-Stone adders for enhanced speed and power efficiency over traditional designs using Cadence Virtuoso.

**Automated Mishap Detection and Prevention System in Vehicles** Feb 2022
Developed an automated accident detection system with notification capabilities, demonstrating embedded system integration and real-time processing.

**Network Topology for College Network Using Cisco Packet Tracer** Jun 2021
Designed and implemented a functional college network topology including configuration and testing.

## PUBLICATIONS

Automated Mishap Detection and Prevention System for Vehicles, Springer, ICICV 2023
DOI: 10.1007/978-981-99-1767-$9_4$