Rakesh K M

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CAREER OBJECTIVE

M.Tech VLSI Design student with hands-on experience in RTL development, ASIC synthesis, and physical design using commercial EDA toolchains. Proficient in end-to-end digital implementation flow including functional verification, static timing analysis, and physical optimization. Seeking opportunities in Physical Design, ASIC implementation, and Digital IC design.

EDUCATION

Vellore Institute of Technology, Chennai
M.Tech. in VLSI Design — 2024 – Present

Sri Sairam Engineering College, Chennai
B.E. in ECE — 2019 – 2023

TECHNICAL SKILLS

HDLs: Verilog, SystemVerilog, TCL

ASIC Flow: RTL Design, Functional Verification, Synthesis, Static Timing Analysis, Floorplanning, Placement, Clock Tree Synthesis, Routing

Tools: Synopsys VCS, Design Compiler, ICC2, Cadence Virtuoso, Innovus, Verilator, GTKWave, Yosys, ModelSim, Quartus

Programming: C, Python, Perl

Others: Timing Optimization, Power Analysis, DRC/LVS, Debugging

PROFESSIONAL EXPERIENCE

ITC Infotech
Associate IT Consultant — Jul 2023 – Jul 2024

- Developed automation scripts for system monitoring and enterprise data processing.
- Worked with Azure, databases, and enterprise tools for system administration.

Cisco Networking Academy
Cyber Security Intern — Apr 2021 – Jul 2021

- Gained experience in IP configuration and secure network setup.

PROJECTS

Performance-Balanced Noise-Canceling Low Noise Amplifier — Dec 2025 – Present
Designing a noise-canceling CMOS LNA in SCL 180nm technology targeting ultra-wideband (3–10 GHz) performance. Achieved $>$ 19 dB forward gain (S21) across the target band while performing S-parameter analysis for input/output impedance matching (S11, S22) and noise figure (NF) optimization in Cadence Virtuoso. Focused on bias stability, transistor sizing, and gain–bandwidth–power trade-offs for balanced RF front-end performance.

Ultra-Lightweight RISC-V Architecture for Anomaly Detection — Nov 2025
Designed and implemented a custom RISC-V processor in a full ASIC flow. Developed RTL modules in Verilog and performed functional verification using Synopsys VCS. Executed synthesis using Design Compiler to evaluate timing, area, and power trade-offs. Performed floorplanning, placement, clock tree synthesis, and routing using ICC2 with SAED32HVT technology libraries. Analyzed setup/hold timing and optimized slack during physical implementation.

Low Power Hybrid Full Adder for Array Multiplier — Mar 2025
Designed 4-bit and 8-bit array multipliers using hybrid full adder cells in 90nm CMOS. Completed schematic design, DRC/LVS verification, and functional validation in Cadence Virtuoso.

Memristor-Based Kogge–Stone Adder — Nov 2024
Designed and simulated 4-bit and 8-bit memristor-based Kogge–Stone adders to improve speed and power efficiency over conventional CMOS implementations. Evaluated architectural performance in Cadence Virtuoso by analyzing critical path delay and power characteristics.

PUBLICATIONS

Automated Mishap Detection and Prevention System for Vehicles, Springer ICICV 2023.
DOI: 10.1007/978-981-99-1767-9_4

CERTIFICATIONS

System Design Through Verilog – NPTEL
Certificate Link

VLSI Design Flow: RTL to GDS – NPTEL
Certificate Link