ECE213: Digital Electronics

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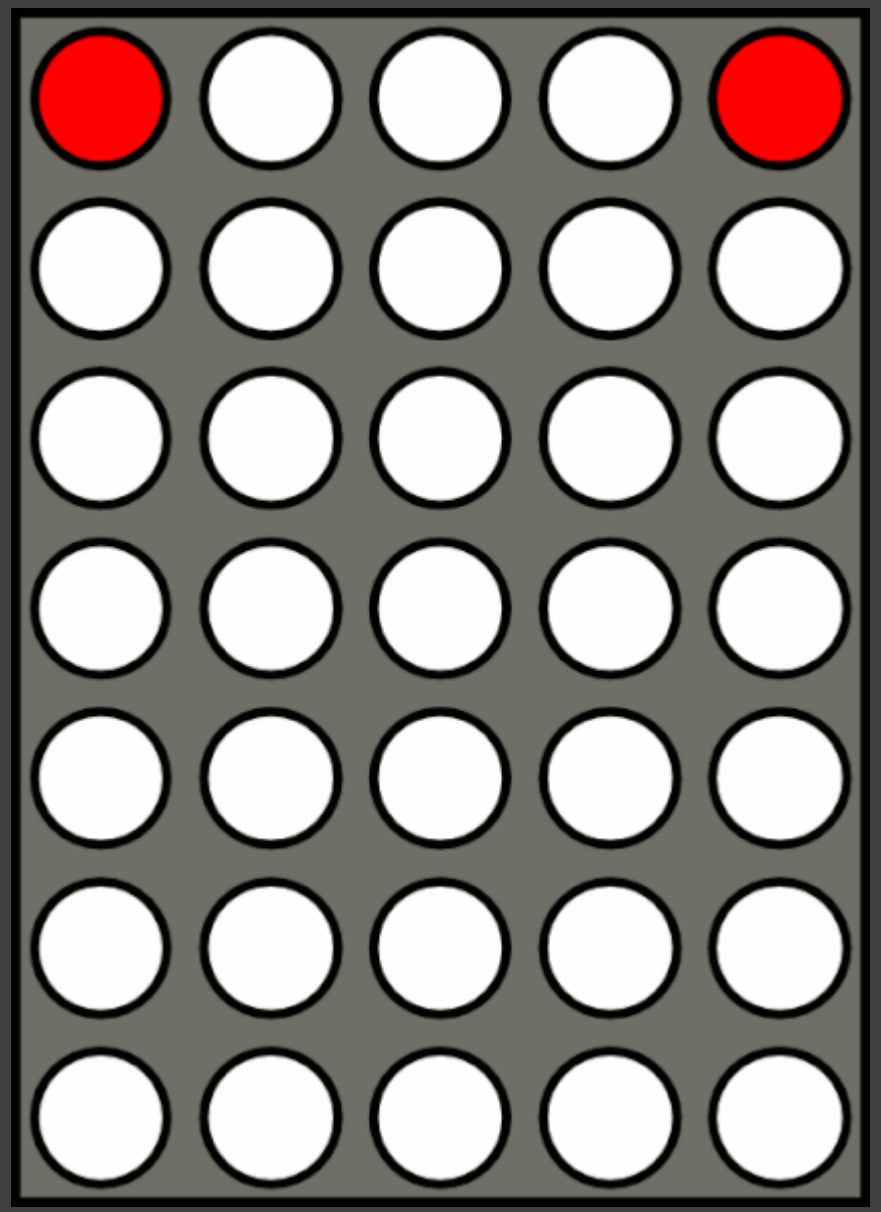
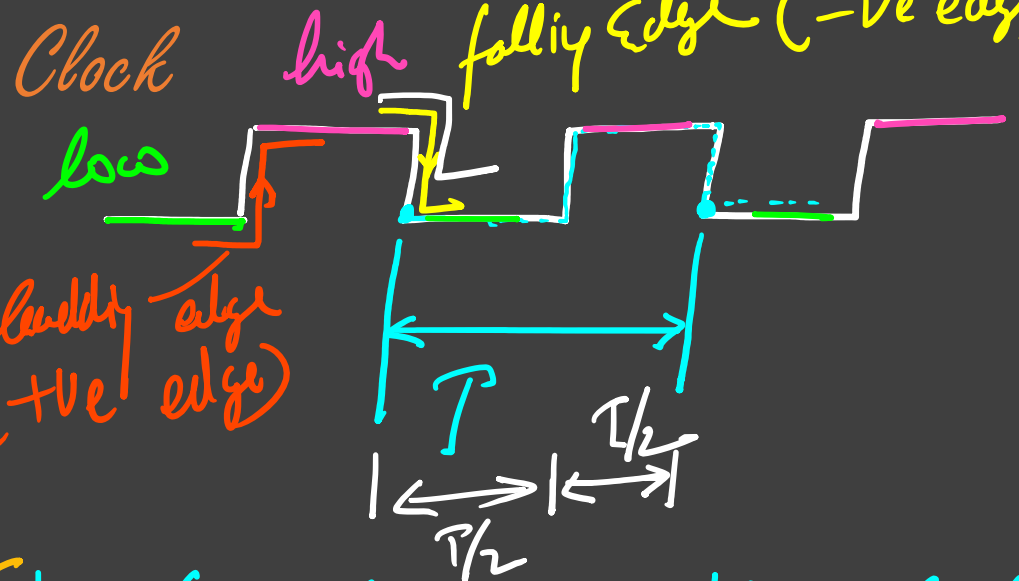
The Course Contents

Unit IV

Introduction to Sequential Logic Circuits : Basic sequential circuits: SR-latch, D-latch, D flipflop, JK flip- flop, T flip-flop, Conversion of basic flip-flops



Introduction to Sequential Logic Circuits



low level (-ve level)
high level (+ve level)
leading edge (+ve edge)
falling edge (-ve edge)

Time period (T) time to complete one cycle.

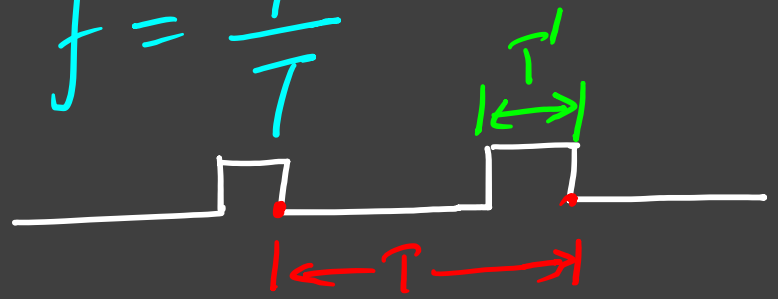
Frequency (f) No of cycles in one unit time sec

$$f = \frac{1}{T}$$

* Duty Cycle : Ratio of time for high level to time per.

$$D.C = \frac{T/2}{T} = 50\%$$

Eg

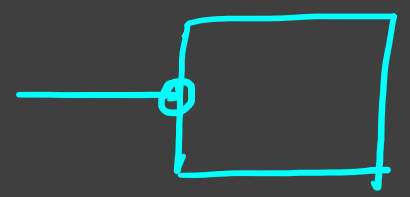


$$D.C = \frac{T'}{T}$$

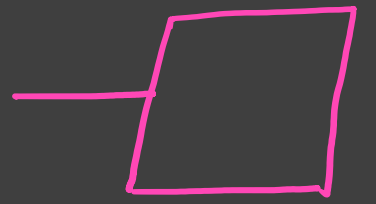
Introduction to Sequential Logic Circuits

Triggering Methods

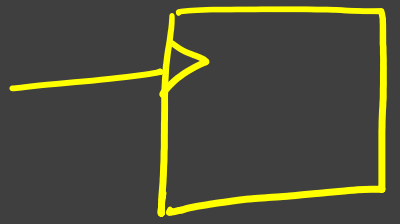
1) -ve level triggering
2) +ve level triggering
3) +ve edge triggering
4) -ve edge triggering

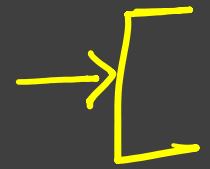


Active 0
Inactive 1



Active 1
Inactive 0





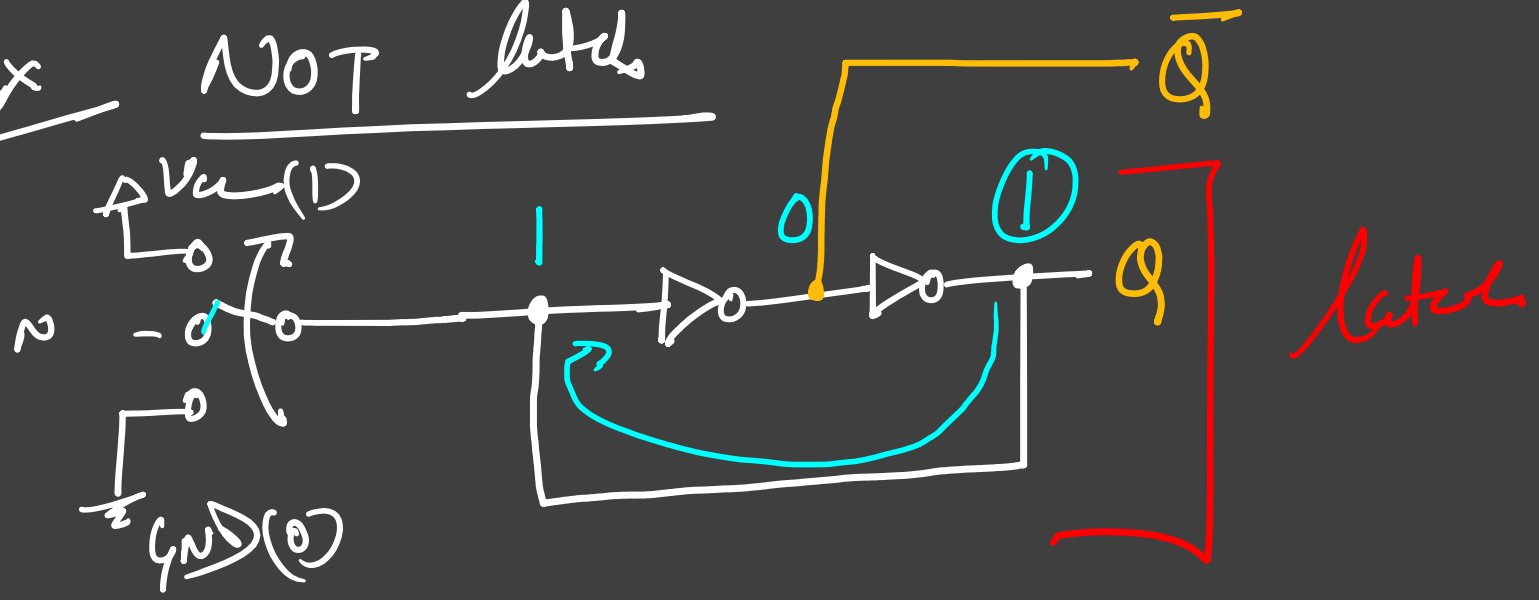
Imp

Introduction to Sequential Logic Circuits

★ Latch : It can store 1-bit data

It is a kind of loop (feedback)

Ex NOT latch



Introduction to Sequential Logic Circuits

SR Latch (NOR)

Set Reset

S	R	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	
0	1	0	1	Reset
1	0	1	0	Set
1	1	–	–	

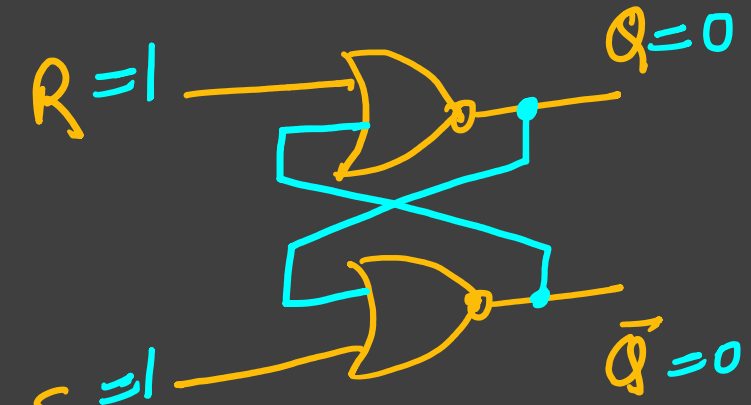
Case 1: If S=0, R=0, No change condition (Memory)

Case 2: If S=0, R=1, Reset condition

Case 3: If S=1, R=0, set condition

case 4: If S=1, R=1, Invalid condition

$Q = \bar{Q}$ (Invalid)



★ NOR Logic

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Set Condition: When the o/p of the ckt set to high, irrespective of previous o/p.

Reset Condition: When the o/p of the ckt set to low, irrespective of prev. o/p.

1) If any of the i/p is high the o/p is low.
2) If any of the i/p is low, then the o/p is the complement of 2nd input

Introduction to Sequential Logic Circuits

SR Latch (NAND)

0 0 | 1 | $\bar{S}$ — Q = 0 1 1

1 — G_1 — Q

1 — G_2 — $\bar{Q}$ = 1 0 1

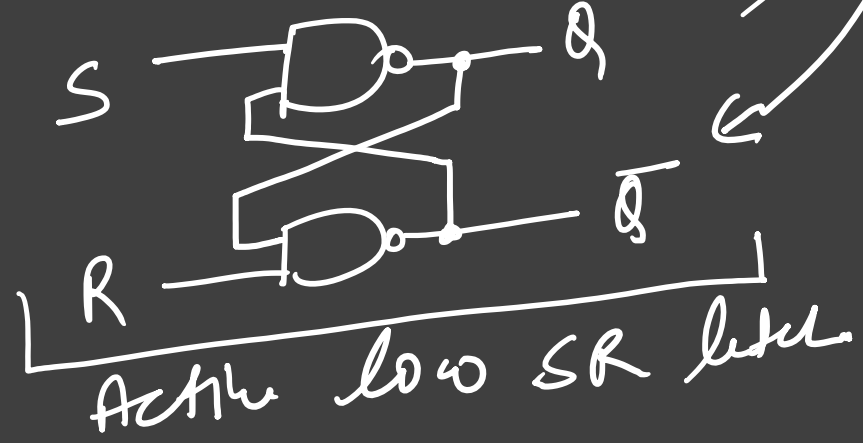
0 1 0 1 | $\bar{R}$

Q = $\bar{Q}$ Invalid

Truth table

S	R	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	→ No change (Memory)
0	1	0	1	→ Reset
1	0	1	0	→ Set
1	1	—	—	→ Invalid

Invalid
Set
Reset
No change



1) If any of the I/P low the o/p will be high
2) If any of the I/P high the o/p will be the Complement of 2nd I/P.

NAND logic

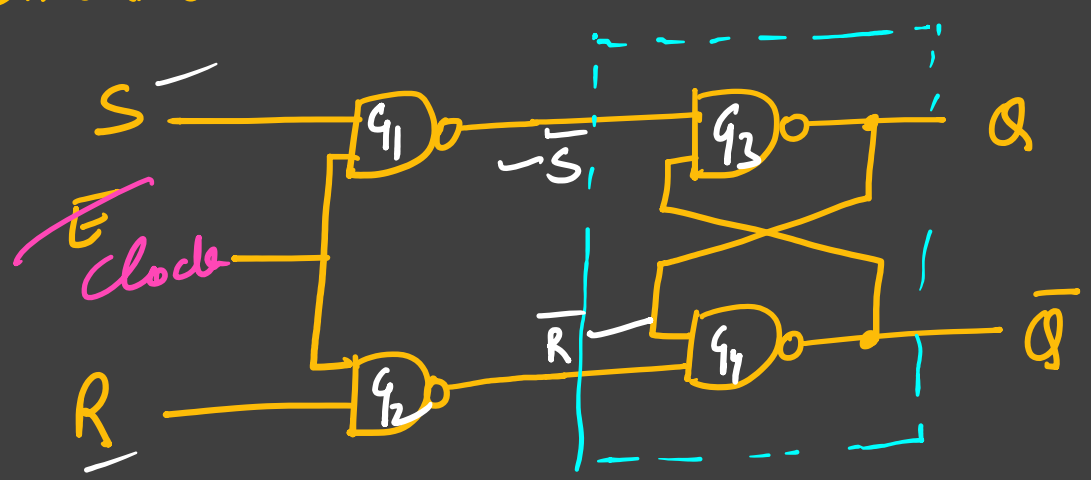
A	B	Y	
0	0	1	
0	1	1	
1	0	1	
1	1	0	

Introduction to Sequential Logic Circuits

Gate SR ~~Latch~~ flip flop (NAND)

Truth Table

E	S	R	Q	$\overline{Q}$	
0	X	X	Q	$\overline{Q}$	NC
1	0	0	Q	$\overline{Q}$	NC
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	–	–	Invalid



If E=0, Gate SR latch will be in no change (Memory) condition
If E=1, Gate SR latch start working as SR Latch.

Introduction to Sequential Logic Circuits

Flip Flop or Latch

≠ Difference in flip flop or Latch

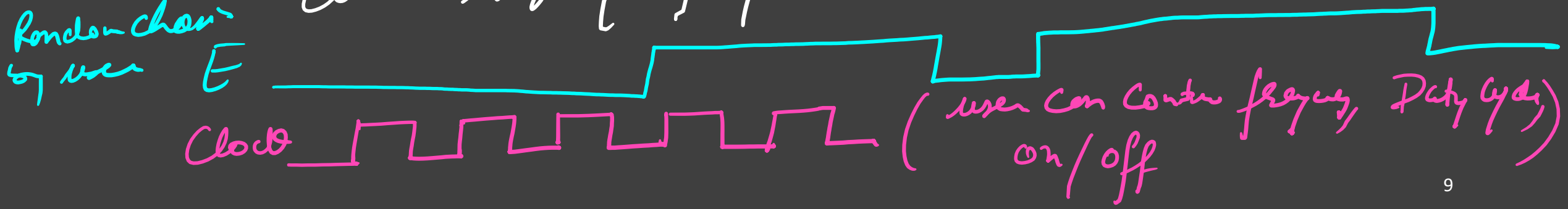
⇒ −ve level trigger
+ve level trigger
] It is a latch

+ve edge trigger
−ve edge trigger
] It is a flip flop.

⇒ Enable signal/input/pin It is a latch

Clock signal/input/pin. It is a flip flop

Random choice by user



Introduction to Sequential Logic Circuits

SR Flip Flop

Truth Table

C	S	R	Q_{n+1}	$\bar{Q}_{n+1}$
0	X	X	Q	$\bar{Q}$
1	0	0	Q	$\bar{Q}$
1	0	1	0	1
1	1	0	1	0
1	1	1	–	–

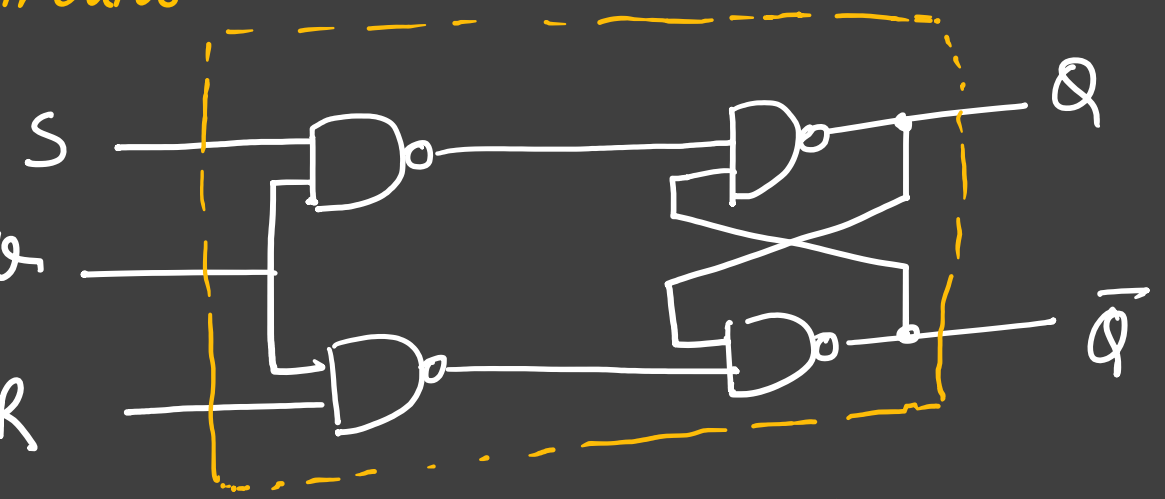
Reset

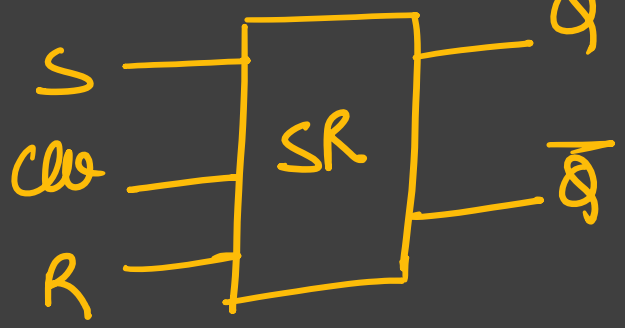
Set

with active clock

Characteristic Table

	S	R	Q_n	Q_{n+1}
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	X
7	1	1	1	X





Excitation Table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0