# ECE213: Digital Electronics


Ajmer Singh

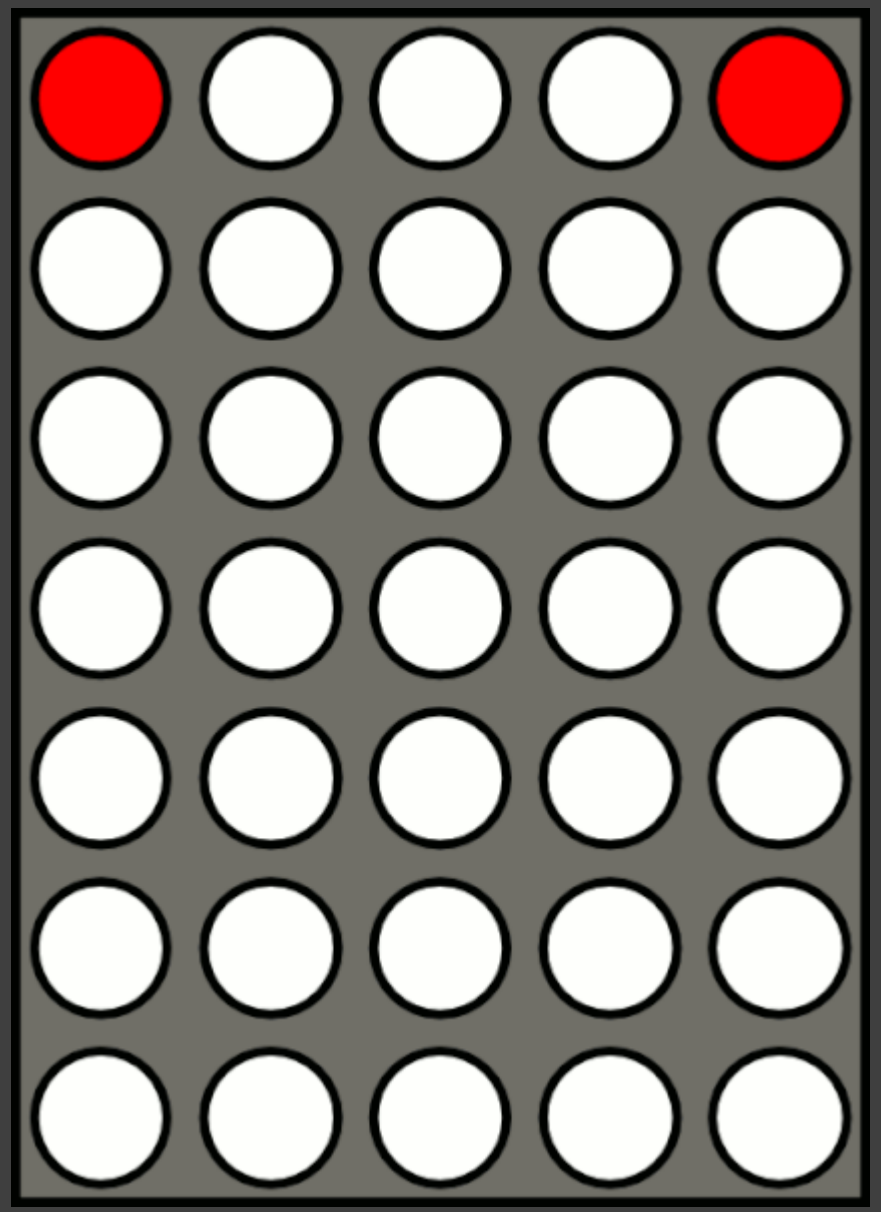
9988921373

ajmer.17381@lpu.co.in


# The Course Contents

## Unit IV

Introduction to Sequential Logic Circuits : Basic sequential circuits: SR-latch, D-latch, D flipflop, JK flip- flop, T flip-flop, Conversion of basic flip-flops



# Introduction to Sequential Logic Circuits

## SR Flip Flop

Truth Table

| C | S | R | $Q_{n+1}$ | $\bar{Q}_{n+1}$ |
|---|---|---|---|---|
| 0 | X | X | Q | $\bar{Q}$ |
| 1 | 0 | 0 | Q | $\bar{Q}$ |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | – | – |

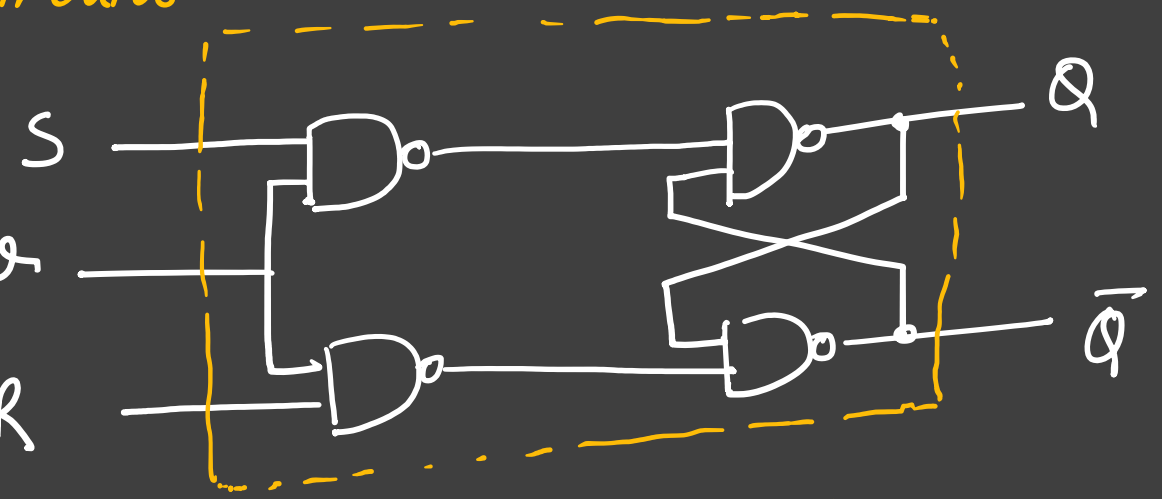
Reset

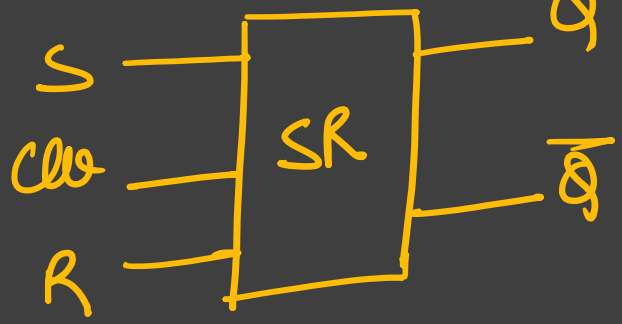
Set

with active clock

Characteristic Table

| | S | R | $Q_n$ | $Q_{n+1}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 1 | 1 | 0 |
| 4 | 1 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | X |
| 7 | 1 | 1 | 1 | X |




Excitation Table

| $Q_n$ | $Q_{n+1}$ | S | R |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | X | 0 |

# do. q'

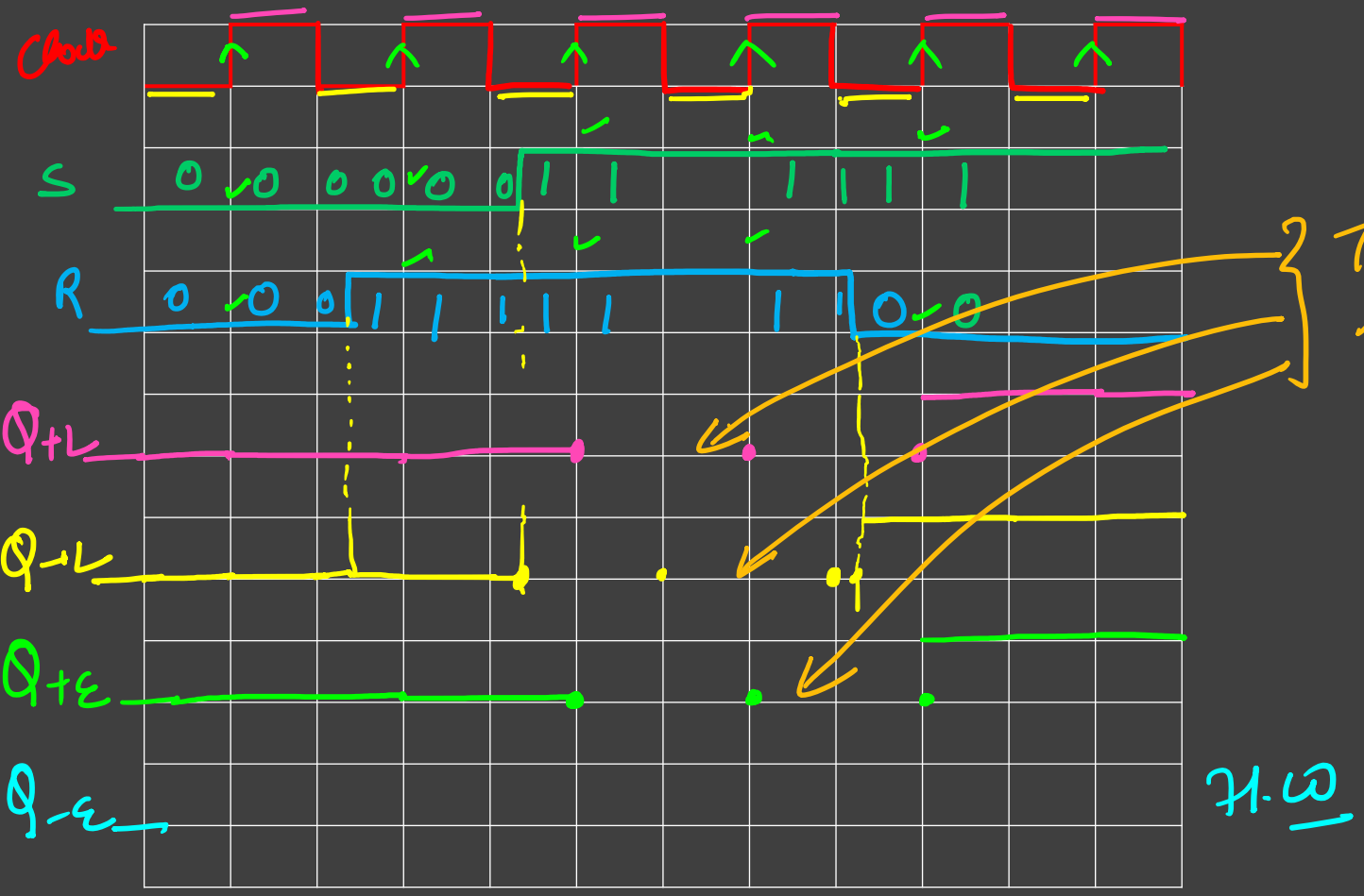
| $SQ_n$ \ R | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | X | X |

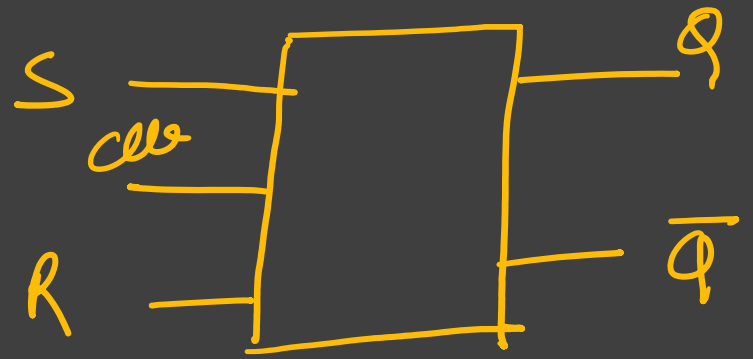
$$Q_{n+1} = S + \bar{R}Q_n$$

# Introduction to Sequential Logic Circuits

## SR Flip Flop

### Timing diagram



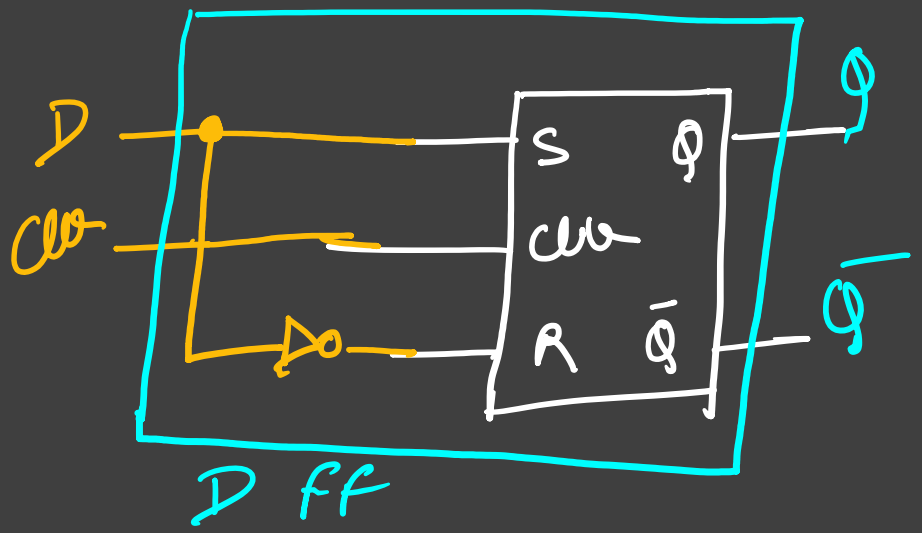




These undefined o/p is due to invalid state of SR FF.

# Introduction to Sequential Logic Circuits

## D Flip Flop / Latch

→ Delay ←




# Truth tse

| C | D | Q | Q̄ |
|---|---|---|---|
| 0 | X | Q | Q̄ |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

# Char. tse

| | D | Qn | Qn+1 |
|---|---|---|---|
| A | 0 | 0 | 0 |
| B | 0 | 1 | 0 |
| C | 1 | 0 | 1 |
| D | 1 | 1 | 1 |

# Excit. tse

| | Qn | Qn+1 | D |
|---|---|---|---|
| A | 0 | 0 | 0 |
| C | 0 | 1 | 1 |
| B | 1 | 0 | 0 |
| D | 1 | 1 | 1 |

# Char. Eq.

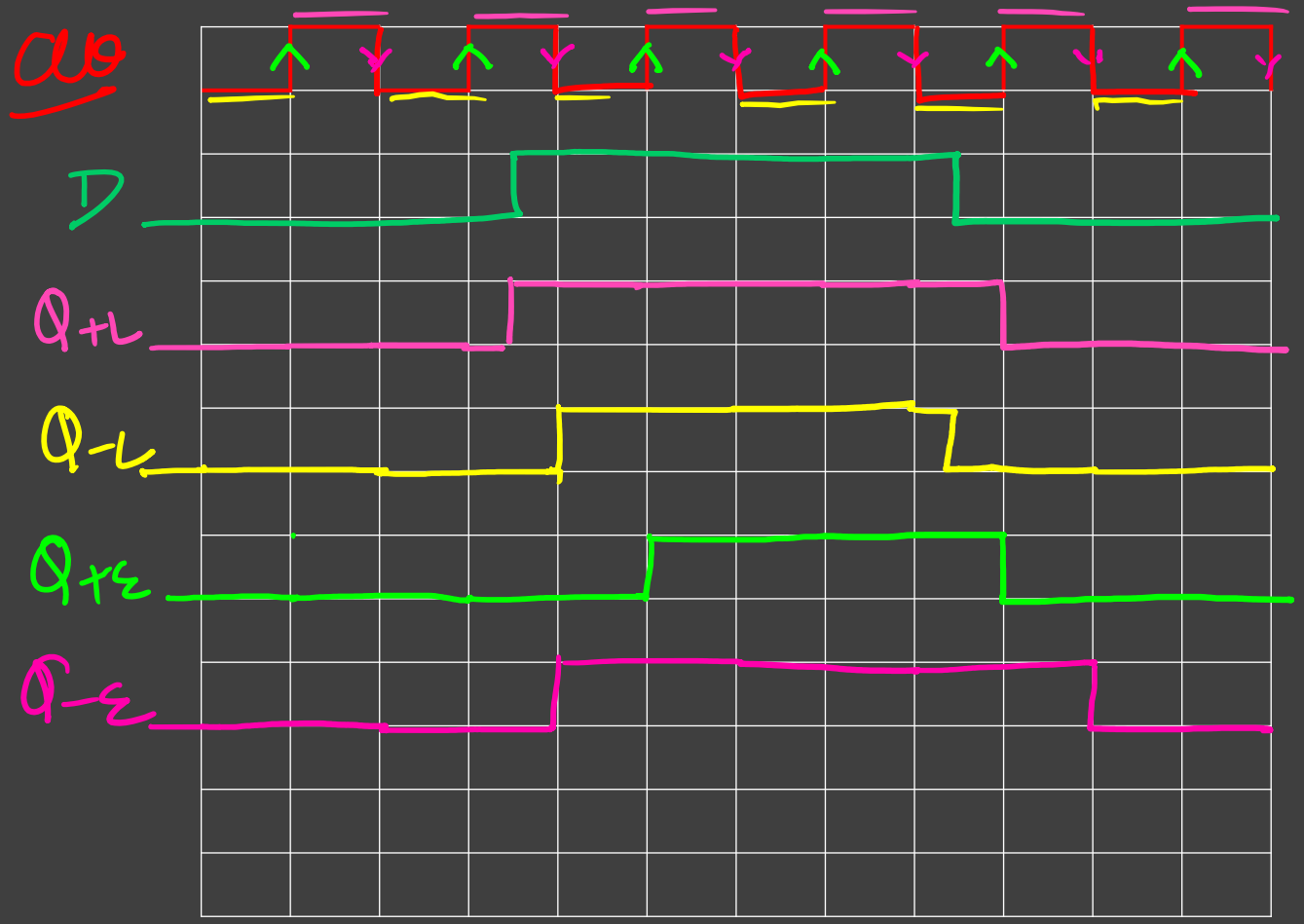

- To avoid the indeterminate state in SR

if D=0, then S=0, R=1 ⇒ Reset

if D=1, then S=1, R=0, ⇒ Set

# Introduction to Sequential Logic Circuits

## D Flip Flop/ Latch

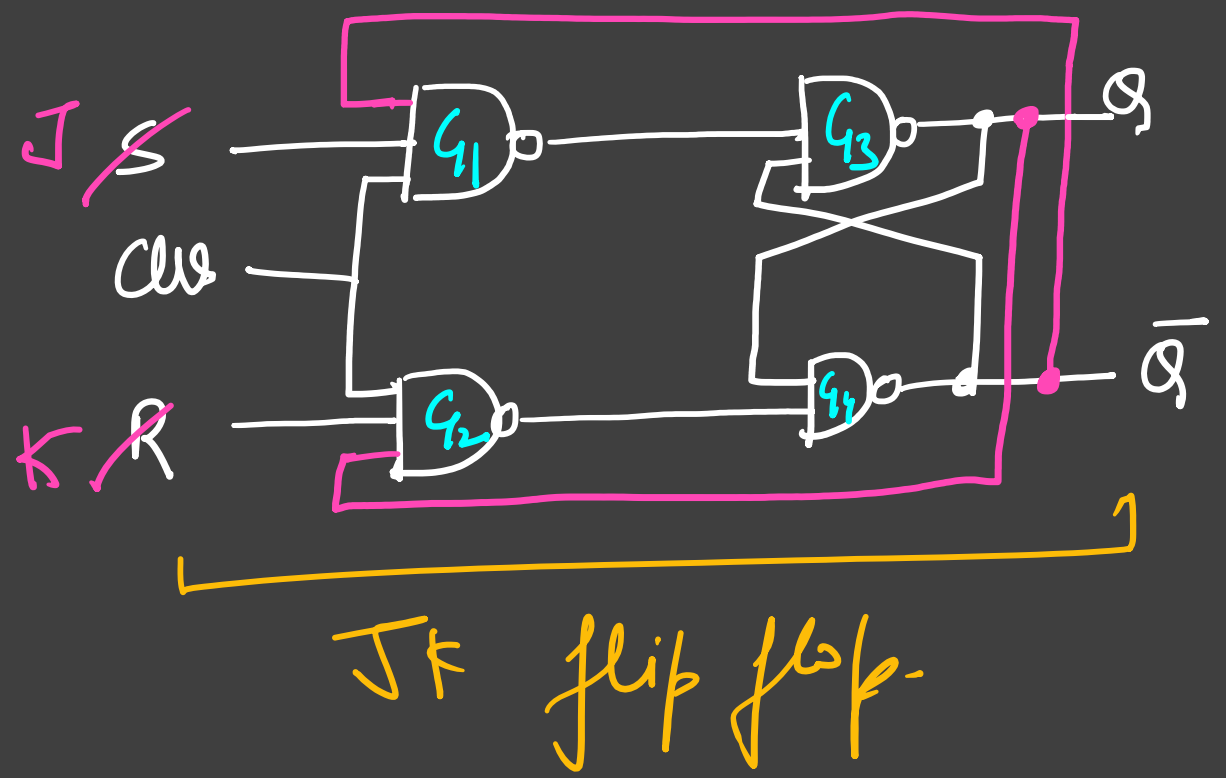


# Introduction to Sequential Logic Circuits

## JK Flip Flop

# To make SR FF to JK follow changes have to do in SR FF

- Change $G_1$ and $G_2$ to 3-input nand Gate
- Provided the feedback from Q and $\overline{Q}$ to $G_2$ and $G_1$ respectively
- Change the I/P terminal for SR to JK respectively



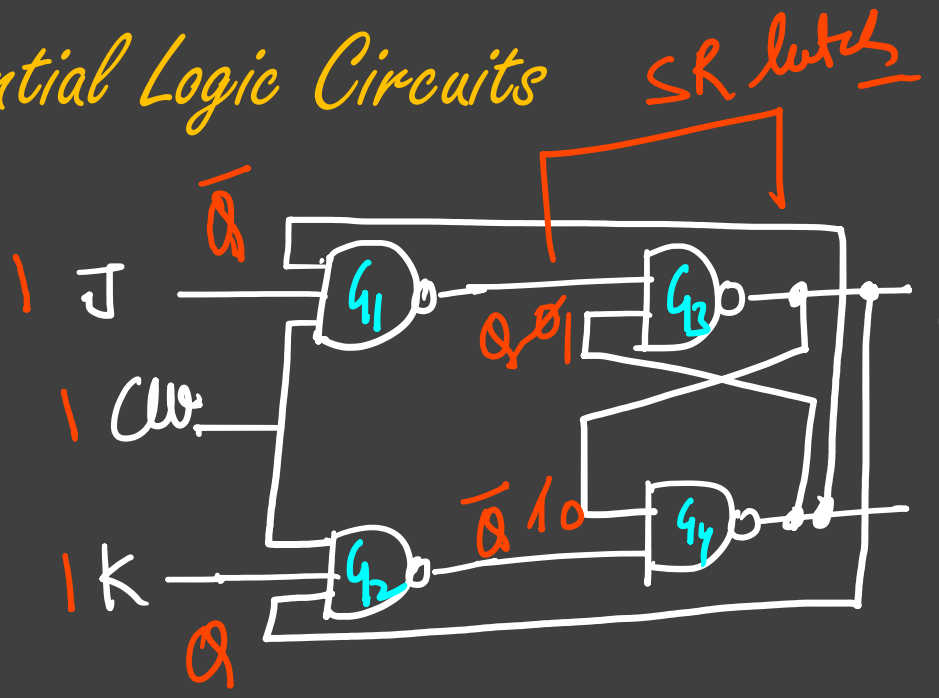

JK flip flop.

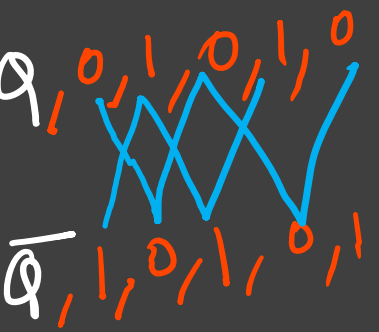
# Introduction to Sequential Logic Circuits

## JK Flip Flop

# Truth table

| | C | J | K | Q | $\bar{Q}$ | |
|---|---|---|---|---|---|---|
| – | 0 | X | X | Q | $\bar{Q}$ | NC |
| → | 1 | 0 | 0 | Q | $\bar{Q}$ | NC |
| → | 1 | 0 | 1 | 0 | 1 | Reset |
| → | 1 | 1 | 0 | 1 | 0 | set |
| → | 1 | 1 | 1 | $\bar{Q}$ | Q | Toggle (comp) (units) |




3-input NAND

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

1) If any i/p is low, the o/p is high.
2) If any two i/ps are high the o/p will be the complement of 3rd i/p.