# ECE213: Digital Electronics


Ajmer Singh

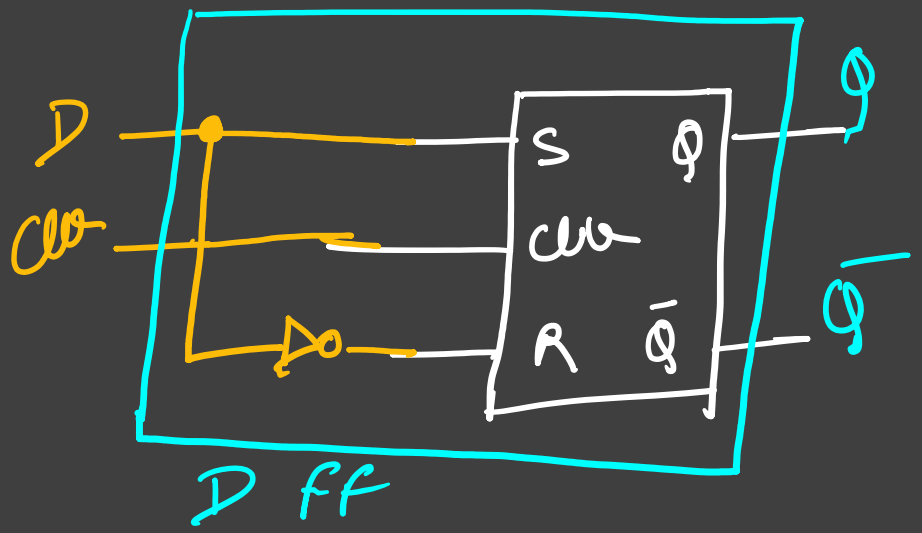
9988921373

ajmer.17381@lpu.co.in


# Introduction to Sequential Logic Circuits

## D Flip Flop / Latch

→ Delay ←




## # Truth table

| | C | D | Q | Q̄ |
|---|---|---|---|---|
| | 0 | X | Q | Q̄ |
| → | 1 | 0 | 0 | 1 |
| → | 1 | 1 | 1 | 0 |

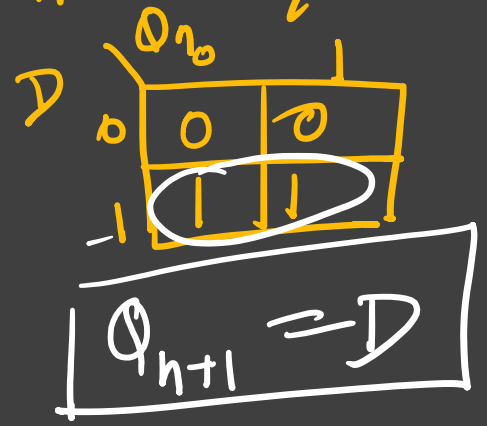
## # char. table

| | D | $Q_n$ | $Q_{n+1}$ |
|---|---|---|---|
| A | 0 | 0 | 0 |
| B | 0 | 1 | 0 |
| C | 1 | 0 | 1 |
| D | 1 | 1 | 1 |

## # Excitation table

| | $Q_n$ | $Q_{n+1}$ | D |
|---|---|---|---|
| A | 0 | 0 | 0 |
| C | 0 | 1 | 1 |
| B | 1 | 0 | 0 |
| D | 1 | 1 | 1 |

## # char. eq.



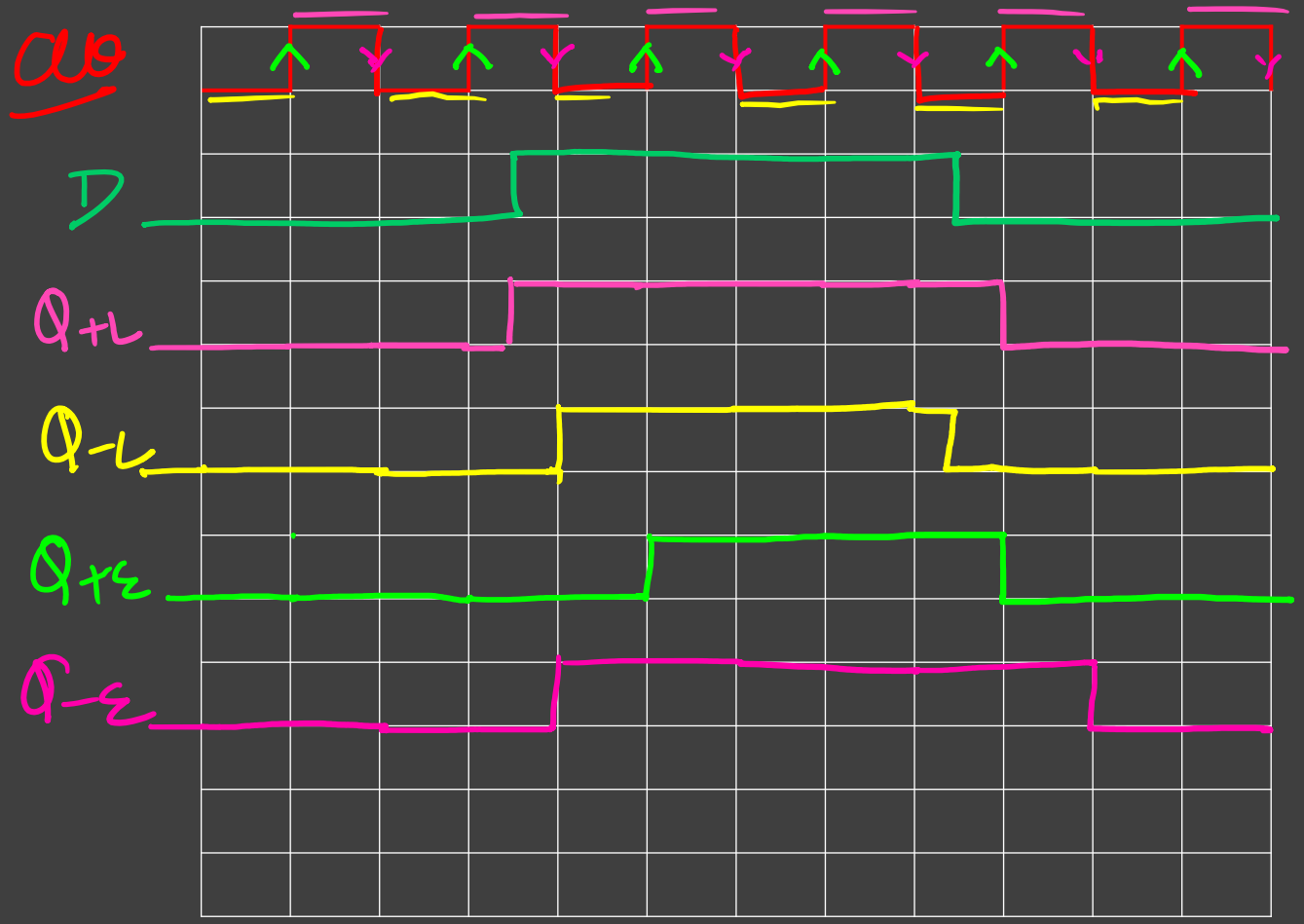

- To avoid the indeterminate state in SR

if D=0, then S=0, R=1 ⇒ Reset

if D=1, then S=1, R=0, ⇒ Set

# Introduction to Sequential Logic Circuits

## D Flip Flop/ Latch

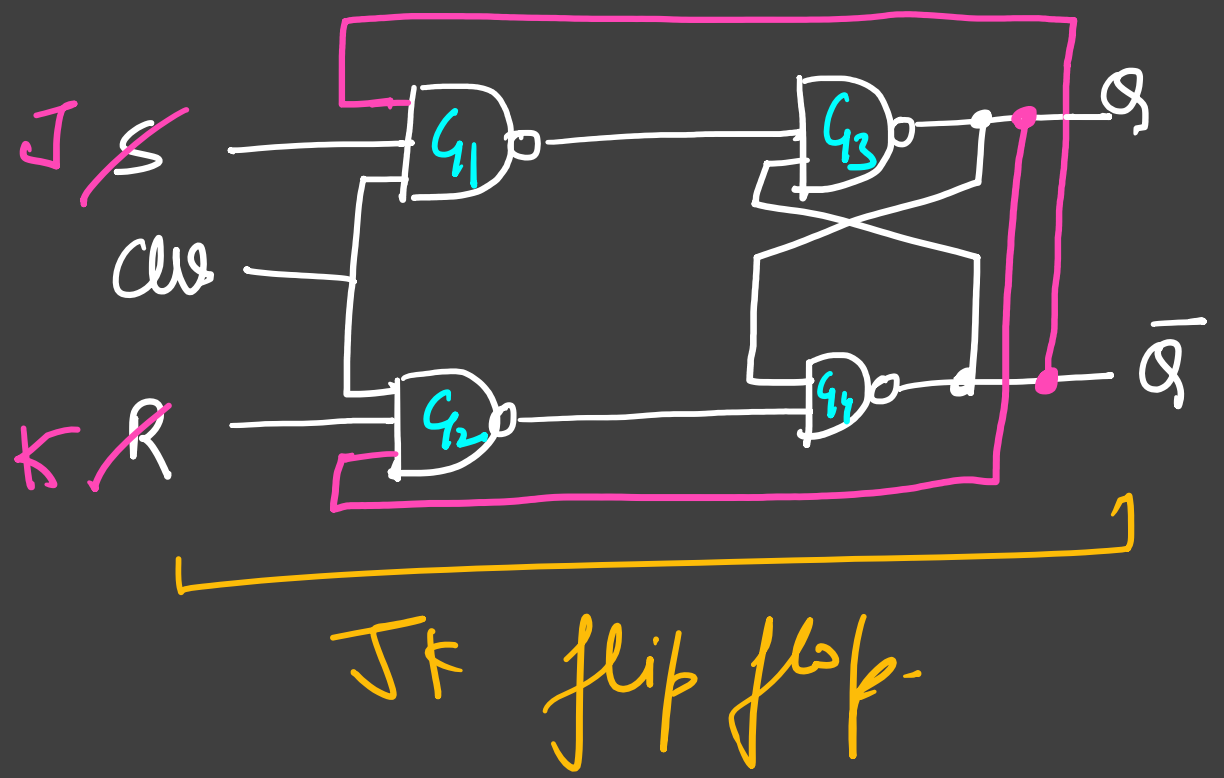


# Introduction to Sequential Logic Circuits

## JK Flip Flop

# To make SR FF to JK follow changes have to do in SR FF

- Change $G_1$ and $G_2$ to 3-input nand Gate
- Provided the feedback from Q and $\overline{Q}$ to $G_2$ and $G_1$ respectively
- Change the I/P terminal for SR to JK respectively




JK flip flop.

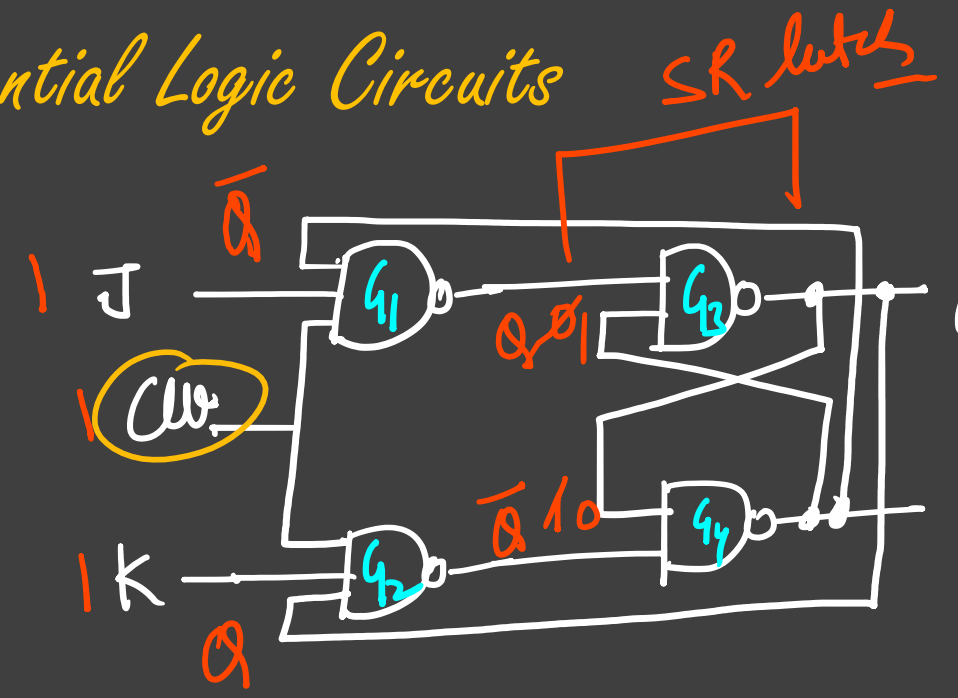
# Introduction to Sequential Logic Circuits

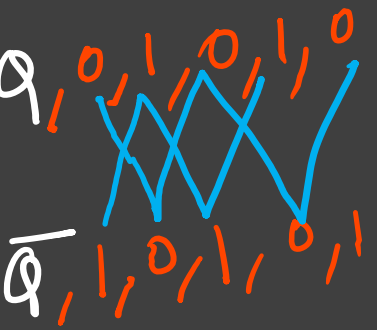
## JK Flip Flop

# Truth table

| C | J | K | Q | $\bar{Q}$ | |
|---|---|---|---|---|---|
| 0 | X | X | Q | $\bar{Q}$ | NC |
| 1 | 0 | 0 | Q | $\bar{Q}$ | NC |
| 1 | 0 | 1 | 0 | 1 | Reset |
| 1 | 1 | 0 | 1 | 0 | set |
| 1 | 1 | 1 | $\bar{Q}$ | Q | Toggle |

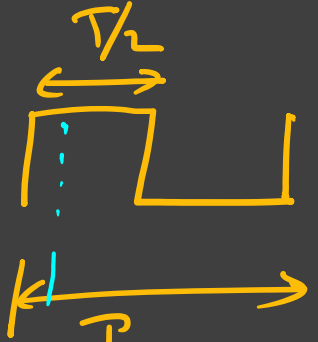
(comp) (units)




3-input NAND

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |




$f_{req} = \frac{1}{T}$

$Duty\ cycle = \frac{T/2}{T}$

$\therefore$ Prop delay $< T/2$

1) If any i/p is low, the o/p is high.
2) If any two i/ps are high the o/p will be the complement of 3rd i/p.

# Introduction to Sequential Logic Circuits

## JK Flip Flop

### # Truth table

| C | J | K | Q | $\bar{Q}$ | |
|---|---|---|---|---|---|
| 0 | x | x | Q | $\bar{Q}$ | |
| 1 | 0 | 0 | Q | $\bar{Q}$ | |
| 1 | 0 | 1 | 0 | 1 | Reset |
| 1 | 1 | 0 | 1 | 0 | set |
| 1 | 1 | 1 | $\bar{Q}$ | Q | toggle |

### # Char. table

| | J | K | $Q_n$ | $Q_{n+1}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 1 | 1 | 0 |
| 4 | 1 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | 1 |
| 7 | 1 | 1 | 1 | 0 |

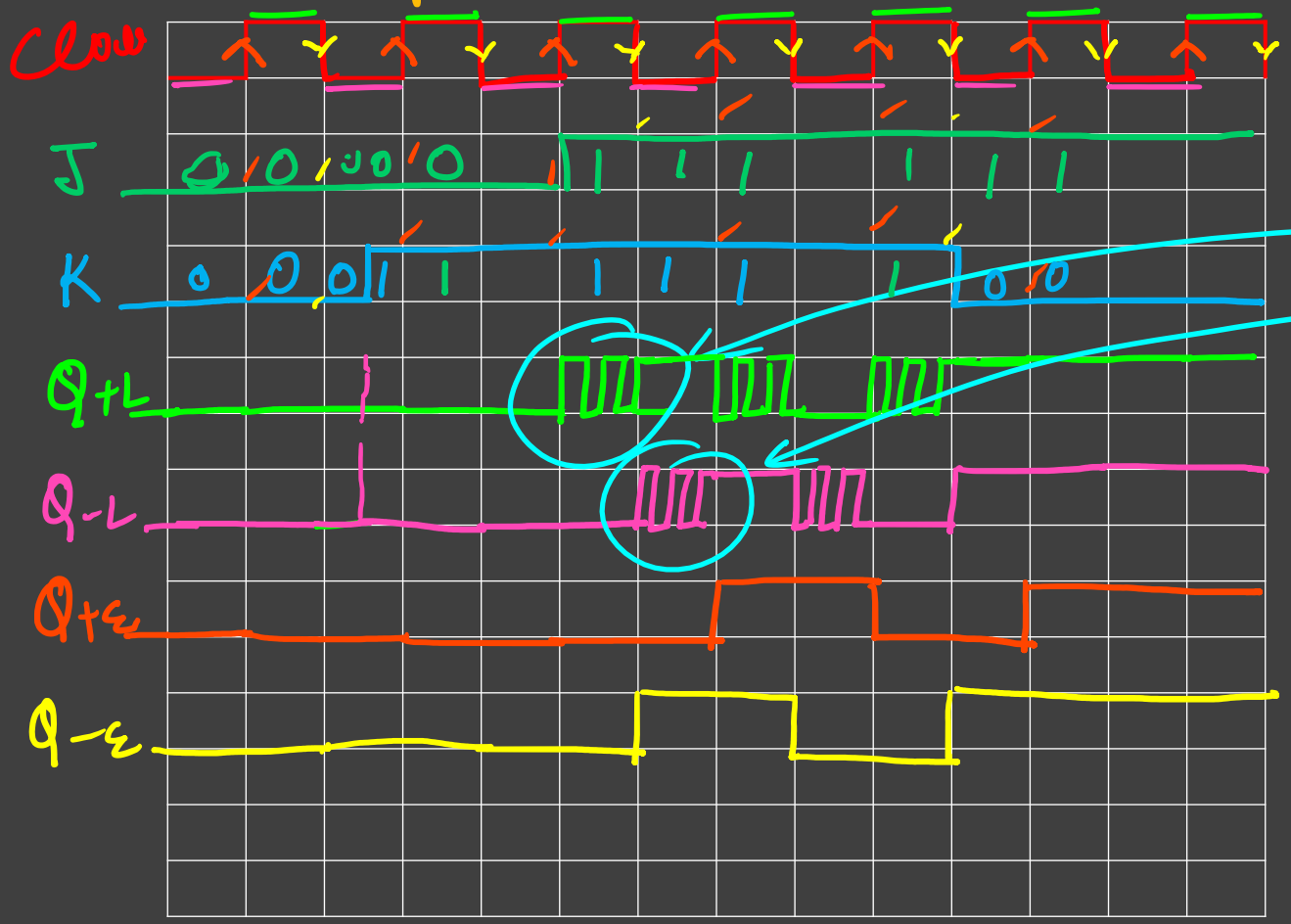
### # Excitation table

| | $Q_n$ | $Q_{n+1}$ | J | K |
|---|---|---|---|---|
| 0,2 | 0 | 0 | 0 | X |
| 4,6 | 0 | 1 | 1 | X |
| 3,7 | 1 | 0 | X | 1 |
| | 1 | 1 | X | 0 |

# Introduction to Sequential Logic Circuits

## JK Flip Flop

# Timing diagram




When the JK flip flop get toggled more than once in one clock. that is called as race around condition

race around condition.

MCQ

# How to avoid the race around condition.

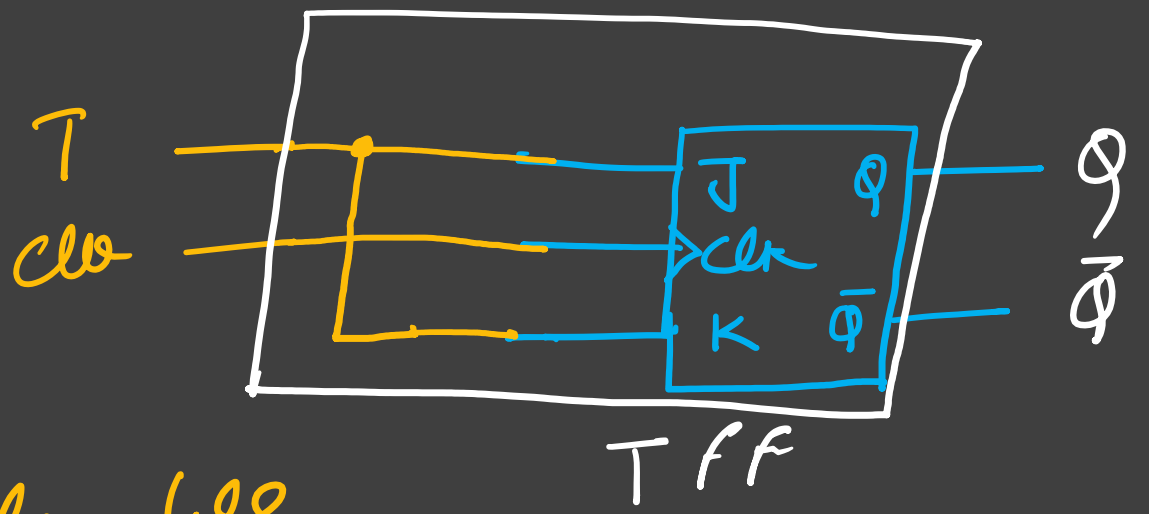
- ~~ii)~~ Edge triggering
- i) Prop delay of FF > T/2
- iii) Master slave FF.

In next class

# Introduction to Sequential Logic Circuits

## T Flip Flop

→ toggle




### # Truth table

| C | T | Q | $\bar{Q}$ | |
|---|---|---|---|---|
| 0 | X | Q | $\bar{Q}$ | NC |
| 1 | 0 | Q | $\bar{Q}$ | NC |
| 1 | 1 | $\bar{Q}$ | Q | Toggle |

### # Char. table

| | T | $Q_n$ | $Q_{n+1}$ | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | → 0 |
| 1 | 0 | 1 | 1 | → 1 |
| 2 | 1 | 0 | 1 | |
| 3 | 1 | 1 | 0 | → 0 |

### # Excite table

| | $Q_n$ | $Q_{n+1}$ | T |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 2 | 0 | 1 | 1 |
| 3 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

# Introduction to Sequential Logic Circuits

## T Flip Flop

# Timing diagram