LOGIC FAMILY

ECE213 – Digital Electronics

Introduction to Digital Family

- ***Digital ICs*** operate at only a few defined levels or states, rather than over a continuous range of signal amplitudes. These devices are used in computers, computer networks, modems, and frequency counters. The fundamental building blocks of digital ICs are logic gates, which work with binary data, that is, signals that have only two different states, called low (logic 0) and high (logic 1).
- Example 7408, 7486, 74266 etc

Digital Family

- ***Small-Scale Integration* (SSI):** with up to 100 electrical components per chip (early 1960s)
- ***Medium-Scale Integration* (MSI):** with 100 to 3,000 electrical components per chip (late 1960s)
- ***Large-Scale integration* (LSI):** with 3,000 to 100,000 electrical components per chip (mid 1970)
- ***Very Large-Scale Integration* (VLSI)**: with 100,000 to 1,000,000 electrical components per chip (1980s).

Linear or Analog IC

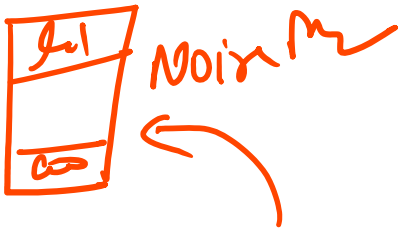
- ***Linear ICs*** have continuously variable output that depends on the input signal level. As the term implies, the output signal level is a linear function of the input signal level. Ideally, when the instantaneous output is graphed against the instantaneous input, the plot appears as a straight line.

➢ Linear ICs are used as audio-frequency (AF) and radio-frequency (RF) amplifiers. The *operational amplifier*(op amp) is a common device in these applications.

➢ Example: 555 Timer IC, µA741 op-amp, LM78XX (Voltage Regulator) etc.

Advantages of IC

- **Several factors have made the integrated circuit popular:**
  - It is reliable with complex circuits.
  - It meets the need for low power consumption.
  - It offers small size and weight.
  - It is economical to produce.
  - It offers new and better solutions to system problems.



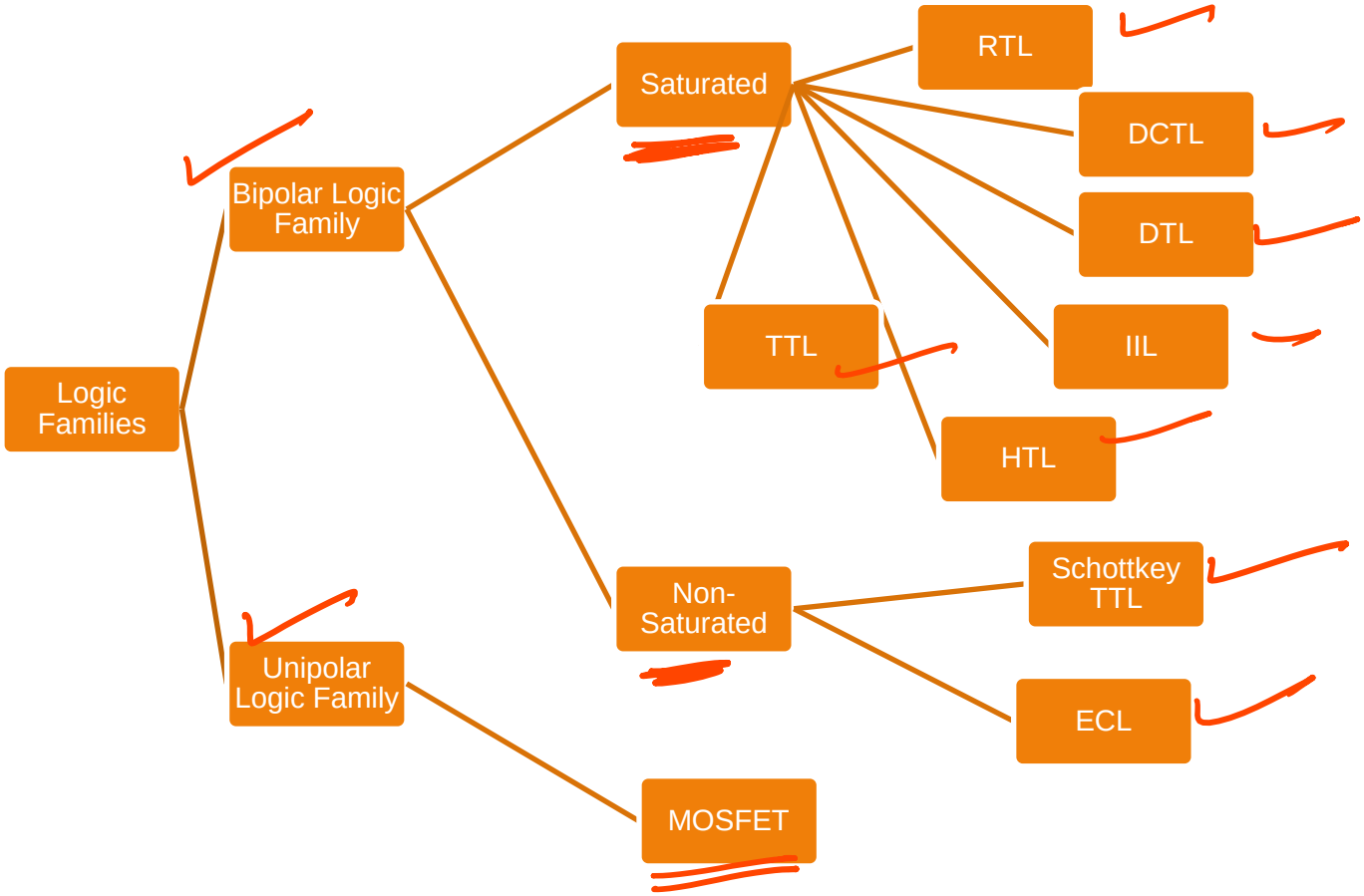
INTRODUCTION

- Logic Family: It is a group of compatible ICs with the same logic levels and the supply voltages for performing various logic functions
- They have been fabricated using a specific circuit configuration.
- They are the building block of logic circuits.
- It is set of techniques used to implement logic within large scale ICs (LSI).

Implementing Logic Circuits

- There are several varieties of transistors – the building blocks of logic gates – the most important are:
  - **BJT (bipolar junction transistors)**
    - In this the current consists of both electron and hole flow, in different parts of the transistor
    - one of the first to be invented
  - **FET (field effect transistors) or [Unipolar Junction Transistor]**
    - In this the charge carriers that carry the current through the device are all of the same type i.e. either holes or electrons, but not both
      - especially Metal-Oxide Semiconductor types (MOSFET's)
      - MOSFET's are of two types: NMOS and PMOS
      - CMOS (Complementary Metal Oxide Semiconductor): It will consist of both N – MOSFET and P - MOSFET

Types of logic families



BIPOLAR ICs

- **Saturated Bipolar families are:**
  - Resistor-Transistor logic (RTL)
  - Direct-Coupled transistor logic (DCTIL)
  - Integrated-injection logic (IIL)
  - Diode-transistor logic (DTL)
  - High-Threshold logic (HTL)
  - Transistor-transistor logic (TTL)
- **Non-Saturated Bipolar families are**:
  - Schottkey TTL
  - Emitter - Coupled logic (ECL)

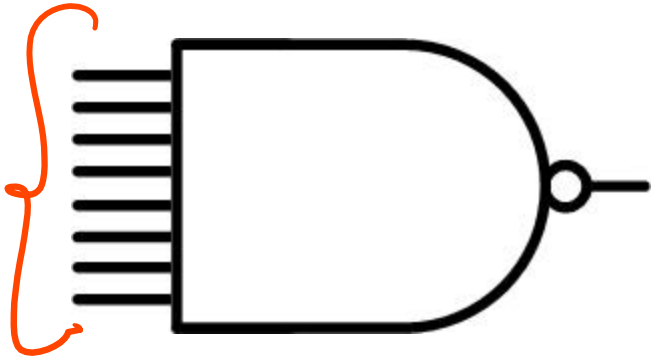
Basic Characteristics of IC's or Logic Family

- Propagation delay
- Power dissipation
- Fan in and fan out
- Noise immunity
- Power supply requirement
- Figure of merits i.e. speed power product
- Operating temperature
- Current and voltage parameters

Fan-In

- Number of input signals to a gate has
  - Not an electrical property
  - Function of the manufacturing process

NAND gate with a Fan-in of 8



Fan-Out (Loading Factor)

- The phenomenon when the output of one logic gate is connected with various inputs of other logic.
- The fan out depend on the nature of input devices that are connected to an output.
- Higher the fan out higher the current supplying capacity of a gate.
- E.g.. Fan out of 5 indicates that the gate can drive (supply current to) at most 5 inputs of same IC family
- If on the logic family, specified fan out of the gate is 10 then we should not load it with more than 10 gates.
- A typical figure of fan-out is ten (10)

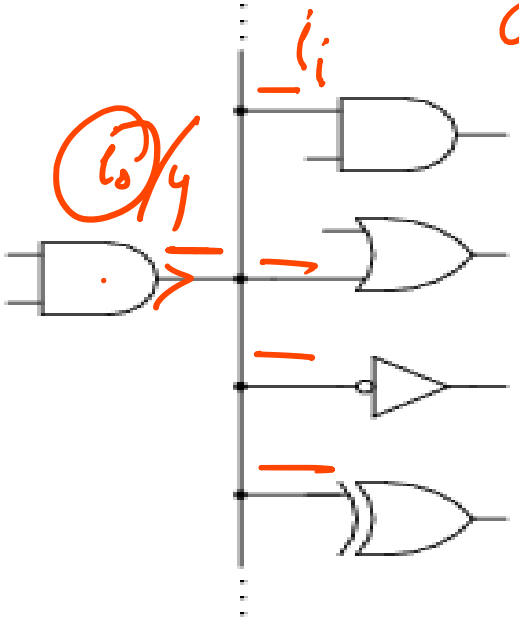


Figure shows, the fan out of the driven gate which is driving N number of gates is N

Noise Margin

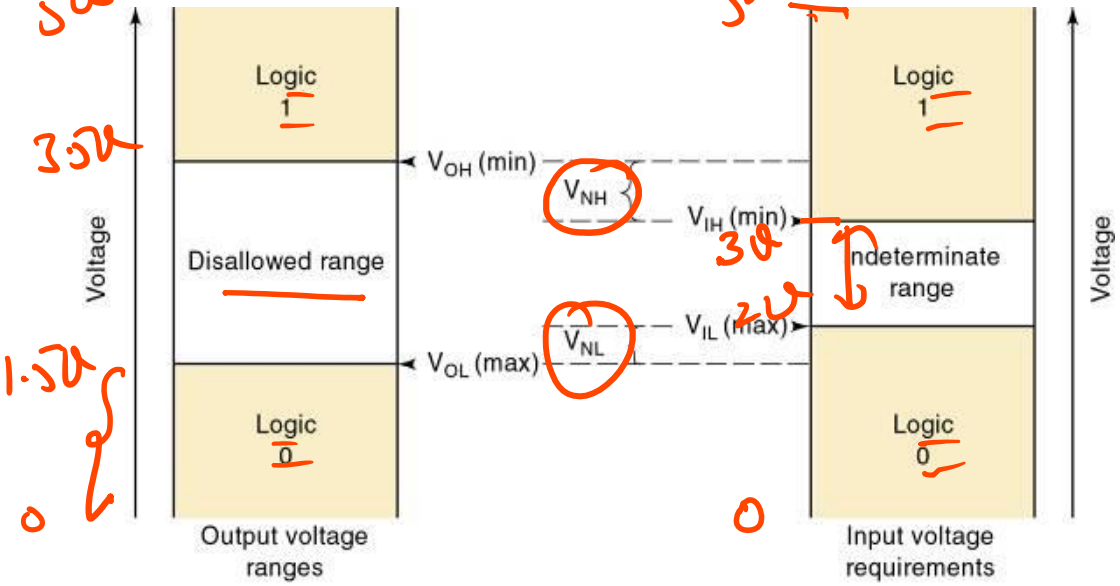
- **Noise immunity** refers to the circuit's ability to tolerate noise without changes in output voltage.
- A quantitative measure of noise immunity is called **noise margin.**

High-state noise

$$V_{NH} = V_{OH}(\text{min}) - V_{IH}(\text{min})$$

Low-state noise

$$V_{NL} = V_{IL}(\text{max}) - V_{OL}(\text{max})$$

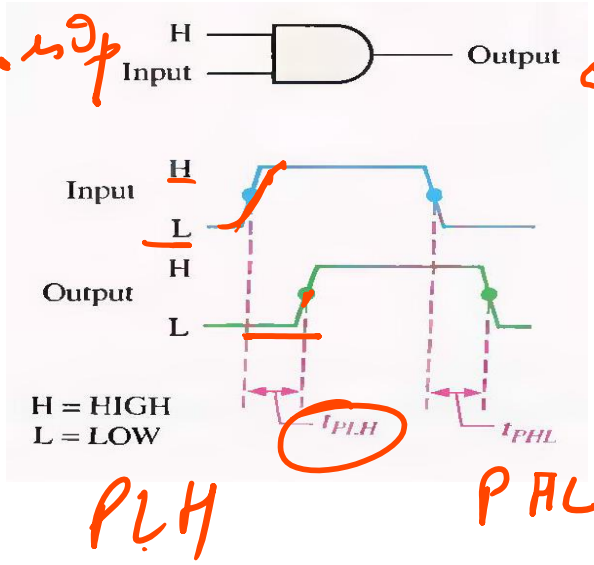


Propagation Delay (Speed of operation)

t_{PHL}: The time between a designated point on the input pulse and the corresponding point on the output pulse when the output is changing from HIGH to LOW.

t_{PLH}: The time between a designated point on the input pulse and the corresponding point on the output pulse when the output is changing from LOW to HIGH.

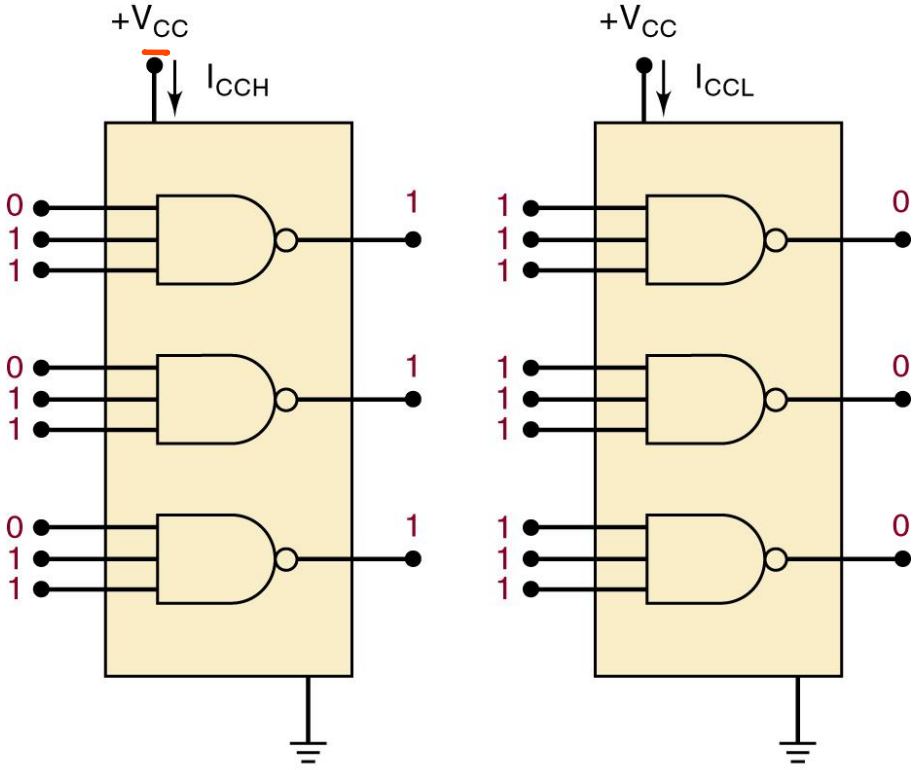
both t_{PLH} & t_{PHL} are measured between the 50% points on the input and output transitions



Power Dissipation

- The amount of power an IC requires is determined by the current, I_{CC} it draws from the supply.
  - Actual power is the product I_{CC} x V_{CC}

In some logic circuits, average current is computed based on the assumption that gate outputs are LOW half the time and HIGH half the time.



$$I_{CC}(\text{avg}) = \frac{I_{CCH} + I_{CCL}}{2}$$

$$P_D(\text{avg}) = I_{CC}(\text{avg}) \times V_{CC}$$

Operating Temperature

- For consumer application , the temperature is 0 to +70°C
- For industrial application , the temperature is -55°C to +125 °C
- The performance of gates will be in the specified limits over these temperature ranges

Figure of Merit (Speed Power Product (SPP)

- Figure of merit is the product of power dissipation and propagation delay. Speed in Nano seconds (nsecs) and Power in Milli Watts (mW)

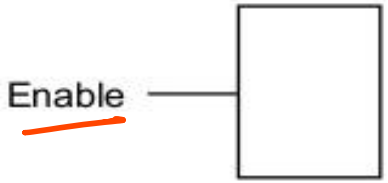
Figure of merit = Propagation delay time x Power Dissipation

- Practically figure of merit should be low as possible.
- **Figure of merit is always compromise between speed and power dissipation. That means if we try to reduce the propagation delay then the power dissipation will increase and vice – versa**
- The SPP is used as a common means for measuring and comparing the overall performance of different IC family.

Logic Level

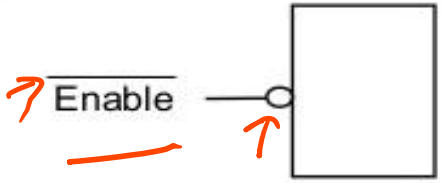
Positive & Negative Logic

Positive logic:



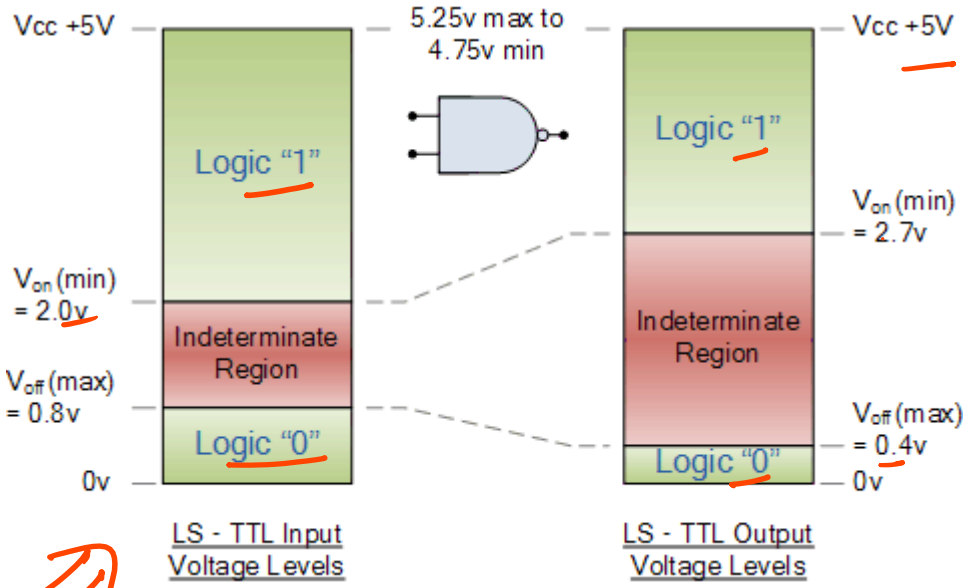
Active High:
0: Disabled
1: Enabled

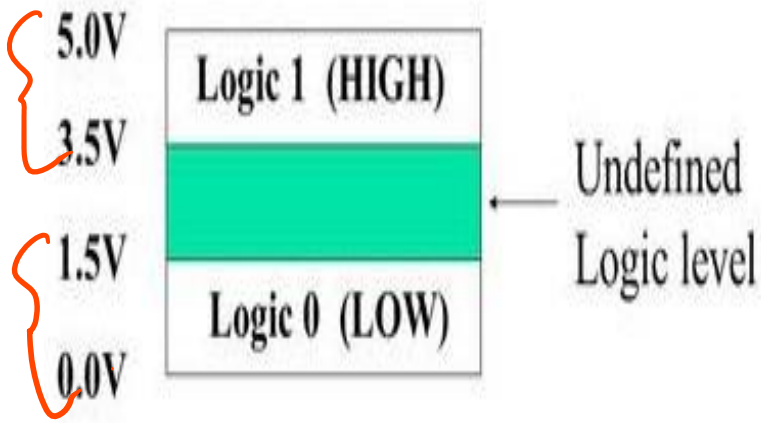
Negative logic:



Active Low:
0: Enabled
1: Disabled

TTL and CMOS Logic Levels





For CMOS

Device Type	Logic 0	Logic 1
TTL	0 to 0.8v	2.0 to 5v (V_{CC})
CMOS	0 to 1.5v	3.0 to 18v (V_{DD})

Highest and Lowest

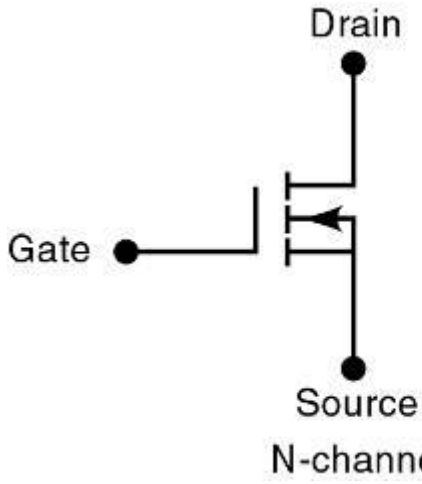
Parameters	Maximum	Minimum
Propagation delay	CMOS	ECL
Speed	ECL	CMOS
Fan Out	CMOS (>50)	TTL (About 10)
Power Dissipation	ECL	CMOS
Noise Immunity or Noise Margin	CMOS	RTL

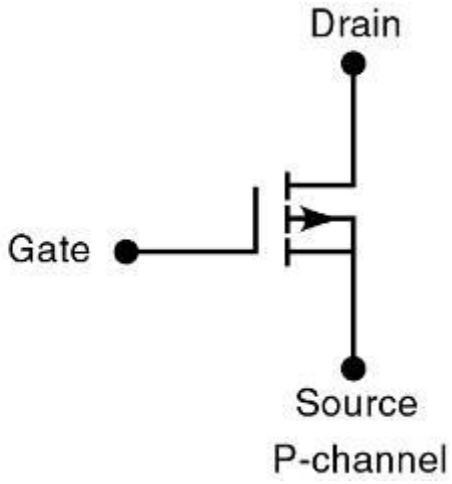
- **The most widely used bipolar technology for digital IC's is TTL**
- **CMOS logic has Smaller physical size.**
- **The IC's used in calculators and watches are of CMOS**

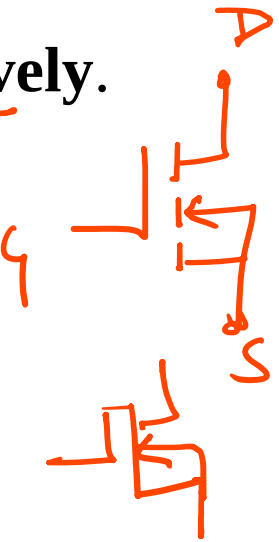
Parameter	CMOS	TTL	ECL
Devices Used	N – MOSFET and P – MOSFET	Bipolar Junction Transistor (BJT) •Multiple Emitter Transistor is used	Bipolar Junction Transistor (BJT)
Category	Unipolar Family	Saturated Bipolar Family	Unsaturated Bipolar Family
Basic Gates Used	NAND / NOR	NAND	OR / NOR
Fan – in	> 10	12 - 14	> 10
Fan – Out	50	10	25
Noise Margin	5V	0.4 V	0.25 V
Noise Immunity	Excellent	Very Good	Good
Power Dissipation per gate	0.01 mW	10 mW	50 mW
Dependence of Power Dissipation on Frequency	Increases with increase in frequency	Does not depend on frequency	
Propagation Delay	70 nSecs	10 nSecs	500 pSecs
Power Supply Voltage	Flexible from 3 V to 15 V	Fixed equal to 5 V	Negative supply
Temperature Range	Wide range upto - 233°C	74 Series: 0 to 70°C 54 Series: - 55 to 125°C	
Unconnected Inputs	Unused inputs should be connected to GND or Vcc. They should never be left floating.	Inputs can remain floating. The floating inputs are treated as logic 1	
Component Density	More than TTL since MOSFETs need smaller space while fabricating an IC	Less than CMOS since BJT needs more space	
Operating Areas	MOSFETs are operated as switches. i.e in the ohmic region or cut off region	Transistors are operated in Saturation Region or cutt off region.	Transistors are operate in either cut off or active region.
Cost	Low	Low	High
Logic Level	Positive [Logic 0: 0 to 1.5 V Logic 1: 3 to 18V]	Positive [Logic: 0 0 to 0.8 V Logic 1: 3 V to 18 V]	Negative

MOS Technology

- There are presently two general types of MOSFETs
  - *Depletion MOSFET*
  - *Enhancement MOSFET*
    - **MOS ICs use enhancement MOSFETs exclusively.**







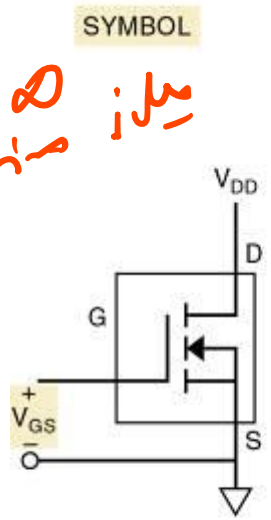
The direction of the arrow indicates either P- or N-channel. The symbols show a broken line between the *source* and the *drain* to indicate there is *normally* no conducting channel between these electrodes.

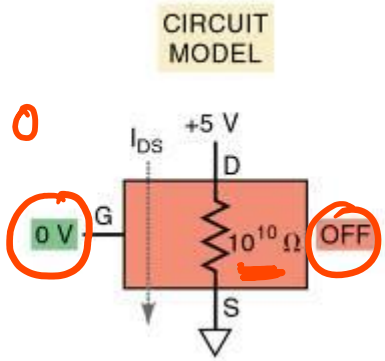
MOS Technology: Basic MOSFET Switch

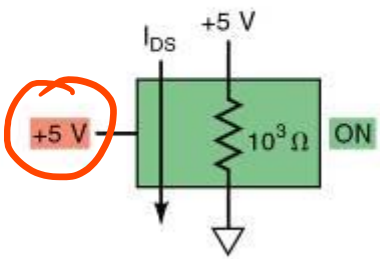
- An N-channel MOSFET is the basic element in a family of devices known as **N-MOS**.
- Drain is always biased positive relative to the source.

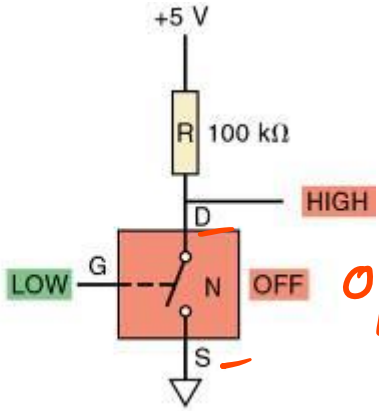
MOS Technology – Basic MOSFET Switch

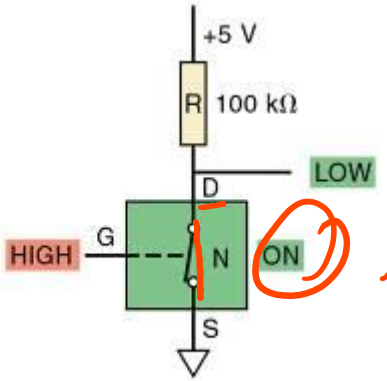
- Gate-to-source voltage V_{GS} is the input voltage.
  - Used to control resistance between drain & source.
    - Determines whether the device is on or off.









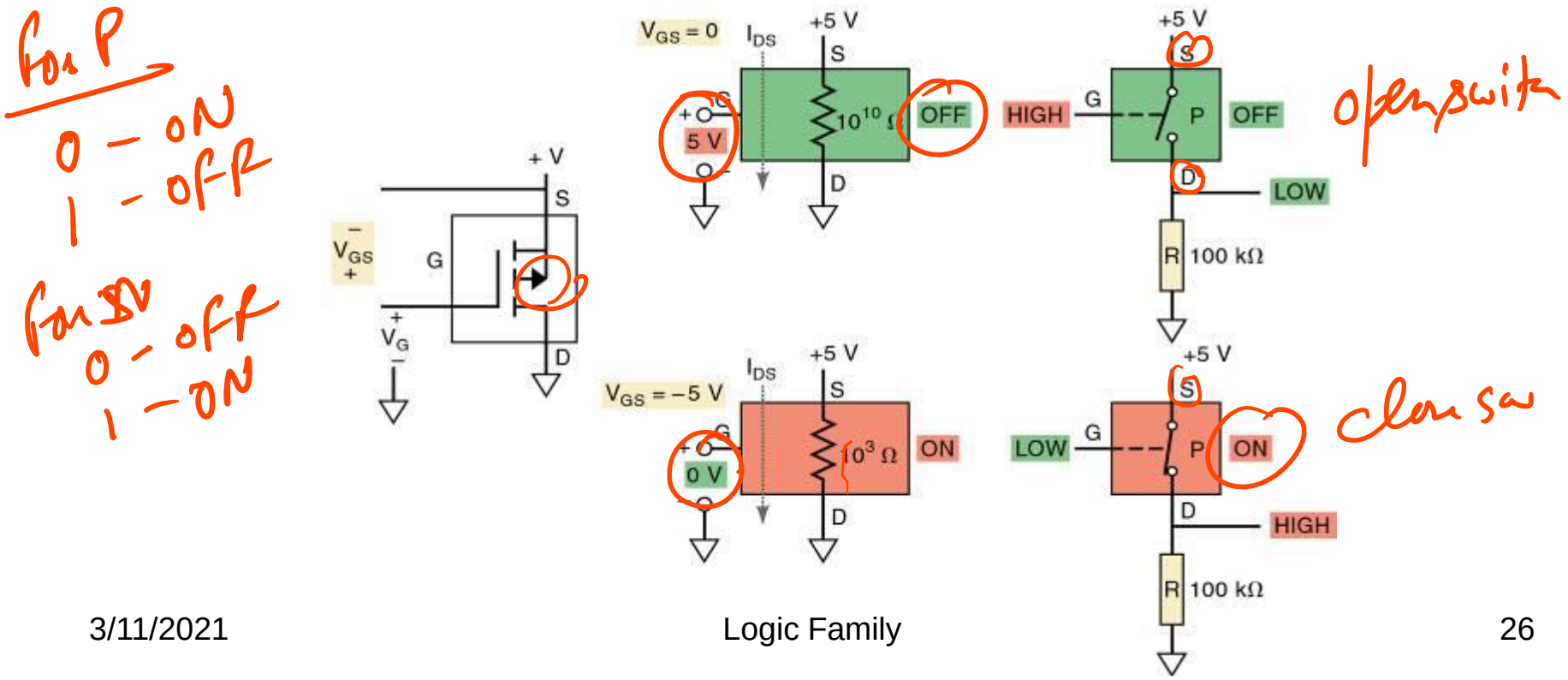


MOS Technology – Basic MOSFET Switch

- The P-channel MOSFET—**P-MOS**—operates in the same manner as the N-channel.
  - Except that it uses voltages of opposite polarity.
- The drain is connected to the lower side of the circuit so it is biased with a more negative voltage relative to the source.

MOS Technology – Basic MOSFET Switch

- To turn the P-MOSFET ON, a voltage *lower* than the source by V_T must be applied to the gate.
  - Voltage at the gate, relative to the source, must be negative.

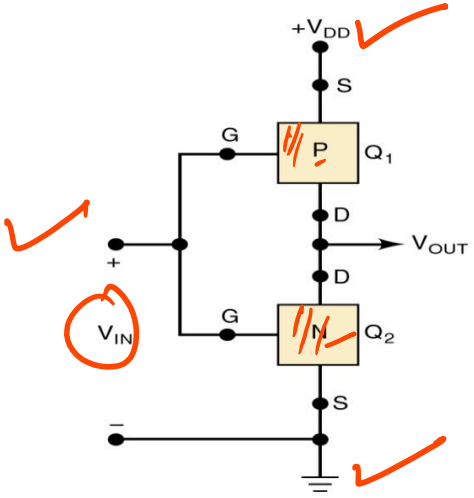


Complementary MOS Logic – CMOS Inverter

- P-MOS & N-MOS circuits began to dominate the LSI and VLSI markets in the 1970s and 1980s.
  - Use fewer components & are much simpler to manufacture than TTL circuits.
- During this era, technology emerged that used P-MOS & N-MOS transistors in the same circuit.
  - Complementary MOS, or **CMOS**, technology.

Complementary MOS Logic
CMOS Inverter

- The CMOS INVERTER has two MOSFETs in series.
  - The P-channel device source is connected to V_{DD} .
  - The N-channel device has its source connected to ground - usually labeled V_{SS}.
  - Gates of the two devices are connected together as a common input.
  - Drains are connected together as common output.

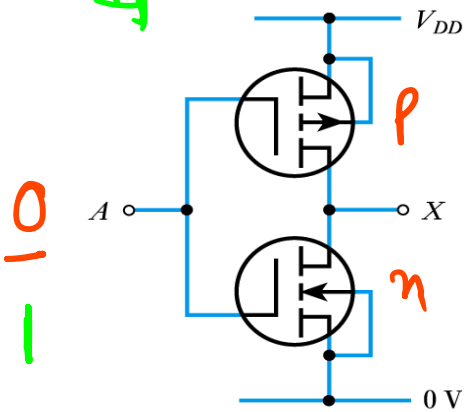


V_{IN}	Q_1	Q_2	V_{OUT}
$+V_{DD}$ (logic 1)	OFF $R_{OFF} = 10^{10}\ \Omega$	ON $R_{ON} = 1\ k\Omega$	≈ 0 V
0 V (logic 0)	ON $R_{ON} = 1\ k\Omega$	OFF $R_{OFF} = 10^{10}\ \Omega$	≈ $+V_{DD}$

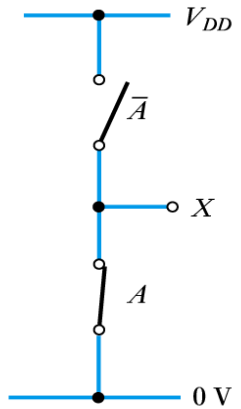
$V_{OUT} = \overline{V_{IN}}$

Basic CMOS INVERTER.

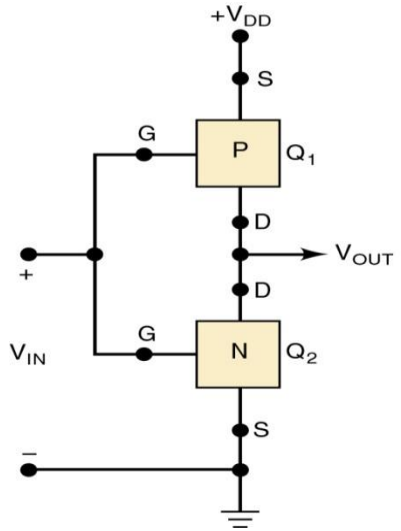
CMOS Inverter



(a) Circuit



(b) Equivalent circuit



V_{IN}	Q_1	Q_2	V_{OUT}
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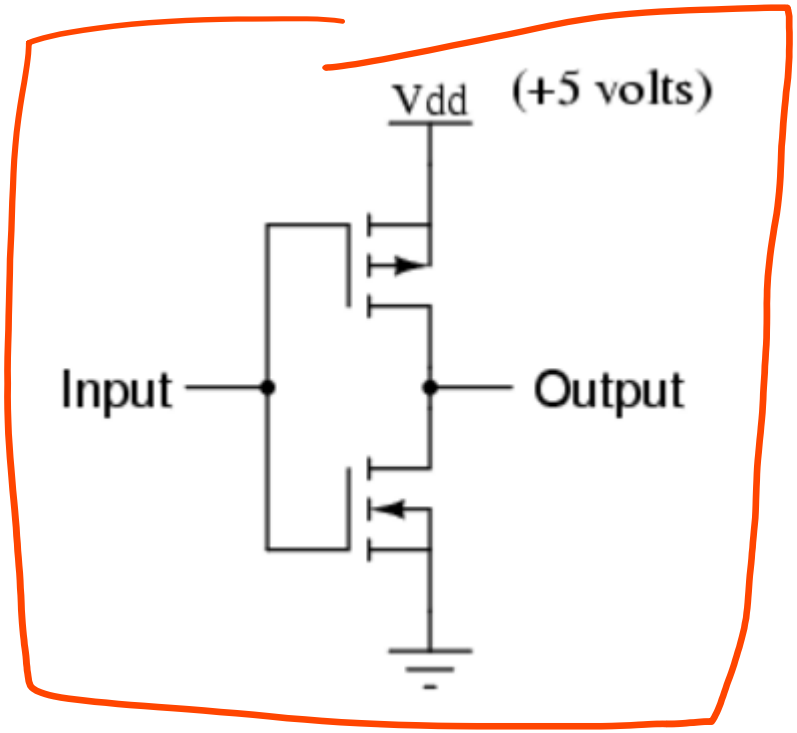
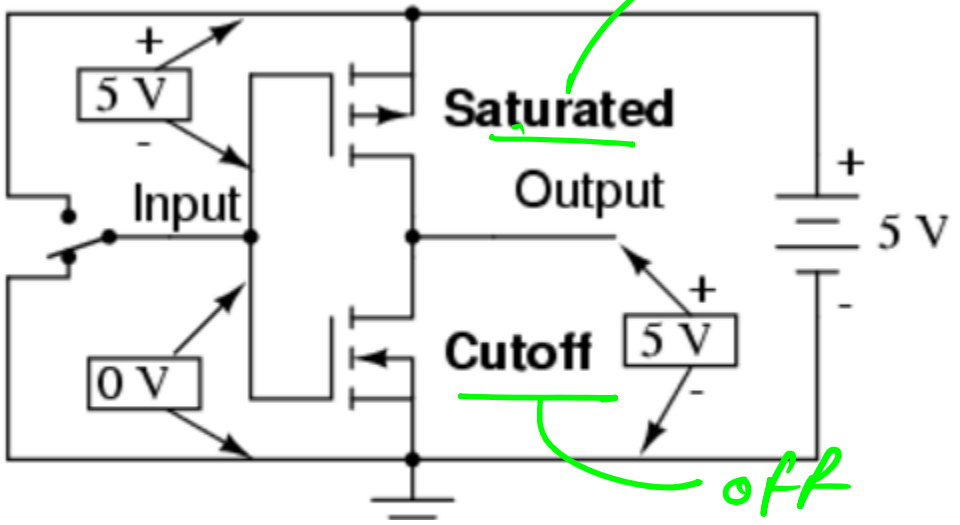
0 V (logic 0)	ON $R_{ON} = 1\ k\Omega$	OFF $R_{OFF} = 10^{10}\ \Omega$	≃ $+V_{DD}$

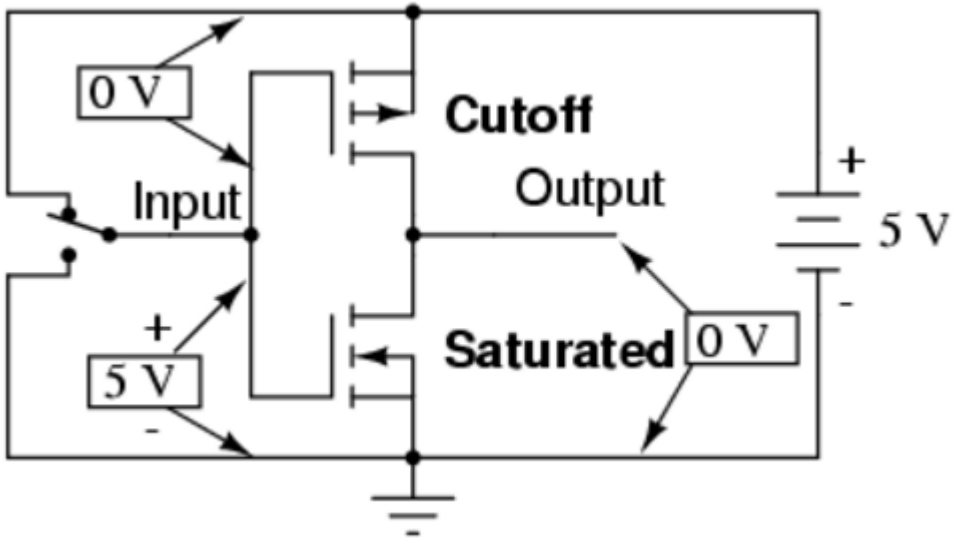
$V_{OUT} = \overline{V_{IN}}$

Basic CMOS INVERTER.

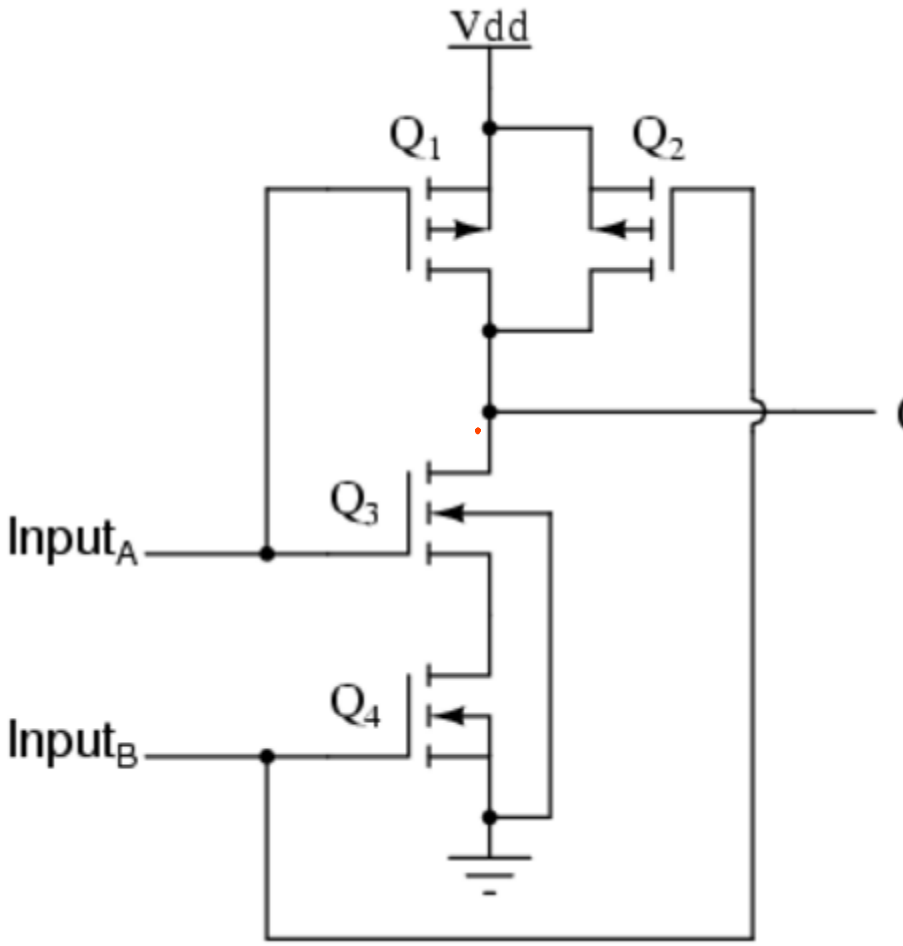
CMOS Inverter





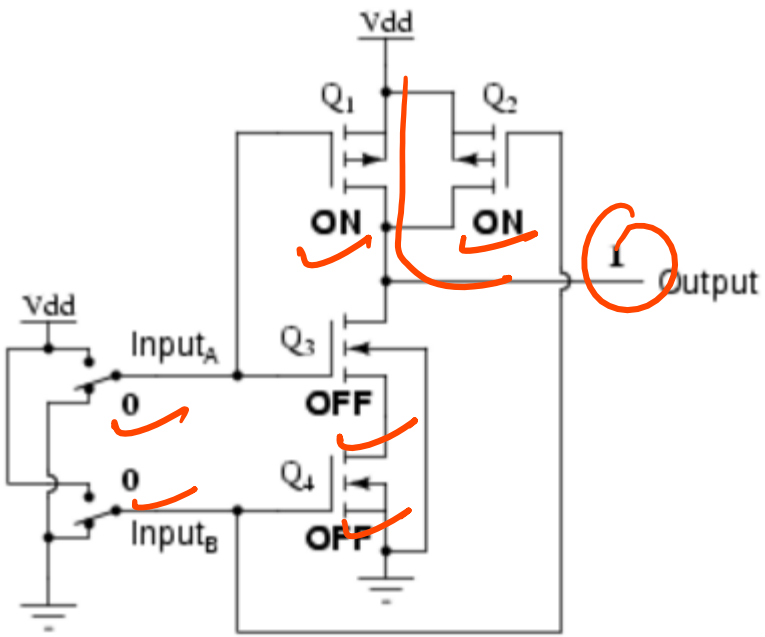


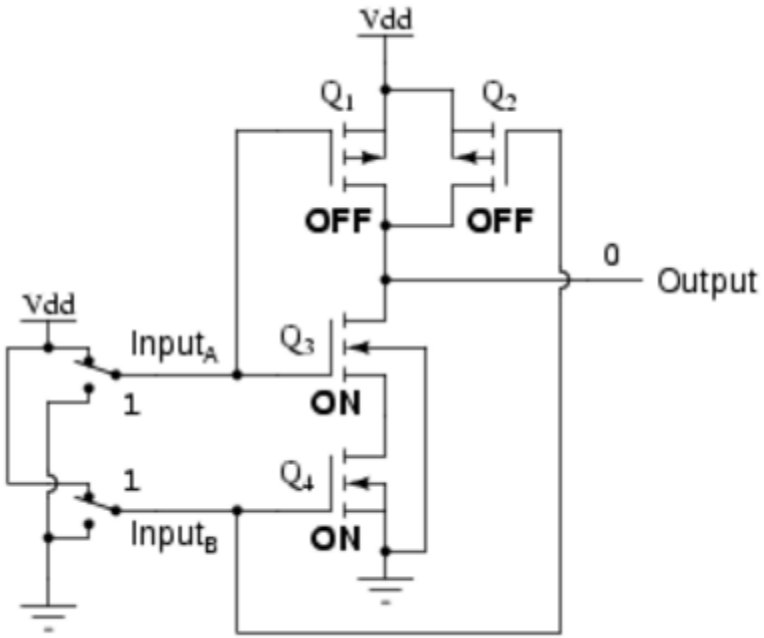
CMOS NAND



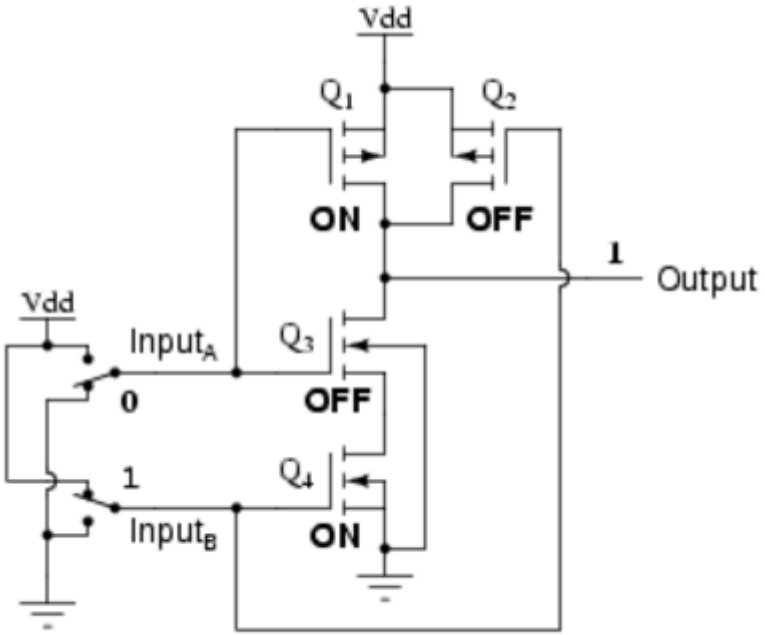
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

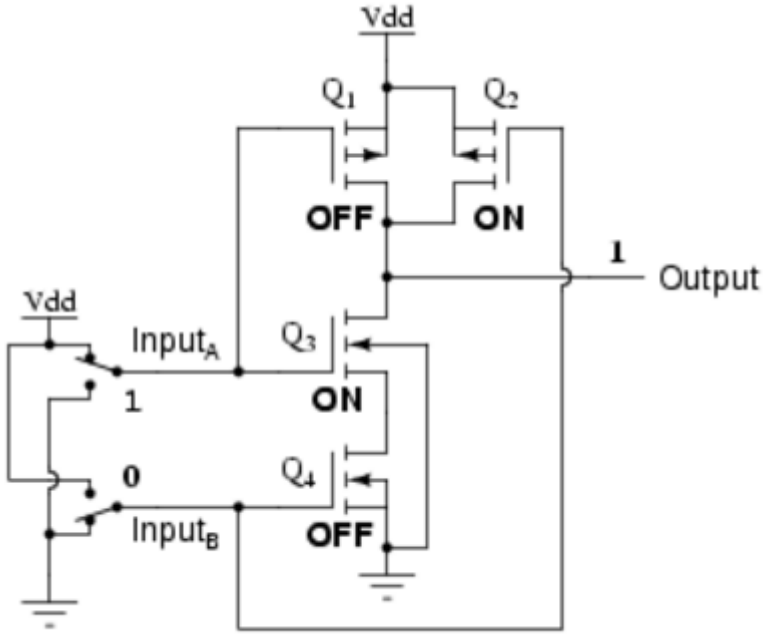
CMOS NAND


Vdd
Q1
Q2
ON
ON
1
Output
Vdd
Input$_A$
Q3
0
OFF
0
Q4
Input$_B$
OFF

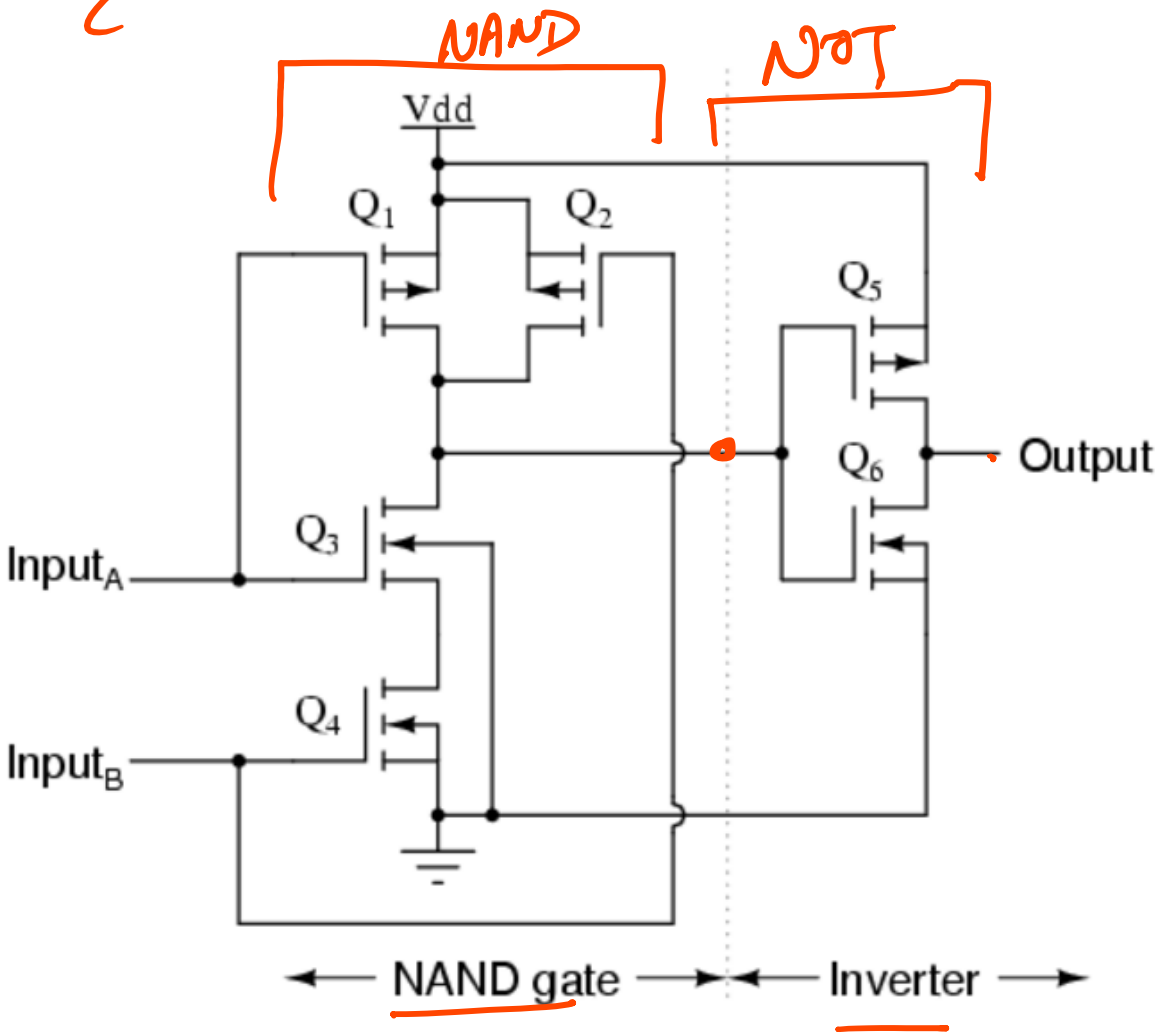

Vdd
Q1
Q2
OFF
OFF
0
Output
Vdd
Input$_A$
Q3
1
ON
1
Q4
Input$_B$
ON

CMOS NAND

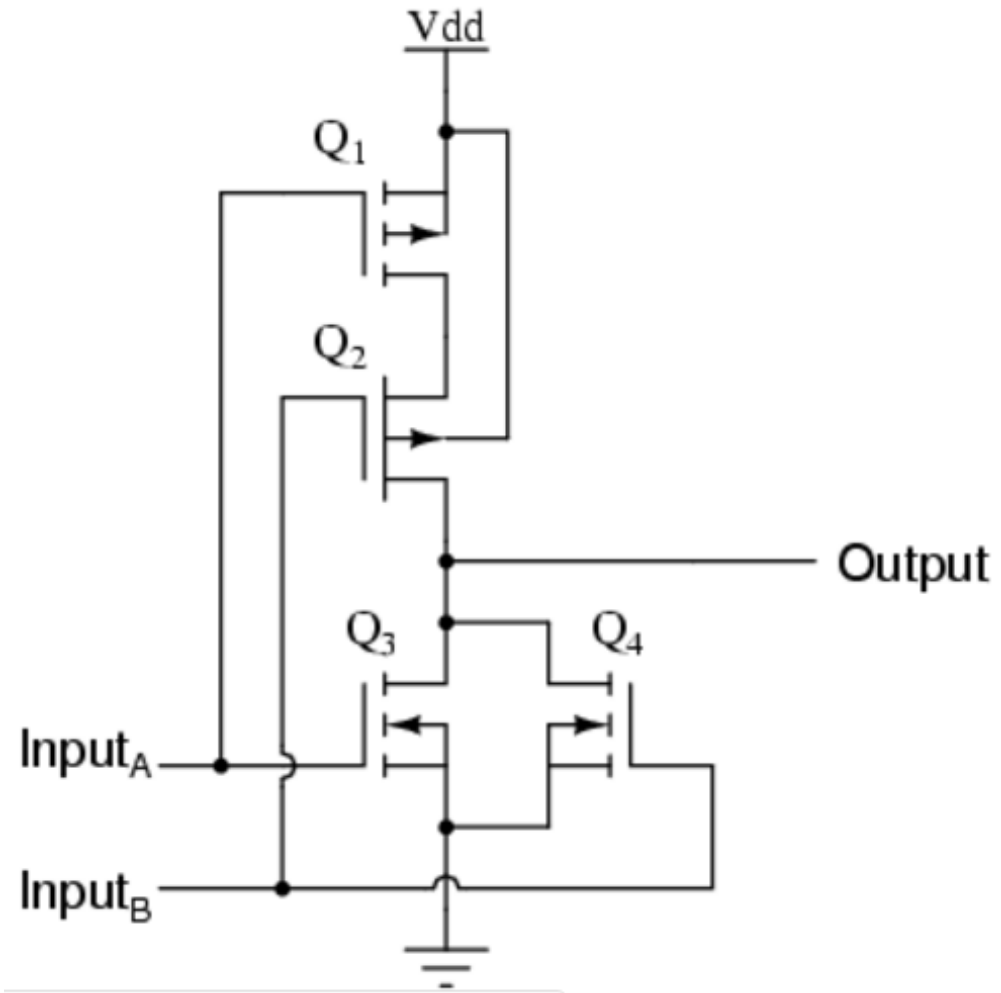

Vdd
Q1
Q2
ON
OFF
1
Output
Vdd
Input_A
Q3
0
OFF
1
Q4
Input_B
ON


Vdd
Q1
Q2
OFF
ON
1
Output
Vdd
Input_A
Q3
1
ON
0
Q4
Input_B
OFF

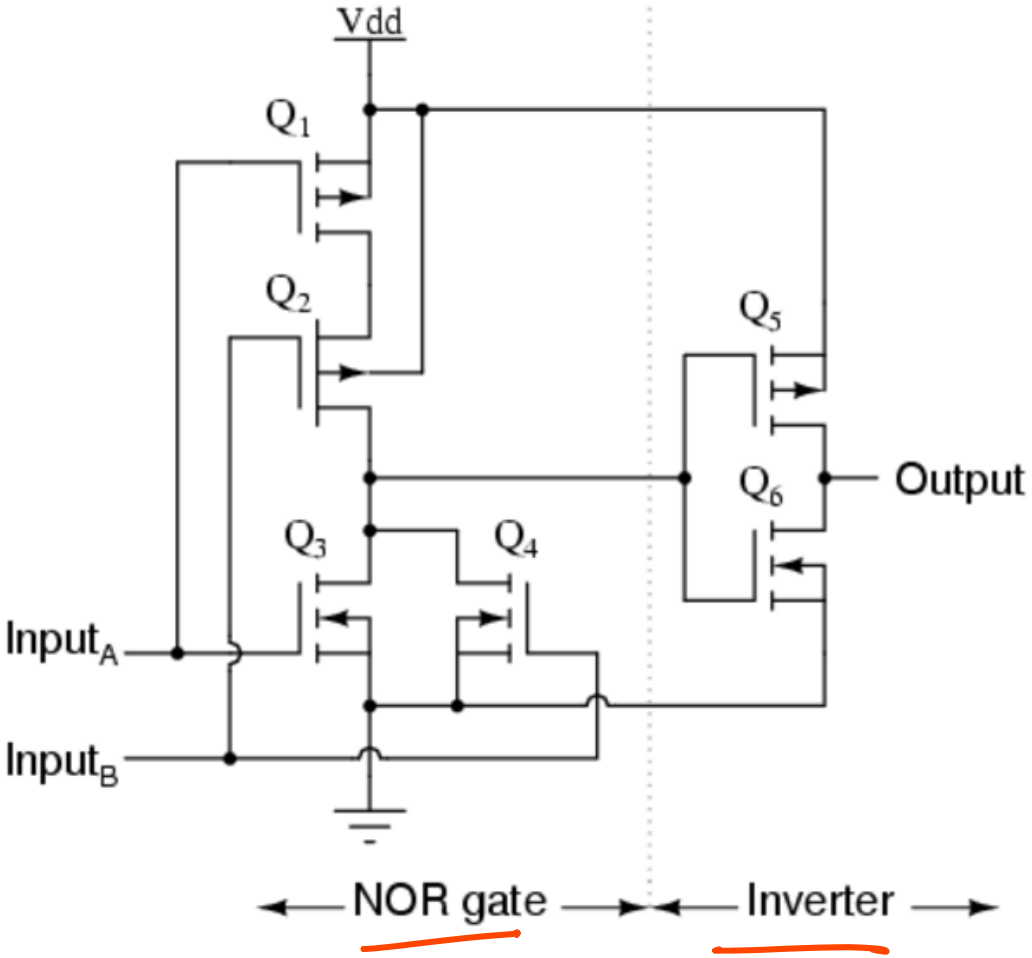
CMOS AND


NAND
NOT
Vdd
Q1
Q2
Q5
Q6
Output
Q3
InputA
Q4
InputB
NAND gate
Inverter

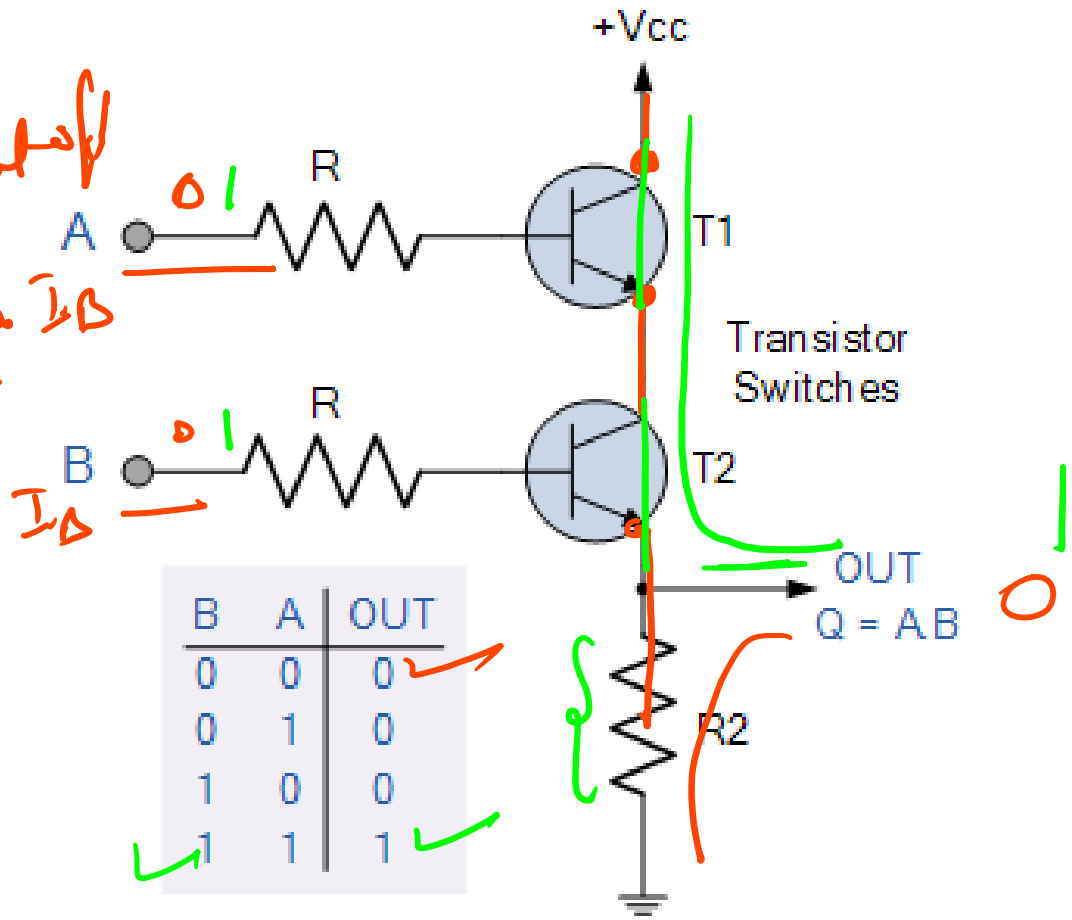
CMOS NOR



CMOS OR

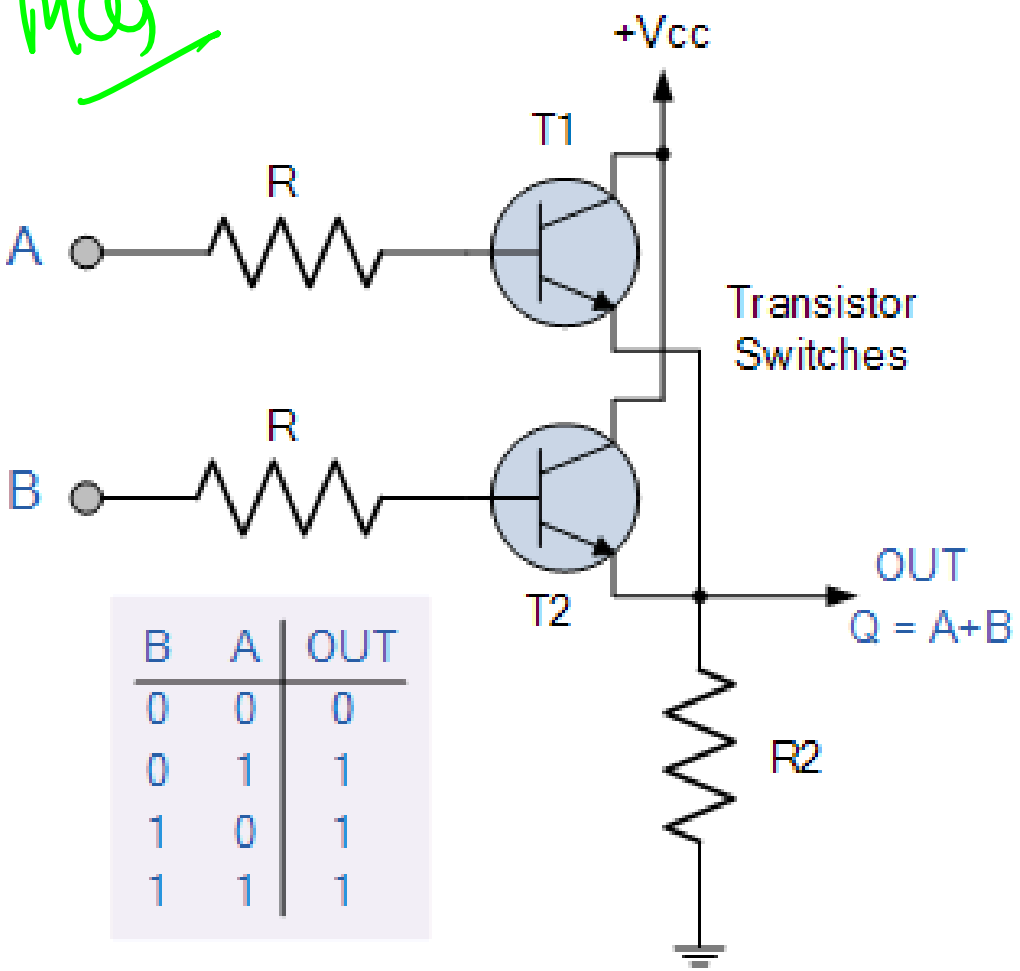


Application of Transistor
2-input Transistor AND Gate

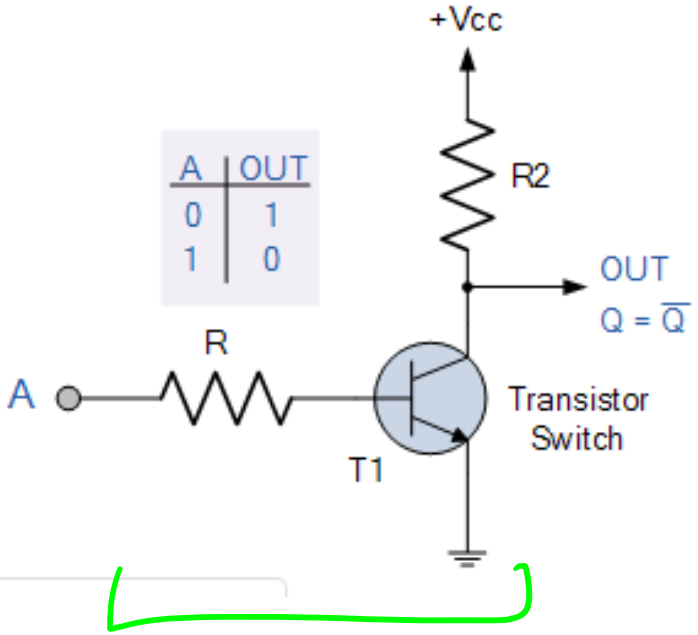


B	A	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Application of Transistor
2-input Transistor OR/NOT Gate



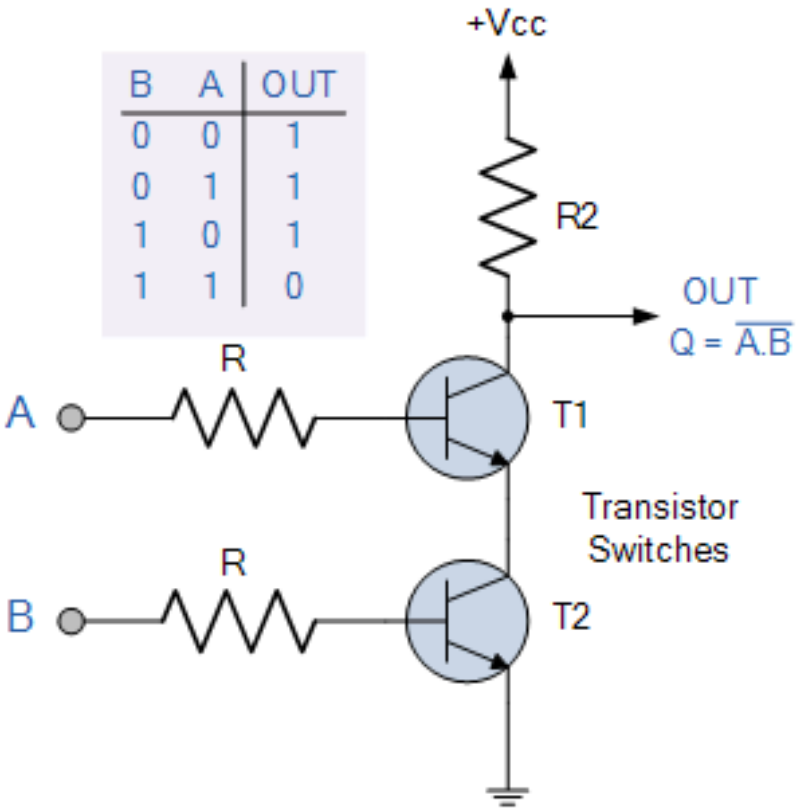
B	A	OUT
0	0	0
0	1	1
1	0	1
1	1	1

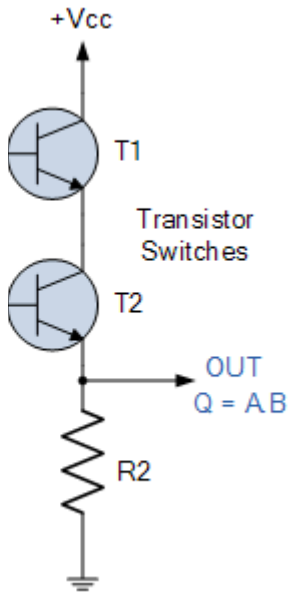


A	OUT
0	1
1	0

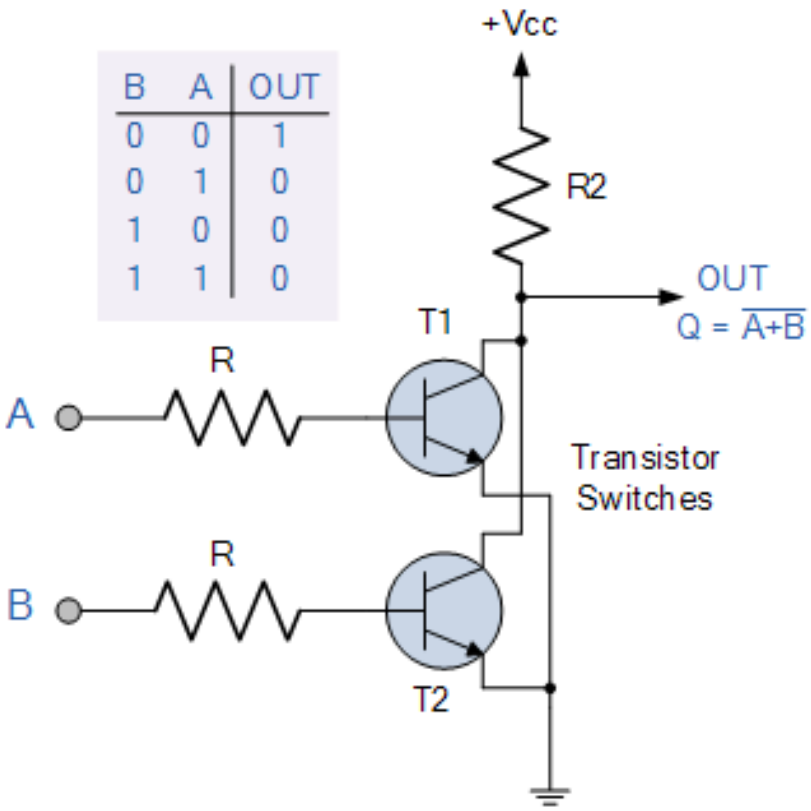
Application of Transistor
2-input Transistor NAND Gate

B	A	OUT
0	0	1
0	1	1
1	0	1
1	1	0

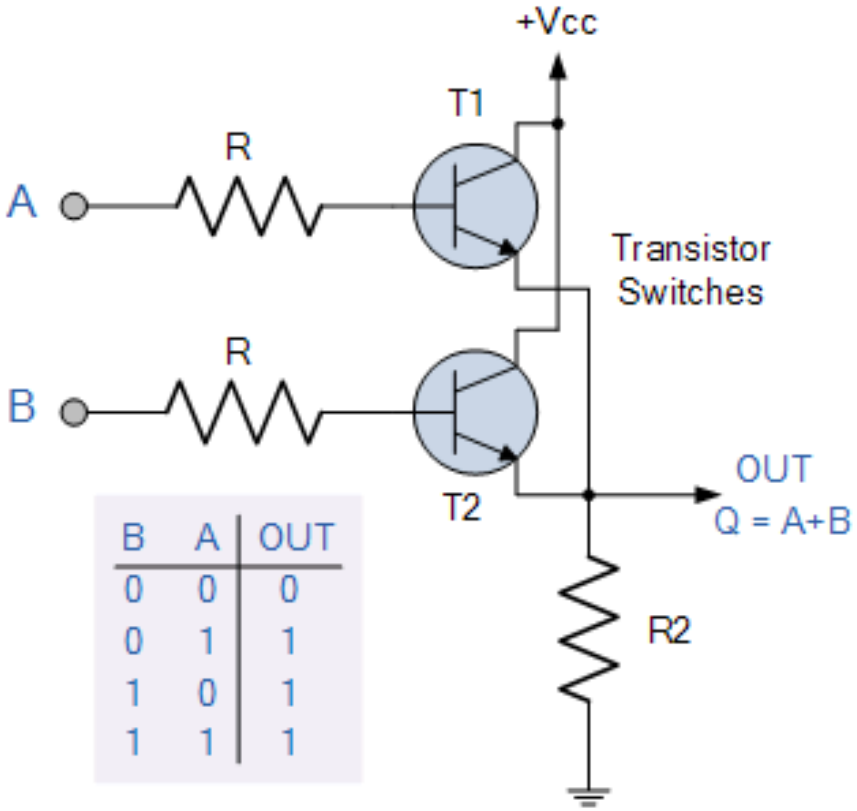




Application of Transistor
2-input Transistor NOR Gate



B	A	OUT
0	0	1
0	1	0
1	0	0
1	1	0



B	A	OUT
0	0	0
0	1	1
1	0	1
1	1	1

TTL Sub Families [For LAB]

Name of TTL Series	Full Form	Speed	Power Consumption
74 Series	Standard Series	74AS / 74 F	74 S
74 L	Low Power TTL	74 S	74
74 H	High Speed TTL	74 ALS	74 AS
74 S	Schottky TTL	74 LS	74 F
74 LS	Low Power Schottky TTL	74	74 LS
74 AS	Advanced Schottky TTL	74 L	74 ALS
74 ALS	Advanced Low Power Schottky		74 L
74 F	Fast TTL		
74 C	CMOS TTL Series		
74 HC	High Speed CMOS TTL series		

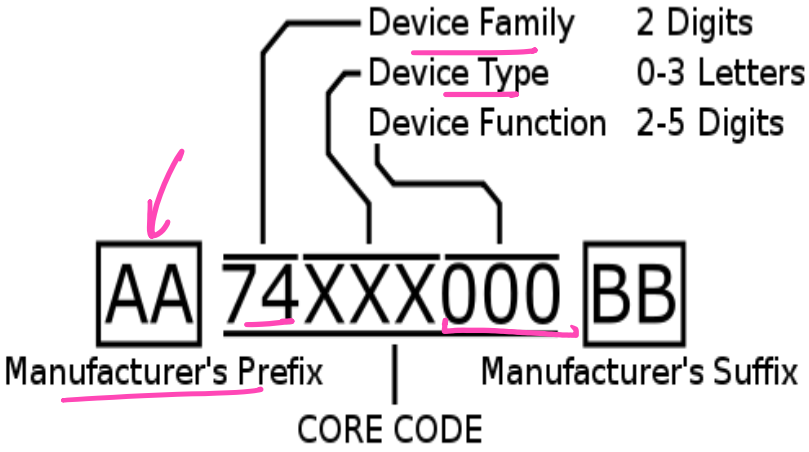
Fastest

Slowest

Highest

Lowest

IC Name



Manufacturer's Suffix
[Indicates the package Code]
For example
N - Plastic DIP package (N)

Code for Manufacturer
DM – National Semiconductor
NS – National Semiconductor
SN – Texas instruments
M – Motorola
TI – Texas Instruments
T- Toshiba
NE – New Era Electronics
F – Fairchild Semiconductor
D – Dallas Semiconductor
H – Hitachi

Gate Timing Diagram

AND Gate Timing Diagram