ECE213: Digital Electronics

Ajmer Singh

9988921373

ajmer.17381@lpu.co.in

The Course Contents

Unit V

Sequential Logic Circuits Applications : Registers: Operation of all basic Shift Registers, Counters: Design of Asynchronous and Synchronous counters, Ring counter and Johnson ring counter

Sequential Logic Circuits Applications

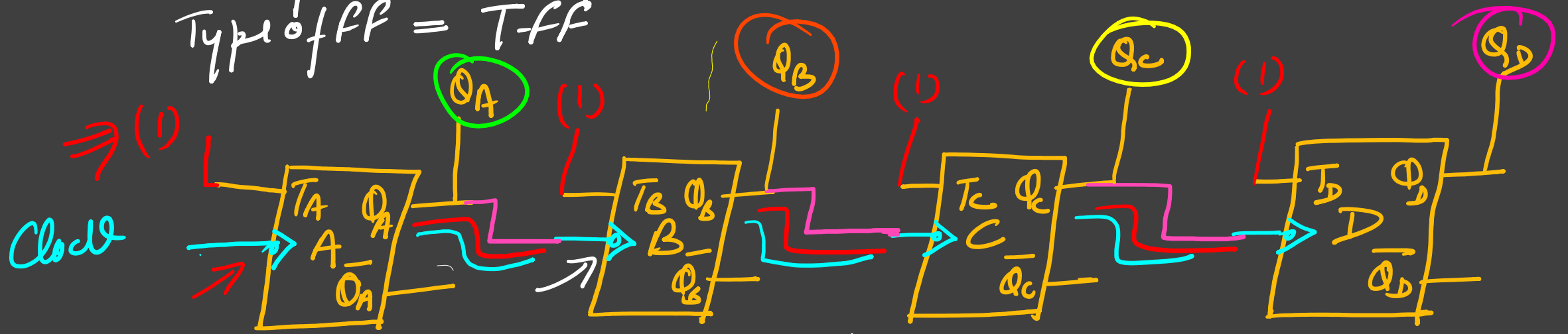
Counters

☆ Asynchronous Counter

4-bit up counter

Sol: No of FF = No of bits = 4

Type of FF = T-FF



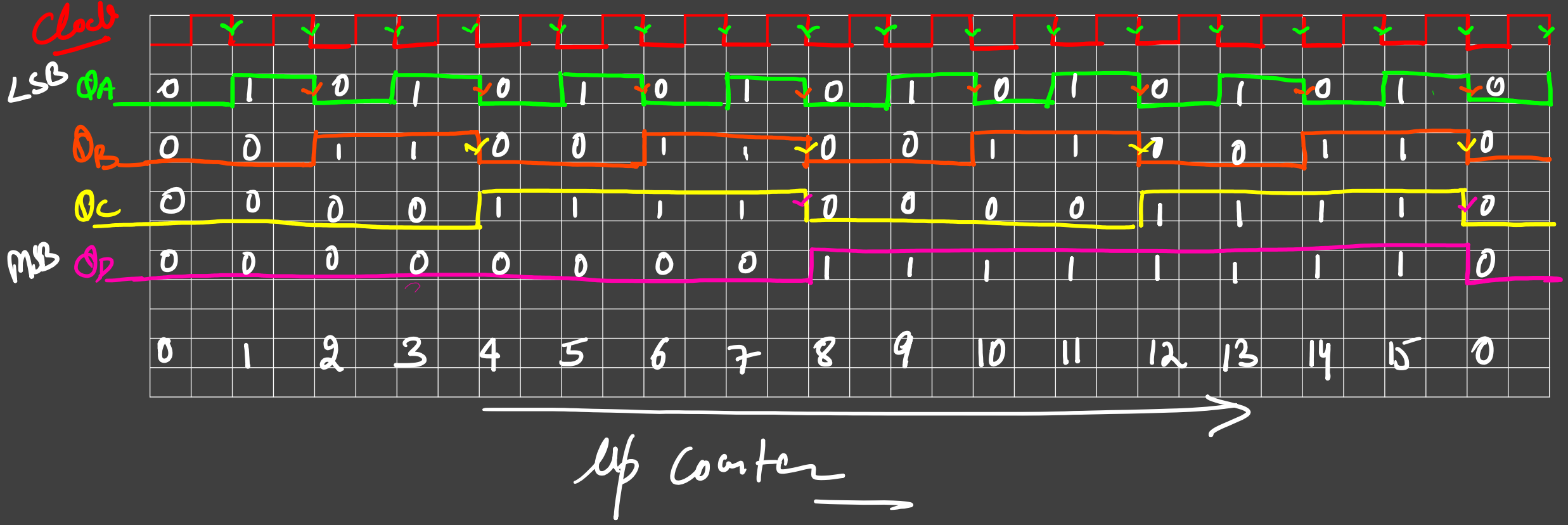
As per the connection the B-FF is going to toggle at the -ve edge of Q_A.

$\therefore$ Q_A is acting as clock for B-FF.

Sequential Logic Circuits Applications

Counters

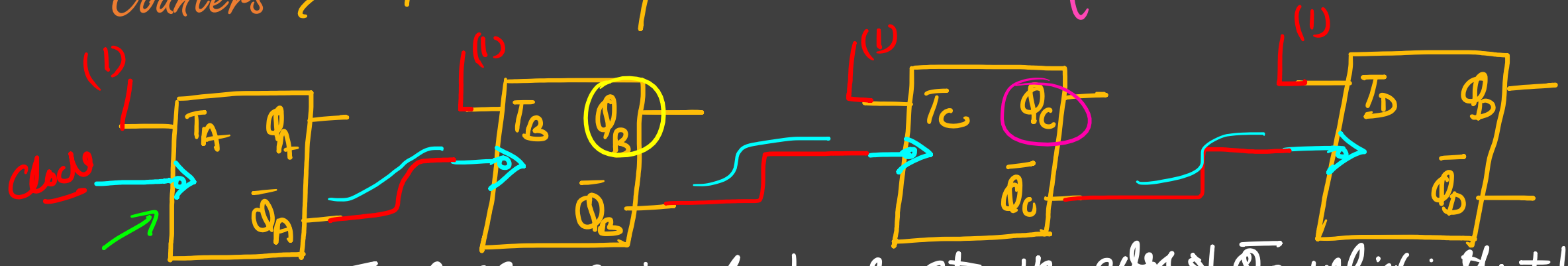
#Timing diagram



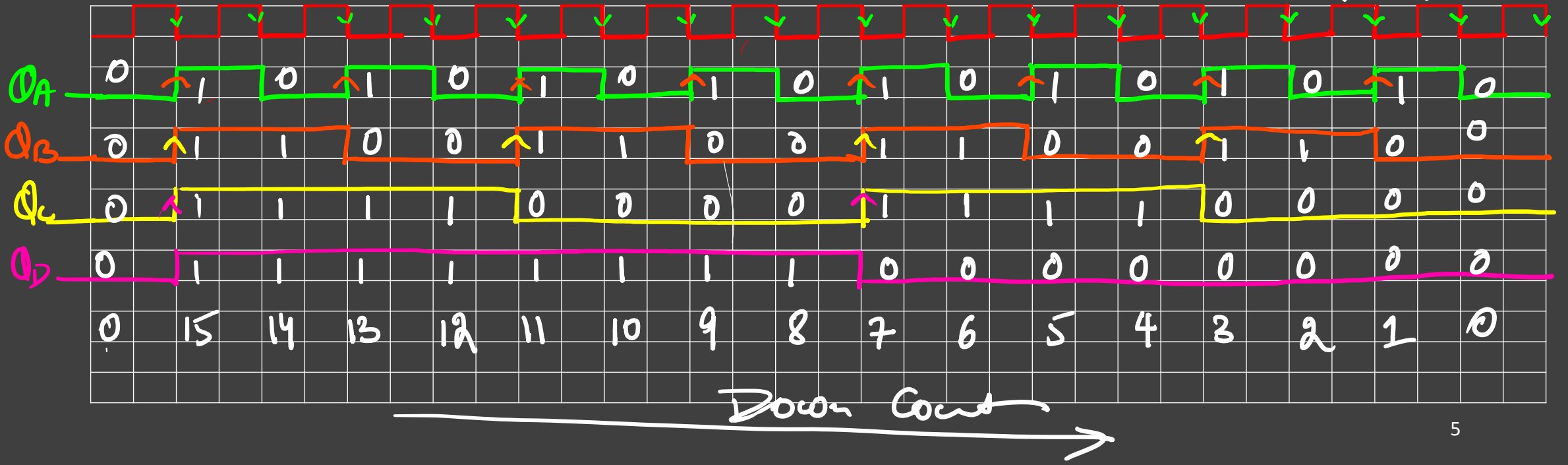
Sequential Logic Circuits Applications

Counters ★ 4-bit Asyn down Counter (with -ve clock)

Note: -ve edge of $\bar{Q}_A$ is same as +ve edge of Q_A.



The B, FF is going to toggle at -ve edge of $\bar{Q}_A$, which is the +ve edge of Q_A



Sequential Logic Circuits Applications

Counters ☆ 4-bit asyn up/docon.

- with -ve edge trigg FF (T-FF)

Note: With -ve edge trig FF, the count seq-up counter, if the clock of next FF get connected with the output of prev (Q)

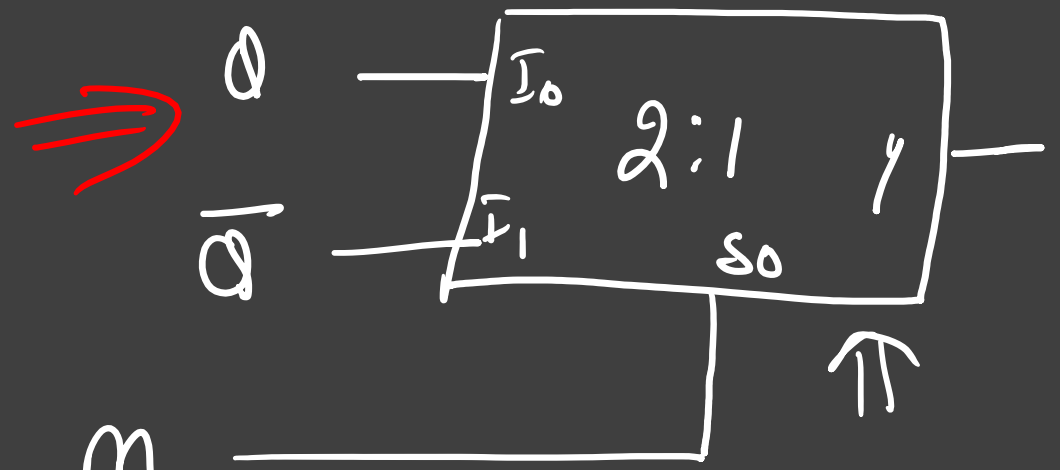
And

With -ve edge trig FF the Count seq Docon Counter, if the clock of next FF get connect with the complement o/p of prev ($\overline{Q}$)

Sequential Logic Circuits Applications

Counters

We have two inputs and one o/p, with one select input (M - mode)



We know the eq of 2:1 Mux -

(2) $y = \bar{S}_0 I_0 + S_0 I_1$

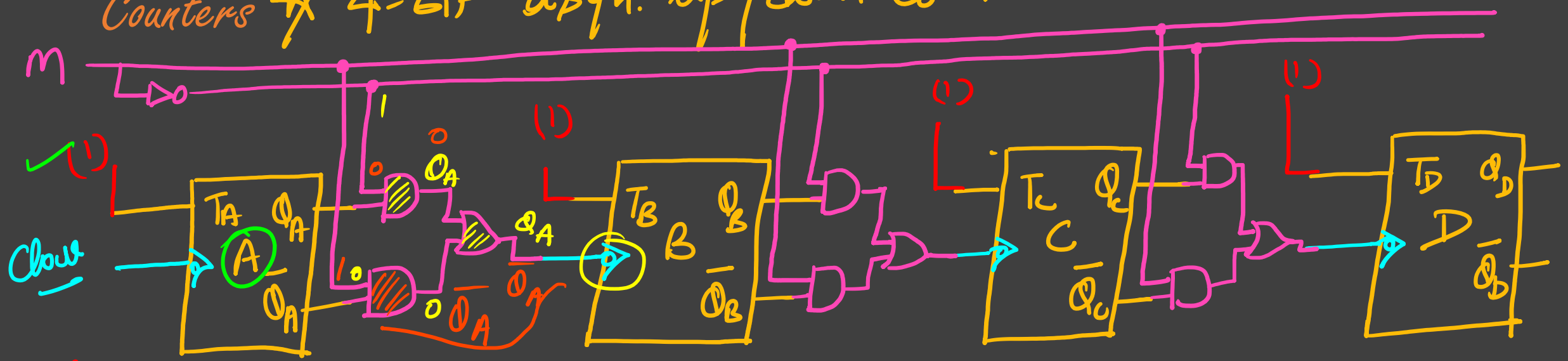
{ If M = 0 (For up count)
If M = 1 (For down count) }

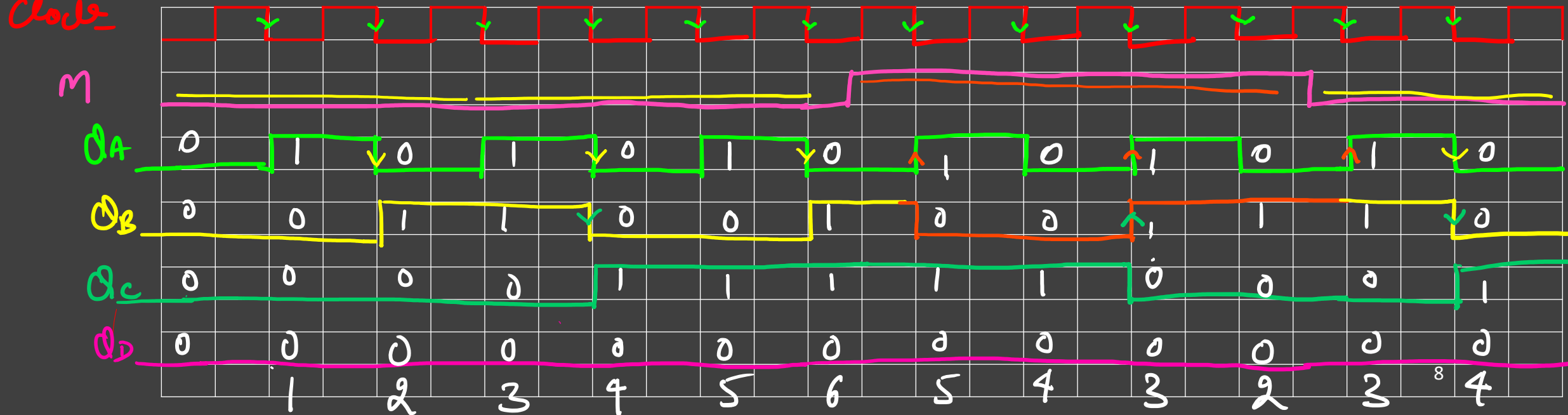
{ Clock = (1) $\bar{M}Q + M\bar{Q}$
$= M \oplus Q$ (3) }

Sequential Logic Circuits Applications

Counters ✶ 4-bit asyn. up/down Counter.

if M=0 (up count)
if M=1 (Down count)

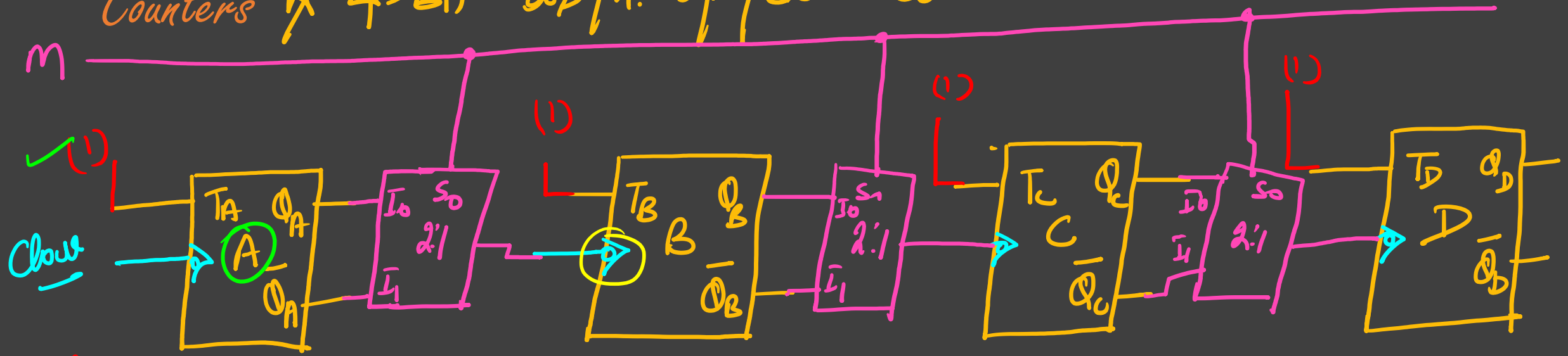


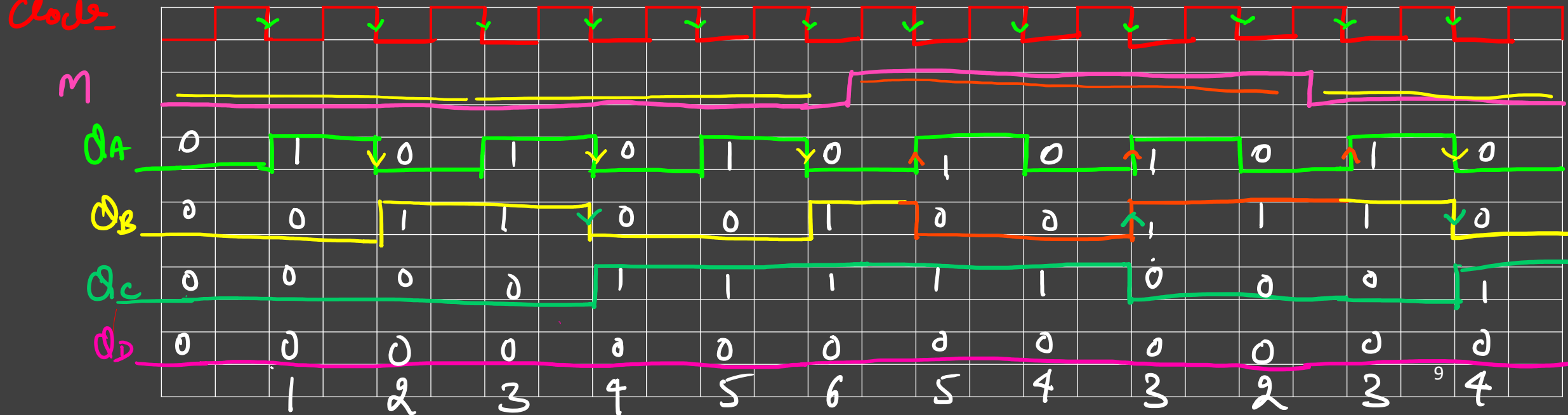


Sequential Logic Circuits Applications

Counters ✶ 4-bit asyn. up/down Counter.

if M=0 (up count)
if M=1 (Down count)





Sequential Logic Circuits Applications

Counters ✱ 4-bit asyn. up/down Counter.

if M=0 (up count)
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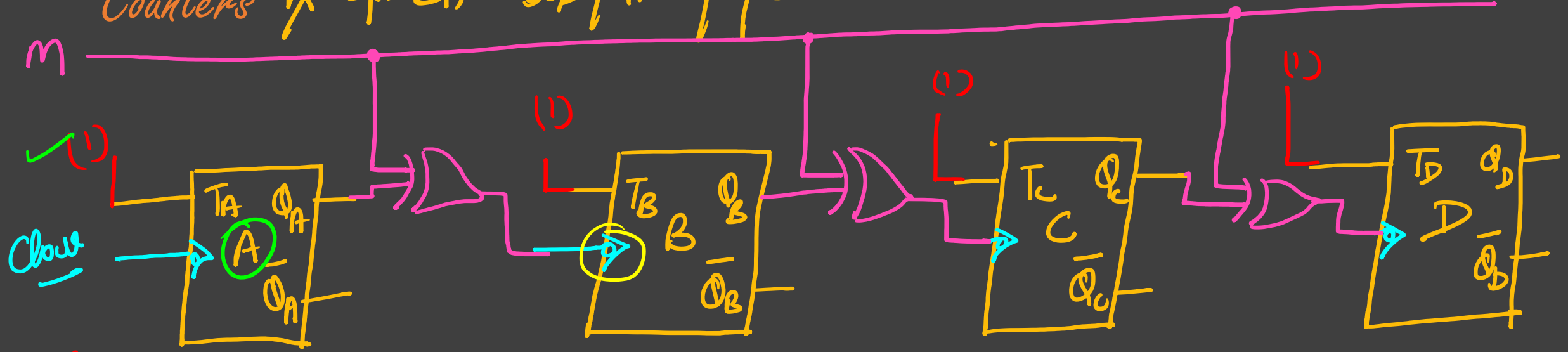
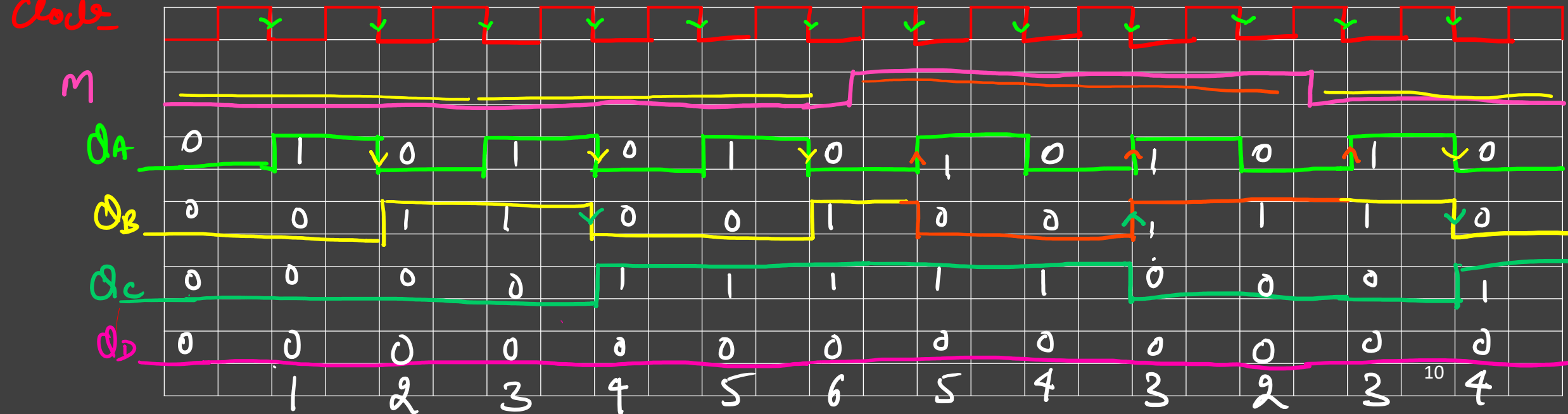




Sequential Logic Circuits Applications

Counters ☆ MOD Counter

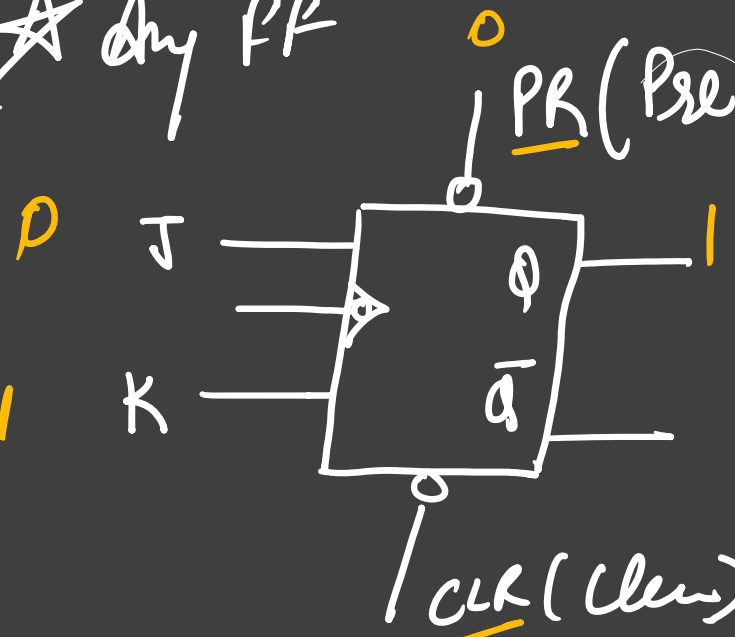
– A decimal numsa counts. 0, 1, 2, 3, 4, 5, 6, 7, 8, 9

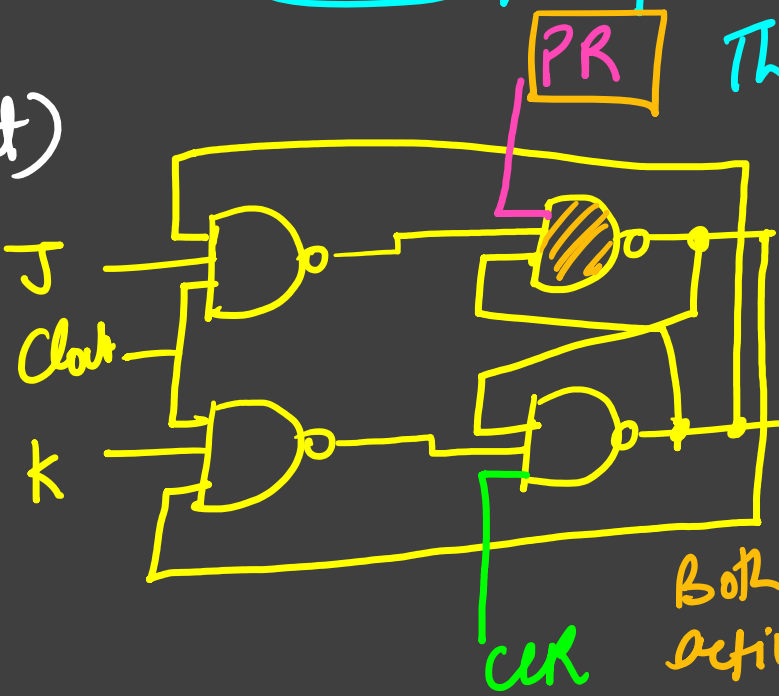
Q. How many no of bits required for decimal Counter?

A: 4-bits

1001

☆ Any FF





The range of 4-bit

0000 ↑ 1111

0000 ↑ 0001 ⋮ 1001 1010

Reset or Clear command

Both PR, CLR are active low input.

Note: If any of the i/p is low the o/p is high.