Lovely Professional University, Punjab

Course Code	Course Title	Course Planner
CSE211	COMPUTER ORGANIZATION AND DESIGN	22157::Gunseerat Kaur

Course Outcomes :Through this course students should be able to

CO1 :: illustrate the design of the various functional units and components of computers.

CO2 :: teach the basics of organizational and architectural issues of a digital computer and Classify and compute the performance of machines, Machine Instructions.

CO3 :: examine the elements of modern instructions sets and their impact on processor design.

CO4 :: compare the design issues in terms of speed, technology, cost, performance.

CO5 :: identify the performance of various classes of Memories, build large memories using small memories for better performance and analyze arithmetic for ALU implementation

CO6 :: understand the concepts of parallel processing, pipelining and interprocessor communication.

	TextBooks (T)		
Sr No	**Title**	**Author**	**Publisher Name**
T-1	COMPUTER SYSTEM ARCHITECTURE	MORRIS MANO	PRENTICE HALL

	Reference Books (R)		
Sr No	**Title**	**Author**	**Publisher Name**
R-1	COMPUTER ARCHITECTURE A QUANTITATIVE APPROACH	HENNESSY,J.L,DAVID A PATTERSON, AND GOLDBERG	PEARSON
R-2	COMPUTER ORGANIZATION AND ARCHITECTURE-DESIGNING FOR PERFORMANCE	WILLIAM STALLINGS	PRENTICE HALL

Other Reading (OR)	
Sr No	**Journals articles as Compulsary reading (specific articles, complete reference)**
OR-1	http://www.svecw.edu.in/Docs%5CITIIBTechIISemLecCOA.pdf ,
OR-2	http://www.pvpsiddhartha.ac.in/dep_it/lecturenotes/CSA/unit-2.pdf ,
OR-3	https://ieeexplore.ieee.org/document/8468702 ,

OR-4	https://ieeexplore.ieee.org/abstract/document/464688 ,
OR-5	https://ieeexplore.ieee.org/abstract/document/6522302 ,

Relevant Websites (RW)		
Sr No	**(Web address) (only if relevant to the course)**	**Salient Features**
RW-1	https://www.lkouniv.ac.in/site/writereaddata/siteContent/20200422161333844 5rohit_engg_pipelining_and_hazzard.pdf	Pipelining process
RW-2	https://www.britannica.com/technology/cache-memory	cache memory

LTP week distribution: (LTP Weeks)	
Weeks before MTE	7
Weeks After MTE	7
Spill Over (Lecture)	

Detailed Plan For Lectures

Week Number	**Lecture Number**	**Broad Topic(Sub Topic)**	**Chapters/Sections of Text/reference books**	**Other Readings, Relevant Websites, Audio Visual Aids, software and Virtual Labs**	**Lecture Description**	**Learning Outcomes**	**Pedagogical Tool Demonstration/ Case Study / Images / animation / ppt etc. Planned**	**Live Examples**
Week 1	Lecture 1	Basics Of Digital Electronics(Registers.)	T-1		Introduction to the course Introduction of digital computer, Logic gates and flip flops	Students will understand about course contents and basic of digital electronics	Demonstration with PPT	Digital electronics is based entirely on the fundamental principles of Boolean logic. Consider the following devices: i . A soda machine which accepts coins and dispenses cans of soda ii. a microwave oven with programmable power levels and timers iii. a hand-held calculator

Week 1	Lecture 1	Basics Of Digital Electronics(Introduction to combinational circuit)	T-1		Introduction to the course Introduction of digital computer, Logic gates and flip flops	Students will understand about course contents and basic of digital electronics	Demonstration with PPT	Digital electronics is based entirely on the fundamental principles of Boolean logic. Consider the following devices: i . A soda machine which accepts coins and dispenses cans of soda ii. a microwave oven with programmable power levels and timers iii. a hand-held calculator
		Basics Of Digital Electronics(introduction to sequential circuits)	T-1		Introduction to the course Introduction of digital computer, Logic gates and flip flops	Students will understand about course contents and basic of digital electronics	Demonstration with PPT	Digital electronics is based entirely on the fundamental principles of Boolean logic. Consider the following devices: i . A soda machine which accepts coins and dispenses cans of soda ii. a microwave oven with programmable power levels and timers iii. a hand-held calculator

Week 1	Lecture 2	Basics Of Digital Electronics(Registers.)	T-1		Introduction to the course Introduction of digital computer, Logic gates and flip flops	Students will understand about course contents and basic of digital electronics	Demonstration with PPT	Digital electronics is based entirely on the fundamental principles of Boolean logic. Consider the following devices: i . A soda machine which accepts coins and dispenses cans of soda ii. a microwave oven with programmable power levels and timers iii. a hand-held calculator
		Basics Of Digital Electronics(Introduction to combinational circuit)	T-1		Introduction to the course Introduction of digital computer, Logic gates and flip flops	Students will understand about course contents and basic of digital electronics	Demonstration with PPT	Digital electronics is based entirely on the fundamental principles of Boolean logic. Consider the following devices: i . A soda machine which accepts coins and dispenses cans of soda ii. a microwave oven with programmable power levels and timers iii. a hand-held calculator

Week 1	Lecture 2	Basics Of Digital Electronics(introduction to sequential circuits)	T-1		Introduction to the course Introduction of digital computer, Logic gates and flip flops	Students will understand about course contents and basic of digital electronics	Demonstration with PPT	Digital electronics is based entirely on the fundamental principles of Boolean logic. Consider the following devices: i . A soda machine which accepts coins and dispenses cans of soda ii. a microwave oven with programmable power levels and timers iii. a hand-held calculator
	Lecture 3	Basics Of Digital Electronics(Multiplexers and De multiplexers)	T-1		Introduction to multiplexers, Decoders, Flip flops	Students will understand how Muxs, Decoders, Flip flops function	Demonstration with diagrams	
		Basics Of Digital Electronics(Decoder and Encoder)	T-1		Introduction to multiplexers, Decoders, Flip flops	Students will understand how Muxs, Decoders, Flip flops function	Demonstration with diagrams	
Week 2	Lecture 4	Basics Of Digital Electronics(Multiplexers and De multiplexers)	T-1		Introduction to multiplexers, Decoders, Flip flops	Students will understand how Muxs, Decoders, Flip flops function	Demonstration with diagrams	
		Basics Of Digital Electronics(Decoder and Encoder)	T-1		Introduction to multiplexers, Decoders, Flip flops	Students will understand how Muxs, Decoders, Flip flops function	Demonstration with diagrams	
	Lecture 5	Register Transfer and Micro Operations(Register Transfer Language and Register Transfer)	T-1	OR-1	Discussion on Bus and Memory Transfers, Bus selection and three state bus buffers	i. Students will understand transfer between Processor registers through buses ii. Understand transfer between Processor register and memory through buses	Demonstration with images	

Week 2	Lecture 5	Register Transfer and Micro Operations(Bus and Memory Transfer)	T-1		Discussion on Bus and Memory Transfers, Bus selection and three state bus buffers	i. Students will understand transfer between Processor registers through buses ii. Understand transfer between Processor register and memory through buses	Demonstration with images	
	Lecture 6	Register Transfer and Micro Operations(Register Transfer Language and Register Transfer)	T-1	OR-1	Discussion on Bus and Memory Transfers, Bus selection and three state bus buffers	i. Students will understand transfer between Processor registers through buses ii. Understand transfer between Processor register and memory through buses	Demonstration with images	
		Register Transfer and Micro Operations(Bus and Memory Transfer)	T-1		Discussion on Bus and Memory Transfers, Bus selection and three state bus buffers	i. Students will understand transfer between Processor registers through buses ii. Understand transfer between Processor register and memory through buses	Demonstration with images	
Week 3	Lecture 7	Basics Of Digital Electronics(shift registers)	T-1 R-1		Operations are performed on the binary data stored in the register	Understand transfer between Processor register and memory through buses	Demonstration with images	
	Lecture 8	Register Transfer and Micro Operations(Logic Micro Operations)	T-1		Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	
		Register Transfer and Micro Operations(Shift Micro Operations)	T-1		Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	

Week 3	Lecture 8	Register Transfer and Micro Operations(Design of arithmetic logic unit.)	T-1	OR-2	Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	
		Register Transfer and Micro Operations(arithmetic microoperations)	T-1		Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	
	Lecture 9	Register Transfer and Micro Operations(Logic Micro Operations)	T-1		Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	
		Register Transfer and Micro Operations(Shift Micro Operations)	T-1		Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	
		Register Transfer and Micro Operations(Design of arithmetic logic unit.)	T-1	OR-2	Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	
		Register Transfer and Micro Operations(arithmetic microoperations)	T-1		Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	
Week 4	Lecture 10	Register Transfer and Micro Operations(Logic Micro Operations)	T-1		Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	
		Register Transfer and Micro Operations(Shift Micro Operations)	T-1		Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	

Week 4	Lecture 10	Register Transfer and Micro Operations(Design of arithmetic logic unit.)	T-1	OR-2	Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	
		Register Transfer and Micro Operations(arithmetic microoperations)	T-1		Operations are performed on the binary data stored in the register	Student will learn about the 16 micro-operations and practice its applications on ALSU	Peer learning, Flipped classroom, Demonstration with images	
	Lecture 11	Computer Organization (instruction codes)	T-1 R-2		Introduction to basic computer organization and show how its operation can be specified with register transfer statement.	i. Students will understand about internal registers,control structure and instruction . ii. Understanding of Common bus system	Flipped classroom, demonstration with images	
		Computer Organization (computer registers)	T-1 R-2		Introduction to basic computer organization and show how its operation can be specified with register transfer statement.	i. Students will understand about internal registers,control structure and instruction . ii. Understanding of Common bus system	Flipped classroom, demonstration with images	
		Computer Organization (common bus system)	T-1 R-2		Introduction to basic computer organization and show how its operation can be specified with register transfer statement.	i. Students will understand about internal registers,control structure and instruction . ii. Understanding of Common bus system	Flipped classroom, demonstration with images	
	Lecture 12	Computer Organization (computer instructions)	T-1 R-2		Explain the basics of instruction execution on a computer.	Understand the characteristics of an instruction set and how it maps to underlying hardware. ii. Identify and analyze the design and function of the basic instruction execution elements of a modern processor	Peer learning, demonstration with images	

Week 4	Lecture 12	Computer Organization (timing and control)	T-1 R-2		Explain the basics of instruction execution on a computer.	Understand the characteristics of an instruction set and how it maps to underlying hardware. ii. Identify and analyze the design and function of the basic instruction execution elements of a modern processor	Peer learning, demonstration with images	
		Computer Organization (instruction cycle)	T-1 R-2		Explain the basics of instruction execution on a computer.	Understand the characteristics of an instruction set and how it maps to underlying hardware. ii. Identify and analyze the design and function of the basic instruction execution elements of a modern processor	Peer learning, demonstration with images	
Week 5	Lecture 13	Computer Organization (memory reference instructions)	T-1 R-1		Discussion on memory reference instructions and interrupt cycle	Students will identify and analyze the design and function of the basic instruction execution elements of a modern processor	Discussion thorough knowledge and understanding of key concepts	
		Computer Organization (input-output and interrupt)	T-1 R-1		Discussion on memory reference instructions and interrupt cycle	Students will identify and analyze the design and function of the basic instruction execution elements of a modern processor	Discussion thorough knowledge and understanding of key concepts	
	Lecture 14	Computer Organization (memory reference instructions)	T-1 R-1		Discussion on memory reference instructions and interrupt cycle	Students will identify and analyze the design and function of the basic instruction execution elements of a modern processor	Discussion thorough knowledge and understanding of key concepts	

Week 5	Lecture 14	Computer Organization (input-output and interrupt)	T-1 R-1		Discussion on memory reference instructions and interrupt cycle	Students will identify and analyze the design and function of the basic instruction execution elements of a modern processor	Discussion thorough knowledge and understanding of key concepts	
	Lecture 15				Online Assignment			
Week 6	Lecture 16	Central Processing Unit (Addressing Modes)	T-1		Describing about different modes of transfer and categories of computer instruction	Students will learn about computer instruction and data transfer instruction	Students will learn about computer instruction and data transfer instruction	
	Lecture 17	Central Processing Unit (General Register Organization)	T-1		Introduction to various data processing operations performed in CPU and storage device that store information	i) Understand the organization and architecture of CPU. ii) To understand stack based processor organization. ii. Instruction set of a stack organized processor	Discussion with examples, peer learning, demonstration with images	
		Central Processing Unit (Stack Organization)	T-1		Introduction to various data processing operations performed in CPU and storage device that store information	i) Understand the organization and architecture of CPU. ii) To understand stack based processor organization. ii. Instruction set of a stack organized processor	Discussion with examples, peer learning, demonstration with images	
	Lecture 18	Central Processing Unit (Reduced instruction set computer)	T-1 R-1	OR-3 OR-4	CISC and RISC variable length instructions in multiple cycles	Students will understand the CISC and RISC Architecture	peer learning, demonstration with images	
		Central Processing Unit (Complex instruction set computer)	T-1 R-1	OR-5	CISC and RISC variable length instructions in multiple cycles	Students will understand the CISC and RISC Architecture	peer learning, demonstration with images	
Week 7	Lecture 19	Central Processing Unit (instruction formats)	T-1		Describing about different modes of transfer and categories of computer instruction including program control instructions	Students will learn about computer instruction and data transfer instruction	Demonstration with images, real examples, peer learning	

		SPILL OVER						
Week 7	Lecture 21				Spill Over			
		MID-TERM						
Week 8	Lecture 22	Input-Output Organization (Peripheral Devices)	T-1 R-1 R-2		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Demonstration with images, PPTs	
		Input-Output Organization (Input Output Interface)	T-1 R-1 R-2		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Demonstration with images, PPTs	
		Input-Output Organization (Data Transfer Schemes)	T-1 R-1 R-2		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Demonstration with images, PPTs	
		Input-Output Organization (Program Control and Interrupts)	T-1 R-1 R-2		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Demonstration with images, PPTs	
	Lecture 23	Input-Output Organization (Input/Output processor.)	T-1		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Demonstration with PPT, videos	
		Input-Output Organization (modes of data transfer)	T-1		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Demonstration with PPT, videos	

Week 8	Lecture 23	Input-Output Organization (Processor status word)	T-1		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Demonstration with PPT, videos	
	Lecture 24	Input-Output Organization (Input/Output processor.)	T-1		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Demonstration with PPT, videos	
		Input-Output Organization (modes of data transfer)	T-1		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Demonstration with PPT, videos	
		Input-Output Organization (Processor status word)	T-1		Introduction to input output subsystem of a computer	Students will understand the mode of communication between the central system and out side environment	Demonstration with PPT, videos	
Week 9	Lecture 25				Online Assignment			

Week 9	Lecture 26	Input-Output Organization (Direct Memory Access Transfer and Input/Output Processor)	T-1 R-1		Discussion on types of data transfer schemes and Discussion on DMA used when multiple bytes are to be transferred between memory and IO devices	i. Students will understand the concept of Direct memory access to memory for data transfers ii. Learn how DMA used when multiple bytes are to be transferred between memory and IO devices iii. Learn DMA Data transfer mechanism between I/O devices and system memory with the least processor intervention using DMAC	Demonstration with PPT, videos, flipped classroom	A sound card may need to access data stored in the computer's RAM, but since it can process the data itself, it may use DMA to bypass the CPU. Video cards that support DMA can also access the system memory and process graphics without needing the CPU. Ultra DMA hard drives use DMA to transfer data faster than previous hard drives that required the data to first be run through the CPU

Week 9	Lecture 26	Input-Output Organization (Priority interrupt)	T-1 R-1		Discussion on types of data transfer schemes and Discussion on DMA used when multiple bytes are to be transferred between memory and IO devices	i. Students will understand the concept of Direct memory access to memory for data transfers ii. Learn how DMA used when multiple bytes are to be transferred between memory and IO devices iii. Learn DMA Data transfer mechanism between I/O devices and system memory with the least processor intervention using DMAC	Demonstration with PPT, videos, flipped classroom	A sound card may need to access data stored in the computer's RAM, but since it can process the data itself, it may use DMA to bypass the CPU. Video cards that support DMA can also access the system memory and process graphics without needing the CPU. Ultra DMA hard drives use DMA to transfer data faster than previous hard drives that required the data to first be run through the CPU

Week 9	Lecture 26	Input-Output Organization (Direct memory access transfer)	T-1 R-1		Discussion on types of data transfer schemes and Discussion on DMA used when multiple bytes are to be transferred between memory and IO devices	i. Students will understand the concept of Direct memory access to memory for data transfers ii. Learn how DMA used when multiple bytes are to be transferred between memory and IO devices iii. Learn DMA Data transfer mechanism between I/O devices and system memory with the least processor intervention using DMAC	Demonstration with PPT, videos, flipped classroom	A sound card may need to access data stored in the computer's RAM, but since it can process the data itself, it may use DMA to bypass the CPU. Video cards that support DMA can also access the system memory and process graphics without needing the CPU. Ultra DMA hard drives use DMA to transfer data faster than previous hard drives that required the data to first be run through the CPU

Week 9	Lecture 27	Memory Unit(Memory Hierarchy and Processor Vs Memory Speed)	T-1 R-1		Describing about RAM and ROM chips , Auxiliary memory is also discussed. Associative memoryDescribing about Argument register Match Logic etc	Students will learn about content addressable memory	Demonstration with PPTs, videos	Content addressable memory is often used in computer networking devices. For example, when a network switch receives a data frame from one of its ports, it updates an internal table with the frame's source MAC address and the port it was received on. It then looks up the destination MAC address in the table to determine what port the frame needs to be forwarded to, and sends it out on that port. The MAC address table is usually implemented with a binary CAM so the destination port can be found very quickly, reducing the switch's latency

Week 9	Lecture 27	Memory Unit(Memory Management)	T-1 R-1		Describing about RAM and ROM chips , Auxiliary memory is also discussed. Associative memoryDescribing about Argument register Match Logic etc	Students will learn about content addressable memory	Demonstration with PPTs, videos	Content addressable memory is often used in computer networking devices. For example, when a network switch receives a data frame from one of its ports, it updates an internal table with the frame's source MAC address and the port it was received on. It then looks up the destination MAC address in the table to determine what port the frame needs to be forwarded to, and sends it out on that port. The MAC address table is usually implemented with a binary CAM so the destination port can be found very quickly, reducing the switch's latency

Week 9	Lecture 27	Memory Unit(main memory)	T-1 R-1		Describing about RAM and ROM chips , Auxiliary memory is also discussed. Associative memoryDescribing about Argument register Match Logic etc	Students will learn about content addressable memory	Demonstration with PPTs, videos	Content addressable memory is often used in computer networking devices. For example, when a network switch receives a data frame from one of its ports, it updates an internal table with the frame's source MAC address and the port it was received on. It then looks up the destination MAC address in the table to determine what port the frame needs to be forwarded to, and sends it out on that port. The MAC address table is usually implemented with a binary CAM so the destination port can be found very quickly, reducing the switch's latency
Week 10	Lecture 28	Memory Unit(Cache Memory)	T-1 R-2	RW-2	Discussion on types of mapping techniques in cache memory	Students will learn about basic concepts of cache memory	Peer learning, Demonstration with PPTs	
		Memory Unit(Associative memory)	T-1 R-2		Discussion on types of mapping techniques in cache memory	Students will learn about basic concepts of cache memory	Peer learning, Demonstration with PPTs	

Week 10	Lecture 29	Memory Unit(Cache Memory)	T-1 R-2	RW-2	Discussion on types of mapping techniques in cache memory	Students will learn about basic concepts of cache memory	Peer learning, Demonstration with PPTs	
		Memory Unit(Associative memory)	T-1 R-2		Discussion on types of mapping techniques in cache memory	Students will learn about basic concepts of cache memory	Peer learning, Demonstration with PPTs	
	Lecture 30	Memory Unit(Virtual memory)	T-1		Introduction to Virtual memory	Students will learn basic paging, frames and virtual memory	demonstration with PPT, videos, flipped classroom	
		Memory Unit(auxiliary memory)	T-1		Introduction to Virtual memory	Students will learn basic paging, frames and virtual memory	demonstration with PPT, videos, flipped classroom	
Week 11	Lecture 31	Introduction to Parallel Processing(Pipelining)	T-1	RW-1	Detailed discussion on instruction pipelining in computer.	Introduction to pipelining and its types	Peer Learning	
		Introduction to Parallel Processing(parallel processing)	T-1		Detailed discussion on instruction pipelining in computer.	Introduction to pipelining and its types	Peer Learning	
	Lecture 32	Introduction to Parallel Processing(Characteristics of multiprocessors)	T-1 R-1		Introduction to parallel processing and multiprocessors	Amdahl's law , chracteristics of multiprocessors	discussion with exampples	
	Lecture 33	Introduction to Parallel Processing(Interconnection Structures)	T-1		Various multiprocessor interconnection structures	Students will learn about Time-shared, Multiport memory, crossbar switch, hypercube interconnection	Discussions with images and diagrams	
Week 12	Lecture 34				Online Assignment			
	Lecture 35	Multiprocessors (Categorization of multiprocessors (SISD,MIMD,SIMD.SPMD) , Introduction to GPU)	T-1		Different categories of multiprocessors, introduction to GPU	Students will learn about multiprocessor calssification, and GPU	Discussion with images	
	Lecture 36	Latest technology and trends in computer architecture (multi-cores processor.)	T-1		Different categories of multiprocessors, introduction to GPU	Students will learn about multiprocessor calssification, and GPU	discussion with images	
Week 13	Lecture 37	Latest technology and trends in computer architecture (microarchitecture)	T-1 R-1		Latest processor architecture study is done	Student will learn about latest processor architectures	Demonstration and discussions	

An instruction plan is only a tentative plan. The teacher may make some changes in his/her teaching plan. The students are advised to use syllabus for preparation of all examinations. The students are expected to keep themselves updated on the contemporary issues related to the course. Upto 20% of the questions in any examination/Academic tasks can be asked from such issues even if not explicitly mentioned in the instruction plan.

Week 13	Lecture 38	Latest technology and trends in computer architecture (latest processor for smartphone or tablet and desktop)	T-1		Discussion on new nonvolatile memory technology and discussion on various processors	Students will learn about new processor and new memory technology with there architectures	Peer Learning	
	Lecture 39	Latest technology and trends in computer architecture (next generation processors architecture)	T-1 R-1		Discussion on new nonvolatile memory technology and discussion on various processors	Students will learn about new processor and new memory technology with there architectures	peer learning	
Week 14	Lecture 40	Latest technology and trends in computer architecture (next generation processors architecture)	T-1 R-1		Discussion on new nonvolatile memory technology and discussion on various processors	Students will learn about new processor and new memory technology with there architectures	peer learning	
		SPILL OVER						
Week 14	Lecture 42				Spill Over			
Week 15	Lecture 43				Spill Over			
	Lecture 44				Spill Over			
	Lecture 45				Spill Over			

Plan for Tutorial: (Please do not use these time slots for syllabus coverage)

Tutorial No.	Lecture Topic	Type of pedagogical tool(s) planned (case analysis,problem solving test,role play,business game etc)
Tutorial1	Problem Solving on Logic Gates	Problem Solving
Tutorial2	Problems based on Bus and Memory transfer and Arithmetic and shift Micro operations	Problem Solving
Tutorial3	Problem Solving on Register transfer and Register transfer language and Instruction Codes	Problem Solving
Tutorial4	Problem Solving on Control Timing Signals and Instruction Cycle	Problem Solving
Tutorial5	Problem Solving on Memory Reference Instructions and Input Output interrupt	Problem Solving
Tutorial6	Problem Solving on program and Micro Program Control,	Problem Solving
Tutorial7	Problem Solving on Data Transfer, Manipulation and Addressing Modes	Problem Solving

An instruction plan is only a tentative plan. The teacher may make some changes in his/her teaching plan. The students are advised to use syllabus for preparation of all examinations. The students are expected to keep themselves updated on the contemporary issues related to the course. Upto 20% of the questions in any examination/Academic tasks can be asked from such issues even if not explicitly mentioned in the instruction plan.

After Mid-Term		
Tutorial8	Problem Solving on Data Transfer Schemes, Program Control and Interrupts	Problem Solving
Tutorial9	Problem Solving on Direct Memory Access and Memory Hierarchy	Problem Solving
Tutorial10	Problem Solving on Cache Memory, Associative Memory and Virtual Memory	Problem Solving
Tutorial11	Problem Solving on Pipelining	Problem Solving
Tutorial12	Problem Solving on Performance of Processors with pipelining	Problem Solving
Tutorial13	Problem solving on interconnection structures	Problem Solving
Tutorial14	Problem Solving on GPU	Problem Solving