

ECE213: Digital Electronics



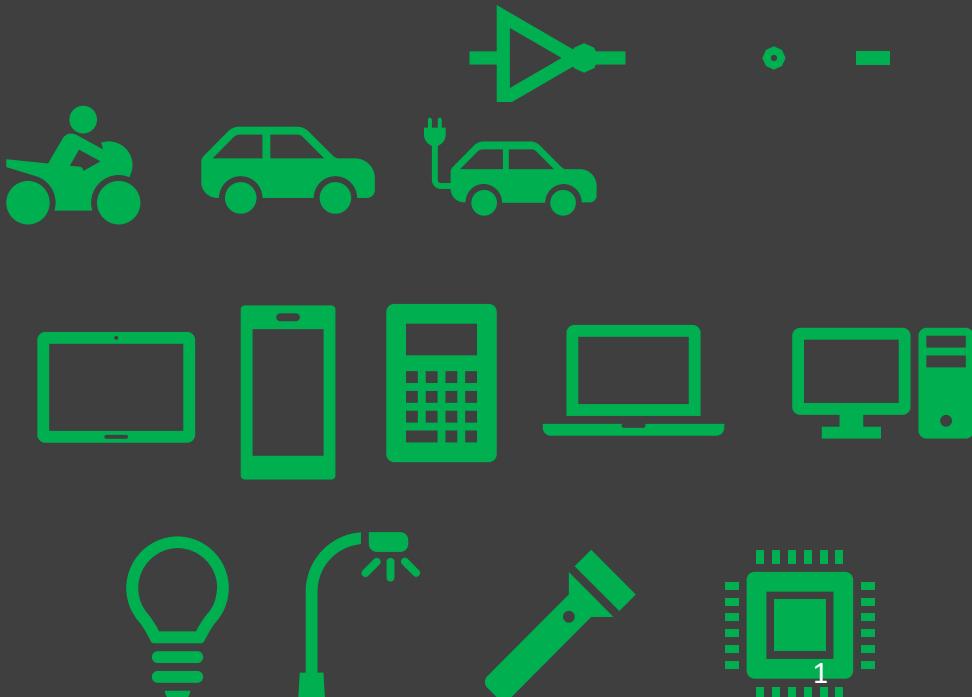
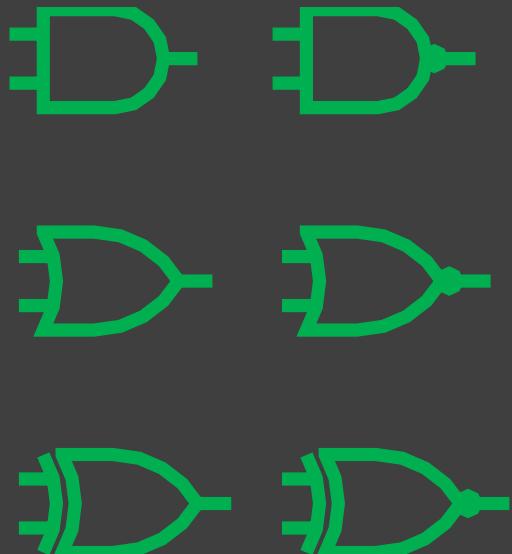
Ajmer Singh



9988921373



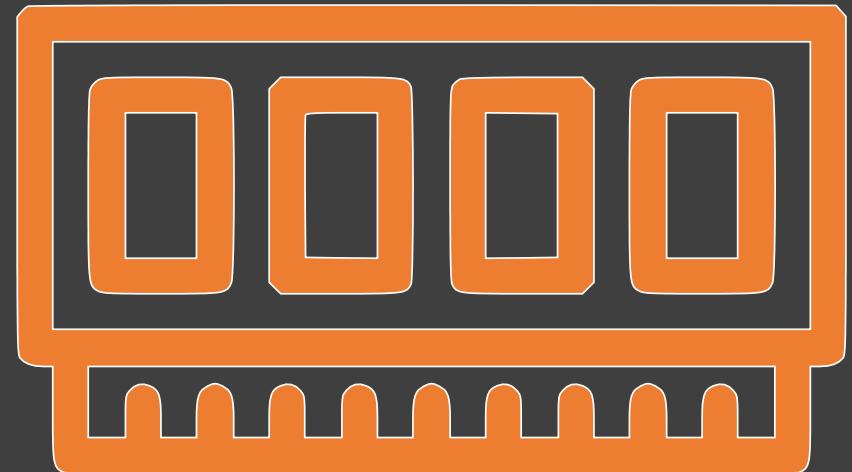
ajmer.17381@lpu.co.in



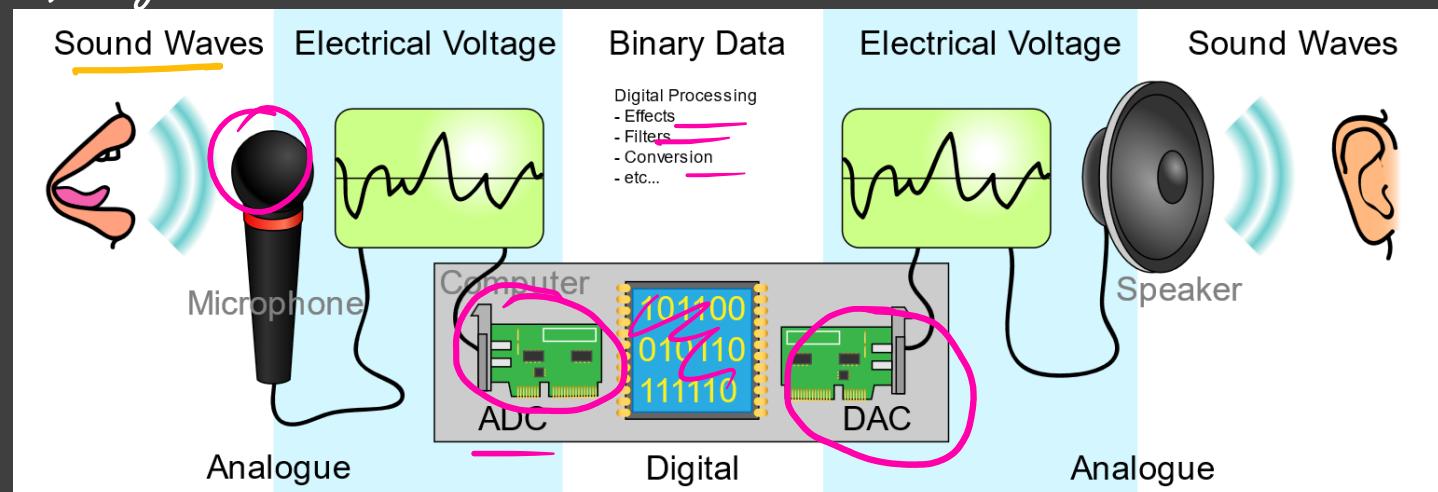
The Course Contents

Unit VI

Memory : Read-only memory, read/write memory - SRAM and DRAM, PLAs and their applications, Sequential PLDs and their applications, Introduction to field programmable gate arrays, PALs and their Applications



* Converters : Analog to Digital Converter, Digital to
Analog Converter ADC
DAC





Memory

Memory

Memory and Programmable Logic



Memory Device:

— Writes
— Reads

Device to which binary information is transferred for storage, and from which information is available for processing as needed.



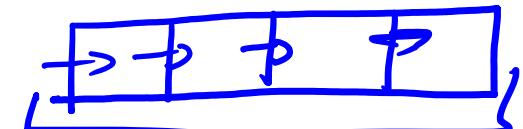
Memory Unit:

is a collection of cells capable of storing a large quantity of binary information. ie. 1001101



⇒ In digital systems, there are two types of memories:

1. RAM
2. ROM



mcq

Memory and Programmable Logic



1. Random-Access Memory (RAM)

RAM is the place in a computer where the operating system, application programs, and data in current use are kept so that they can be quickly reached by the computer's processor.



2. Read-Only Memory (ROM):

ROM is a type of memory that is as fast as RAM, but has two important differences: It can not be changed, and it retains its contents even when the computer is shut off. It is generally used to start your computer up and load the operating system.

Using a ROM as a PLD: A programmable logic device or PLD is an electronic component used to build digital circuits. Before the PLD can be used in a circuit it must be programmed.

mcq

Examples of PLDs: programmable logic array (PLA), programmable array logic (PAL), and field-programmable logic gate array (FPGA). (PAL: Program. AND, fixed OR, PLA: Program. AND/OR)

A Random-Access Memory

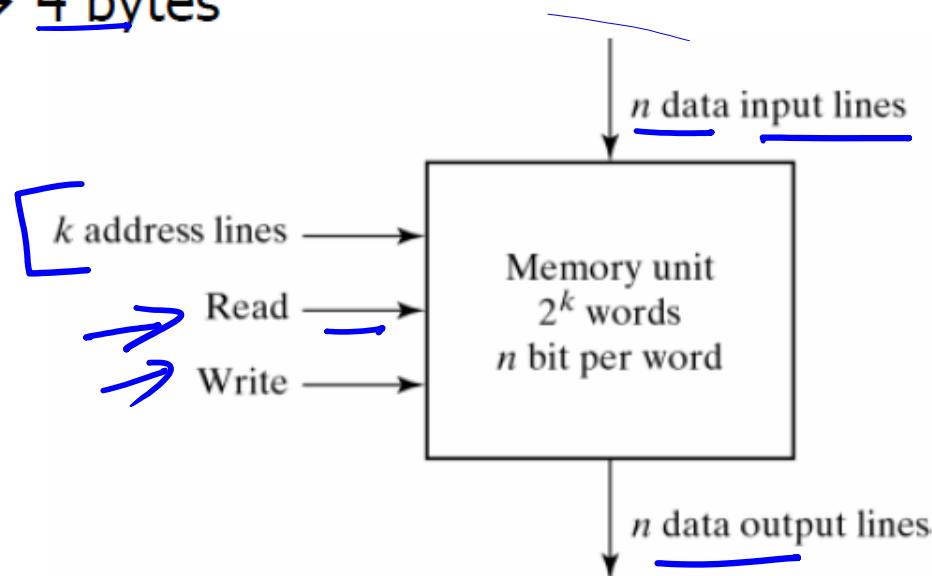
Memory unit:

Stores binary information in groups of bits called words.

Memory word:

group of 1's and 0's and may represent a number,
character(s), instruction, or other binary-coded information.

A Most computer memories use words that are multiples of 8 bits (byte).
32-bit word → 4 bytes



4-bit address
{ 0000 : 16 locations
 |
 1111

Random-Access Memory

In Dec. 10³, 000

Each word in memory is assigned an address 0 up to $2^k - 1$ ($k = \#$ of address lines).

$$2^{10} \quad | \quad k=10$$
$$2^{10} - 1 = 1023$$

1024×16 bits

16×1024

$2 \times 8 \times 1024$ bits

$2K$ bytes

2K bytes

Q

How many bytes is this memory module?

Memory address		Memory content
Binary	decimal	
0000000000	0	1010101110001001
0000000001	1	0000110101000110
0000000010	2	
	:	
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Fig. 7-3 Content of a 1024×16 Memory

$$\eta = 16$$

- A) 16 byte
- B) 2 x 16 byte
- C) 1 Kbyte
- D) 2 Kbyte

me

Unit	Shortened	Capacity
• Bit	b	1 or 0 (on or off)
• Byte	B	8 bits
• Kilobyte	KB	1024 bytes
• Megabyte	MB	1024 kilobytes
• Gigabyte	GB	1024 megabytes
• Terabyte	TB	1024 gigabytes
• Petabyte	PB	1024 terabytes
• Exabyte	EB	1024 petabytes
• Zettabyte	ZB	1024 exabytes
• Yottabyte	YB	1024 zettabytes

$$2^3 \cdot 2^{10} = 2^{20}$$

$$2^4 \cdot 2^{20} = 2^{24}$$

$$2^5 \cdot 2^{20} = 2^{25}$$

$$2^6 \cdot 2^{20} = 2^{26}$$

RAM: Write and Read Operations

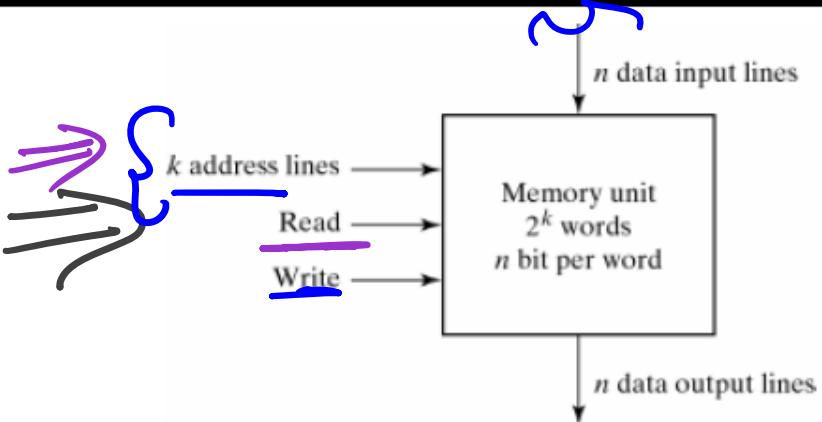


Fig. 7-2 Block Diagram of a Memory Unit

To transfer a new word to be stored into memory: (Writing operation)

- 1. Apply the binary address of the word to address lines.
2. Apply the data bits that must be stored in memory to the data input lines.
3. Activate the write input.

To transfer a stored word out of memory: (Read operation)

- 1. Apply the binary address of the word to address lines.
2. Activate the read input.

MU

★ Memory Types

Integrated circuit RAM units are available in two possible operating modes: static and dynamic.

Static RAM (SRAM) consists of internal latches that store the binary information. The stored information remains valid as long as power is applied to the unit.

★ **Dynamic RAM (DRAM)** stores the binary information in the form of electric charges on capacitors provided by the MOS transistors. **MosFET**

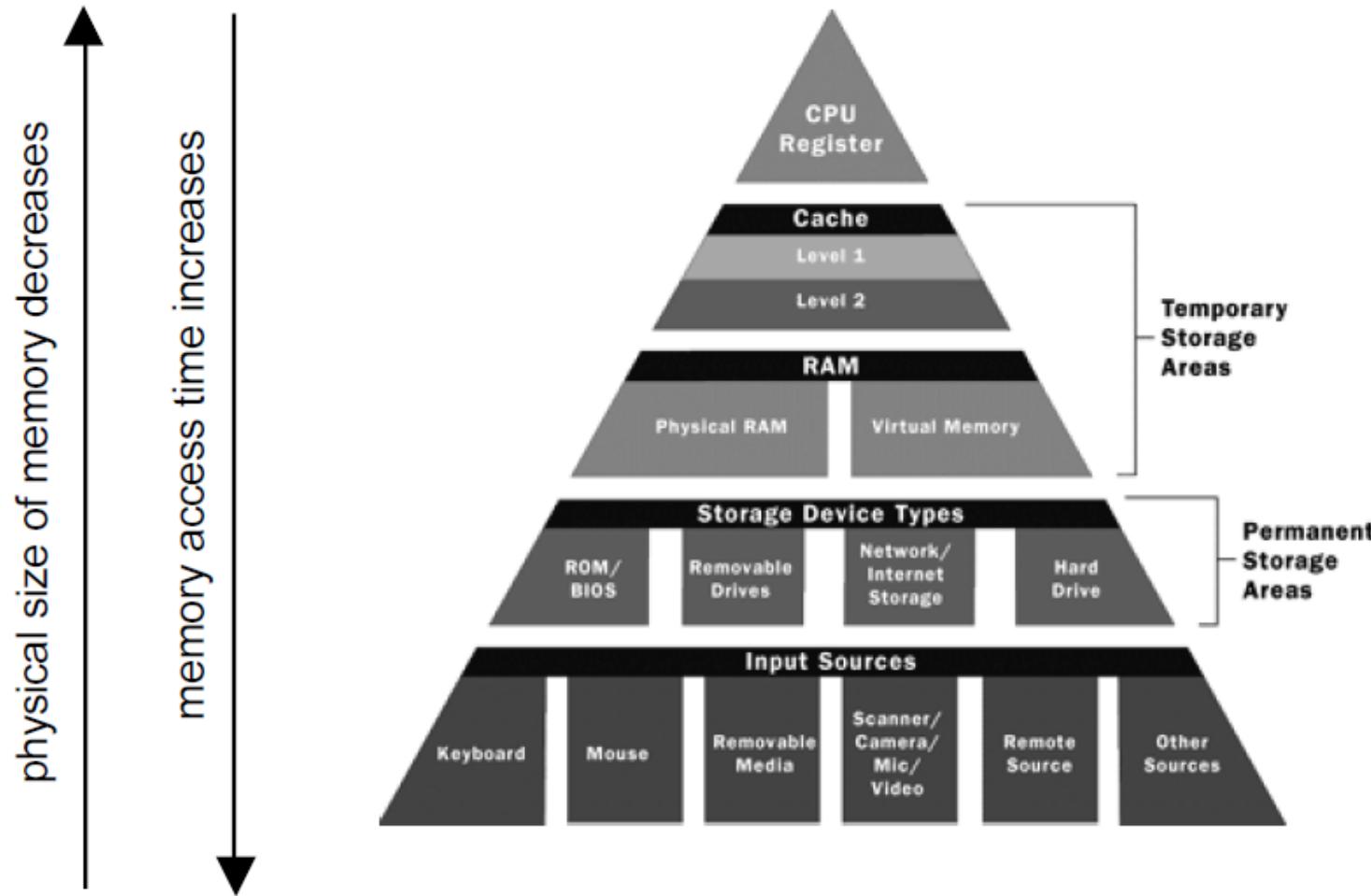
Disadv } The charge on the capacitors tends to decay with time and the capacitors must be periodically recharged by refreshing of the dynamic memory every few milliseconds.

- DRAM offers reduced power consumption, large integration of units on chip.
- SRAM is faster; has shorter read and write cycles, SRAM is used in cache. Disadvantages: high power consumption, low density, expensive.

One T

6T

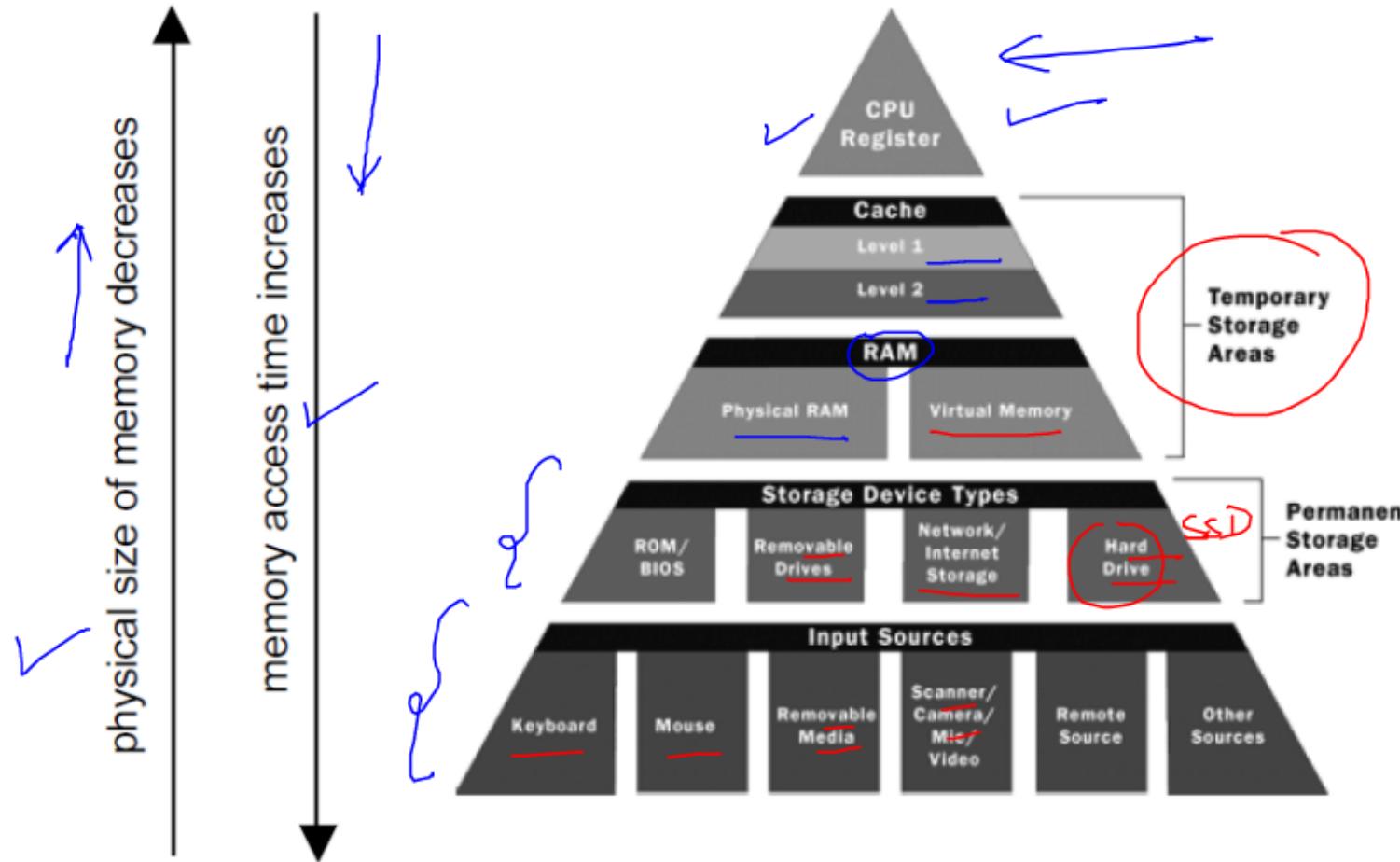
Memory Hierarchy





Memory Hierarchy

MCQ



4.7GB CD - ROM
4.7GB DVD - ROM
Blu-ray

Volatile vs. Non-Volatile Memory

- RAM (static and dynamic) is said to be volatile, since information is lost when power is turned off.
- Non-volatile memory retains its information even when power is turned off.
 1. Magnetic disks: stored data is represented by the direction of magnetization.
 2. CD: compact disc is a piece of polycarbonate (a type of plastic) on which a spiral track has been impressed. This spiral track is a series of indentations ("pits") separated by flat areas ("land").
 3. ROM: The internal storage elements are set to their values once and after that are only read.



Volatile vs. Non-Volatile Memory

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Auditor A/B

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EPROMS and PROMS

Erasable Programmable Read-Only Memory (EPROM) is a special type of memory that retains its contents until it is exposed to ultraviolet light.

To write to EPROM, you need a special device called a *PROM Programmer* or *PROM burner (programmer)*. An EPROM differs from a PROM in that a PROM can be written to only once and cannot be erased.

EPROMs are widely used in personal computers since they enable the manufacturer to change the contents of the PROM before the computer is actually shipped. This means that bugs can be removed and new versions installed shortly before delivery.

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EEPROMS and FLASH

Electrically Erasable Programmable Read-Only Memory (EEPROM), is like EPROM except that the previously programmed connections can be erased with an electrical signal.

Flash memory is a type of EEPROM. Information stored in flash memory is usually written in blocks rather than a byte or word at a time.

Virtual Memory?

With virtual memory, the computer can look for areas of RAM that have not been used recently and copy them onto the hard disk. This frees up space in RAM to load the new application. Because it does this automatically, you don't even know it is happening, and it makes your computer feel like it has unlimited RAM space even though it has only 1 GB installed.

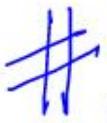
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RAM Memory Cell

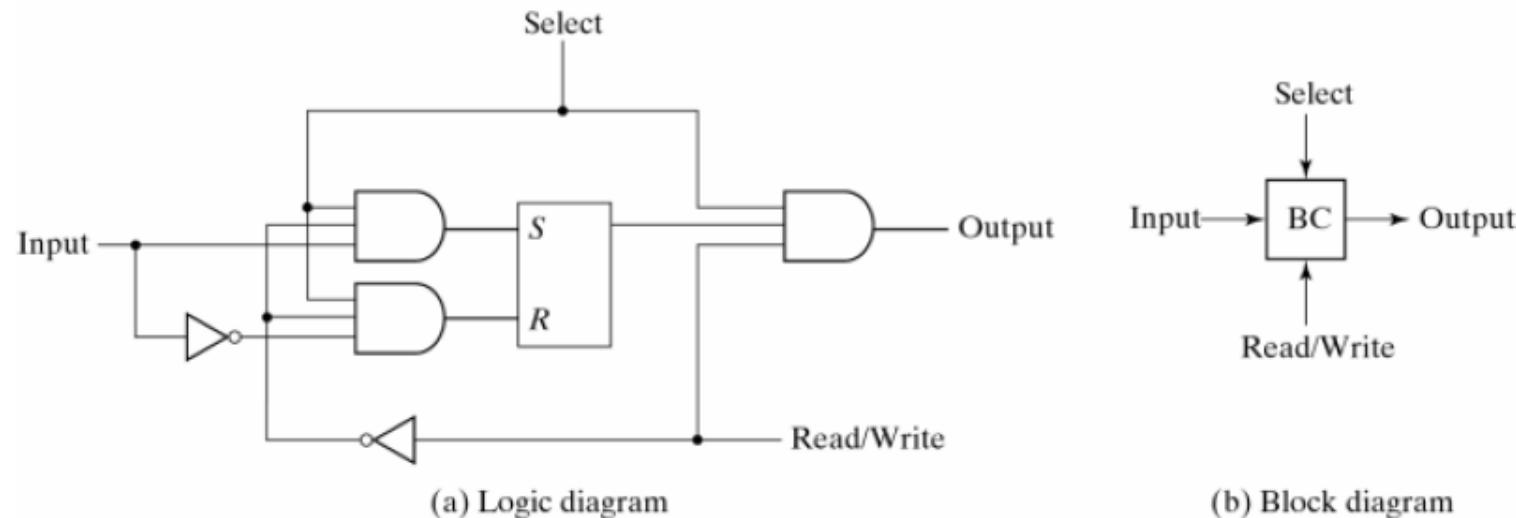


Fig. 7-5 Memory Cell

The storage part of the cell is modeled by an *SR* latch with associated gates.

A 1 in the read/write input provides the read operation by forming a path from the latch to the output.

A 0 in the read/write input provides the write operation by forming a path from the input to latch.

RAM Memory Cell

D-PR

If any of the input
is low the o/p is low.

The storage part of the cell is modeled by an SR latch with associated gates.

A 1 in the read/write input provides the read operation by forming a path from the latch to the output.

A 0 in the read/write input provides the write operation by forming a path from the input to latch.

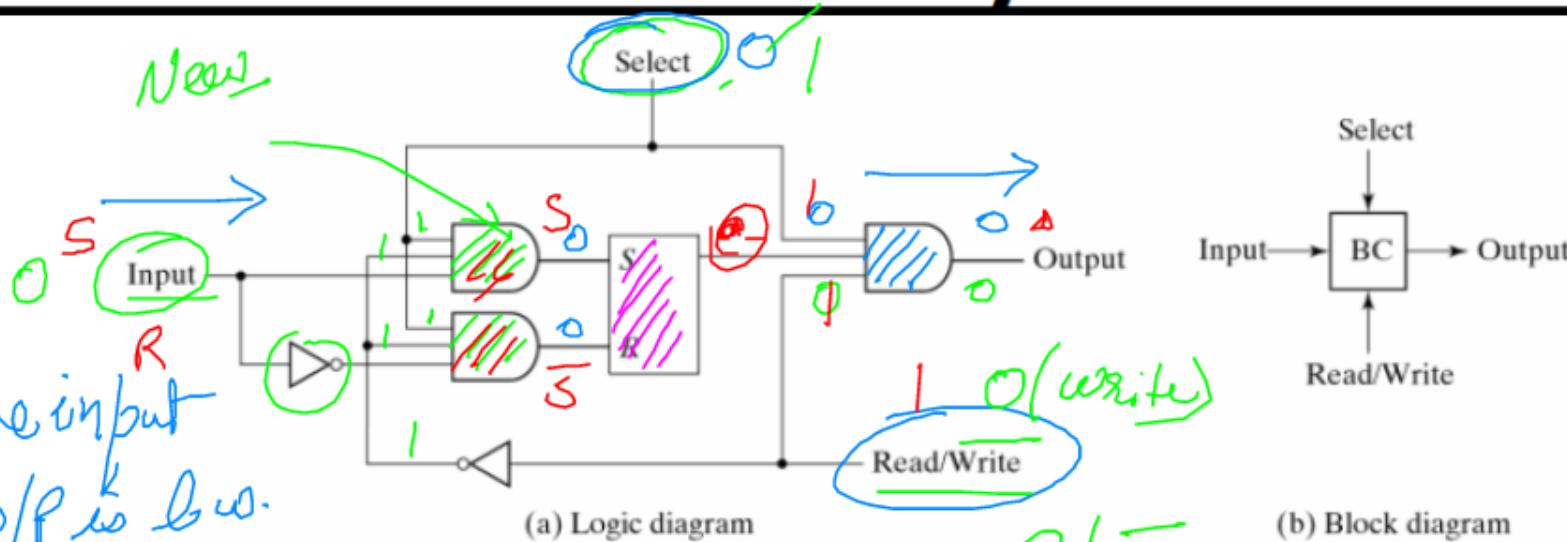


Fig. 7-5 Memory Cell



4 x 4 RAM

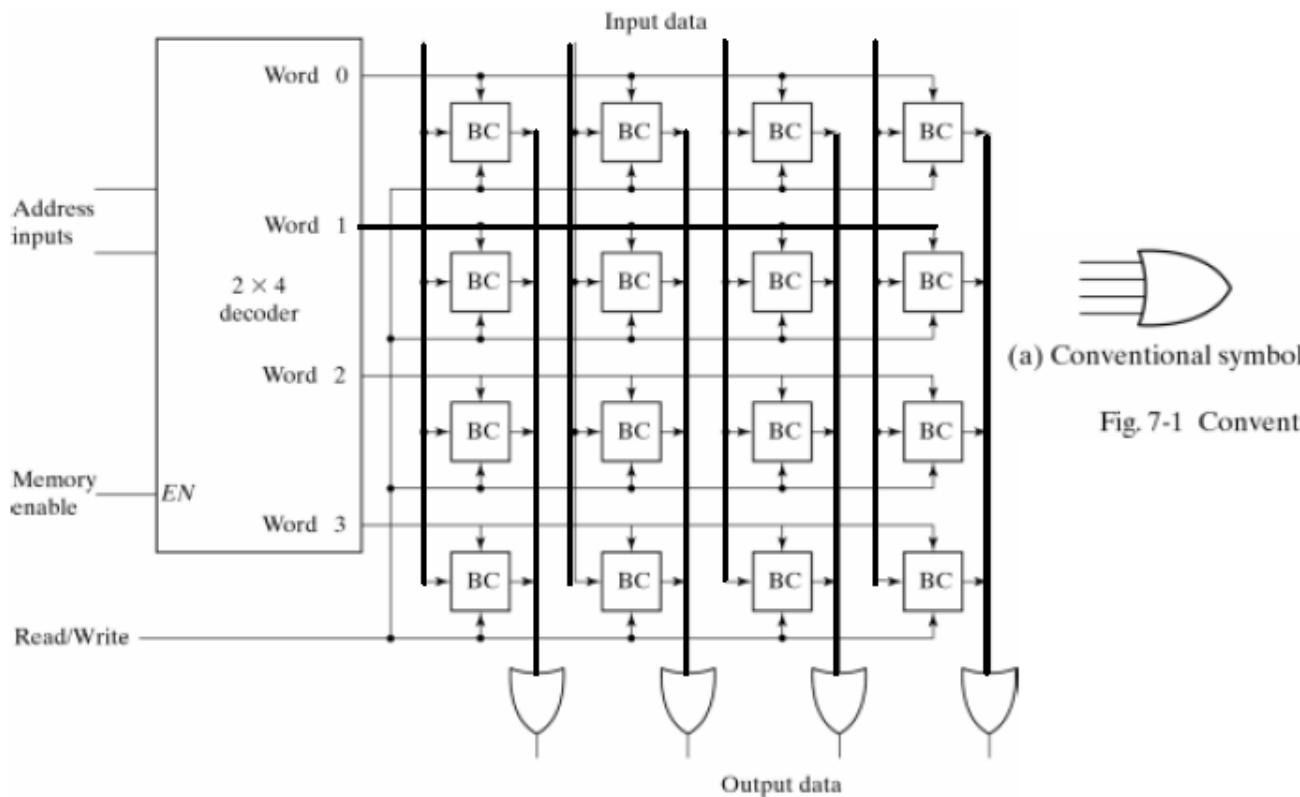


Fig. 7-6 Diagram of a 4×4 RAM



Fig. 7-1 Conventional and Array Logic Diagrams for OR Gate

WRITE operation: the data available in the input lines are transferred into the four binary cells of the selected word. The memory cells that are not selected are disabled.

READ Operation: the four bits of the selected word go through OR gates to the output terminals.

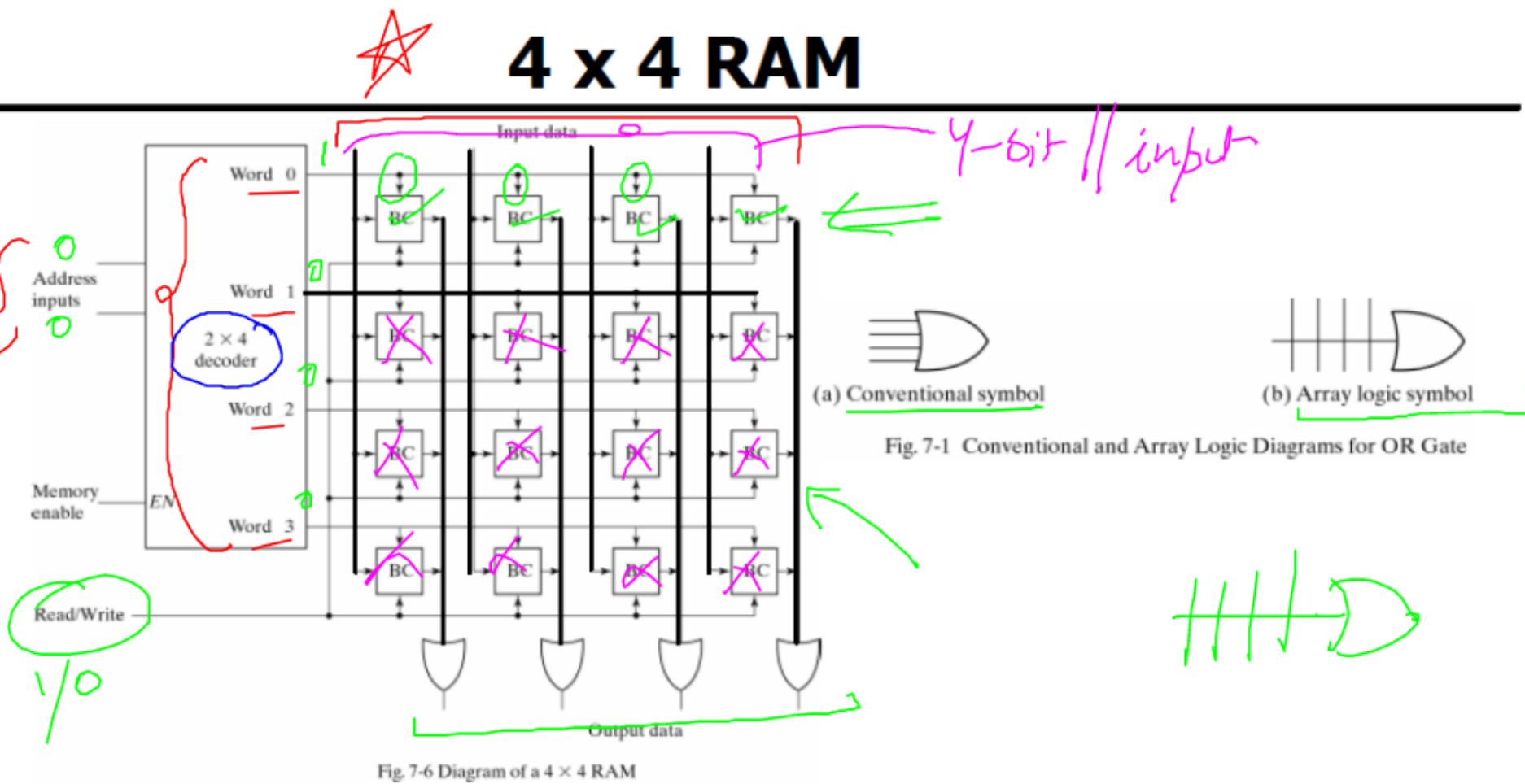
4 x 4 RAM

$y \times k$
No. of address
The length of the word

$$y = 2^k$$

$k = 2$

2:4 decoder



WRITE operation: the data available in the input lines are transferred into the four binary cells of the selected word. The memory cells that are not selected are disabled.

READ Operation: the four bits of the selected word go through OR gates to the output terminals.

Commercial RAM

MCQ

Commercial RAM → thousands of words, with each word 1 - 64 bits.

A memory with 2^k words of n bits/word requires k address lines that go into a $k \times 2^k$ decoder.

$k \times 2^k$

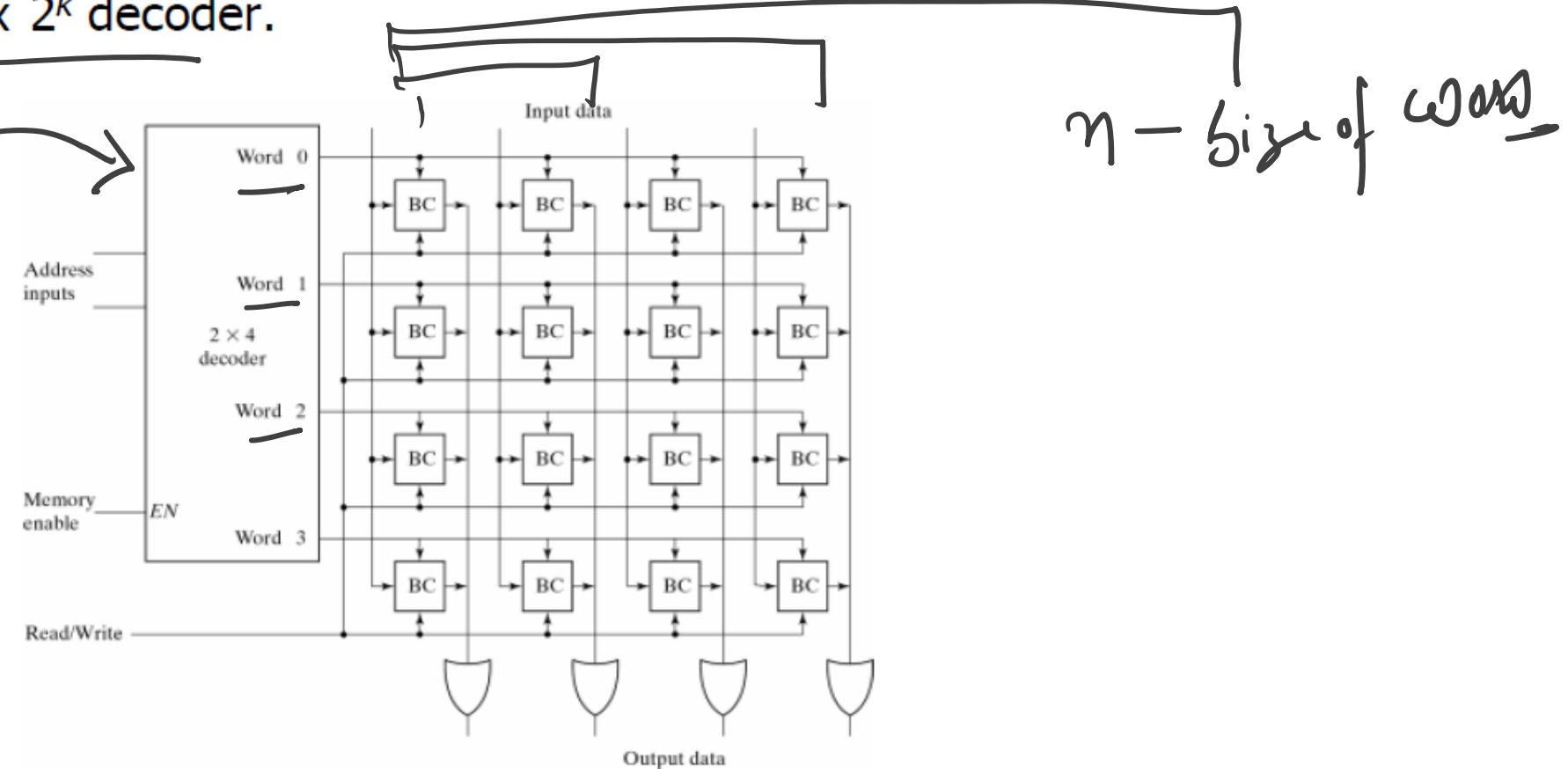


Fig. 7-6 Diagram of a 4×4 RAM

★ Two Dimensional Decoding

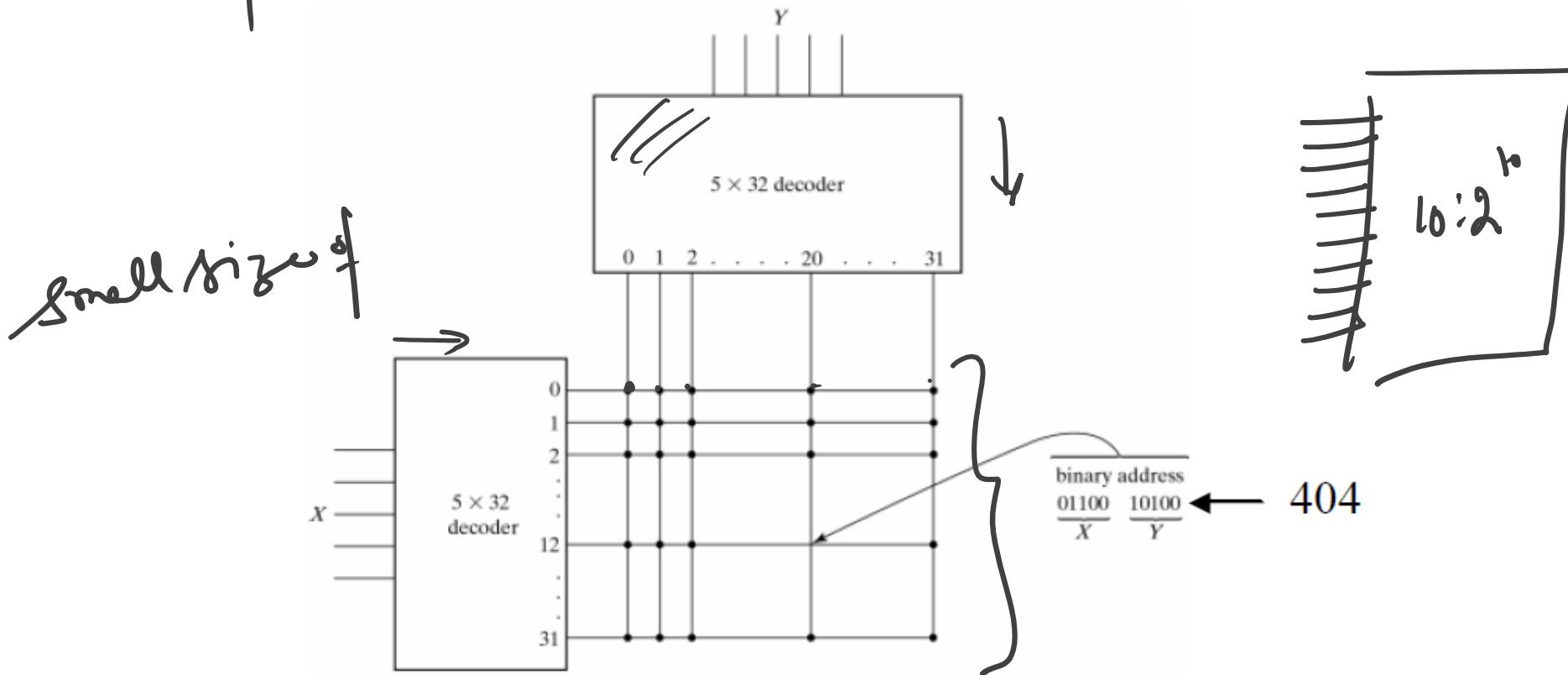


Fig. 7-7 Two-Dimensional Decoding Structure for a 1K-Word Memory

The idea of two-dimensional decoding is to arrange the memory cells in an array that is as close as possible to square. Use two $k/2$ -input decoders instead of one k -input decoder. One decoder performs the row selection and the other the column selection in a two dimensional matrix configuration.
How many words can be selected?

Read-Only Memory (ROM)

Read-only memory is a memory device in which permanent binary information is stored.

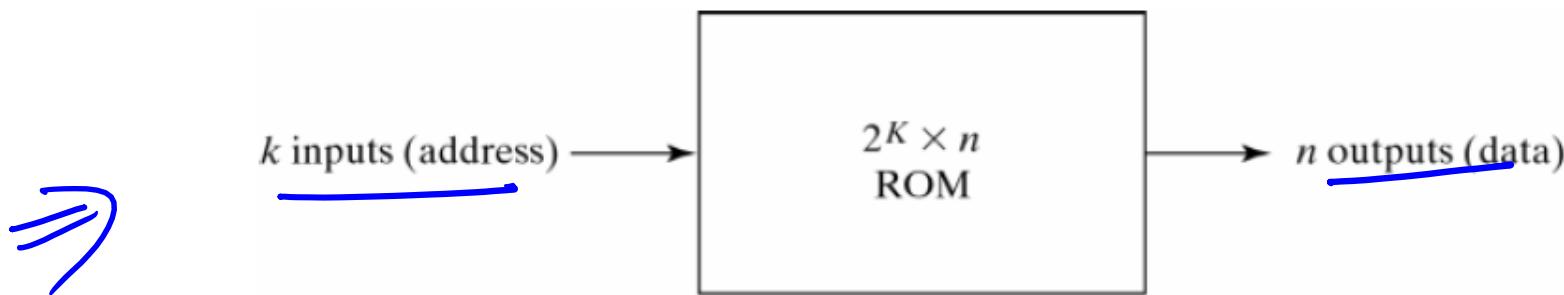
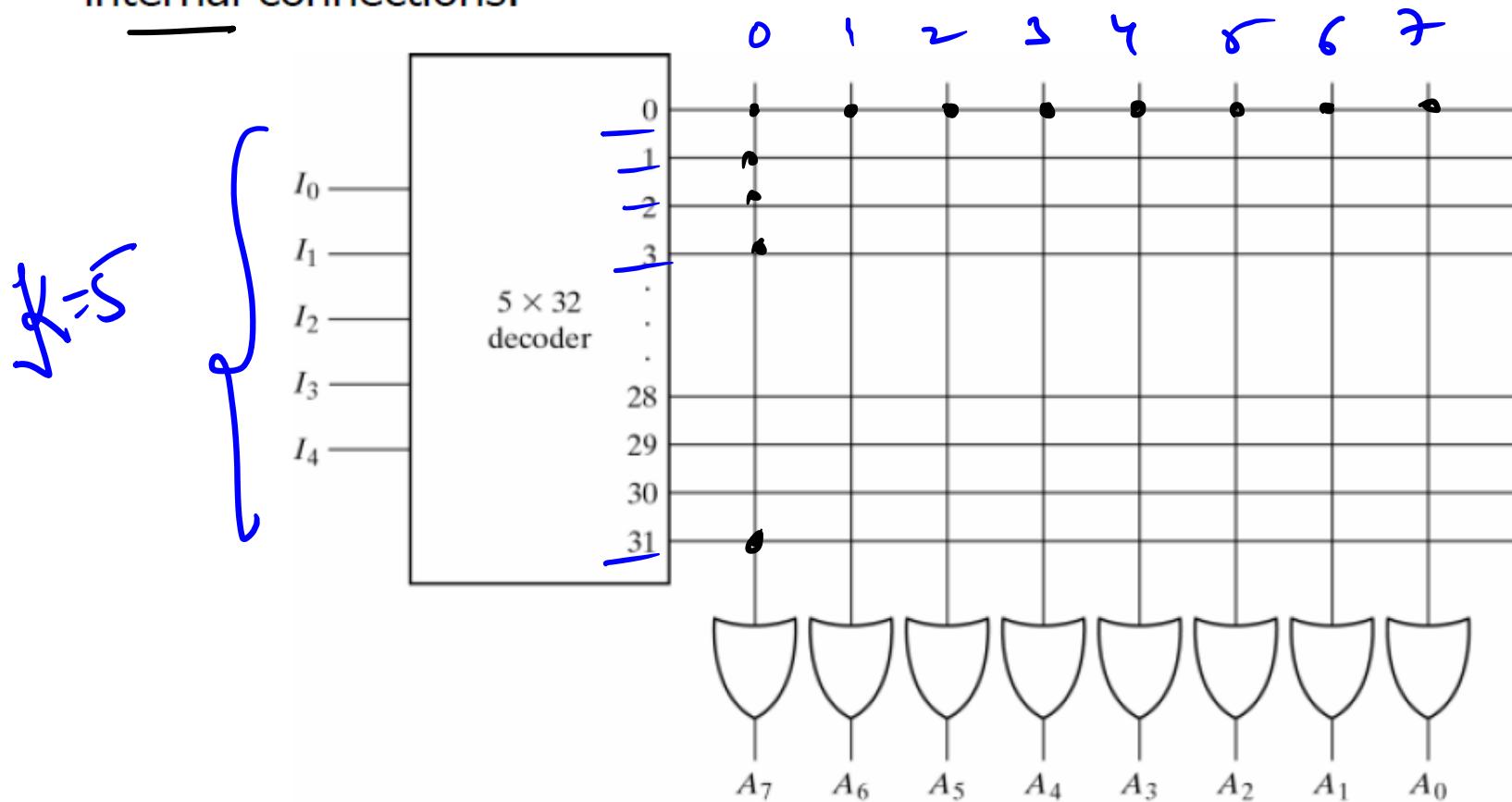


Fig. 7-9 ROM Block Diagram

- The number of words in a ROM is determined from the k address input lines needed to specify the 2^k words.
- Why doesn't the ROM have any data inputs?
A1

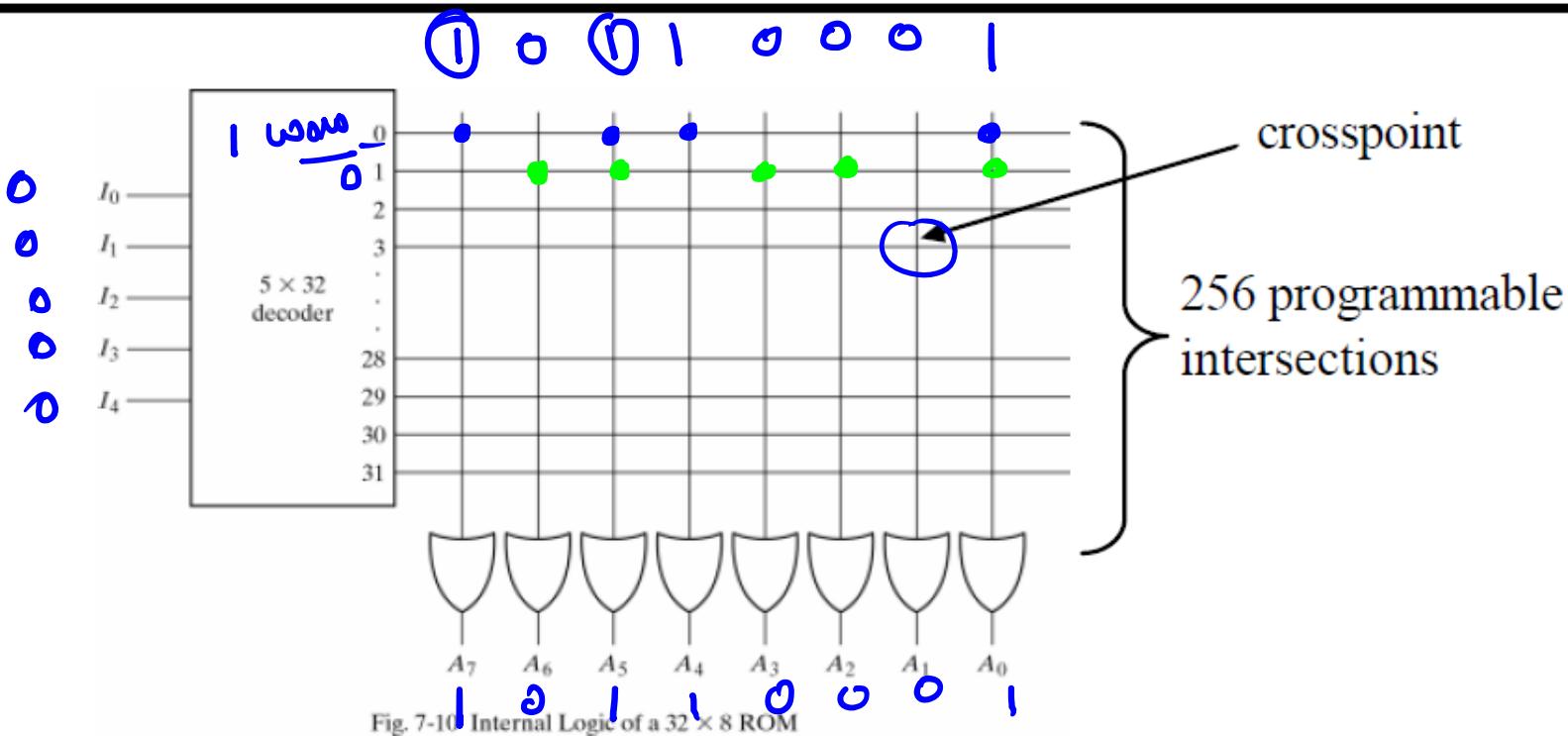
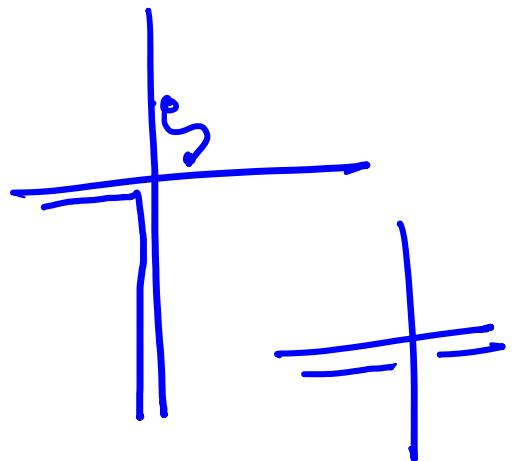
Read-Only Memory (ROM)

A 32 x 8 ROM consists of 32 words of 8 bits each. The five input lines are decoded by into 32 distinct outputs (memory addresses) using a $5 + 2$ decoder. Each OR gate has 32 input connections → 32 x 8 ROM has internal connections 32×8 . In general, a $2^k \times n$ ROM will have $k \times 2^k$ decoder and n OR gates with $2^k \times n$ internal connections.





Read-Only Memory



A programmable connection (a crosspoint) between two lines is logically equivalent to a switch that can be closed (two lines are connected) or open (two lines are disconnected). A switch can be a fuse that normally connects the two points, but can be opened by blowing the fuse using a high voltage pulse.

Programming Read-Only Memory

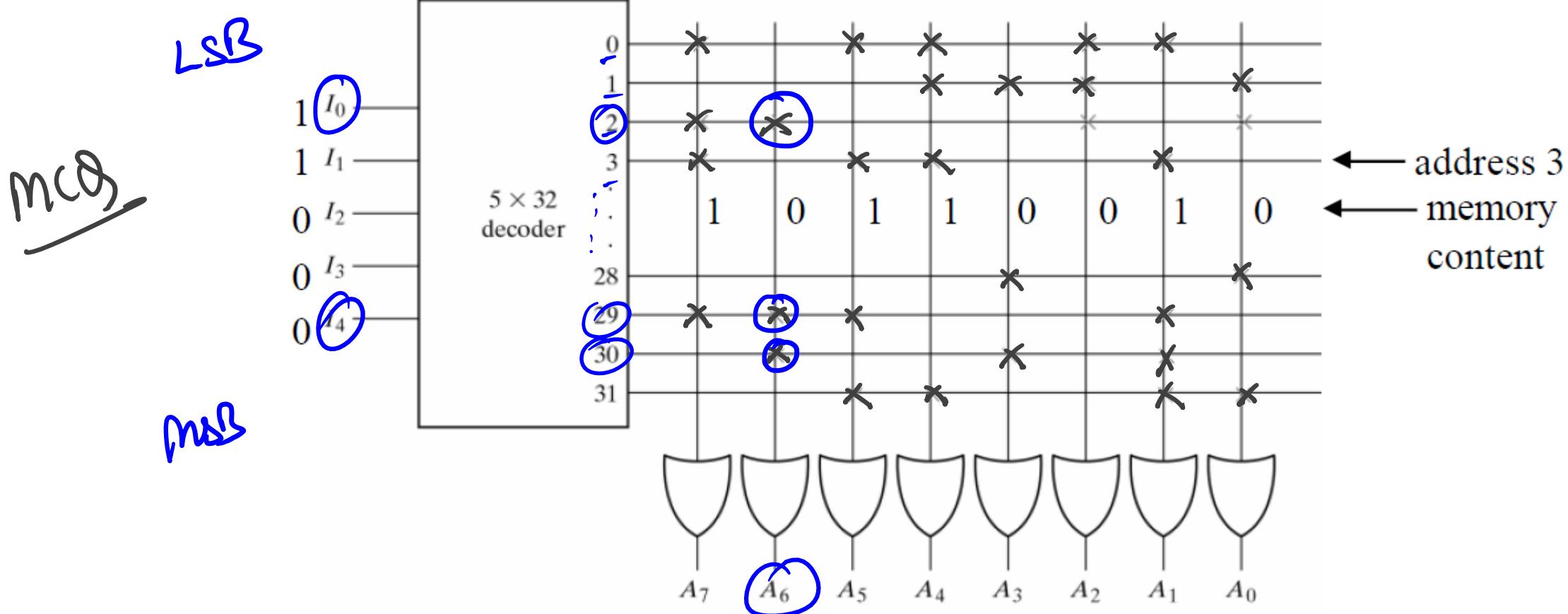


Fig. 7-11 Programming the ROM According to Table 7-3

Output A_6 can be expressed in sum of minterms as: $A_6(I_4, I_3, I_2, I_1, I_0) = \Sigma(2, \dots, 29, 30)$

How to express of A_6 ?

$$A_6(I_4, I_3, I_2, I_1, I_0) = \Sigma(2, \dots, 29, 30)$$

Q

Constructing 256K x 8 RAM

64K x 8
256K x 8

1. How many 64K x 8 RAM chips are needed to provide a memory capacity of 256KB? 4 chips.
2. How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips?
3. How many lines must be decoded for the chip select inputs of all chips?

00
01
10
11

Q2:

$$256KB = \underline{256K} \times 8$$

$$256 \times K \\ 2^8 \times 2^{10} = 2^{18}$$

for 64K x 8

$$2^{16} \times 8$$

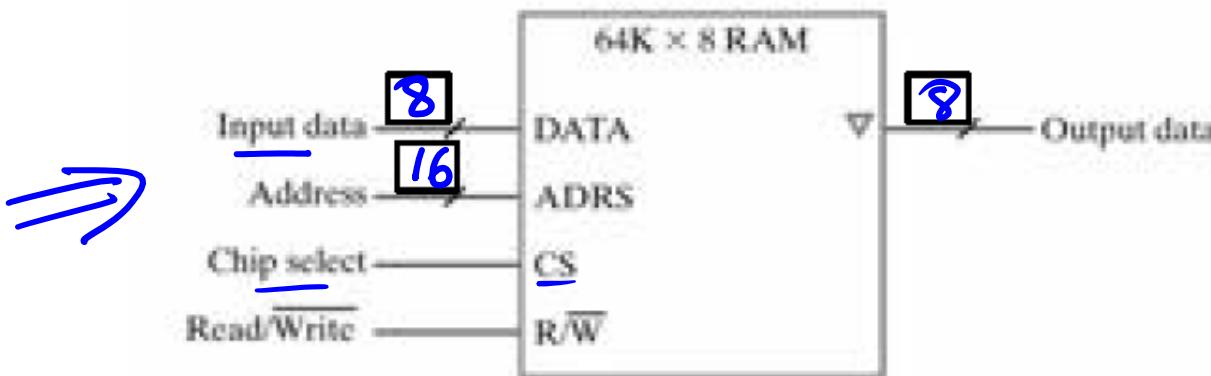
$$\text{No of chip select lines} = 18 - 16 = \underline{\underline{2}}$$



64K X 8 RAM chip

Capacity: 64K words of 8 bits each

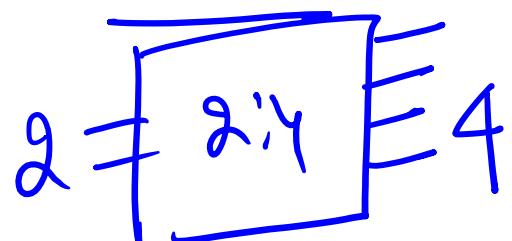
+
parallel bus



Q: What is the size of word in 64K x 8 RAM
A: 8

CD
C1
C2
C3

- Q: How many chips are needed to construct 256K x 8? 4 chips
Q: What is the size of the decoder?



m08

256K X 8 RAM

- Three-state outputs are connected together to form 8 data output lines.

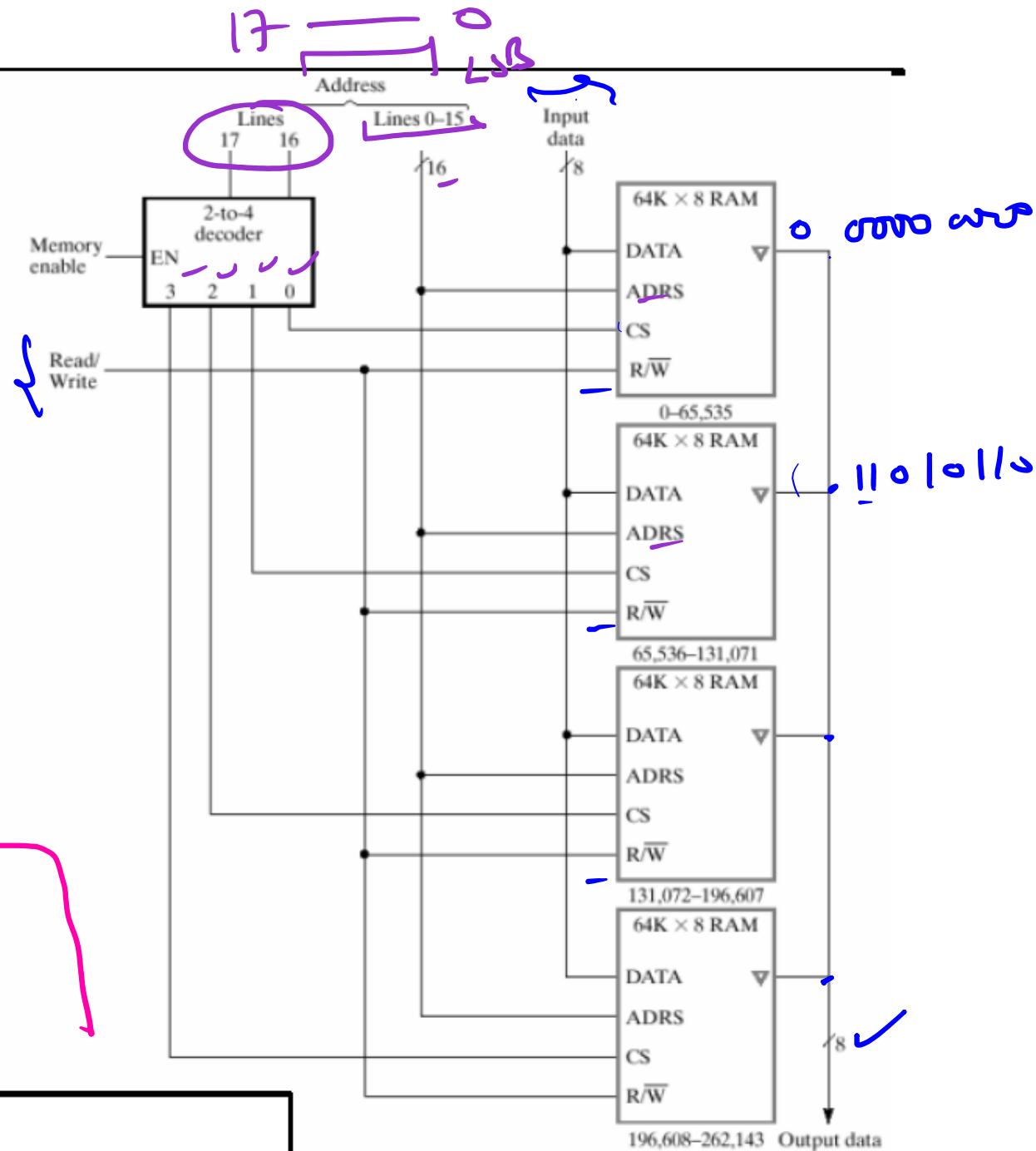
- Just one chip select (CS) will be active at any time.

- RAM requires 18-bit address:
16 LSB address are applied to the inputs of each RAM.
2 MSB are applied to 2-to-4 decoder.

- Address bits 16 and 17 are used for chip selection.

Q: How many 16×4 RAM required to make 512×4 RAM

A: $512 / 16 = 32$.



32 X 8 ROM chip

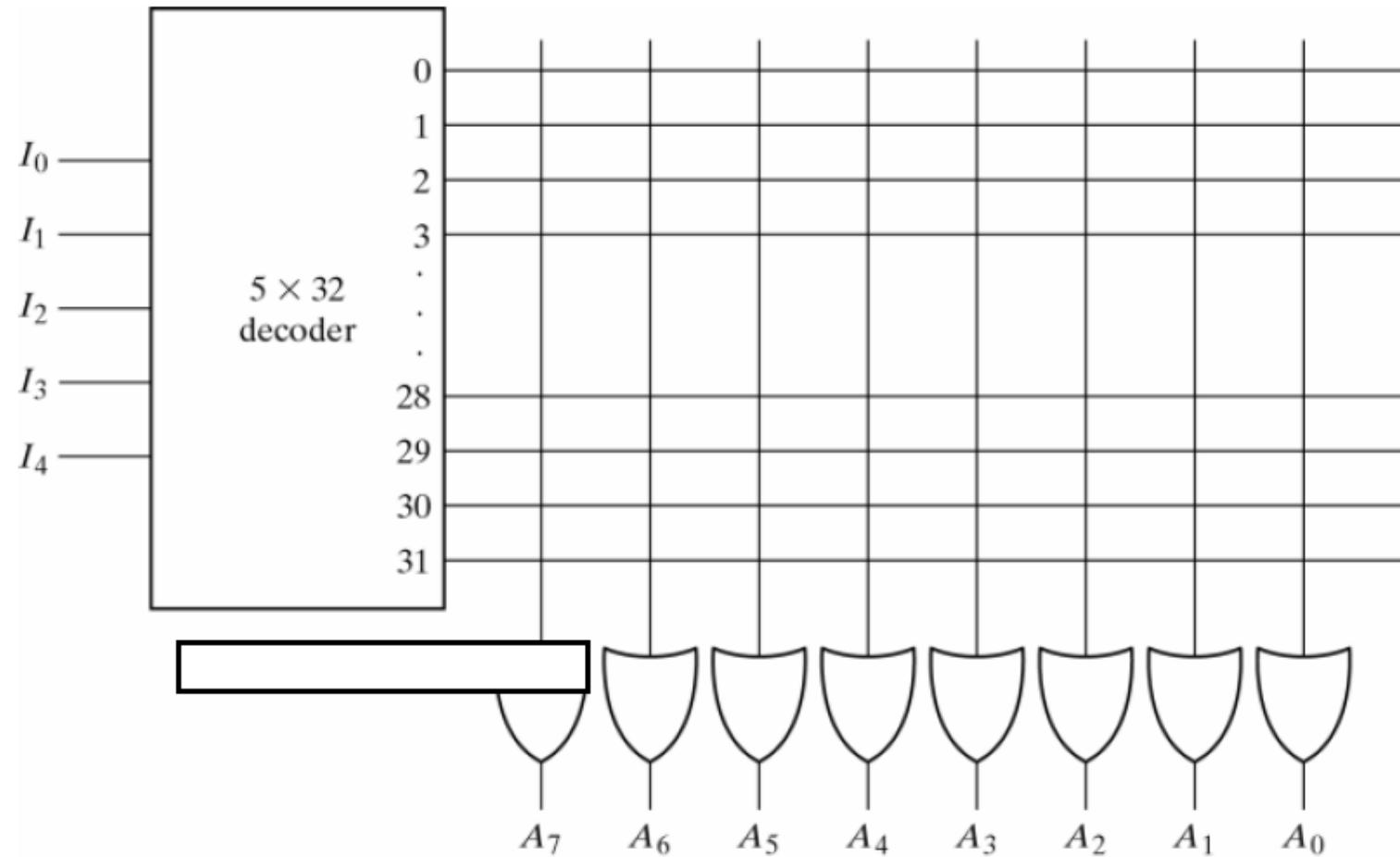
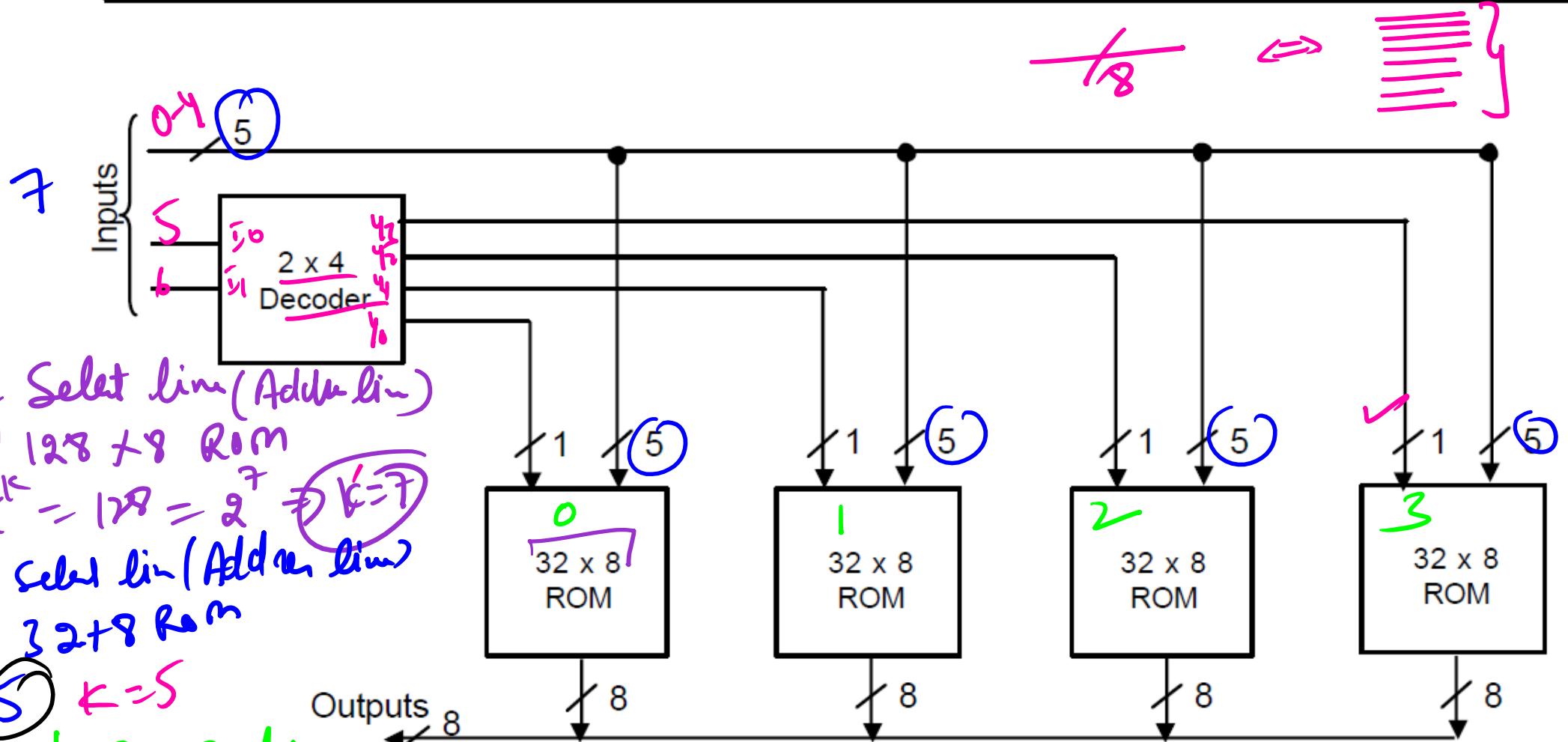


Fig. 7-10 Internal Logic of a 32×8 ROM

128 X 8 ROM chip



Q: No. of Select line (Address line)

for 128 x 8 ROM

$$2^k = 128 \Rightarrow k = 7$$

Q: # of Select line (Address line)

for 32x8 ROM

$$5 \quad k=5$$

Q: # No. of 32x8 chip required to construct 128x8 chip

$$A: \frac{128}{32} = 4$$

A size of decoders
 $k - k_2 = 7 - 5 = 2 \cdot 2^2 = 2:4$

Programmable Logic Device (PLD)

Programmable logic devices (PLD) are designed with configurable logic and flip-flops linked together with programmable interconnect.

mq

PLDs provide specific functions, including

- Device-to-device interfacing ✓
- Data communication ✓
- Signal processing ✓
- Data display ✓
- Timing and control operations, and almost every other function a system must perform

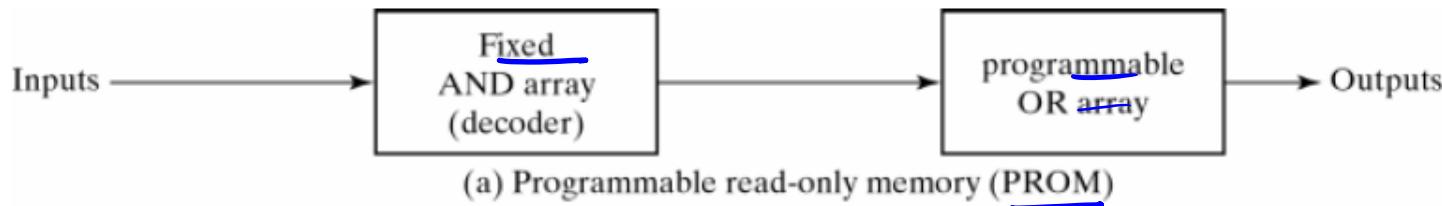
MCQ

PLDs (continued)

AND

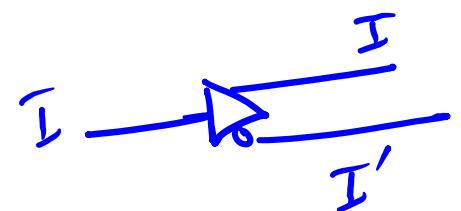
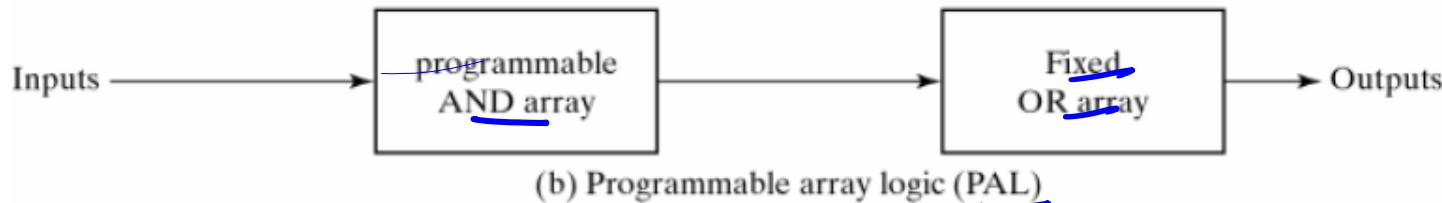
OR

(a)

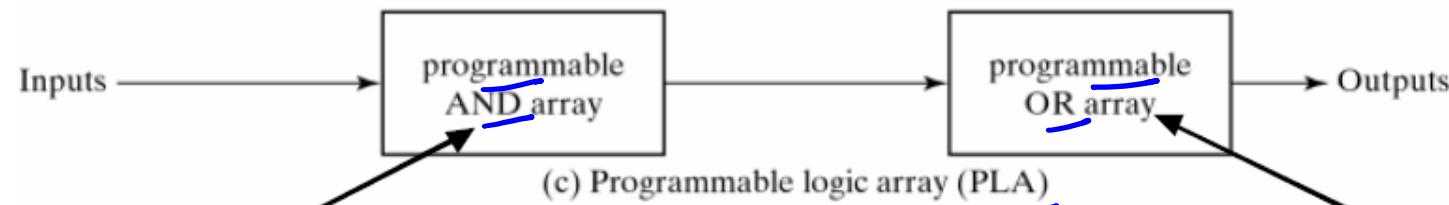


AOI
AND
OR
Sum

(b)



(c)



product terms
for Boolean functions

Fig. 7-13 Basic Configuration of Three PLDs

sum terms
for Boolean functions



PLA Logic Implementation

Key to Success: Shared Product Terms

Example:

Equations

$$\begin{aligned}F_0 &= A + \bar{B}\bar{C} \\F_1 &= \bar{A}\bar{C} + AB \\F_2 &= \bar{B}\bar{C} + AB \\F_3 &= \bar{B}C + A\end{aligned}$$

All the negated unique Minterm

Personality Matrix

Product term	Inputs			Outputs			
	A	B	C	F ₀	F ₁	F ₂	F ₃
AB	1	1	-	0	1	1	0
$\bar{B}C$	-	0	1	0	0	0	1
$\bar{A}\bar{C}$	1	-	0	0	1	0	0
$\bar{B}\bar{C}$	-	0	0	1	0	1	0
A	1	-	-	0	1	0	1

Reuse
of
terms

Input Side:

- 1 = asserted in term
- 0 = negated in term
- = does not participate

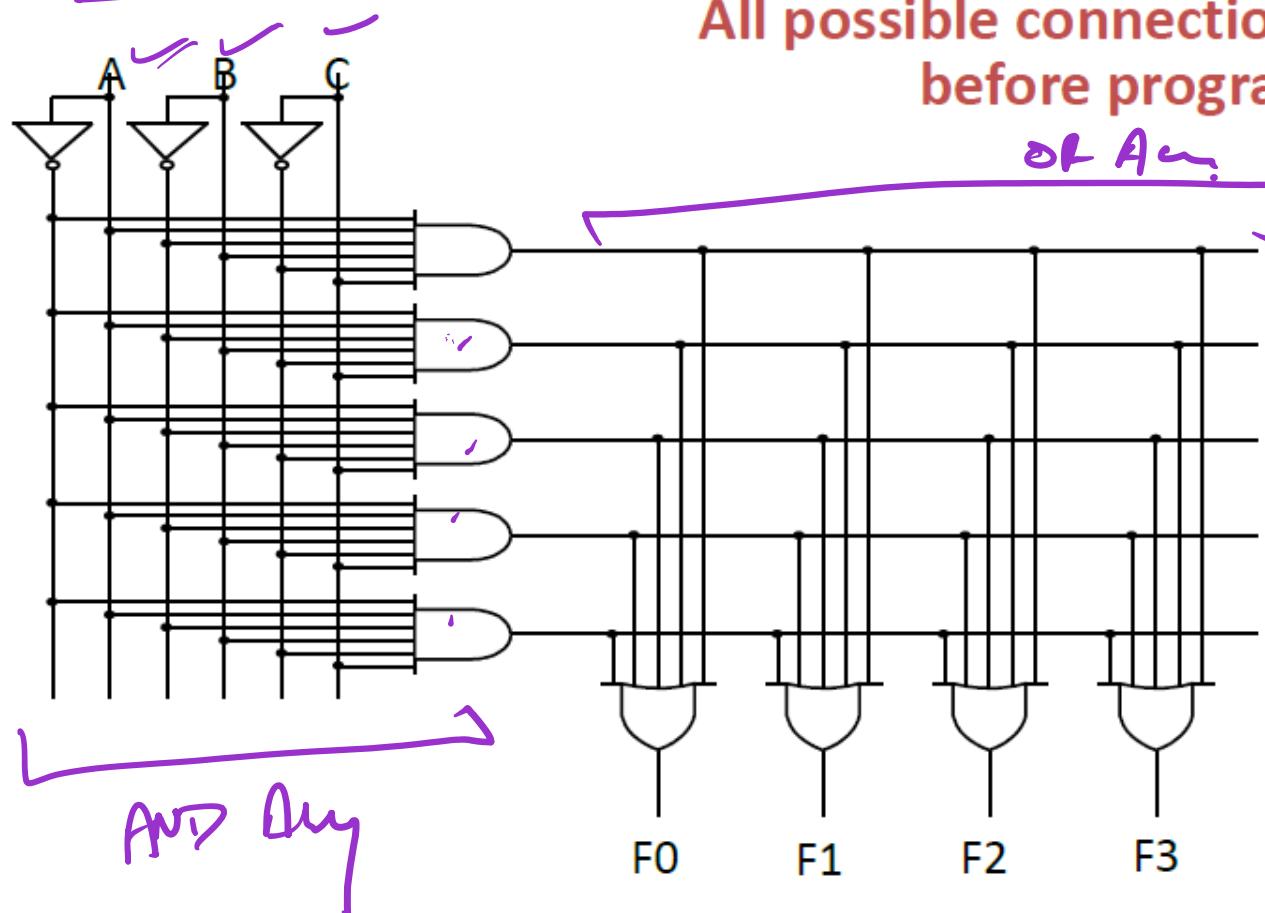
Output Side:

- 1 = term connected to output
- 0 = no connection to output

PLA Logic Implementation

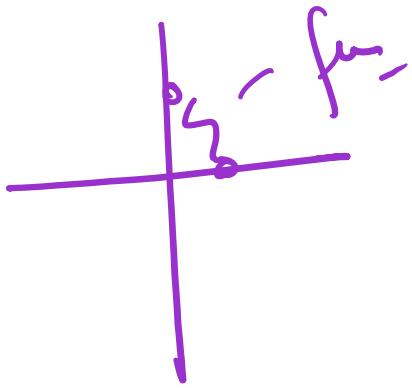
Example Continued - Unprogrammed device

All possible connections are available
before programming

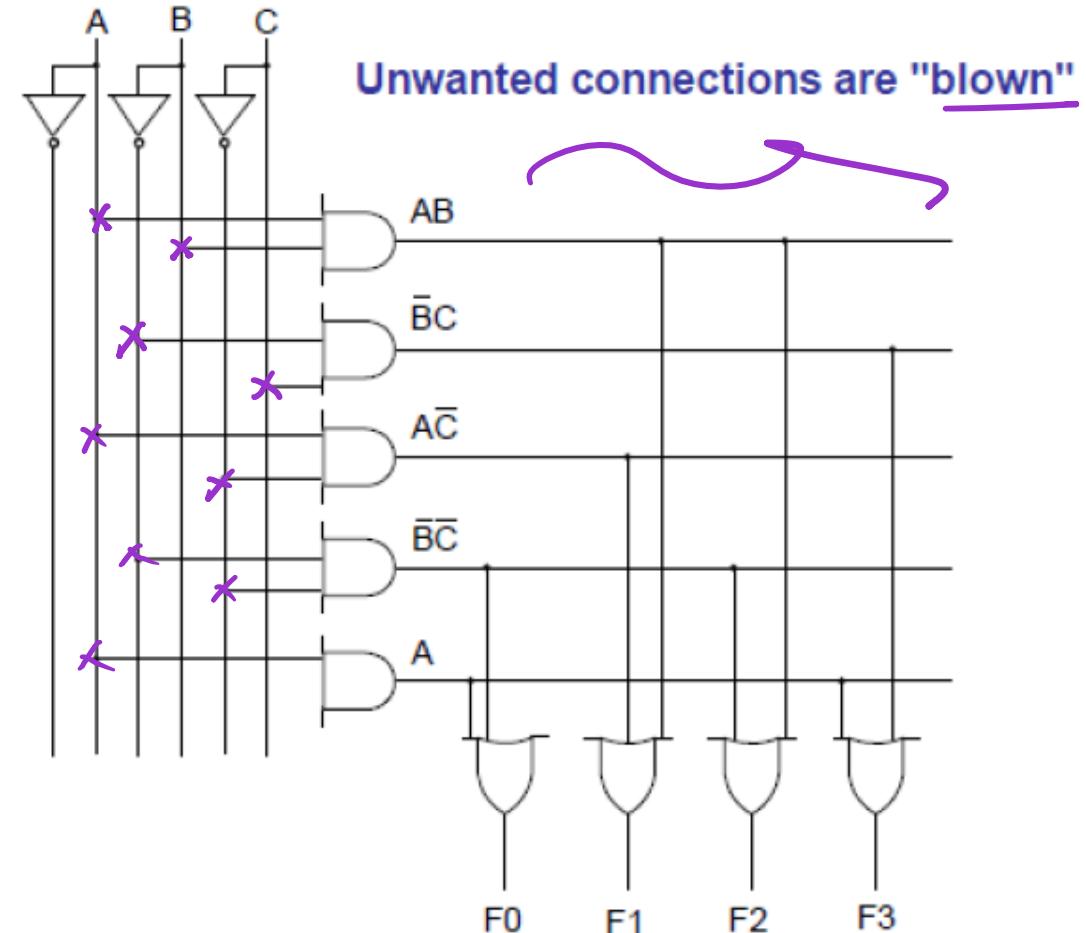


PLA Logic Implementation

Example Continued - Programmed part



Note: some array structures
work by making connections
rather than breaking them



PLA Logic Implementation

or Any



Alternative representation

AND OR

Short-hand notation
so we don't have to
draw all the wires!

X at junction indicates
a connection

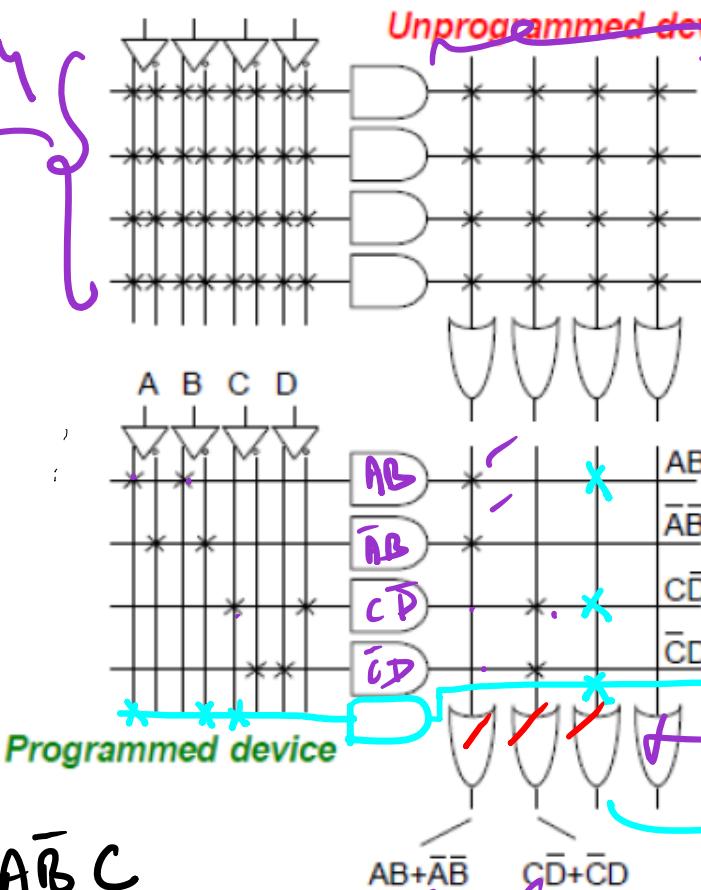
Notation for implementing

$$F_0 = AB + \bar{A}\bar{B}$$

$$F_1 = C\bar{D} + \bar{C}D$$

$$F_3 = \underline{AB} + \underline{C\bar{D}} + \underline{\bar{A}\bar{B}C}$$

- (Q) How many unique minterms are formed?
- A) 3 B) 4 C) 5 D) 6



(Q) How many AND gates
are required in PLA
implent

- A) # of unique Minterm
B) # of unique Maxterm
C) # of input variab.
D) # of o/p functions

D) 6



Programmable Array Logic (PAL)

The programmable array logic (PAL) is a logic device with fixed OR array and a programmable AND array. It is easier to program but not as flexible as PLA.

Boolean functions must be simplified to fit into each section → product term cannot be shared among two or more gates.

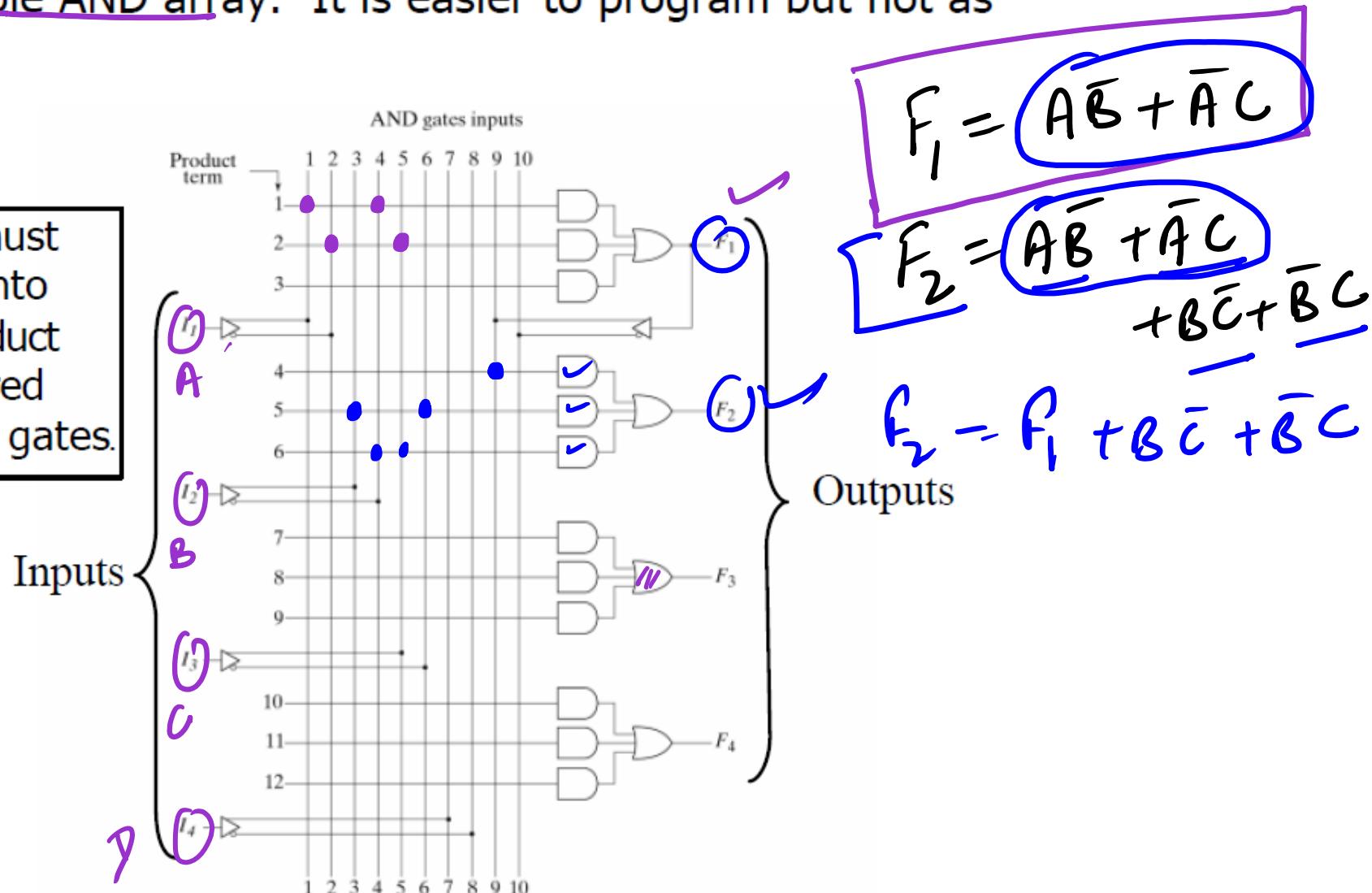


Fig. 7.16 PAL with Four Inputs (I_1 to I_4) and Three Outputs (F_1 to F_3) and Their WLL AND-OR Structure

Sequential Programmable Logic Devices

Simple or Sequential Programmable Logic Device (SPLD):
Includes flip-flops and AND-OR array within the IC chip.

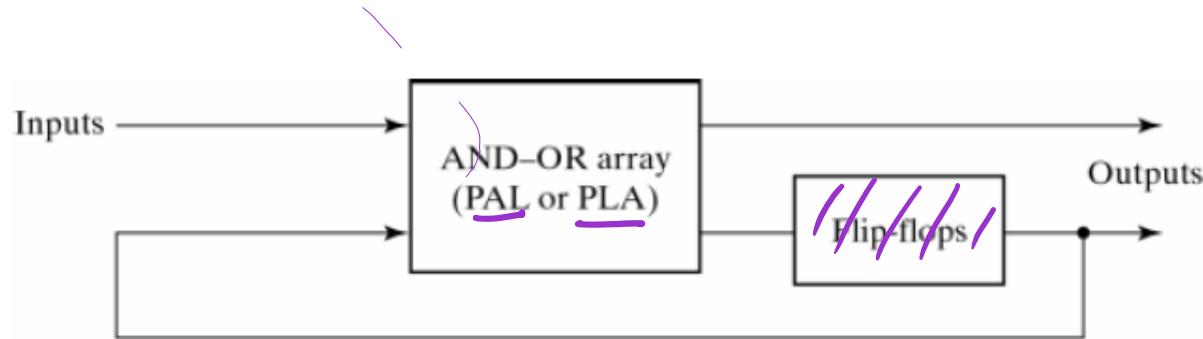


Fig. 7-18 Sequential Programmable Logic Device

- A) PAL
- B) PLA
- C) SPLD
- D) None of the above

Sequential Programmable Logic

A microcell is a section of a SPLD that contains a sum-of-product combinational logic and a flip-flop. A commercial SPLD contains 8 - 10 microcells in an IC package.

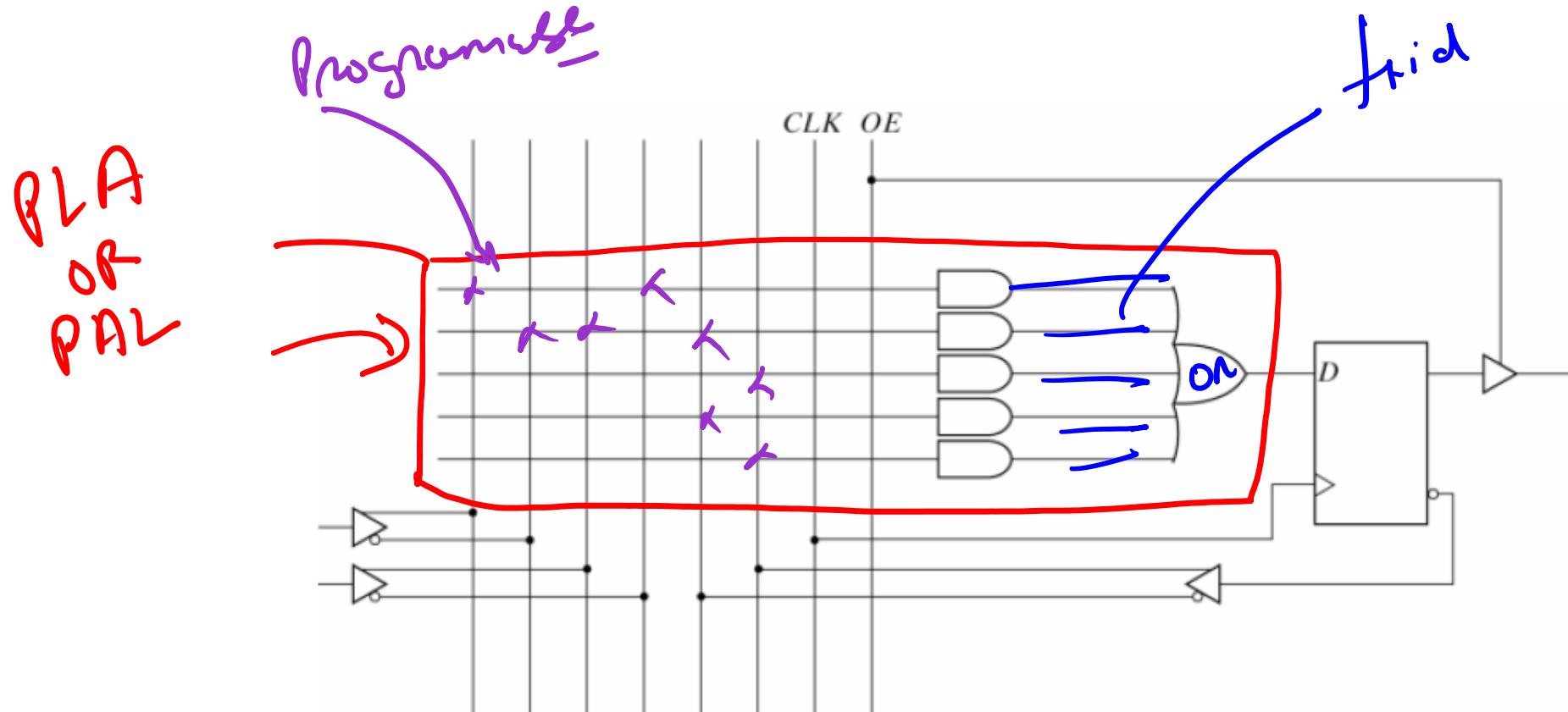


Fig. 7-19 Basic Macrocell Logic

#Complex Programmable Logic Device (CPLD)

Complex Programmable Logic Device (CPLD):

The design of a complete digital system using PLD requires the use of several PLD's in a Complex Programmable Logic Device (CPLD) integrated on a single chip.

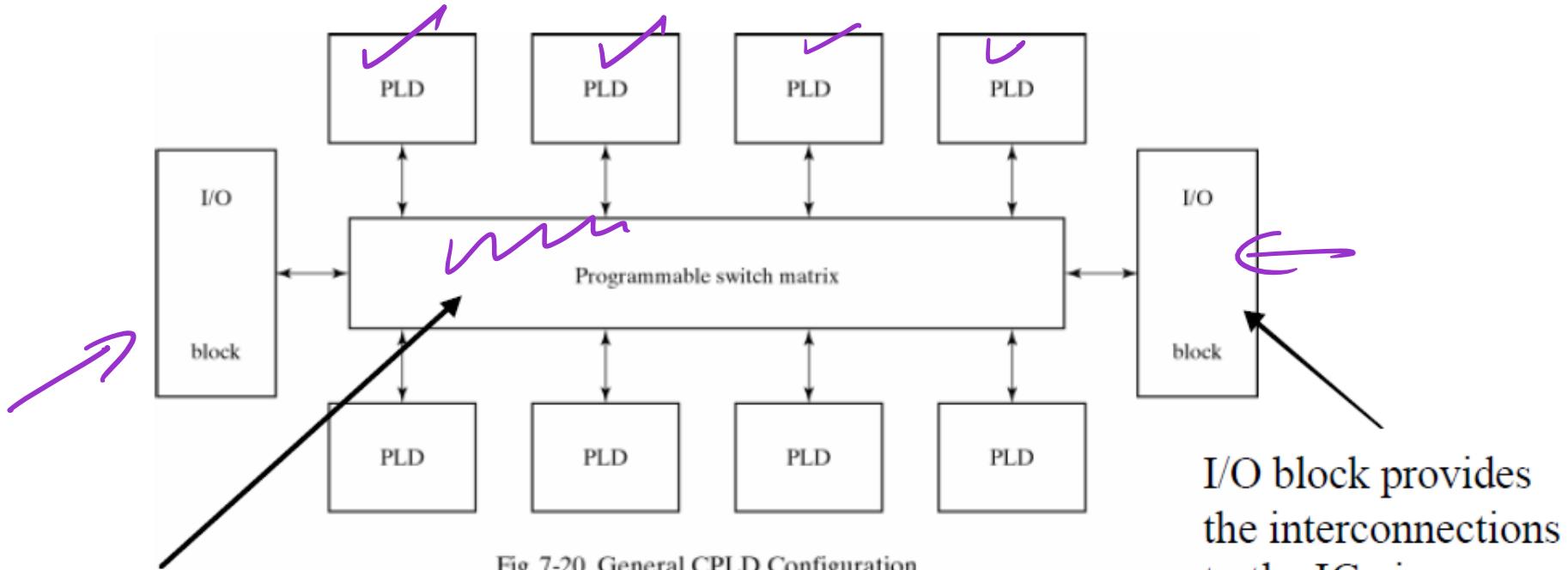


Fig. 7-20 General CPLD Configuration

switch matrix received inputs from I/O and directs them to the individual microcells.

I/O block provides the interconnections to the IC pins

#

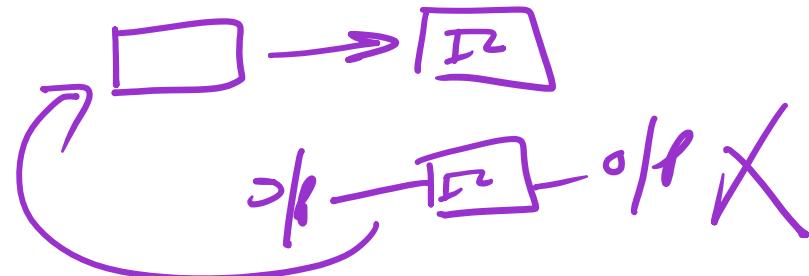
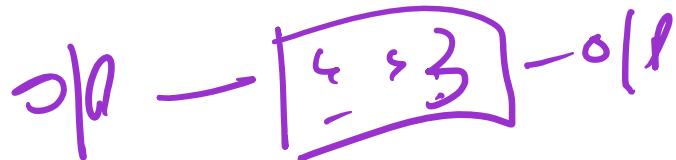
Field-Programmable Gate Array (FPGA)

MC

Field-Programmable Gate Array (FPGA): is a VLSI circuit whose function is defined by a user's program rather than by the manufacturer of the device (CPLD)

MS |
LSI
VLSI

- Depending on the particular device, the program is either 'burned' in permanently or semi-permanently as part of a board assembly process, or is loaded from an external memory each time the device is powered up.
- The Field-Programmable Gate Arrays provide the benefits of custom CMOS VLSI, while avoiding the initial cost and time delay.





mo9

Evolution of implementation technologies

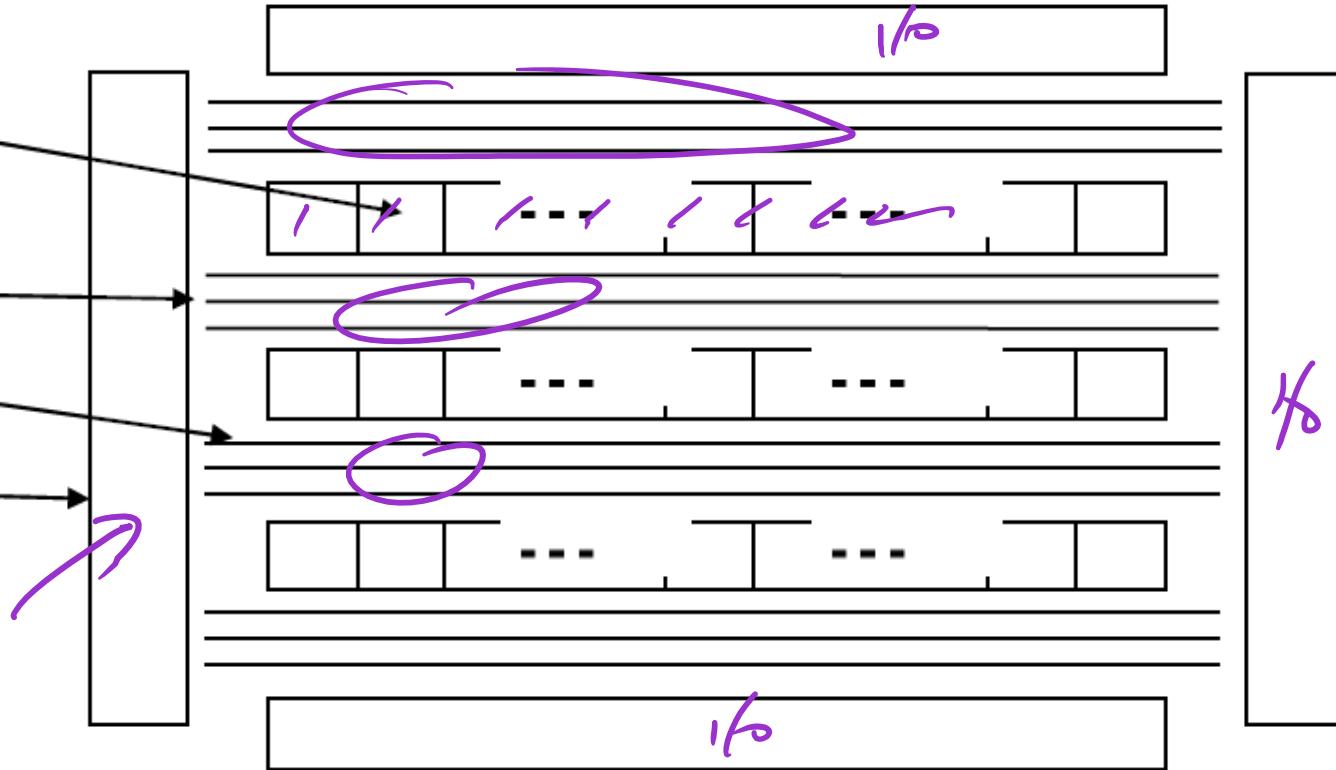
- Logic gates (1950s-60s)
- Regular structures for two-level logic (1960s-70s)
 - muxes and decoders, PLAs
- Programmable sum-of-products arrays (1970s-80s)
 - PLDs, complex PLDs
- Programmable gate arrays (1980s-90s)
 - densities high enough to permit entirely new class of application, e.g., prototyping, emulation, acceleration

**trend toward
higher levels
of integration**



Gate Array Technology (IBM - 1970s)

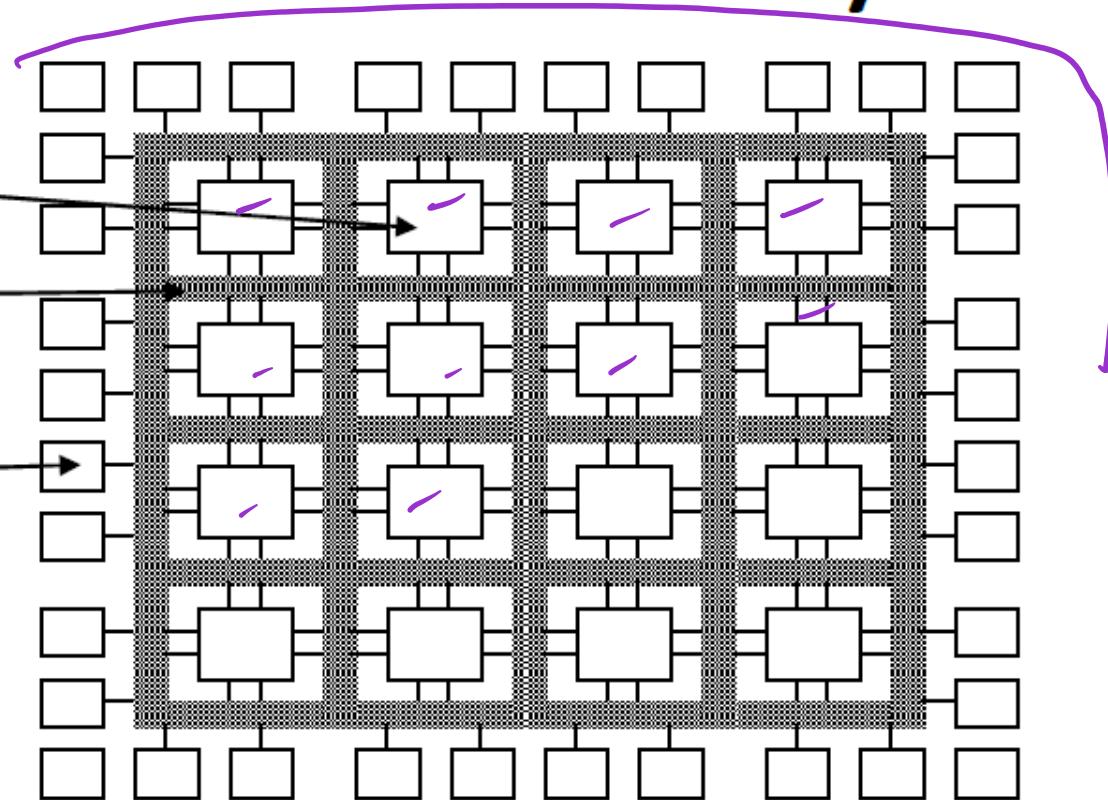
- Simple logic gates
 - combine transistors to implement combinational and sequential logic
- Interconnect
 - wires to connect inputs and outputs to logic blocks
- I/O blocks
 - special blocks at periphery for external connections
- Add wires to make connections
 - done when chip is fabbed
 - “mask-programmable”
 - construct any circuit





Field-Programmable Gate Arrays

- Logic blocks
 - to implement combinational and sequential logic
- Interconnect
- I/O blocks
 - special logic blocks at periphery of device for external connections
- Key questions:
 - how to make logic blocks programmable?
 - how to connect the wires?
 - *after the chip has been fabbed*



SRAM vs DRAM

There are two types of Random Access

SRAM (Static RAM) and DRAM (Dynamic RAM)

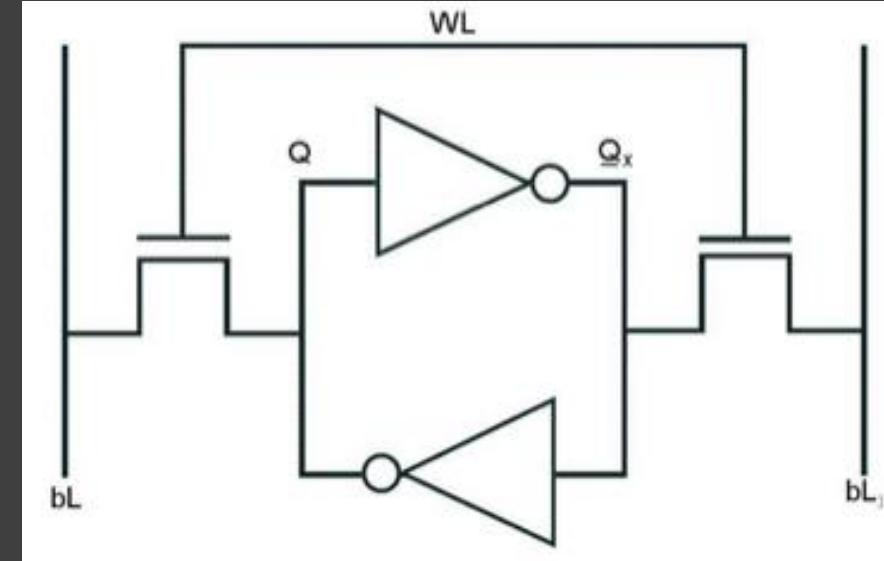
MCH

SRAM	DRAM
Static	Dynamic
More Number of transistor <i>6T</i>	Less number of Transistor <i>1P and 1C</i>
Costlier <i>why more transistors</i>	Cheap
Fast	Slow
Cache memory	computer main memory
No refresh required, hold the data as long as the power supply is not cut off	Requires the data to be refreshed periodically

6T SRAM

SRAM is read-write (R/W) memory circuits are designed to allow(writing) of data bits to be stored in the memory array as well as their retrieval (reading)

The memory circuit is said to be *static* if the stored data can be retained indefinitely (as long as a sufficient power supply voltage is provided) without a periodic refresh operation.



To write data WL=1 enable NMOS, Binary data apply to BL and BLB, Node Q and QB hold opposite and stable value.

To write '1' and node Q → WL=1, BL=1 and BLB=0; output at Q=1 and QB=0.

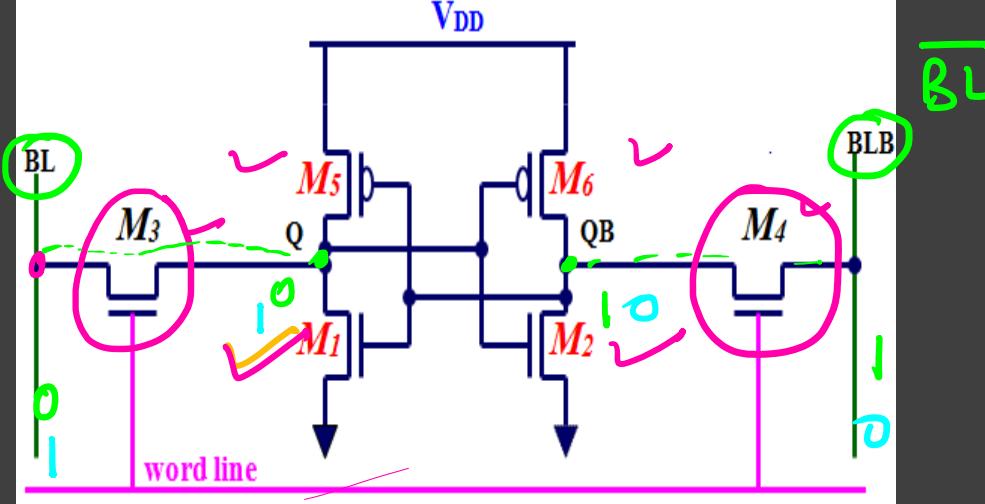
To write '0' and node Q → WL=1, BL=0 and BLB=1; output at Q=0 and QB=1.

Q/I

GTS RAM

word line

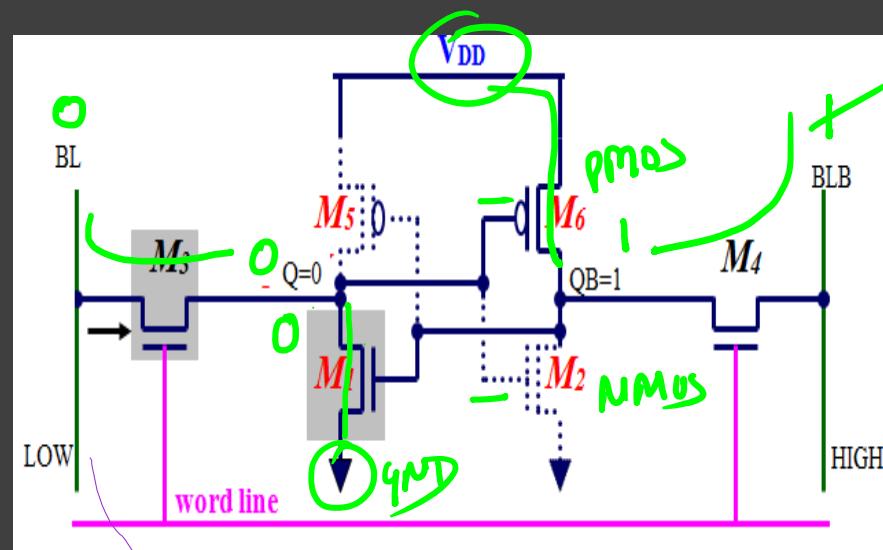
WL=1 M3 and M4 ON
Binary data over BL and BLB
transfer to Q and QB



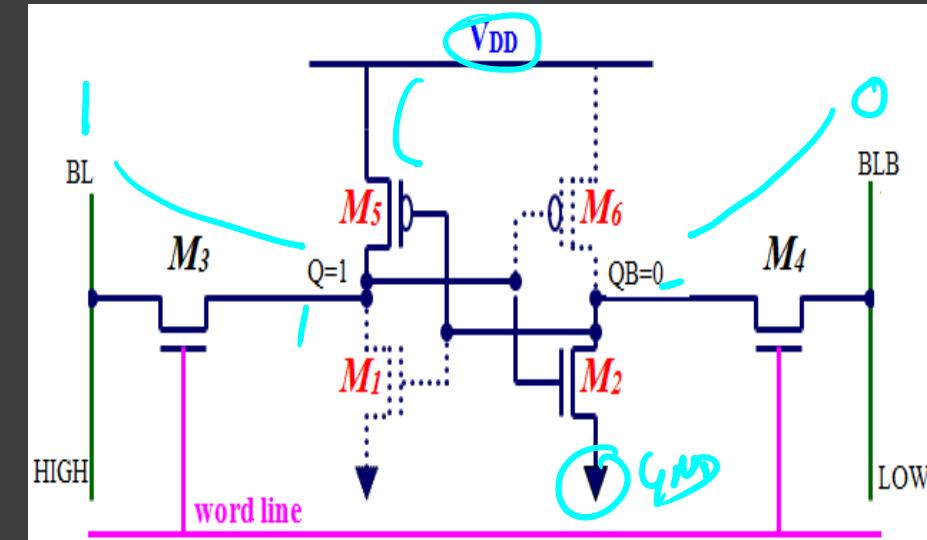
BL

MosFET
P-Mos N-Mos
Active - low res
deact - high res

A
B



★ To write '0' and node Q → BL=0 and BLB=1
M1M6 → ON M2 M5 → OFF
output at Q=0 and QB=1.



★ To write '1' and node Q → BL=1 and BLB=0;
M2M5 → ON, M1M6 → OFF,
output at Q=1 and QB=0.



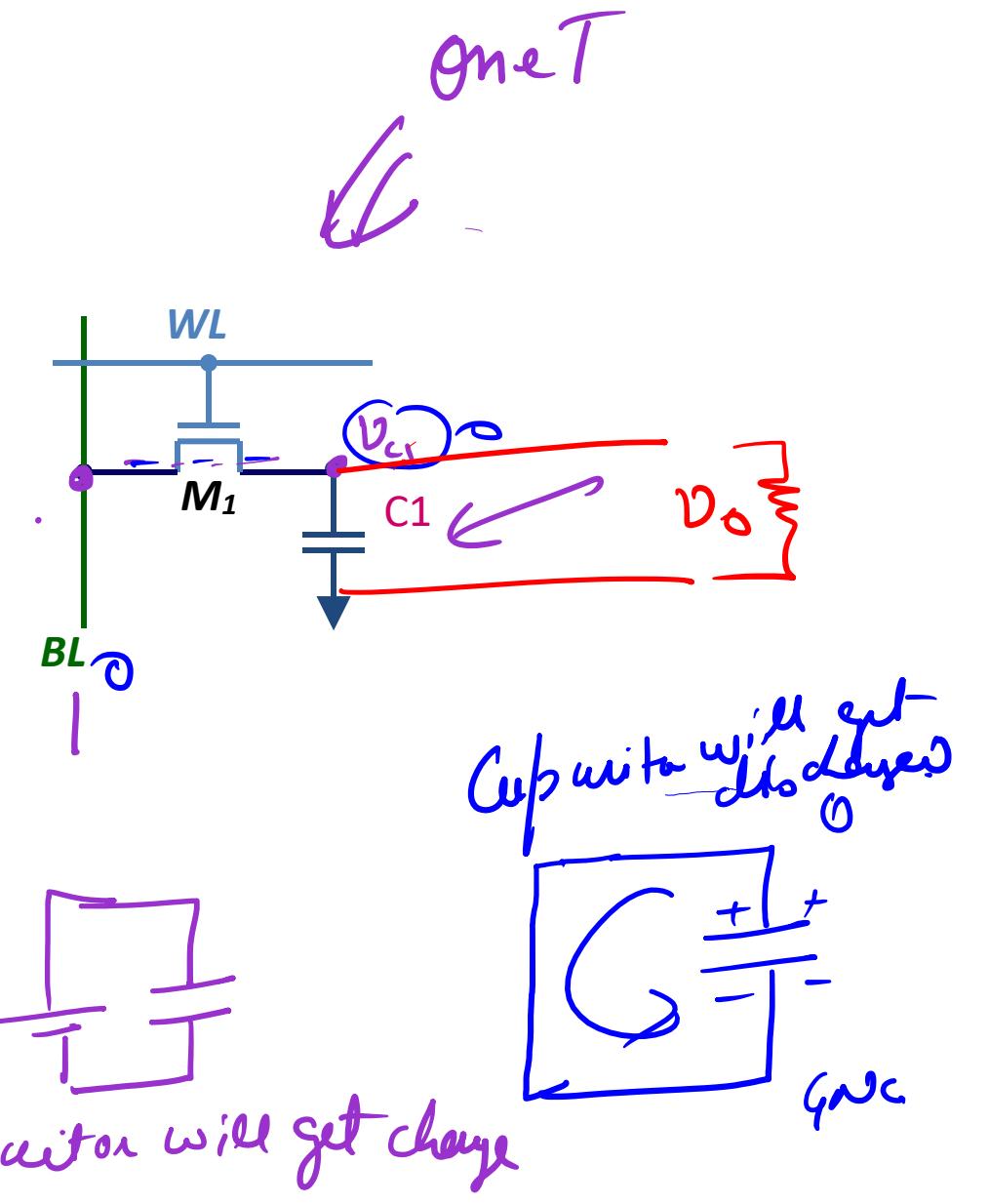
DRAM

The binary information is stored as the charge in
Capacitor (C_1)

★ Write "1" OP: $BL = 1$, WL = 1 (M_1 ON) $\Rightarrow C_1$
charges to "1"

★ Write "0" OP: $BL = 0$, WL = 1 (M_1 ON) $\Rightarrow C_1$
discharges to "0"

→ Read OP: destroys stored charge on $C_1 \Rightarrow$
destructive refresh is needed after every data
read operation



- Why is SRAM more preferably in non-volatile memory?
 - A. low-cost
 - B. high-cost
 - C. low power consumption
 - D. transistor as a storage element

- How many MOSFETs are required for SRAM?

- A. 2
- B. 4
- C. 6
- D. 8

~~A~~ Next CA

- 30 MCQ 1 mark each
with 0.25 -ve marking
for wrong answer.
- Syllabus units & units
- Date Last lecture (8 May 2021)
in Tutorial class