ECE213: Digital Electronics

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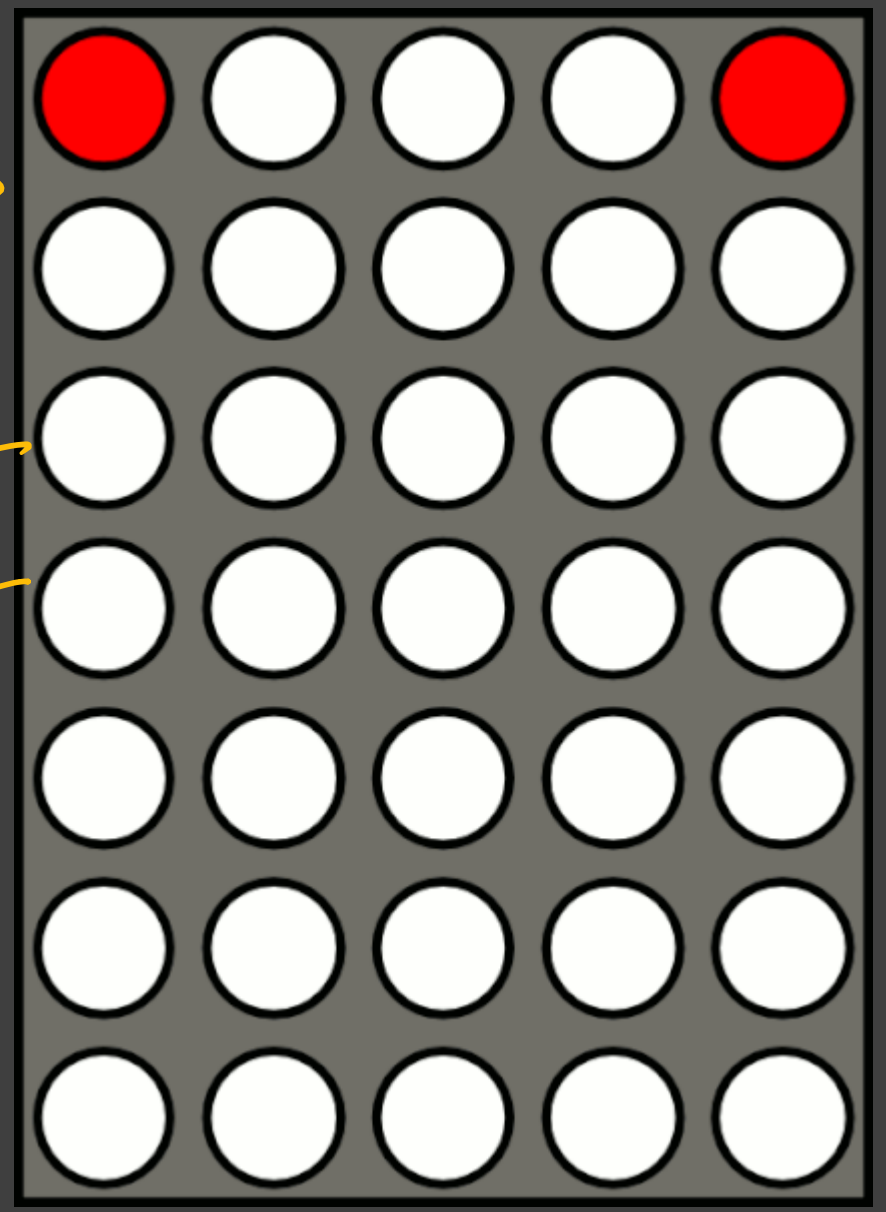
The Course Contents

Unit IV

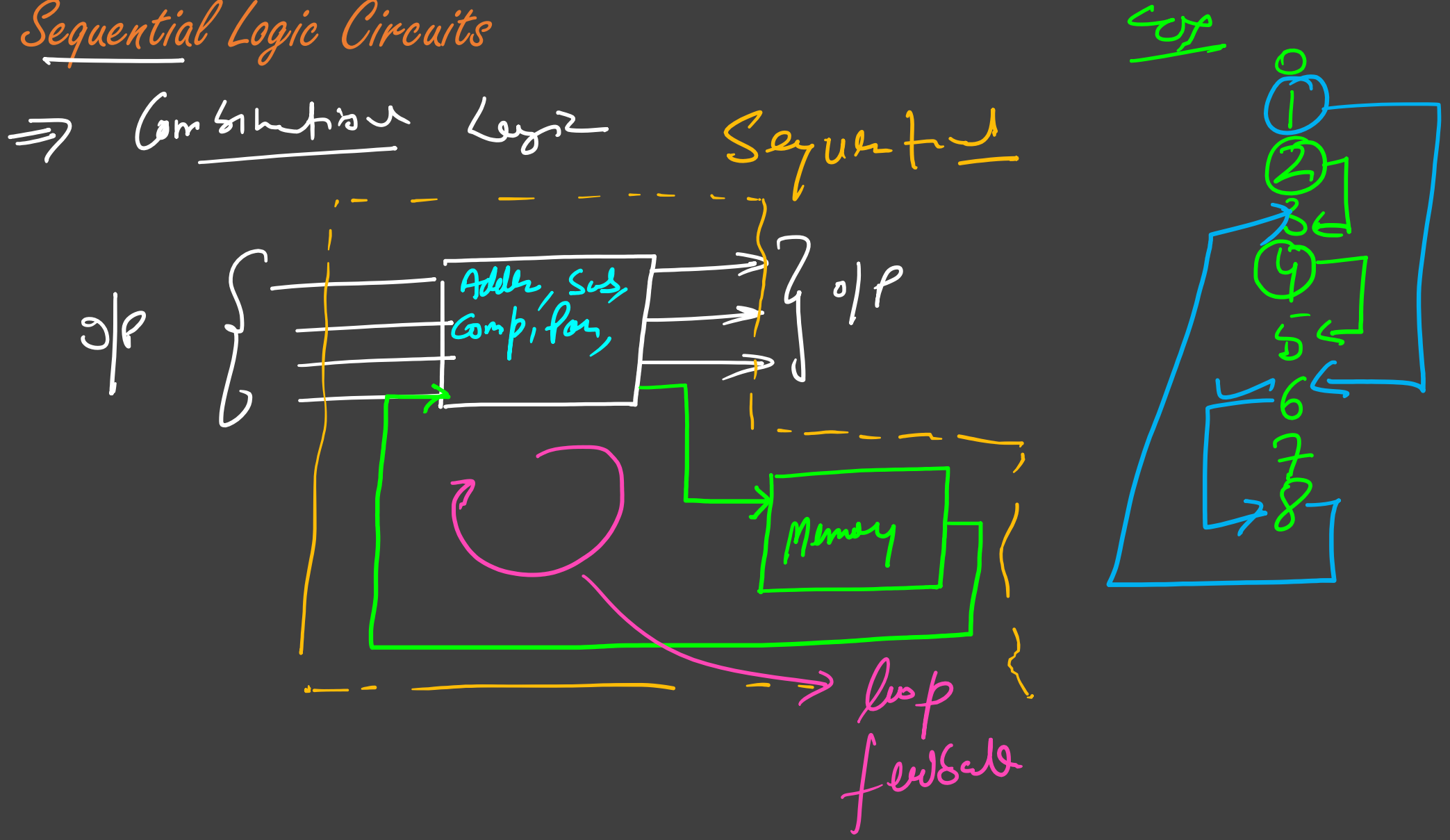
Introduction to Sequential Logic Circuits : Basic sequential circuits: SR-latch, D-latch, D flipflop, JK flip- flop, T flip-flop, Conversion of basic flip-flops

Next o/p depends on the present o/p



Introduction to Sequential Logic Circuits

Sequential Logic Circuits

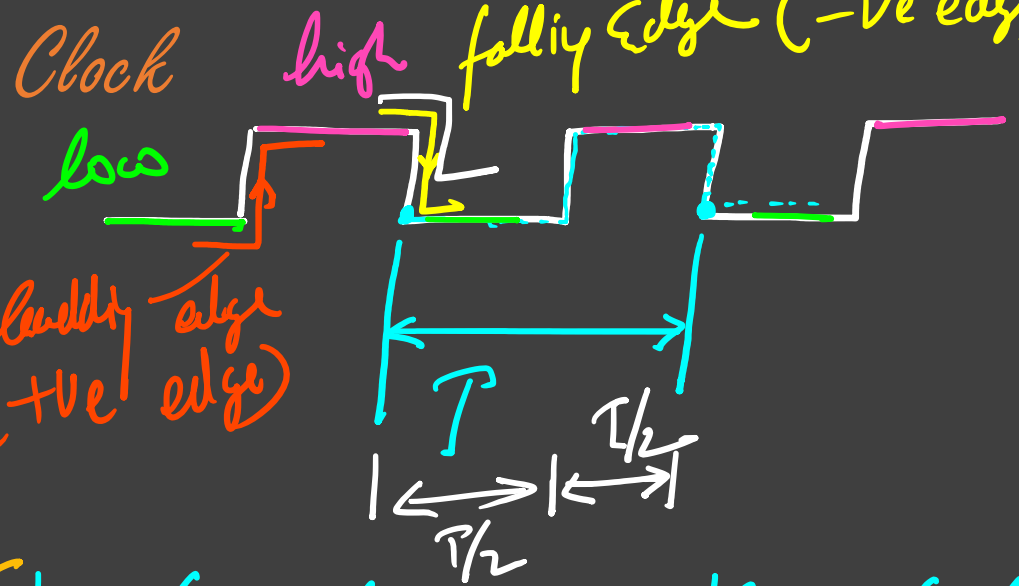


Introduction to Sequential Logic Circuits

Sequential Logic Circuits

	Combinational Circuit	Sequential Circuit
Definition	Combinational Circuit is the type of circuit in which output is independent of time and only relies on the input present at that particular instant.	On other hand Sequential circuit is the type of circuit where output not only relies on the current input but also depends on the previous output.
Feedback	In Combinational circuit as output does not depend on the time instant, no feedback is required for its next output generation.	On other hand in case of Sequential circuit output relies on its previous feedback so output of previous input is being transferred as feedback used with input for next output generation.
Performance	As the input of current instant is only required in case of Combinational circuit, it is faster and better in performance as compared to that of Sequential circuit.	On other hand Sequential circuit are comparatively slower and has low performance as compared to that of Combinational circuit.
Complexity	No implementation of feedback makes the combinational circuit less complex as compared to sequential circuit.	However on other hand implementation of feedback makes sequential circuit more complex as compared to combinational circuit.
Elementary Blocks	Elementary building blocks for combinational circuit are logic gates.	On other hand building blocks for sequential circuit are flip flops.. It can store one bit data.
Operation	Combinational circuit are mainly used for arithmetic as well as Boolean operations.	On other hand Sequential circuit is mainly used for storing data.

Introduction to Sequential Logic Circuits



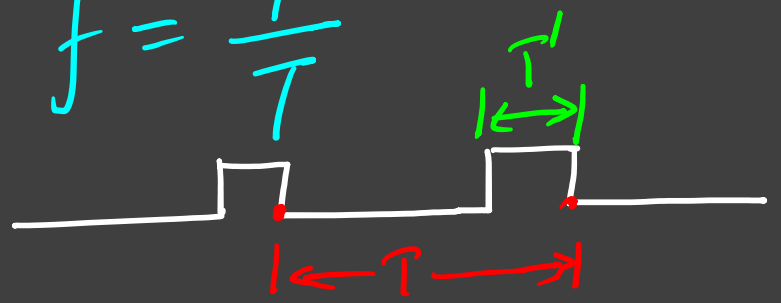
low level (-ve level)
high level (+ve level)
leading edge (+ve edge)
falling edge (-ve edge)

Time period (T) time to complete one cycle.

Frequency (f) No of cycles in one unit time sec

$$f = \frac{1}{T}$$

Eg



$$D.C = \frac{T'}{T}$$

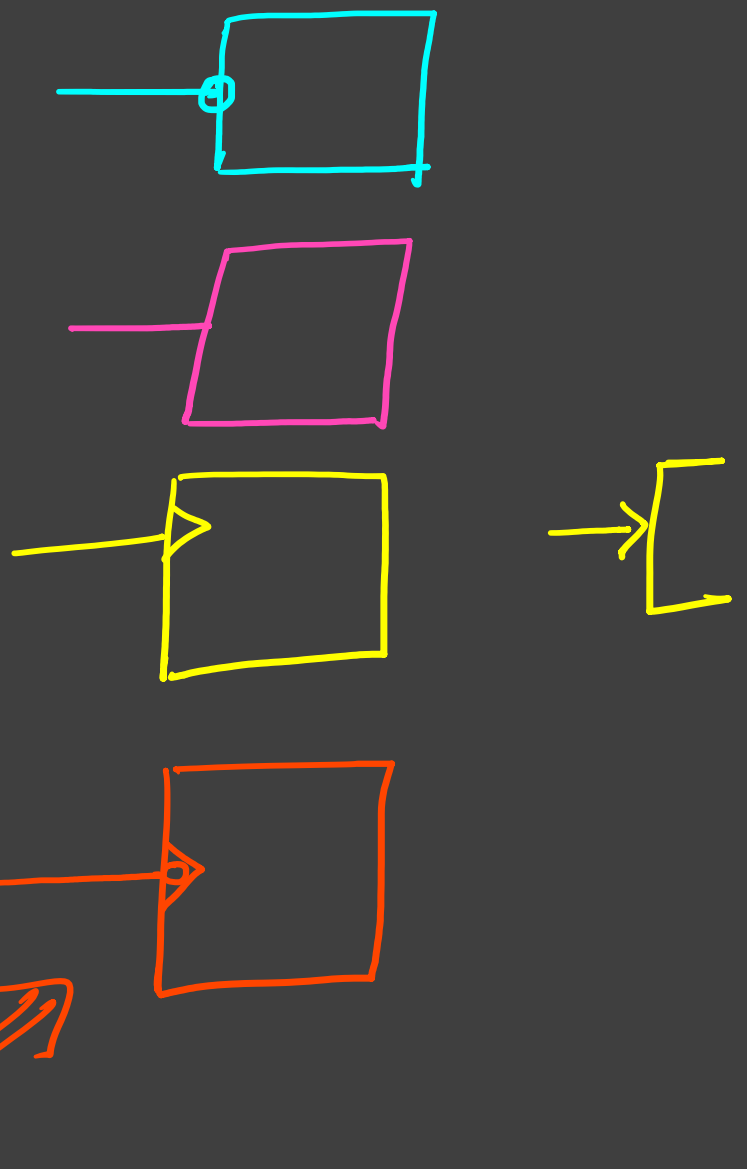
* Duty Cycle : Ratio of time for high level to time per.

$$D.C = \frac{T/2}{T} = 50\%$$

Introduction to Sequential Logic Circuits

Triggering Methods

1) -ve level triggering
2) +ve level triggering
3) +ve edge triggering
4) -ve edge triggering

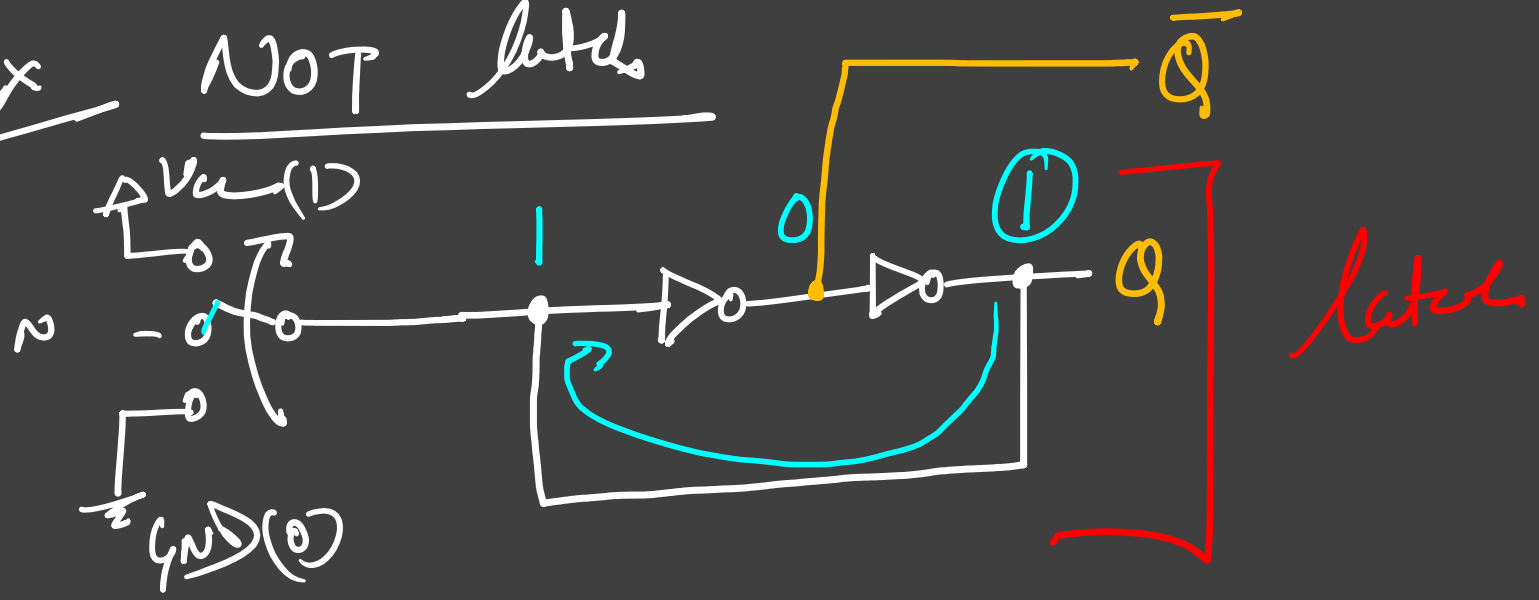


Introduction to Sequential Logic Circuits

★ Latch : It can store 1-bit data

It is a kind of loop (feedback)

Ex NOT latch



Introduction to Sequential Logic Circuits

SR Latch (NOR)

Set | Reset

S	R	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	
0	1	0	1	Reset
1	0	1	0	Set
1	1	–	–	

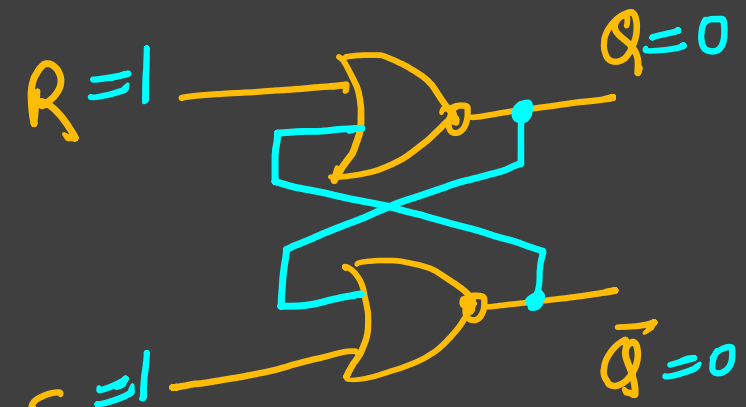
Case 1: If S=0, R=0, No change condition (Memory)

Case 2: If S=0, R=1, Reset condition

Case 3: If S=1, R=0, set condition

case 4: If S=1, R=1, Invalid condition

$Q = \bar{Q}$ (Invalid)



Set Condition: When the o/p of the Ckt set to high, irrespective of previous o/p.

Reset Condition: When the o/p of the Ckt set to low, irrespective of prev. o/p.

★ NOR Logic

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

1) If any of the i/p is high the o/p is low.

2) If any of the i/p is low, then the o/p is the complement of 2nd input