Which one of the following logic gates is not a universal building block?

a. Three input NAND gate

b. Two input NAND gate

c. Two input XOR gate

d. Two input NOR gate

Which one of the following logic gate has truth table given below?

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

a. Exclusive OR
b. NOR
c. Exclusive NOR
d. NAND

What is the number of inputs and outputs of a half-adder?

a. 2 inputs and 1 output

b. 2 inputs and 2 outputs

c. 2 inputs and 3 outputs

d. 3 inputs and 2 outputs

What is the number of inputs and outputs of a full-adder?

a. 2 inputs and 1 output

b. 2 inputs and 2 outputs

c. 2 inputs and 3 outputs

d. 3 inputs and 2 outputs

Which one of the following electronic circuits can be used to store 1-bit of data?

a. Encoder

b. OR gate

c. Flip-Flop

d. Decoder

A combinational logic circuit which sends data coming from a single source to two or more separate destinations is called which one of the following?

a. Decoder

b. Encoder

c. Multiplexer

d. Demultiplexer

Which one of the following multiplexer would have a 4-bit data select input?

a. 4:1 multiplexer

b. 2:1 multiplexer

c. 16:1 multiplexer

d. 8:1 multiplexer

Selective-set operation is implemented by

a. A ← A + B

b. A ← A.B

c. A ← A XNOR B

d. A ← A OR B

insert operation is implemented by

a. (A.B)+C

b. A.B+A.B

c. A.B'+C

d. A.B'

An instruction cycle refers to which one of the following?

a. Fetching an instruction

b. Executing an instruction

c. Fetching an instruction, decoding it, reading the contents of the effective addresses of the operands and executing instruction

d. Clock cycle time

In which one of the following addressing modes is the actual operand provided as a part of the instruction?

a. Direct
b. Immediate
c. Indirect
d. Relative

When an interrupt occurs, which one of the following takes place?

a. Execution of the current instruction is completed and the address of the next instruction is saved before the interrupt service program starts
b. Execution of the current instruction is aborted and its address is saved before the interrupt service program starts
c. Execution of the current instruction is completed and the interrupt service program starts
d. Execution of the current instruction is aborted and the interrupt service program starts

In case of Memory-reference instruction, the most appropriate value of opcode and address mode bit i.e. I among following are:

a. 000 and 0
b. 111 and 0
c. 111 and 1
d. All of these

In case of Memory-reference instruction, Address mode bit i.e. I=0 represents:

a. Direct address
b. Indirect address
c. Immediate address
d. None of these

In Memory-reference instruction, Address mode bit i.e. I=1 represents:

a. Direct address
b. Indirect address
c. Immediate address
d. None of these

A memory-reference instruction uses ___ bits to specify an address.

a. 12

b. 16

c. 8

d. 4

A basic computer has three instruction code formats. Each format has ____ bits.

a. 12

b. 16

c. 8

d. 4

The register-reference instructions are recognized by the operation code ____ with a ____ in the leftmost bit of the instruction.

a. 111 0

b. 111 1

c. 110 0

d. 110 1

The Input-Output instructions are recognized by the operation code ____ with a ____ in the leftmost bit of the instruction.

a. 111 0

b. 111 1

c. 110 0

d. 110 1

In Input-Output instructions, how many bits are used to specify the type of input-output operation or test performed?

a. 12

b. 16

c. 8

d. 4