# ECE213: Digital Electronics

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# The Course Contents
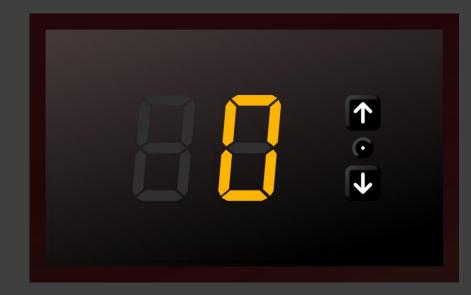
*Counters*

☆ Asynchronous Counter

# 4-bit up comtr

Sol: No of FF = No of bits = 4

Type of FF = T-FF



As per the connw the B-FF is going to toggle at the -ve edge of $Q_A$.
∴ $Q_A$ is acting as clock for B-FF.

Counters

#Timing dig



| Clock | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LSB $Q_A$ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $Q_B$ | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| $Q_C$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| MSB $Q_D$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 0 |

Up Counter

# Sequential Logic Circuits Applications

Counters ★ 4-bit Asyn down Counter (with -ve clock)

Note! -ve edge of $\overline{Q_A}$ is same as +ve edge of $Q_A$.



The B, FF is going to toggle at -ve edge of $\overline{Q_A}$, which is the +ve edge of $Q_A$

| | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $Q_A$ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | |
| $Q_B$ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | |
| $Q_C$ | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | |
| $Q_D$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |

Down Count →

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# Sequential Logic Circuits Applications

Counters ★ 4-bit Asyn down Counter (with the clk)

Note:- -Ve edge of $\overline{Q_A}$ is same as +Ve edge of $Q_A$.



The B, FF is going to toggle at +Ve edge of $Q_A$,

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $Q_A$ | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $Q_B$ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| $Q_C$ | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| $Q_D$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Down Count →

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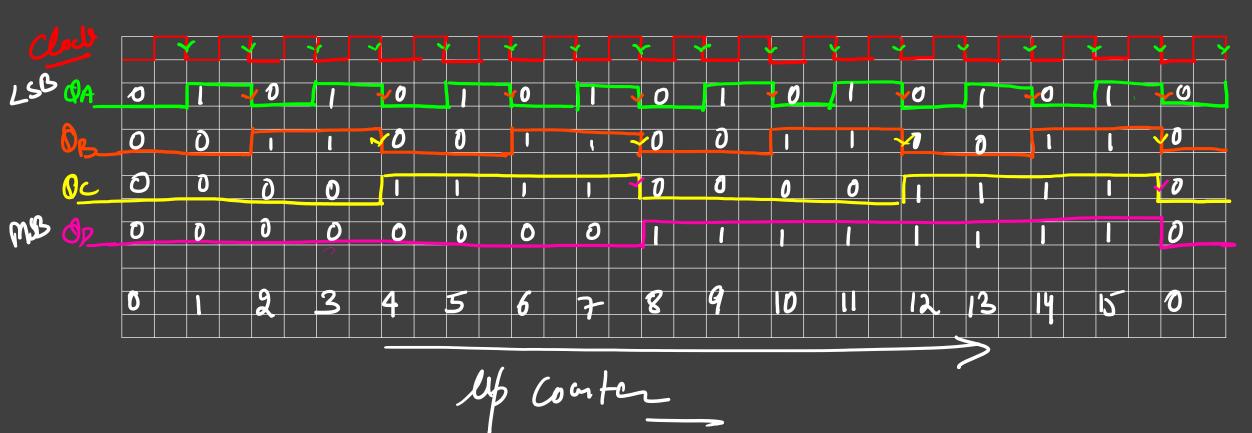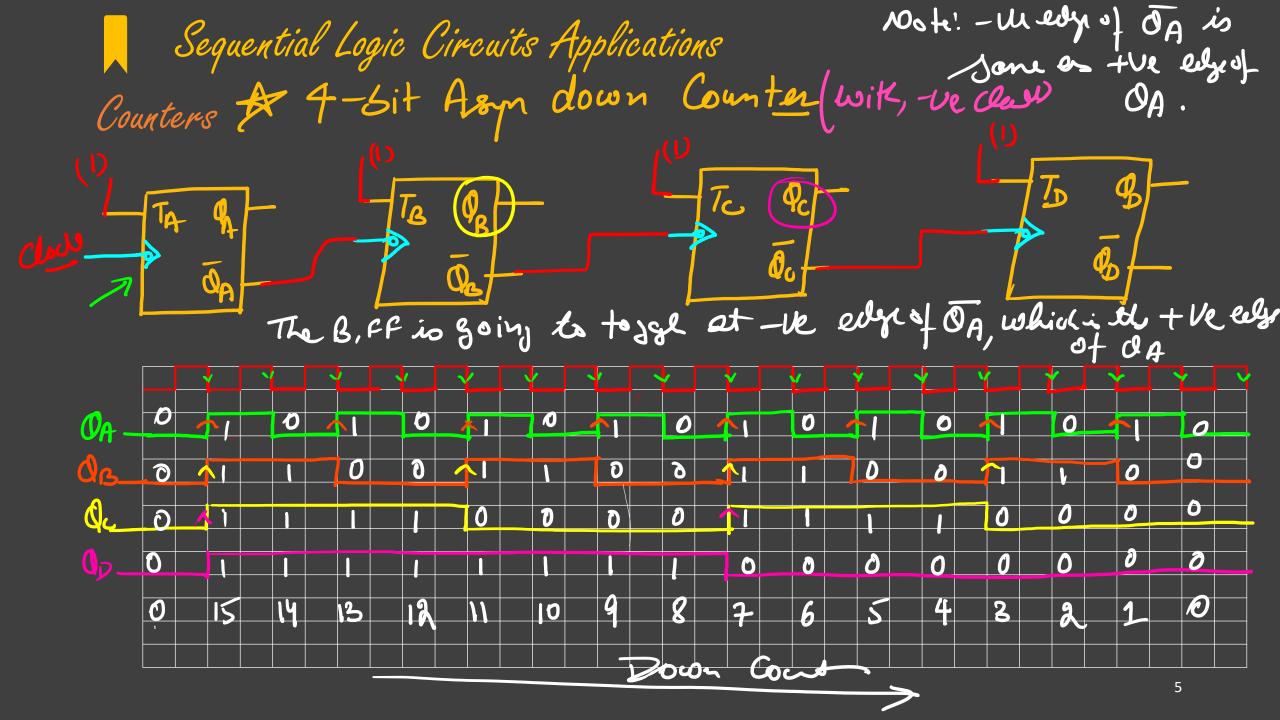
# *Sequential Logic Circuits Applications*

*Counters* # Asyn count

| Type of Clock | Clock to Next FF | Type of Counter |
|---|---|---|
| —ve edge | from $Q$ | Up Count |
| —ve edge | from $\bar{Q}$ | Down Counter |
| +ve edge | from $Q$ | Down Count |
| +ve edge | from $\bar{Q}$ | Up Count |