ECE216: Digital Electronics Laboratory

Exp -6

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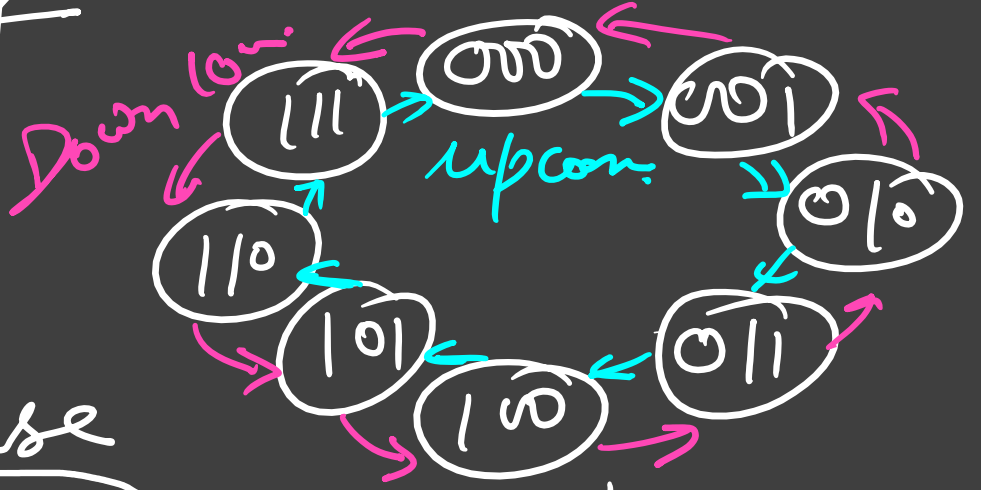
★ Design the up counter (3-bit sync up cnt)

Step1 Define the no. of flip flop. (3) ABC

Step2 Type of FF, T-FF

Note: If J = K = 1, then JK FF act as T flip flop

Step3. State diagram, State table



Excitation table of FF

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

No change

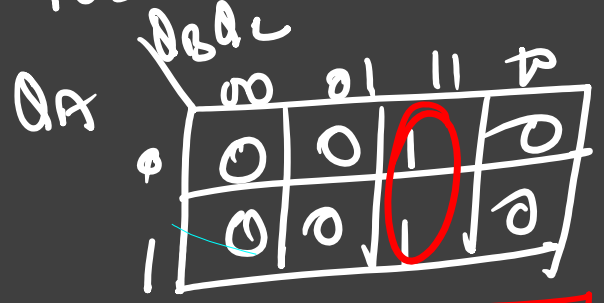
Toggle

Order → ★ State table

Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

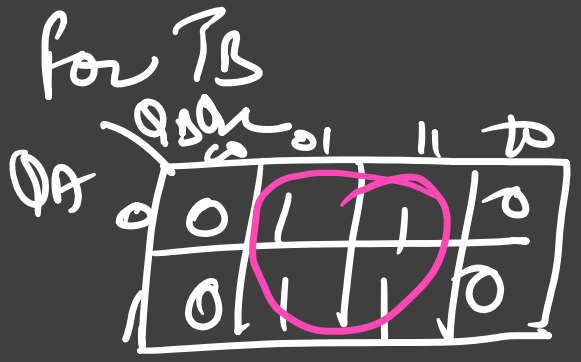
Step: solve for Boolean eq.

for T_A



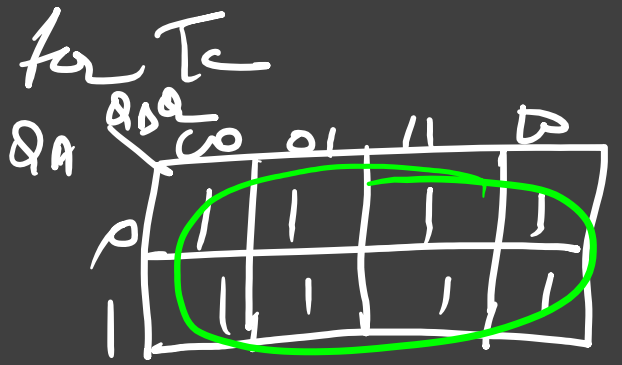
$T_A = Q_B Q_C$

for T_B



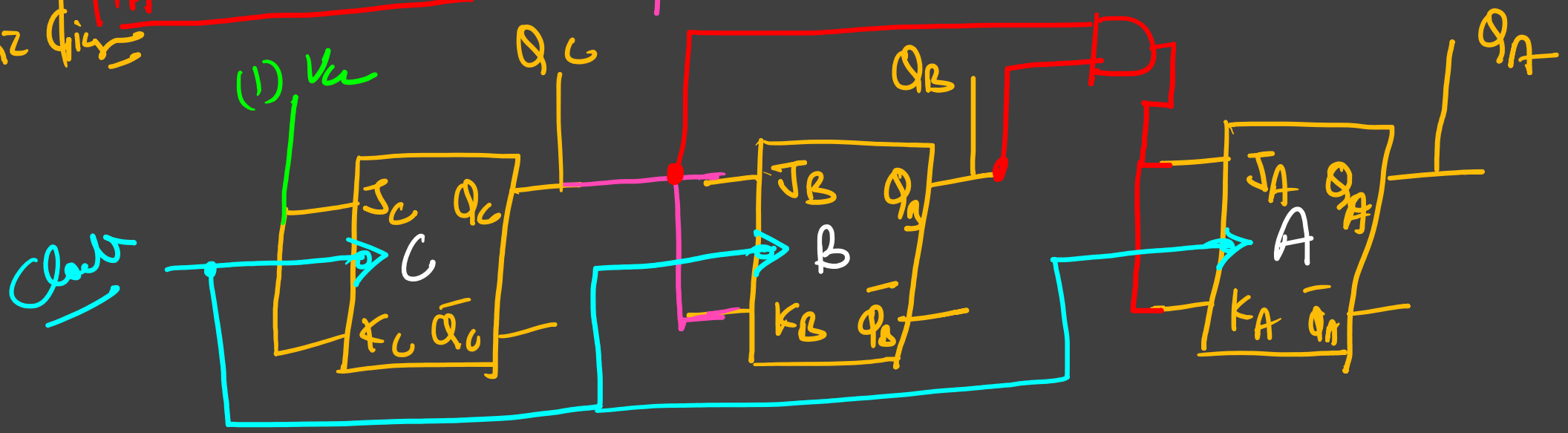
$T_B = Q_C$

for T_C



$T_C = 1$

Logic diagram



5. Cautions:

1. Do not press the IC on breadboard until pins are aligned with pours.
2. Make connection properly.
3. There should not any short circuit in the circuit.
4. Avoid the heating of IC.
5. Provide proper clock pulse.

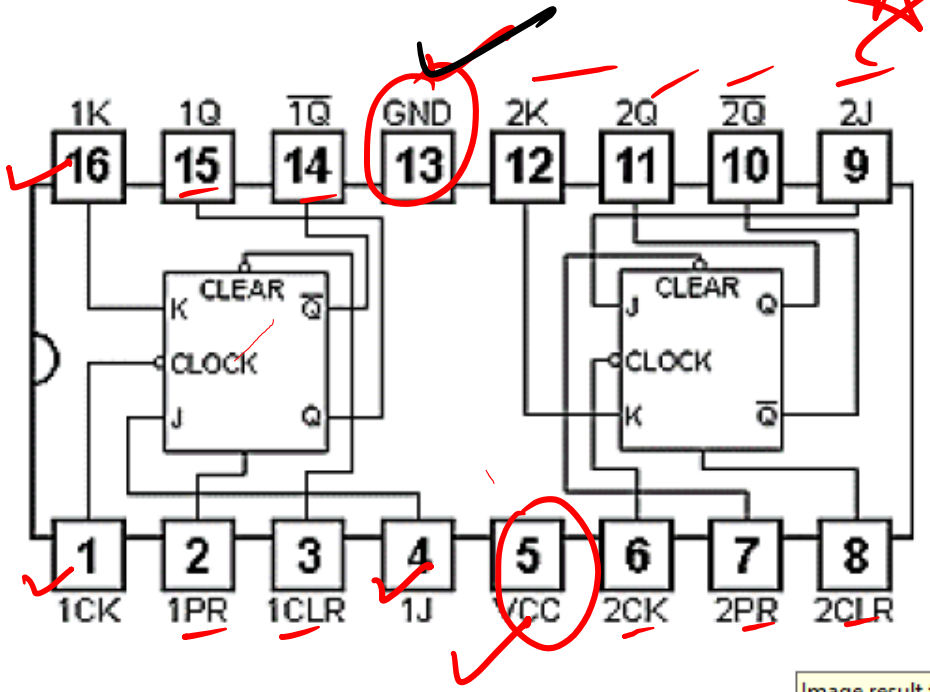
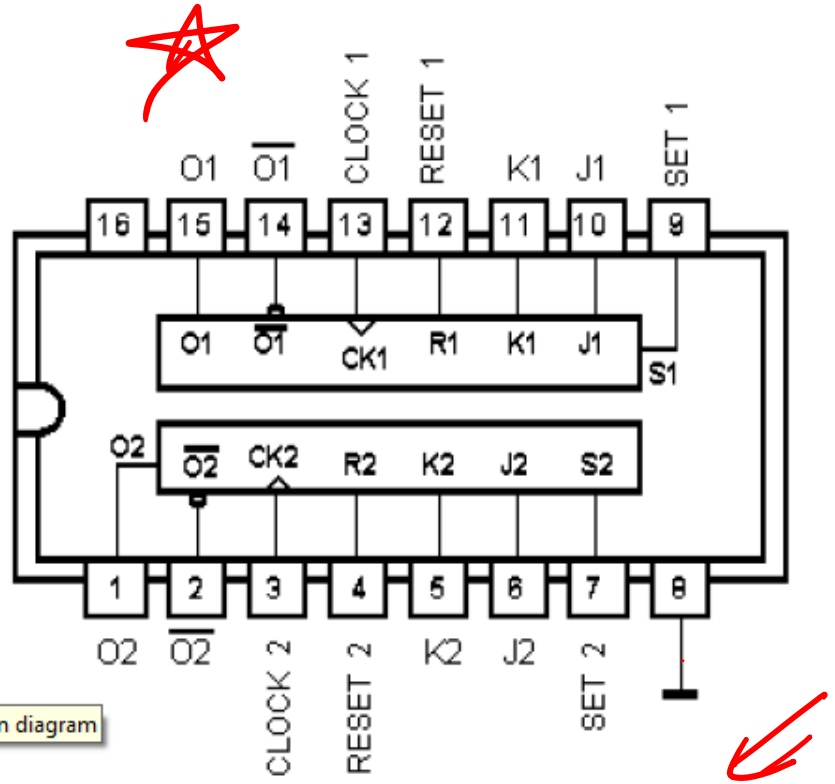


Image result for 4027 ic pin diagram

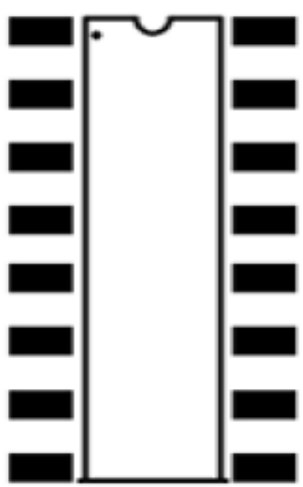


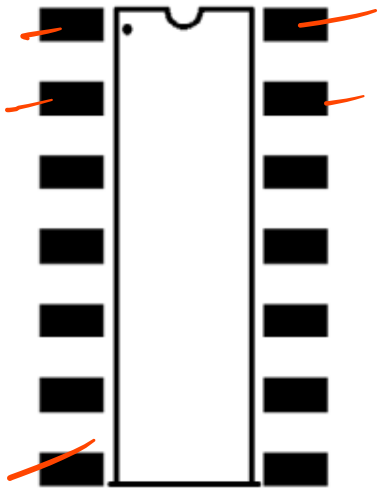
Pin configuration of IC 7476

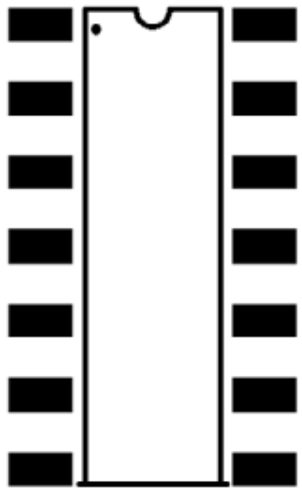
Pin configuration of IC 4027

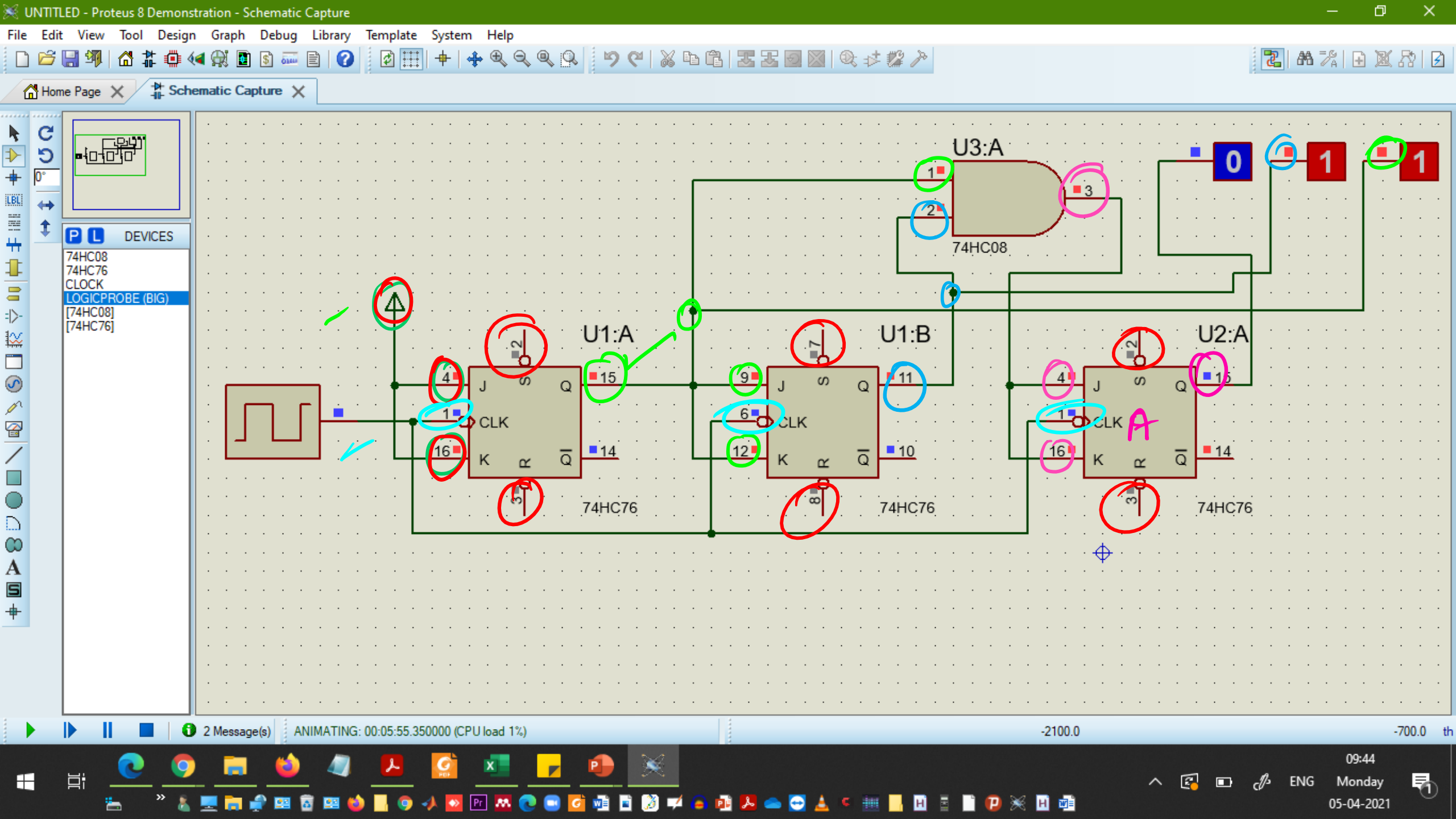
6. Learning Outcomes: Student will be able to design counter using flip flop.

Pin configuration of ICs:








UNTITLED - Proteus 8 Demonstration - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Home Page
Schematic Capture
DEVICES
74HC08
74HC76
CLOCK
LOGICPROBE (BIG)
[74HC08]
[74HC76]
U3:A
74HC08
U1:A
U1:B
U2:A
74HC76
74HC76
74HC76
J
K
CLK
S
R
Q
QI
0
1
1
2 Message(s)
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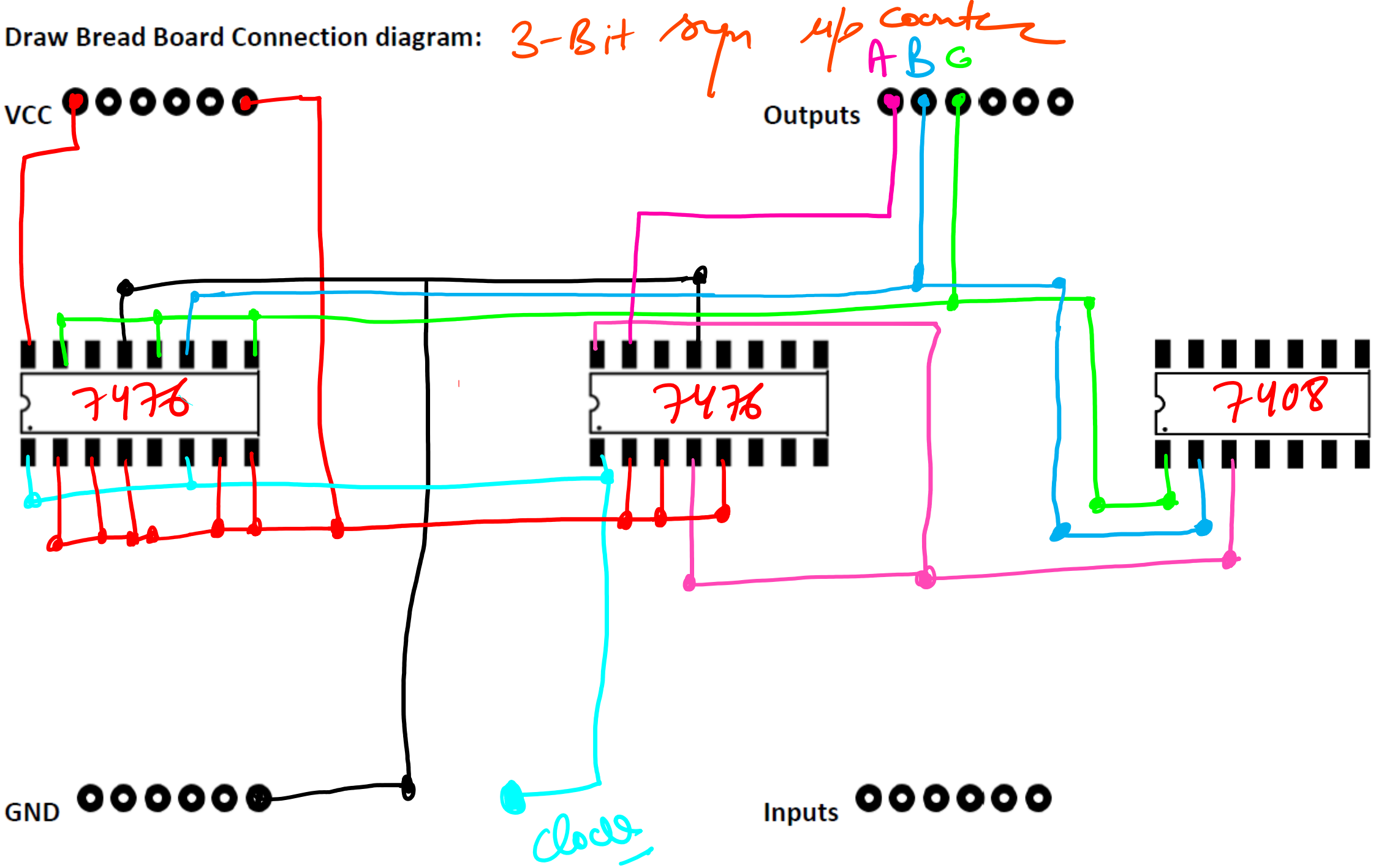
-700.0
09:44
Monday
05-04-2021
ENG

Draw Bread Board Connection diagram:



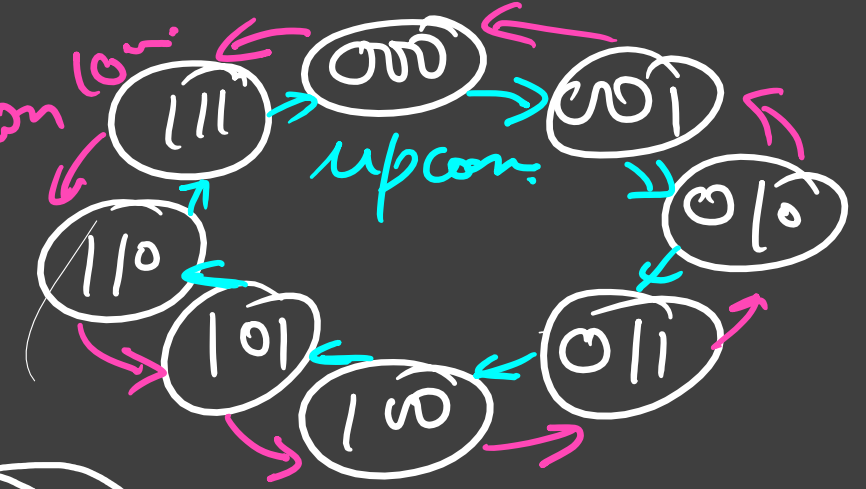
★ Design the up counter (3-bit syn ~~up~~ Down)

Step1 Define the no. of flip flop. (3) ABC

Step2 Type of FF, T-FF

Note: If J = K = 1, then JK FF act as T flip flop

Step3. State diagram, State table



Excitation table of FF

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

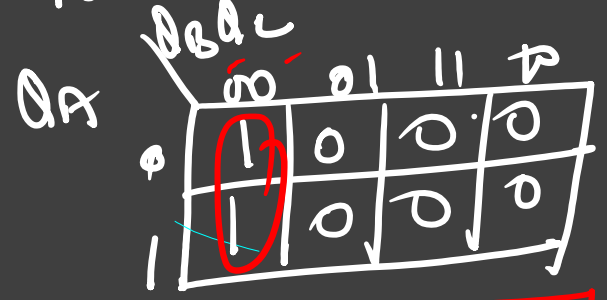
No change → 0, Toggle → 1

Order → ★ State table

Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	T_A	T_B	T_C
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	0	0	1
1	0	0	0	1	1	1	1	1
1	0	1	1	0	0	0	0	1
1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	0	0	1

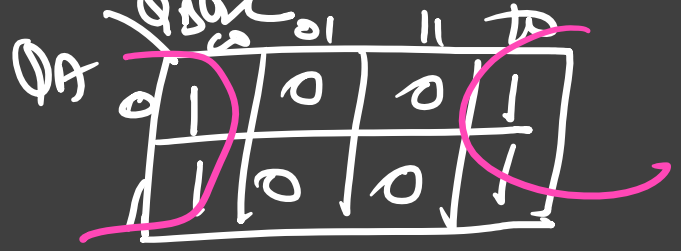
Step 2: solve for Boolean eq.

for T_A



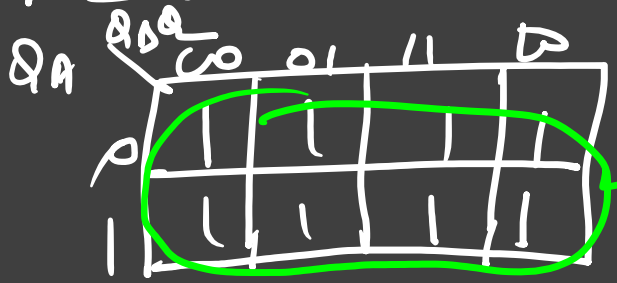
$$T_A = \overline{Q_B}\,\overline{Q_C}$$

for T_B



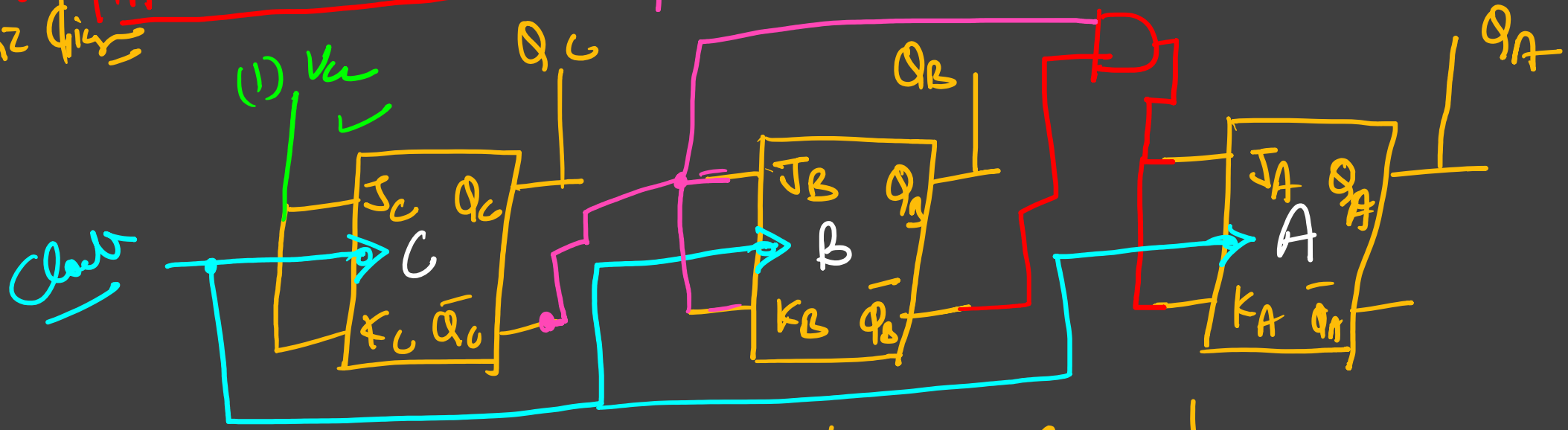
$$T_B = \overline{Q_C}$$

for T_C

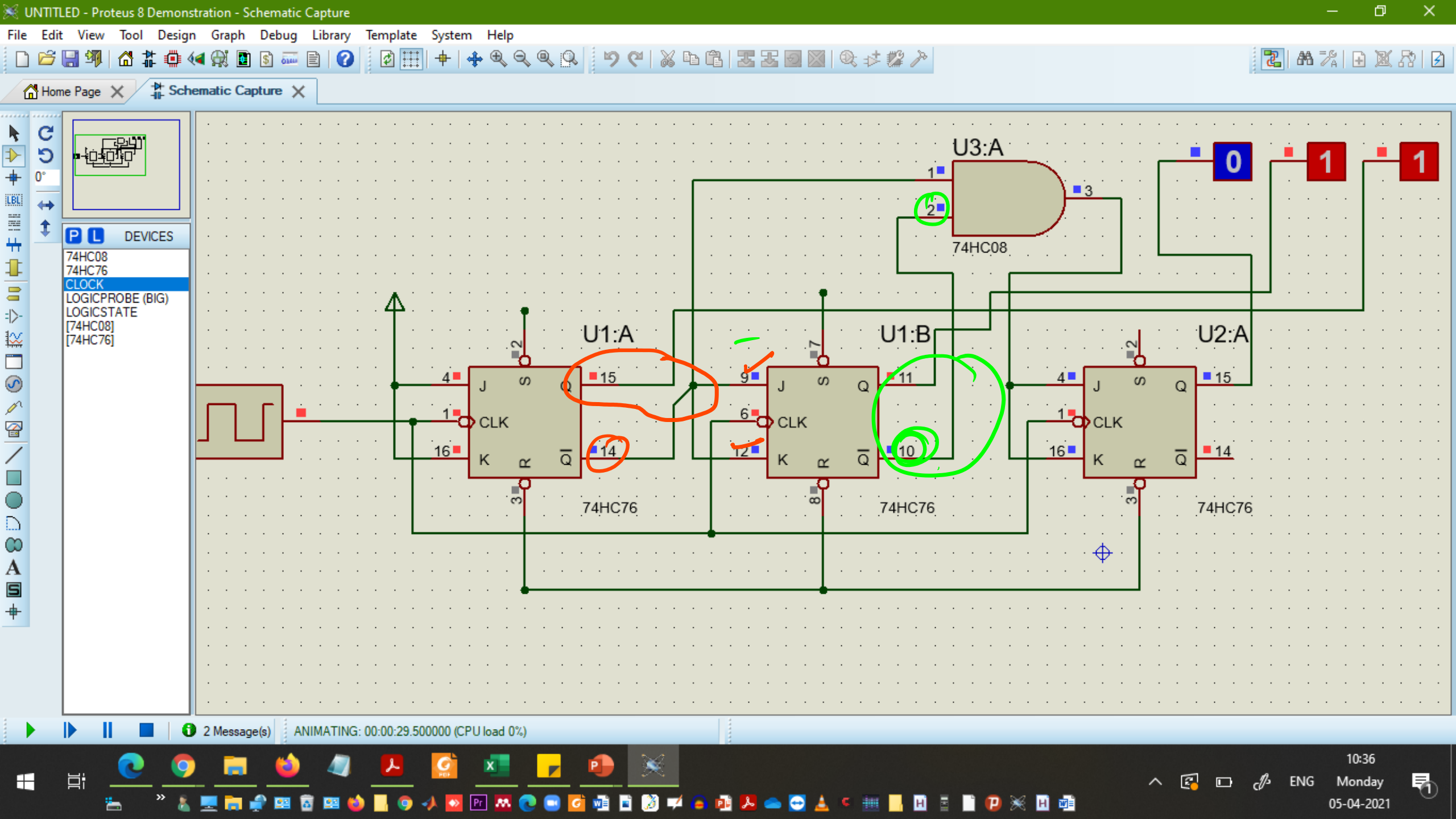


$$T_C = 1$$

Logic diagram



3-bit synchronous counter


UNTITLED - Proteus 8 Demonstration - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Home Page
Schematic Capture
DEVICES
74HC08
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CLOCK
LOGICPROBE (BIG)
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[74HC08]
[74HC76]
U3:A
74HC08
U1:A
U1:B
U2:A
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K
R
QI
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2 Message(s)
ANIMATING: 00:00:29.500000 (CPU load 0%)
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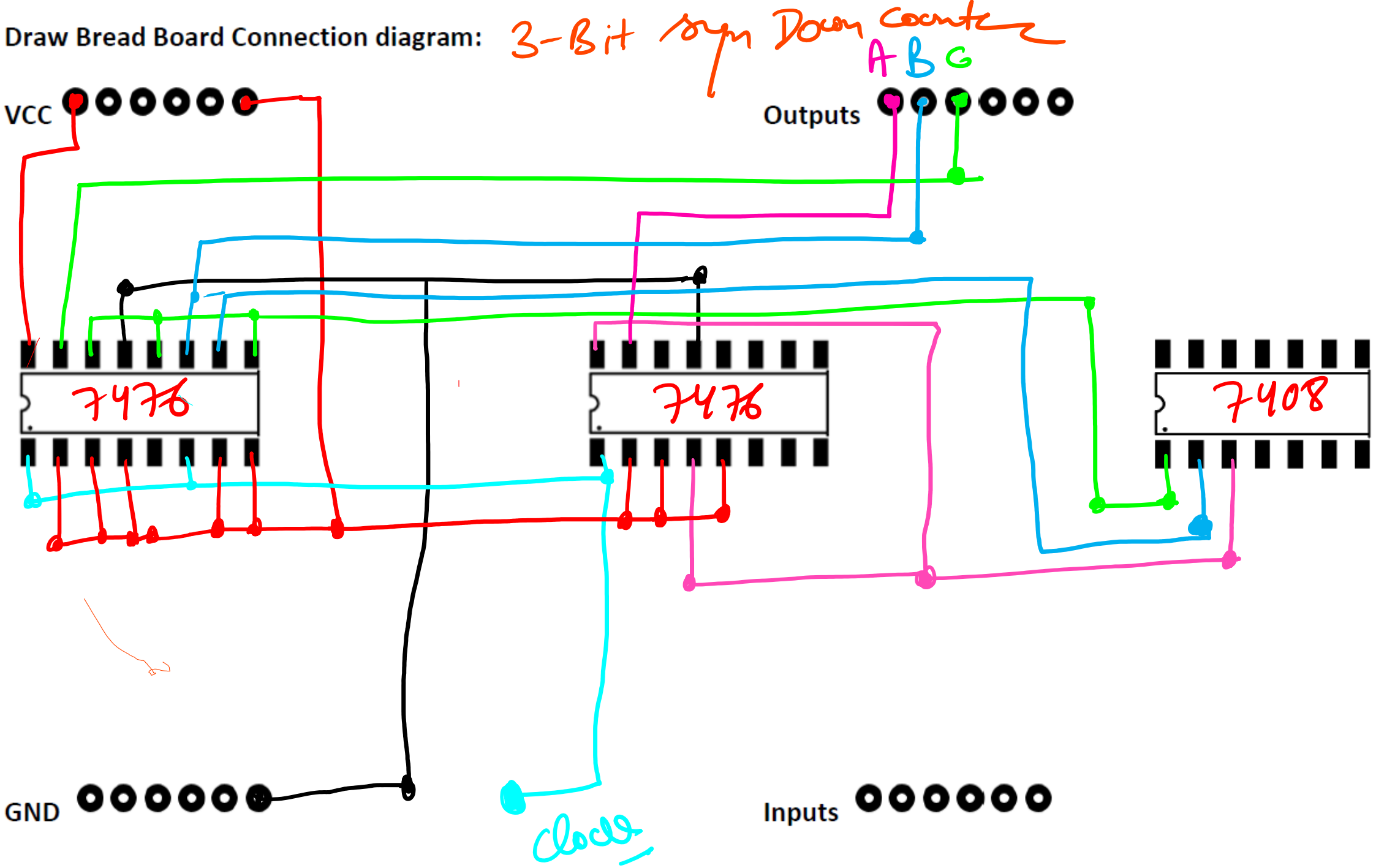
Monday
05-04-2021
ENG

Draw Bread Board Connection diagram:



Next week (12 April 2021)

CA3 — Syllabus Exp 5 on Exp 6

JK
SR
D
T

3-bit up
3-bit Down
4-bit up
4-bit down
2- bit up
2- bit down

7476 or 7022

10 marks for counter up (20 Min)
10 marks for simulation (20 Min)
10 marks for oral/ Short answer (15-20 Min)
and effort