

ECE216: Digital Electronics Laboratory

Exp -5

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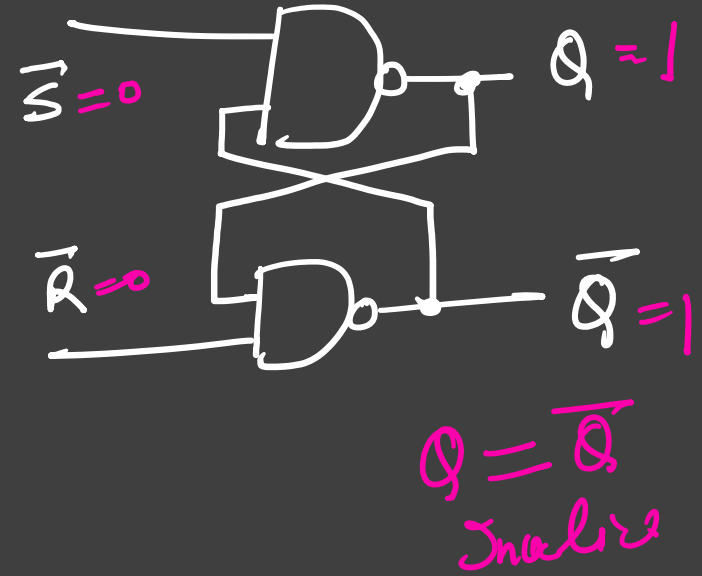
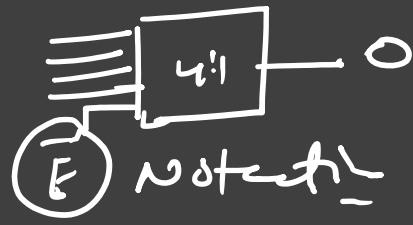
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Exps JK flip flop

- SR Latch (NOR)

	<u>S</u>	<u>R</u>	Q	\bar{Q}	
<u>A</u>	0	0	Q	\bar{Q}	memory
<u>B</u>	0	1	0	1	Reset ✓
<u>C</u>	1	0	1	0	Set ✓
<u>D</u>	1	1	-	-	Invalid ✓

- SR (NAND) Latch



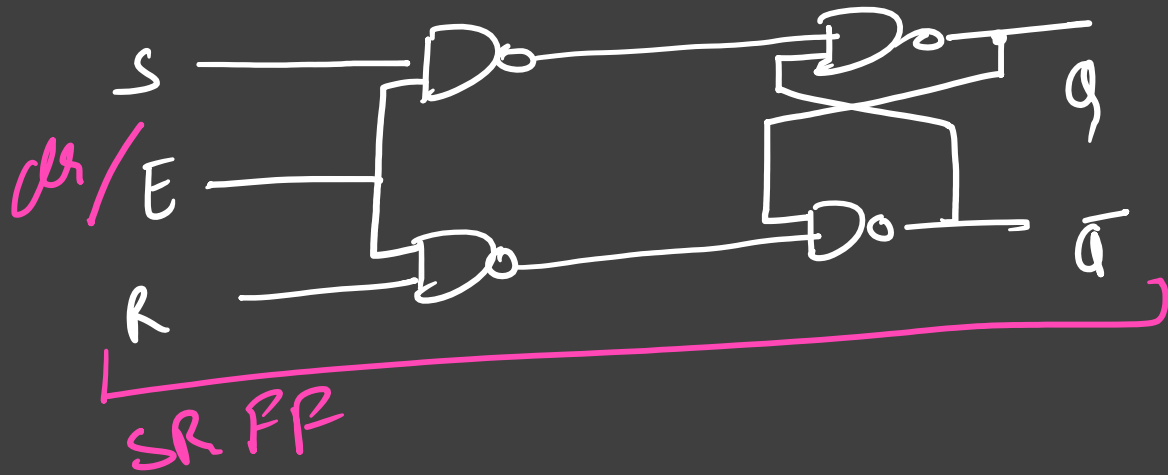
Active high SR Latch (NOR)

Active low SR Latch (NAND)

✓ 1) if any i/p is low, the o/p is high
 ✓ 2) if any i/p is high, the o/p is the complement of 2nd i/p.

A	B	Y
0	0	1
0	1	1 ✓
1	0	1 ✓
1	1	0

★ Gate SR Latch



- ① $E = 0$, in No change condition
- ② $E = 1$, work as SR Latch.

Q. Differ in Latch or FF

A. 1st

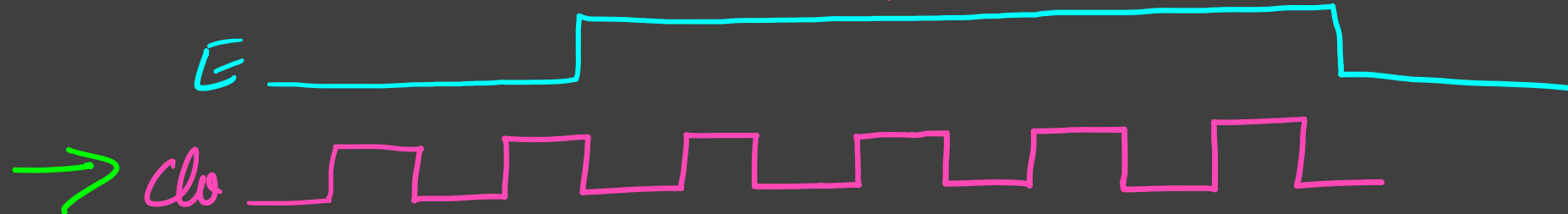
latch $\begin{cases} -V_{cc} & \text{level} \\ +V_{cc} & \text{level} \end{cases}$

FF. $\begin{cases} -V_{cc} & \text{edge} \\ +V_{cc} & \text{edge} \end{cases}$

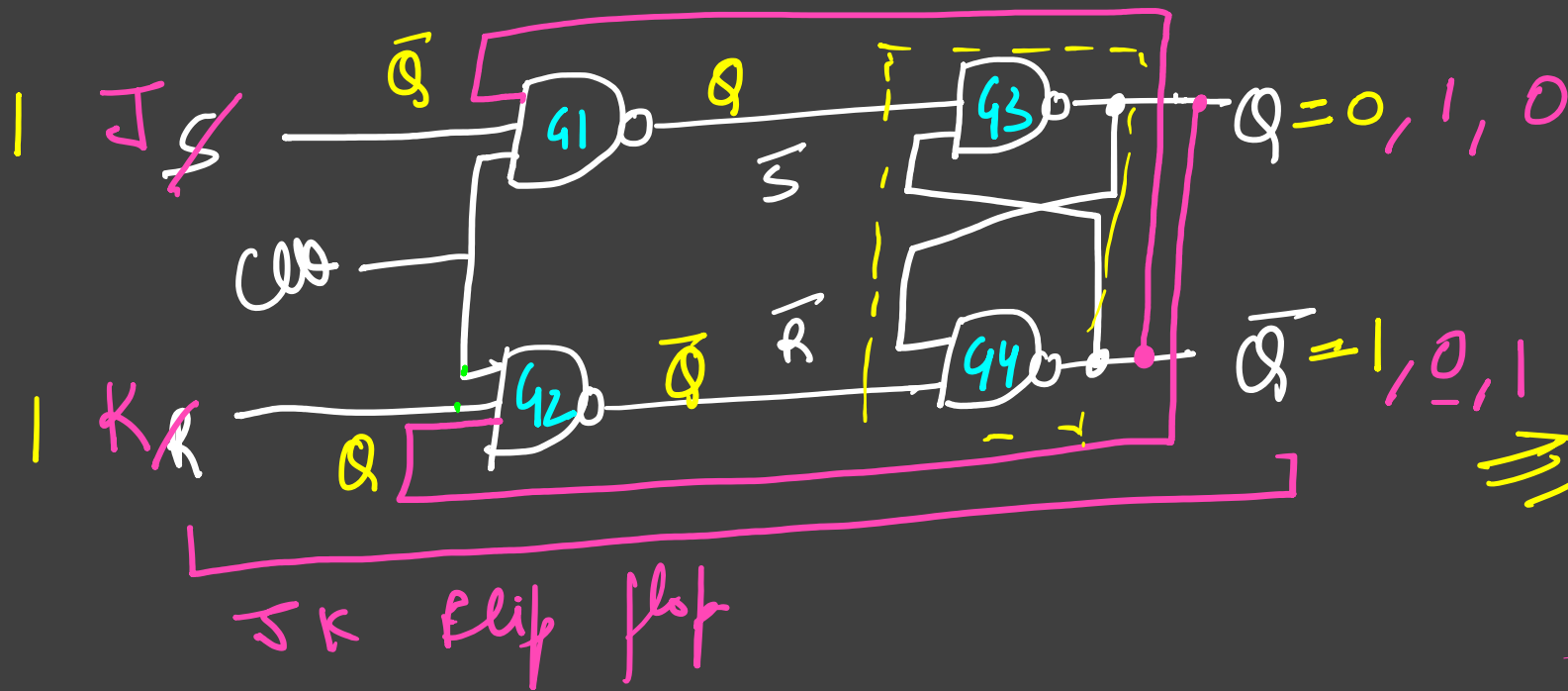
2nd

Enable Signal (latch)

Clock Signal (FF.)



JK Flip flop



J	K	Q	\bar{Q}
0	0	Q	\bar{Q}
0	1	0	1
1	0	1	0
1	1	\bar{Q}	Q

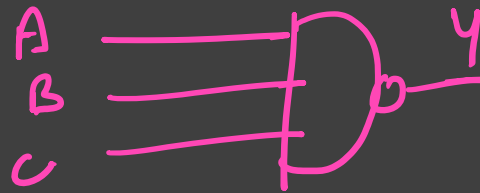
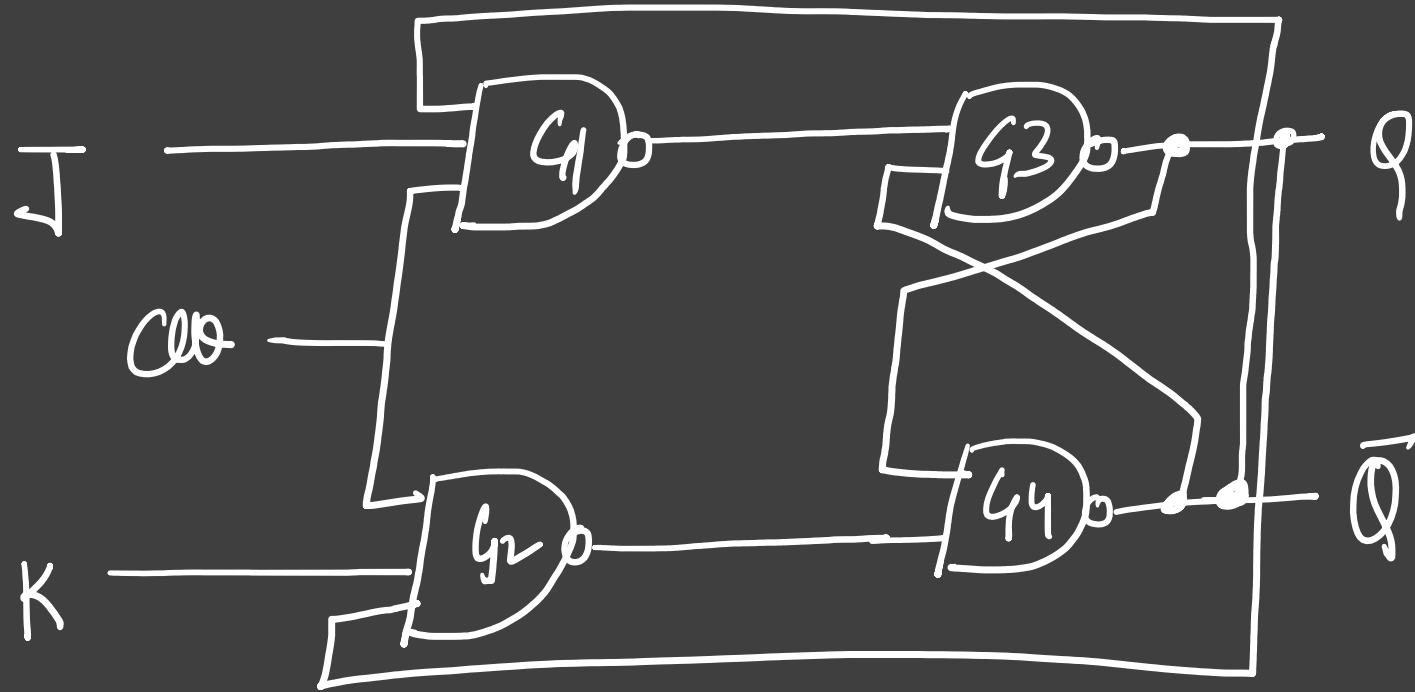
no change
Reset
Set
Toggle

S	R	Q	\bar{Q}
1	0	1	0
0	1	0	1

1) If any 1/p is low, o/p is high
 2) If any 2-1/p's are high, the o/p is the complement of 3rd i/p

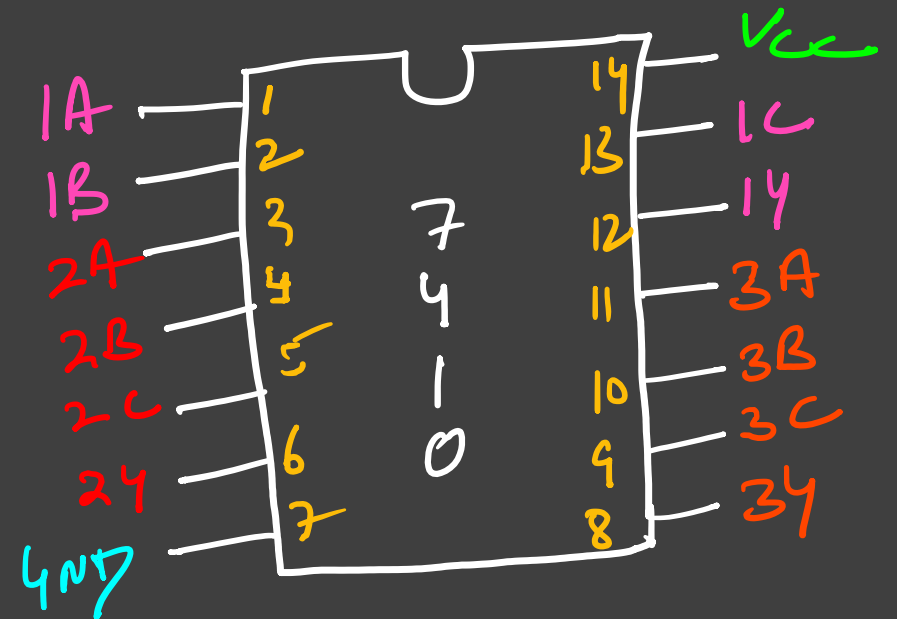
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

★ JK Flip flop



IC 7400 (2-input
NAND Gate)
for G3, G4,

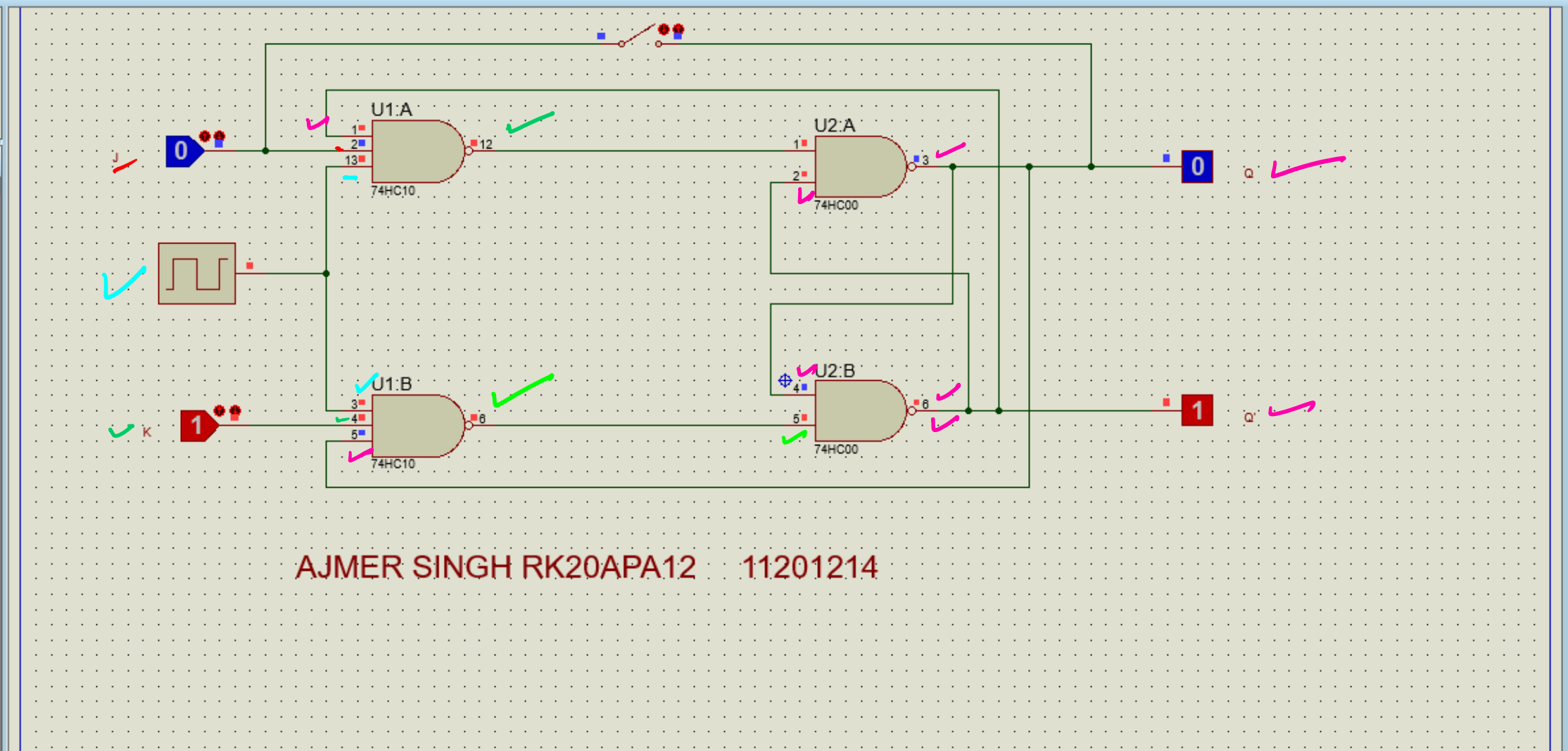
IC 7410 (3-input
NAND Gate)
for G1, G2,



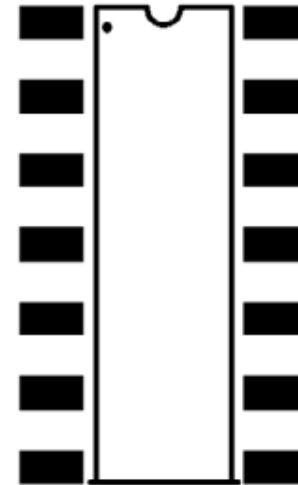
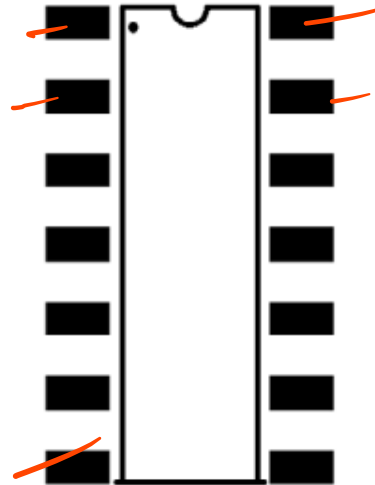
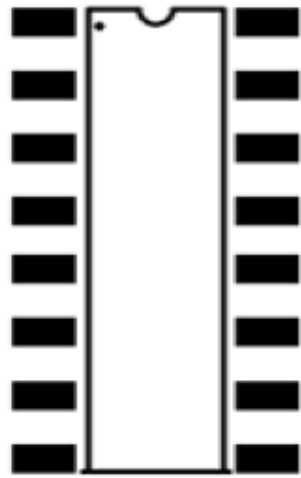
GRAPHICS

COMPONENT

- PIN
- PORT
- MARKER
- ACTUATOR
- INDICATOR
- VPROBE
- IPROBE
- TAPE
- GENERATOR
- TERMINAL
- SUBCIRCUIT
- 2D GRAPHIC
- WIRE DOT
- WIRE
- BUS WIRE
- BORDER
- TEMPLATE

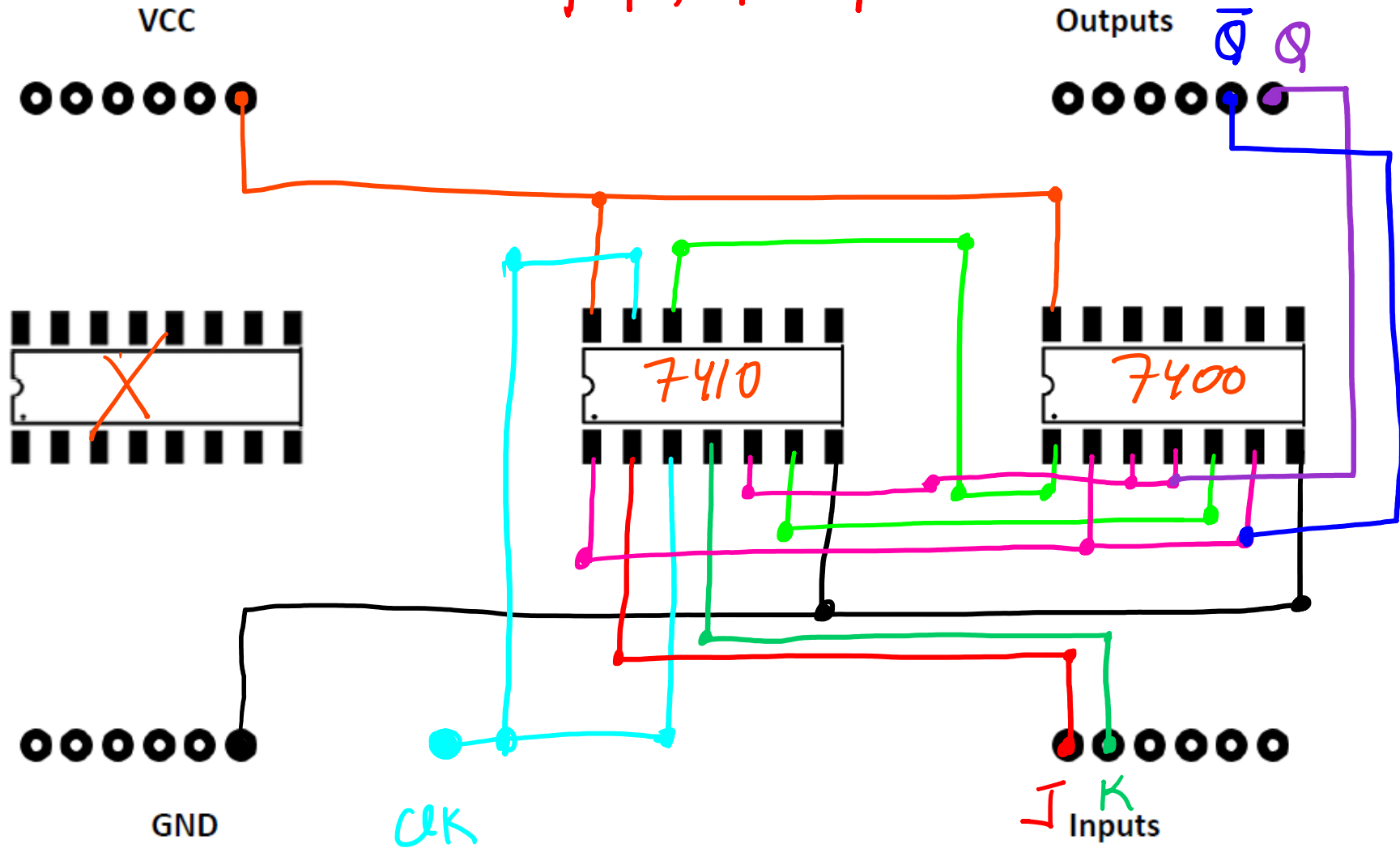


Pin configuration of ICs:



Draw Bread Board Connection diagram:

JK flip flop using Gates. (7410, 7400)



Q: In the Given Circuit, at what value of S & R the circuit shows invalid state

<u>A</u>	<u>S</u>	<u>R</u>
✓ A	0	0
B	0	1
C	1	0

D	1	1
---	---	---

No choice

