ECE213: Digital Electronics

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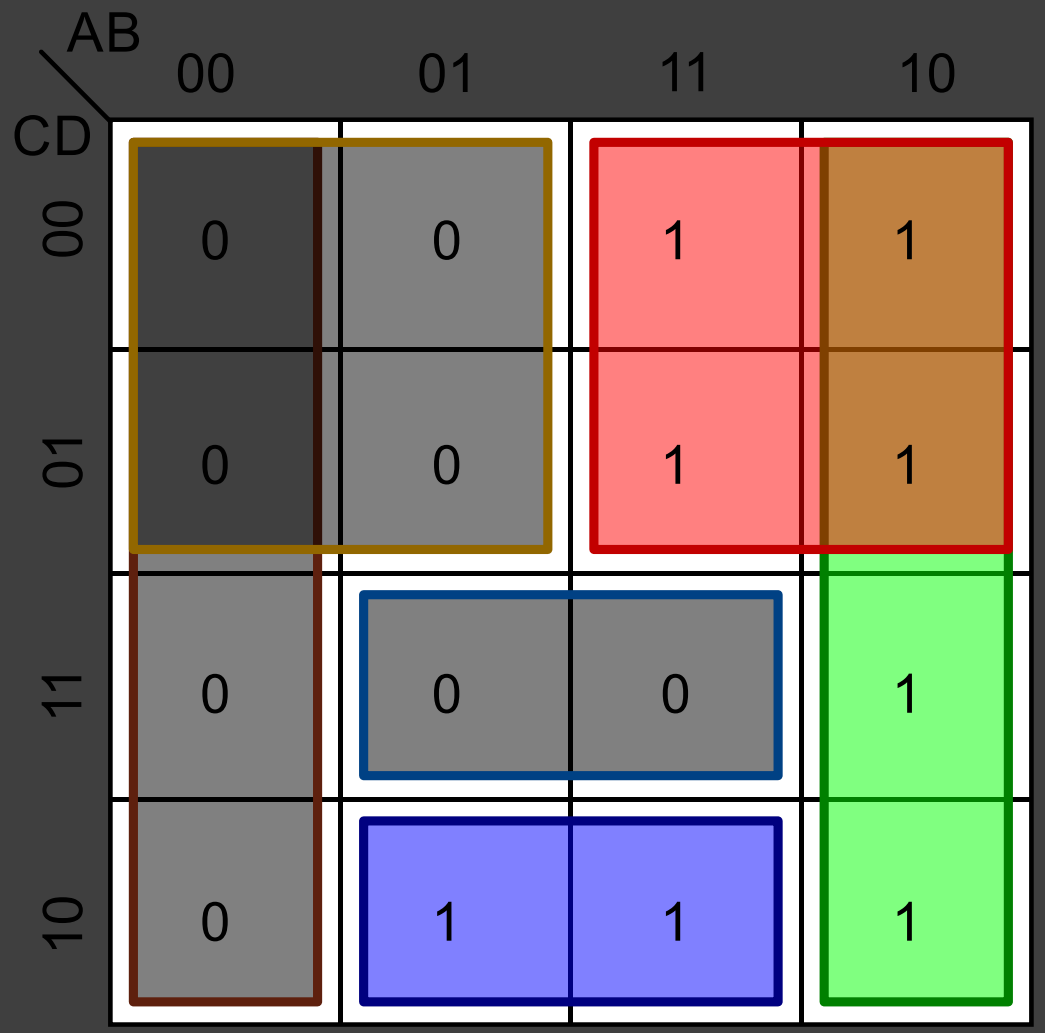
The Course Contents

Unit II

Combinational Logic System : Truth table, Basic logic operation, Boolean Algebra, Basic postulates, Standard representation of logic functions -SOP forms, Simplification of switching functions - K-map, Synthesis of combinational logic circuits, Logic gates, Fundamental theorems of Boolean algebra, Standard representation of logic functions POS forms

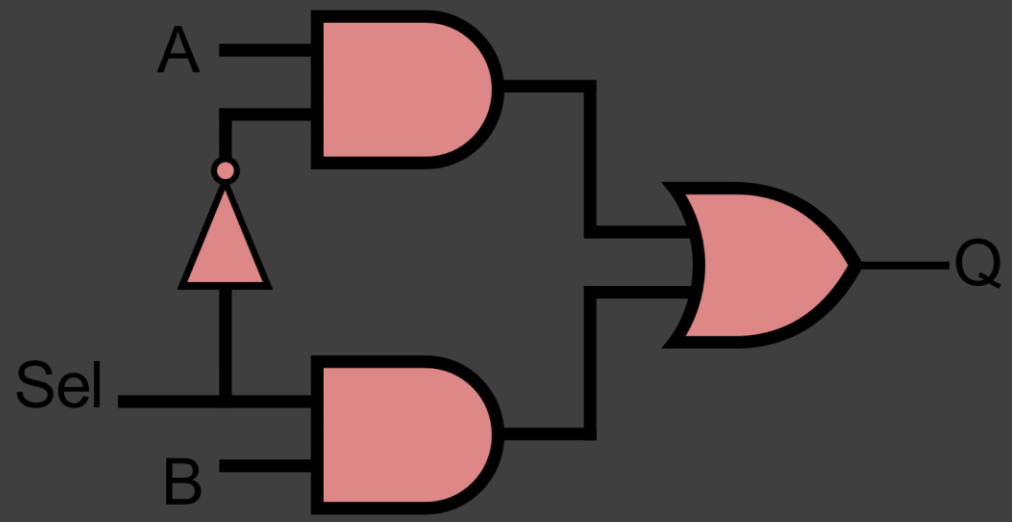


The Course Contents

Unit III

Introduction to Combinational Logic Circuits : Adders, Subtractors, Comparators, Multiplexers and Demultiplexers, Decoders, Encoders, Parity circuits

Introduction to Logic Families : Introduction to different logic families, Structure and operations of TTL, MOS and CMOS logic families



Combinational Logic System

Multiplexers and Demultiplexers

2:1 Mux

No. of I/P 2

No. of O/P 1

No. of Sel. lines 1

As the no. i/p width 3-inputs

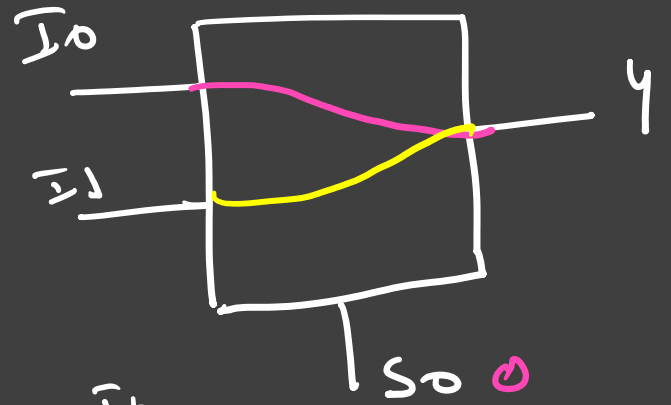
Multi $2^n : 1$

$n=1$	2:1
$n=2$	4:1
$n=3$	8:1
$n=4$	16:1

2^6

2^{11}

S_0	I_1	I_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



Y	$\bar{I}_1 I_0$	01	11	I_0
$\bar{S}_0$	0	1	1	0
S_0	0	0	1	1

$$Y = \bar{S}_0 I_0 + S_0 I_1$$

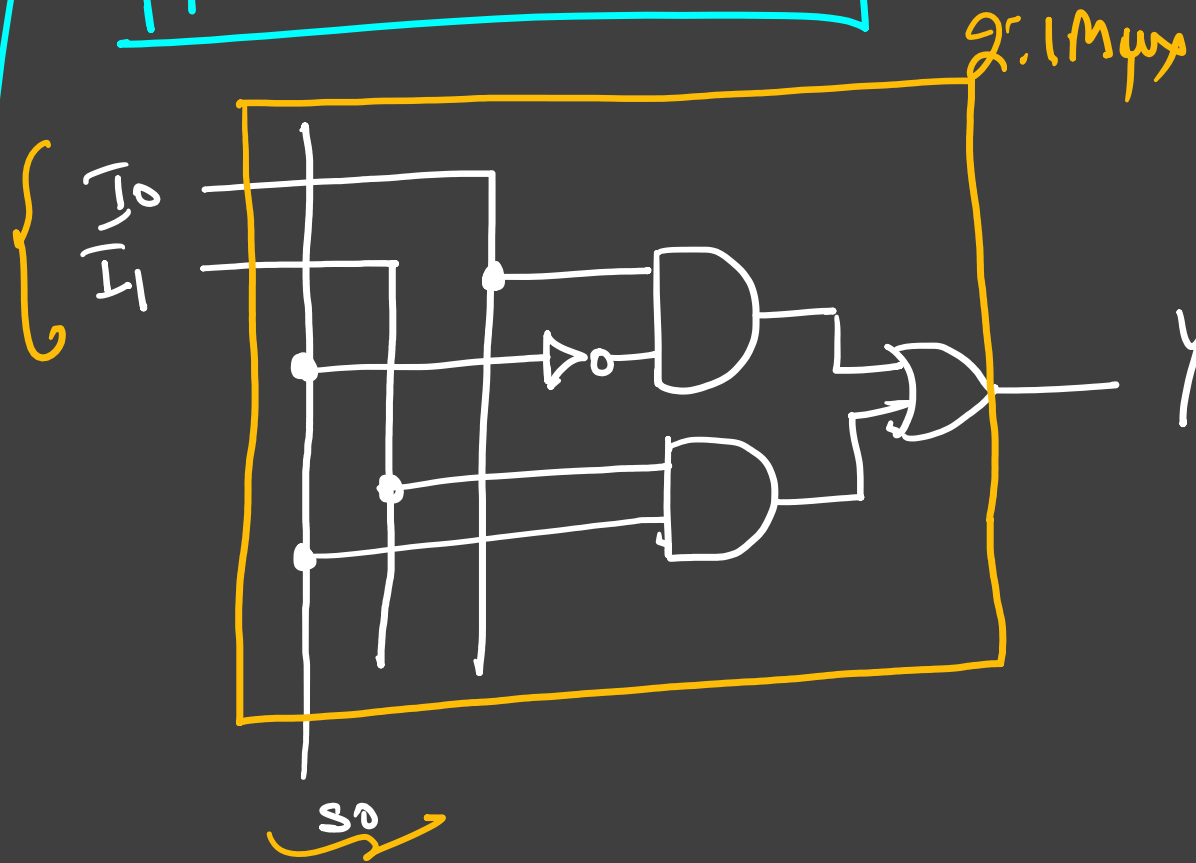
Combinational Logic System

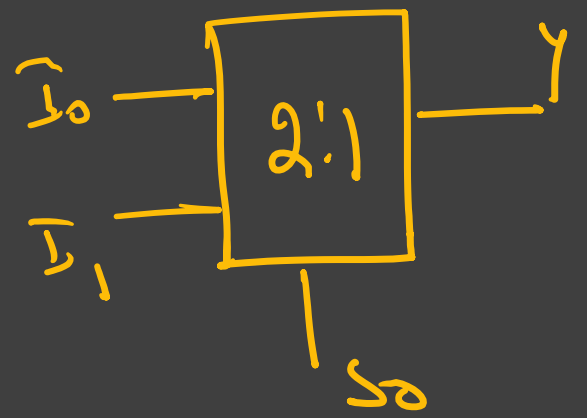
Multiplexers and Demultiplexers

2:1 Mux

S_0	Y
0	I_0
1	I_1

$$Y = \bar{S_0} I_0 + S_0 I_1$$





Combinational Logic System

Multiplexers and Demultiplexers

4:1 Mux

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

Q.1 Logic circuit of 4:1 Mux using the basic gates

Combinational Logic System

Multiplexers and Demultiplexers

★ **8:1 Mux**

$$Y = \bar{S}_2\bar{S}_1\bar{S}_0 I_0 + \bar{S}_2\bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3$$

$$+ S_2\bar{S}_1\bar{S}_0 I_4 + S_2\bar{S}_1 S_0 I_5 + S_2 S_1 \bar{S}_0 I_6 + S_2 S_1 S_0 I_7$$

★ **16:1 Mux**

Combinational Logic System

Multiplexers and Demultiplexers

A 32:1 Mux

Combinational Logic System

Mux Tree use to b make the large size of Mux using small size of Mux.

Ex: Design the 4:1 Mux using 2:1 Mux

Sol: Step1: Find the no of I/Ps in req Mux

$N_R = 4$

Step2: Find the no of I/P in avail Mux

$N_A = 2$

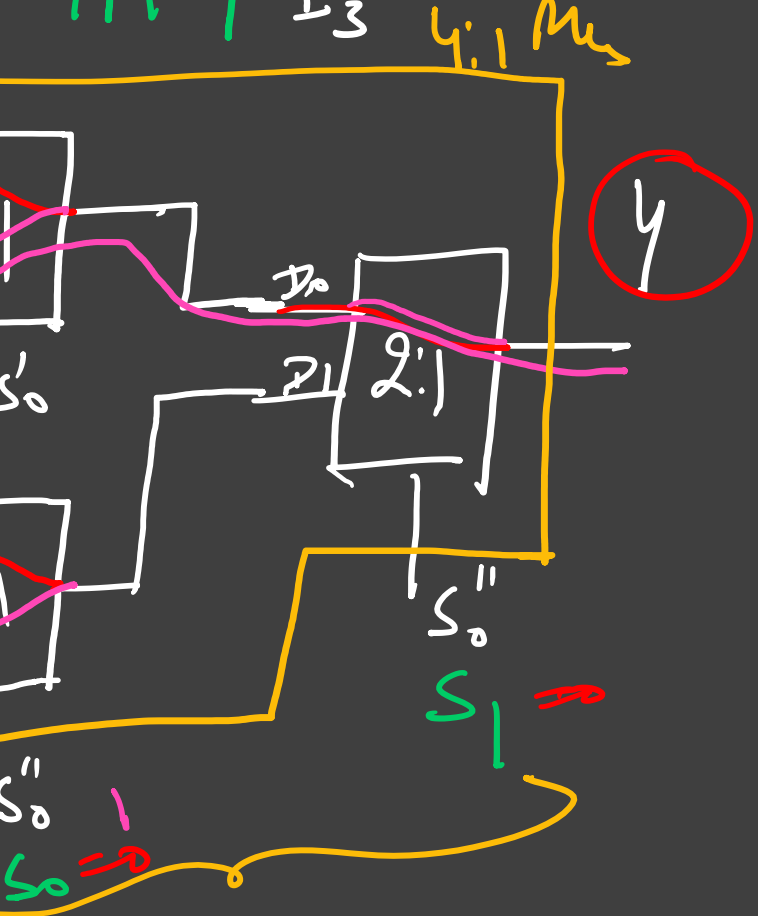
Step3: Find the Num/Den.

$\frac{N_R}{N_A} = \frac{4}{2} = 2$

$\frac{2}{2} = \frac{1}{1}$

$\frac{1}{3}$

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



Combinational Logic System

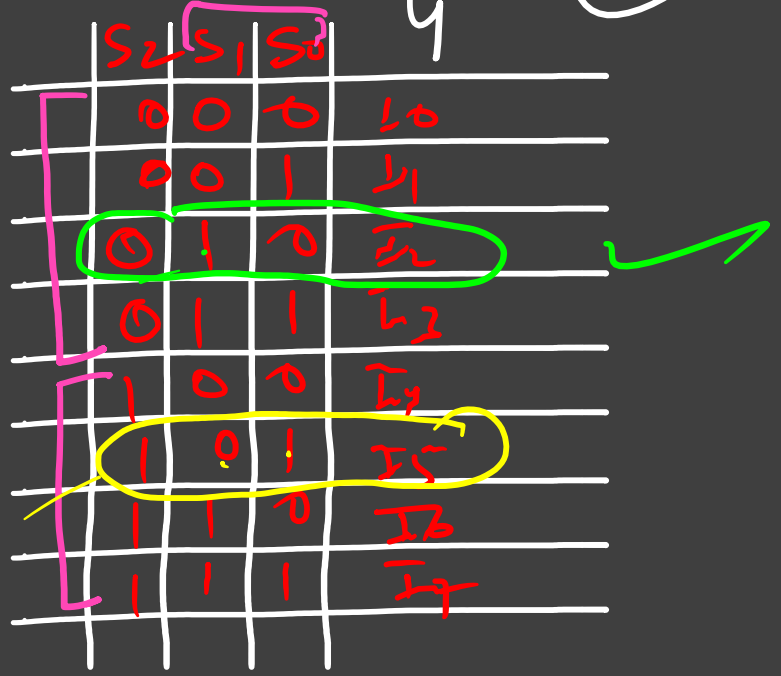
Mux Tree

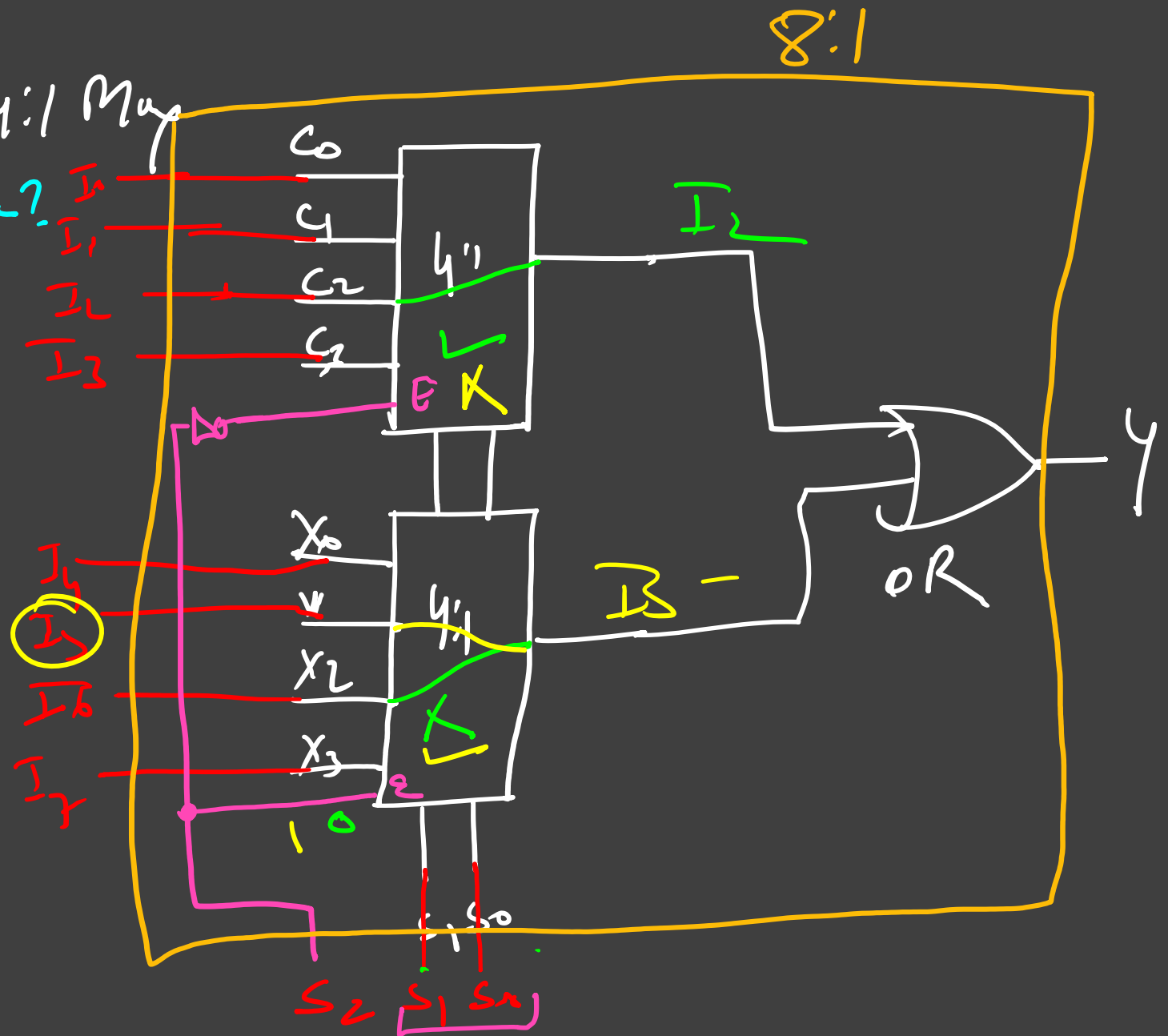
Ex Implement 8:1 Mux using 4:1 Mux

Q How many 4:1 Mux required?

$N_R = 8$; $N_A = 4$

$l_0 = \frac{8}{4} = 2$





Combinational Logic System

Mux Tree

Q How many 2:1 Mux required to implement 16:1 Mux,

A:

A) 4
B) 8
C) 15
D) 16

$N_R = 4$; $N_A = 2$

$\frac{16}{2} = 8$

$\frac{8}{2} = 4$

$\frac{4}{2} = 2$

$\frac{2}{2} = 1$

15 Mux

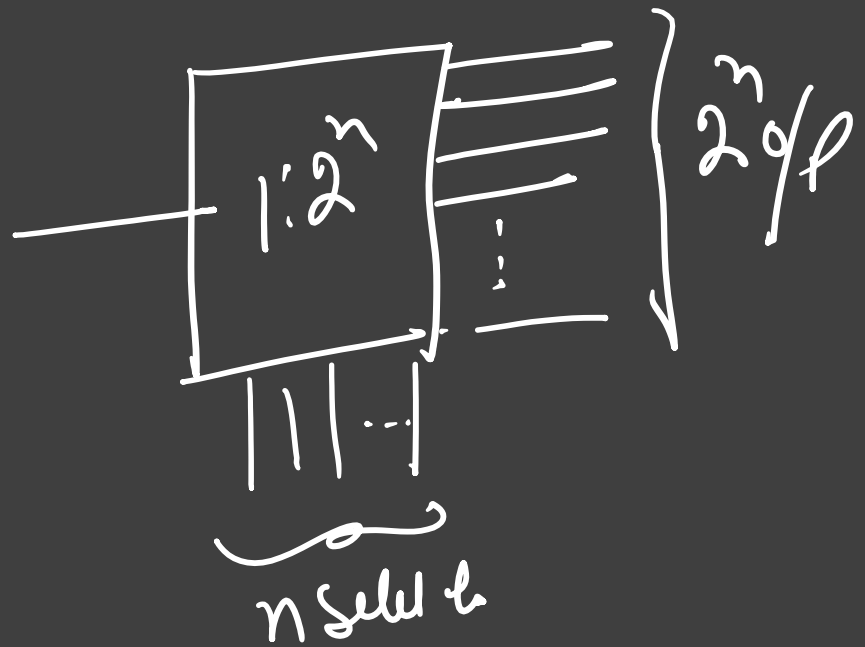
De Mux

1 : 2^n

No. of i/p

No. of o/p

No. of Selection

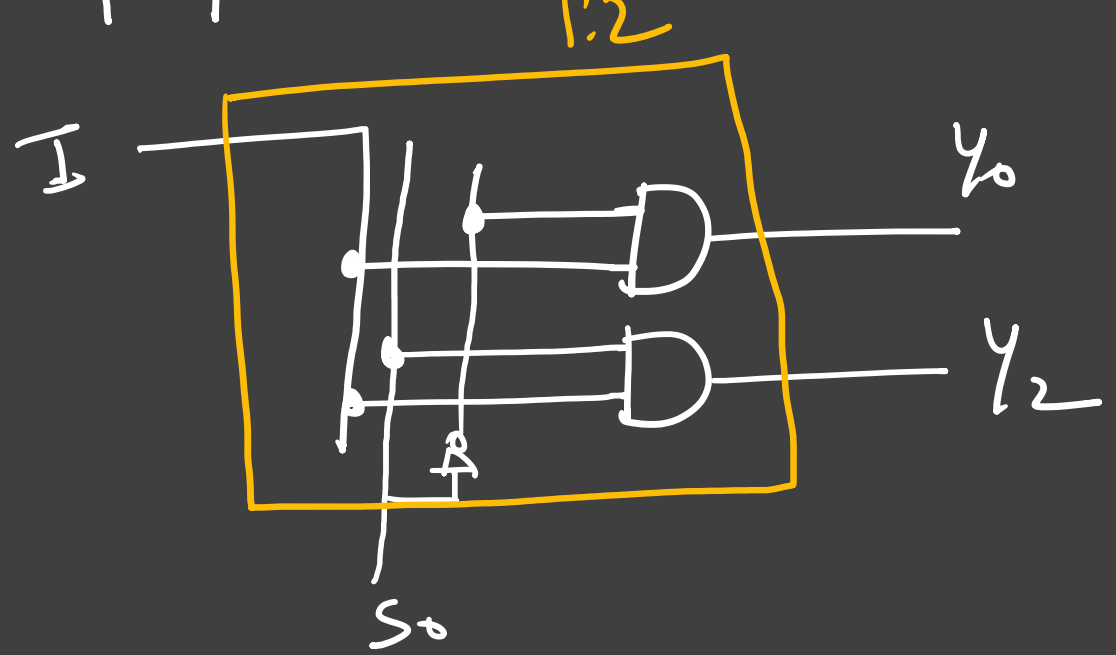


1:2 De Mux

S_0	I	Y_0	Y_1
0	0	0	0
0	1	1	0
1	0	0	0
1	1	0	1

$Y_0 = \overline{S_0}\, I$

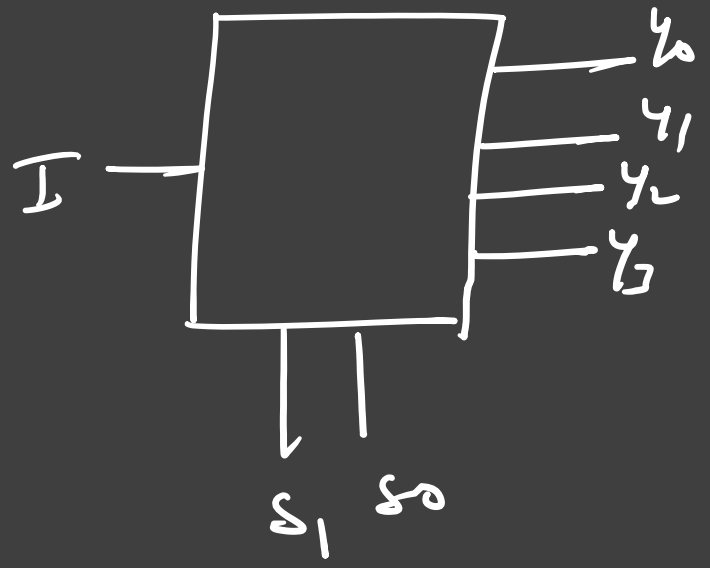
$Y_1 = S_0 I$



1:4 DeMux

S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	I	0	0	0
0	1	0	I	0	0
1	0	0	0	I	0
1	1	0	0	0	I

$$Y_0 = \overline{S_1}\,\overline{S_0}\,I$$
$$Y_1 = \overline{S_1}\,S_0\,I$$
$$Y_2 = S_1\,\overline{S_0}\,I$$
$$Y_3 = S_1\,S_0\,I$$

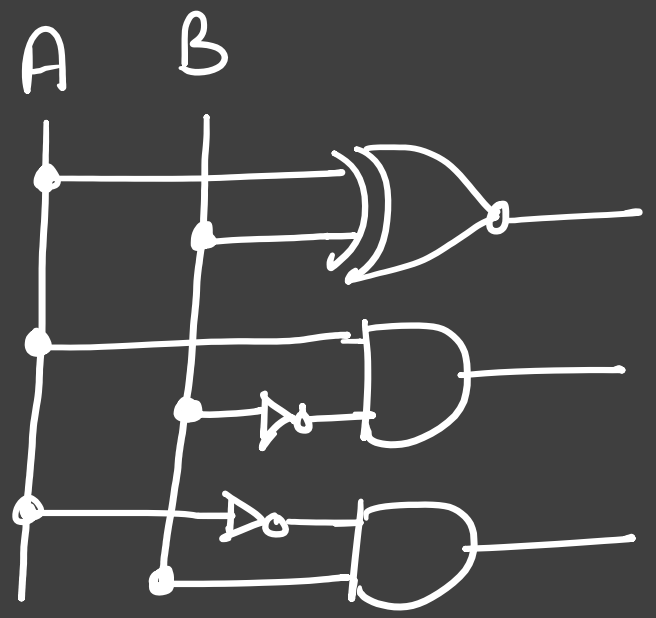


1:8 DeMux

$$Y_0 = \overline{S_2}\,\overline{S_1}\,\overline{S_0}\,I$$
$$Y_1 = \overline{S_2}\,\overline{S_1}\,S_0\,I$$
$$Y_2 = \overline{S_2}\,S_1\,\overline{S_0}\,I$$
$$Y_3 = \overline{S_2}\,S_1\,S_0\,I$$
$$Y_4 = S_2\,\overline{S_1}\,\overline{S_0}\,I$$
$$Y_5 = S_2\,\overline{S_1}\,S_0\,I$$
$$Y_6 = S_2\,S_1\,\overline{S_0}\,I$$
$$Y_7 = S_2\,S_1\,S_0\,I$$

Comparators : ☆ 1-bit Comparator

A	B	Y_1 A=B	Y_2 A>B	Y_3 A<B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0



$Y_1 (A=B)$

$Y_2 (A>B)$

$Y_3 (A<B)$

$$Y_1 = \bar{A}\bar{B} + AB = A \odot B$$

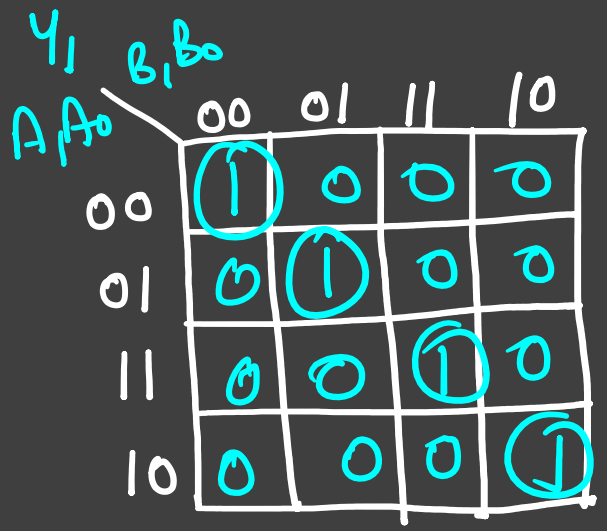
$$Y_2 = A\bar{B}$$

$$Y_3 = \bar{A}B$$

2-bit Comparator

$Y_1 (A=B)$, $Y_2 (A<B)$, $Y_3 (A>B)$

A		B				
A_1	A_0	B_1	B_0	Y_1	Y_2	Y_3
0	0	0	0	1	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	1	0	0
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	1	0	0
1	0	1	1	0	1	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	1	0	0



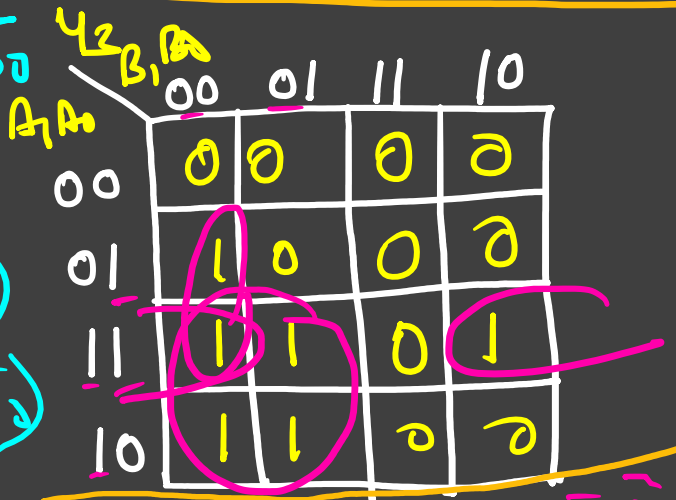
$$Y_1 = \bar{A}_1\bar{A}_0\bar{B}_1\bar{B}_0 + \bar{A}_1A_0\bar{B}_1B_0 + A_1A_0B_1B_0 + A_1\bar{A}_0B_1\bar{B}_0$$

$$= \bar{A}_1\bar{B}_1(\bar{A}_0\bar{B}_0 + A_0B_0) + A_1B_1(A_0B_0 + \bar{A}_0\bar{B}_0)$$

$$= (\bar{A}_1\bar{B}_1 + A_1B_1)(A_0B_0 + \bar{A}_0\bar{B}_0)$$

$$\boxed{Y_1 = \overline{A_1 \oplus B_1}\ \overline{A_0 \oplus B_0}}$$

$$\boxed{Y_2 = \bar{A}_1B_1 + \bar{A}_1\bar{A}_0B_0 + \bar{A}_0B_1B_0}$$



$$\boxed{Y_3 = A_1\bar{B}_1 + A_0\bar{B}_1\bar{B}_0 + A_1A_0\bar{B}_0}$$

★ Parity circuits

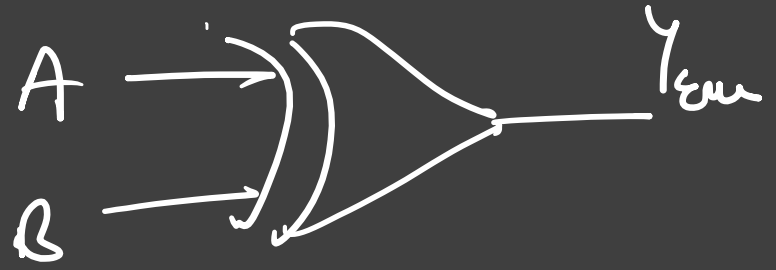
Even / odd

The no of one in the Group should be even/odd for Even Parity / odd Parity

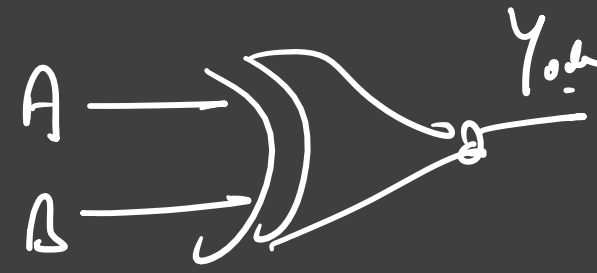
Ex Design 2-bit Parity Generator (Even Parity)

A	B	Y_{even}	Y_{odd}
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

$Y = A \oplus B$



$Y_{odd} = \overline{A \oplus B}$



Parity checker circuit (Combinational)

For 3-bit Parity checker circuit

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$Y = A \oplus B \oplus C$