ECE216: Digital Electronics Laboratory

Exp -5

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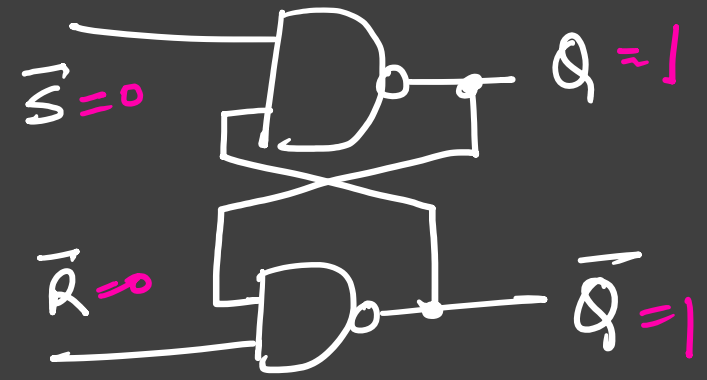
Exps JK flip flop

- SR Latch (NOR)

	S	R	Q	$\bar{Q}$	
A	0	0	Q	$\bar{Q}$	No condi's (Memory)
B	0	1	0	1	Reset
C	1	0	1	0	Set
D	1	1	–	–	Invalid

- Active high SR Latch (NOR)
- Active low SR Latch (NAND)

- SR (NAND) Latch

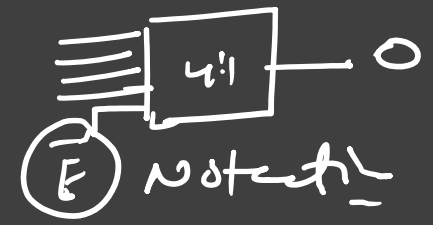


$Q = \bar{Q}$
Invalid

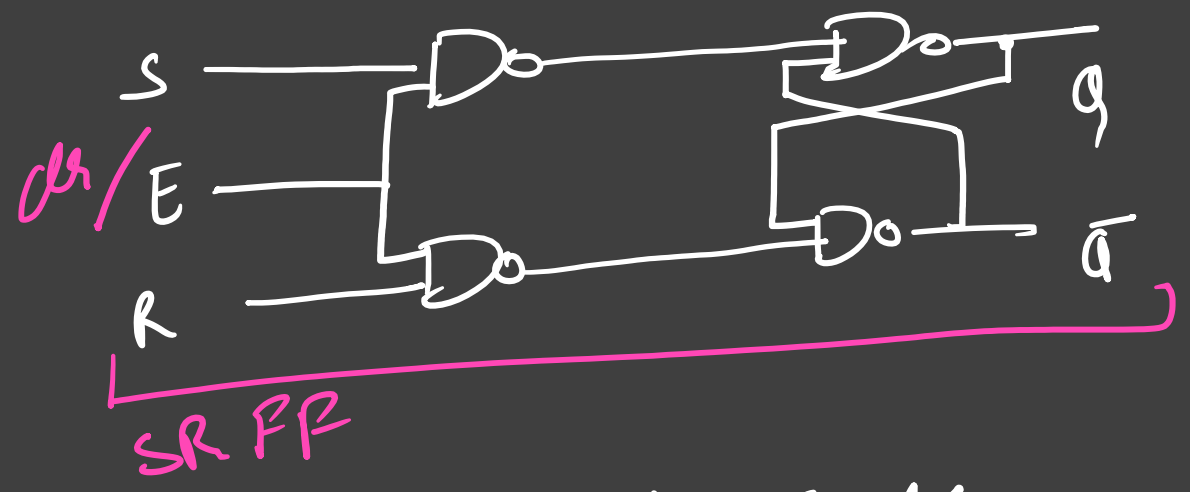
i) If any I/P is low, the o/p is high

ii) If any I/P is high, the o/p is the complement of 2nd i/p.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



☆ Gate SR Latch



- If E = 0, in No change Condition
- If E = 1, work as SR Latch.

Q. Diff in Latch or FF

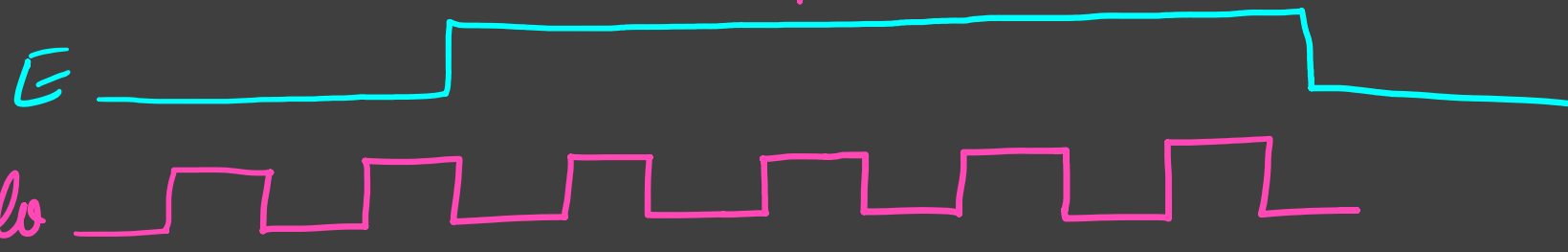
A. 1st

Latch [−ve level, +ve level

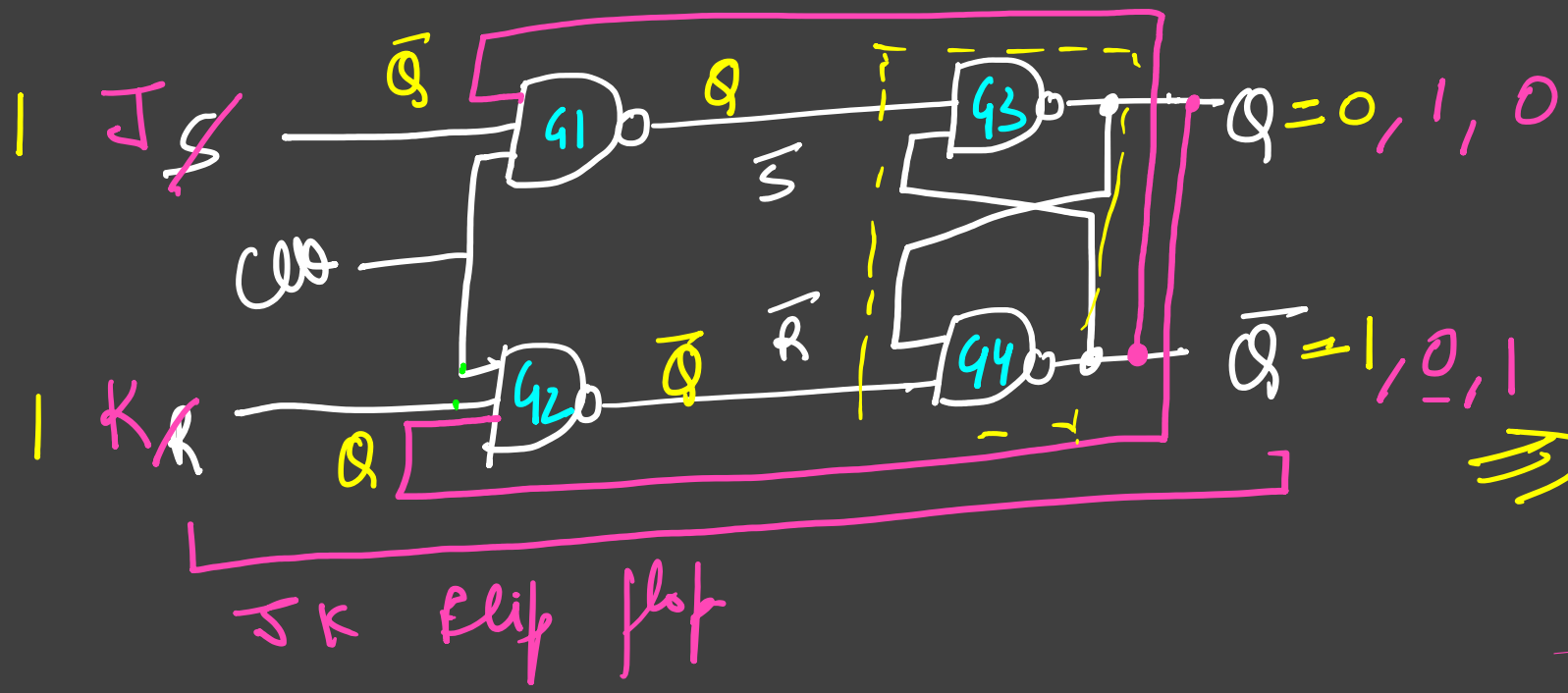
FF. [−ve edge, +ve edge

2nd Enable Signal (Latch)

Clock Signal (F.F.)



★ JK flip flop



JK flip flop

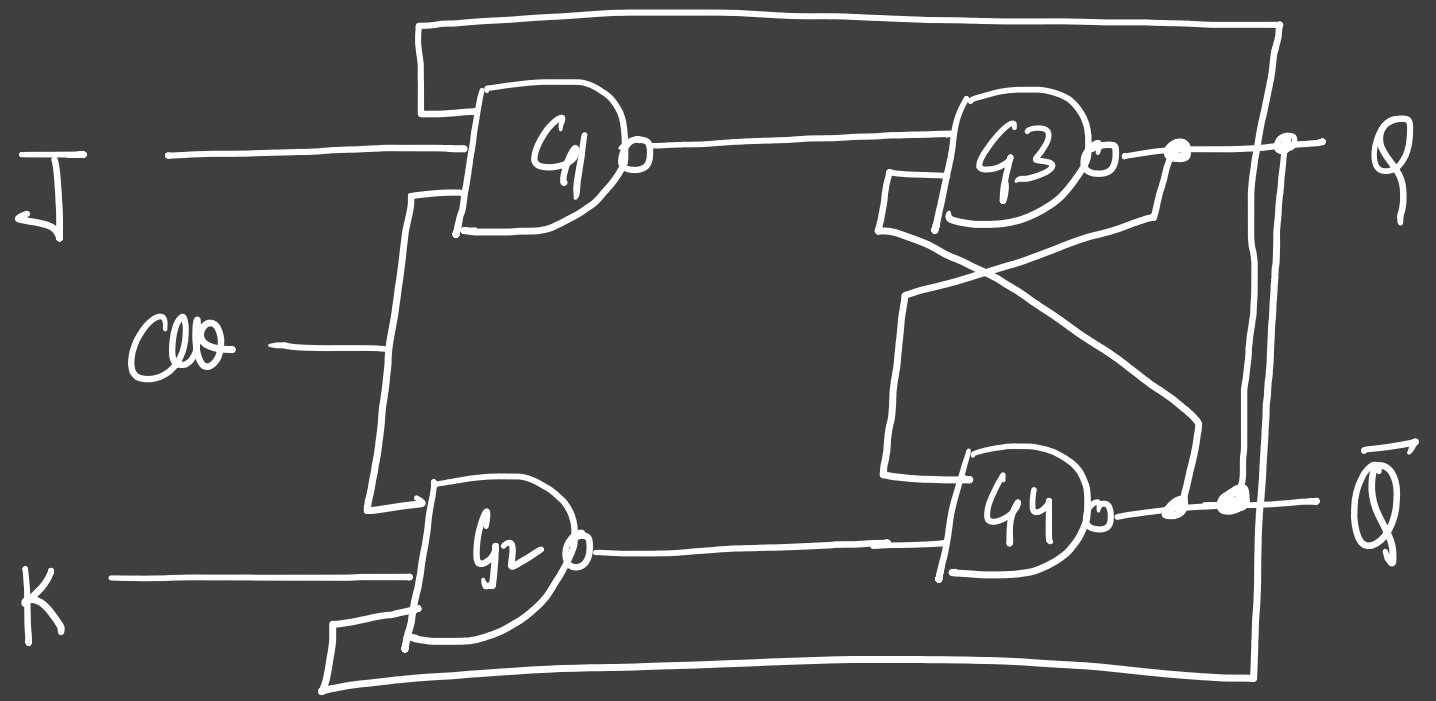
J	K	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	$\bar{Q}$	Q	Toggle

S	R	Q	$\bar{Q}$
1	0	1	0
0	1	0	1

1) If any i/p is low, o/p is high
2) If any 2-i/ps are high, the o/p is the complement of 3rd i/p

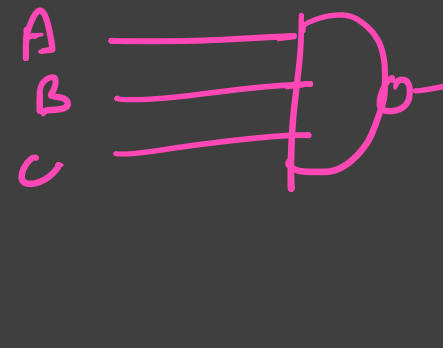
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

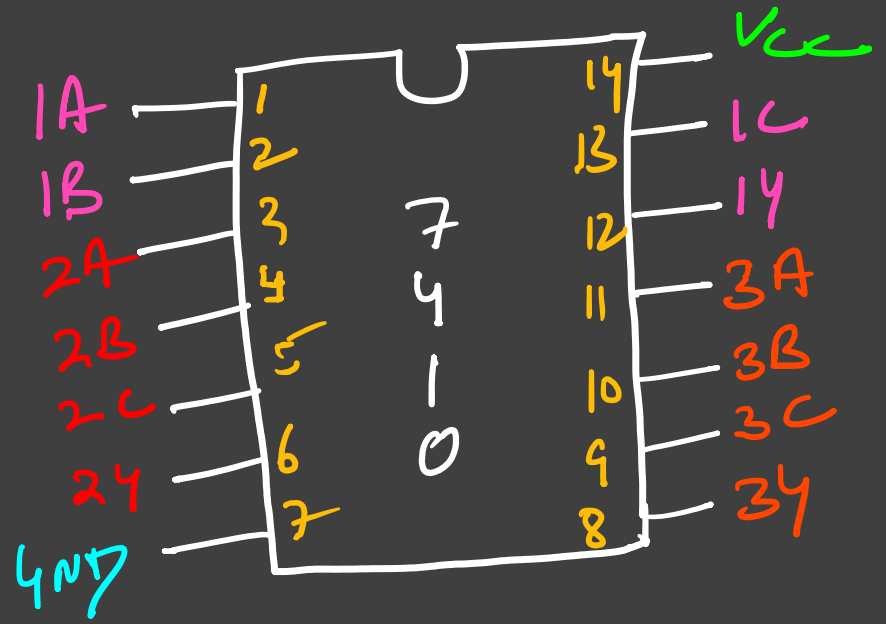
JK flip flop

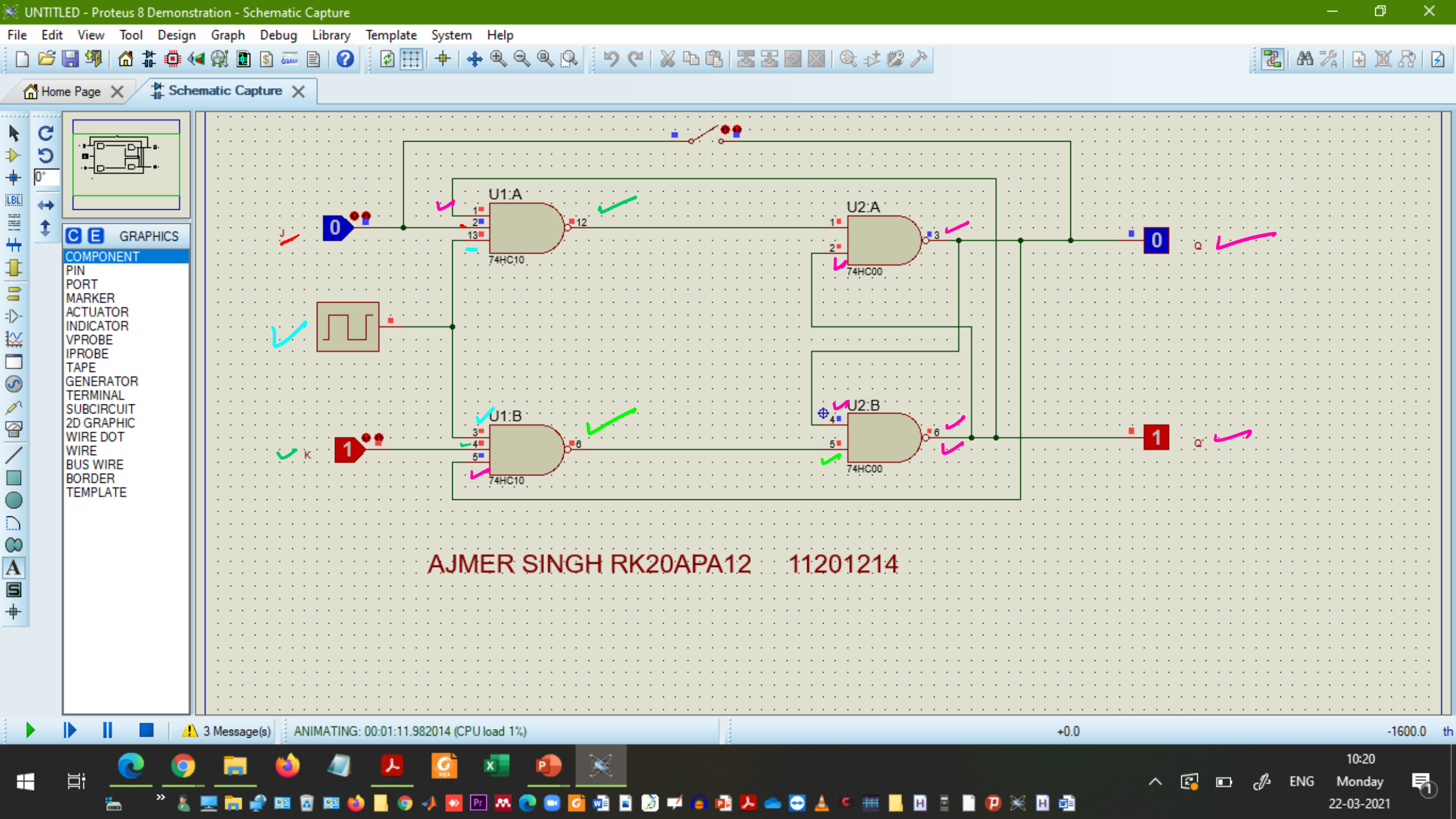


IC 7400 (2-input NAND Gate)
for G3, G4,

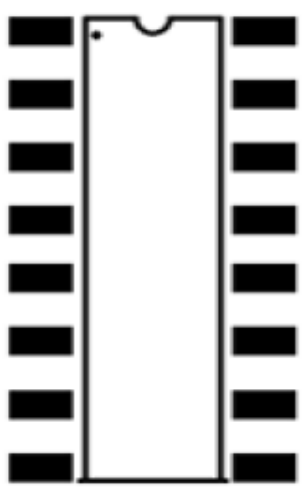
IC 7410 (3-input NAND Gate)
for G1, G2,

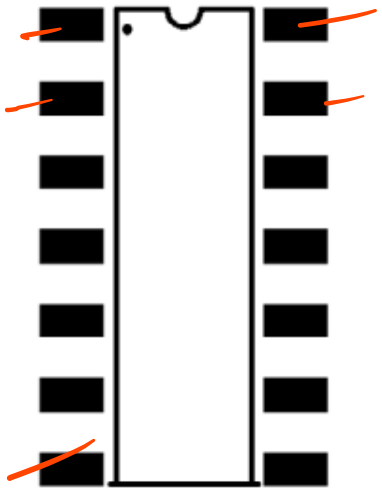


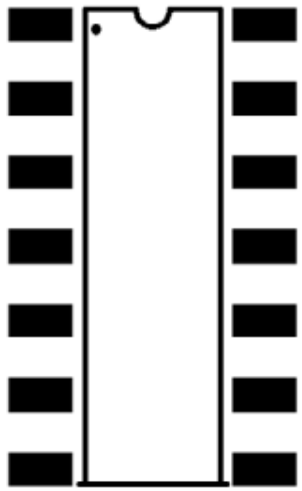



UNTITLED - Proteus 8 Demonstration - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Home Page
Schematic Capture
GRAPHICS
COMPONENT
PIN
PORT
MARKER
ACTUATOR
INDICATOR
VPROBE
IPROBE
TAPE
GENERATOR
TERMINAL
SUBCIRCUIT
2D GRAPHIC
WIRE DOT
WIRE
BUS WIRE
BORDER
TEMPLATE
U1:A
U1:B
U2:A
U2:B
74HC10
74HC00
J
K
Q
Q'
AJMER SINGH RK20APA12 11201214
3 Message(s)
ANIMATING: 00:01:11.982014 (CPU load 1%)
+0.0
-1600.0
10:20
Monday
22-03-2021
ENG

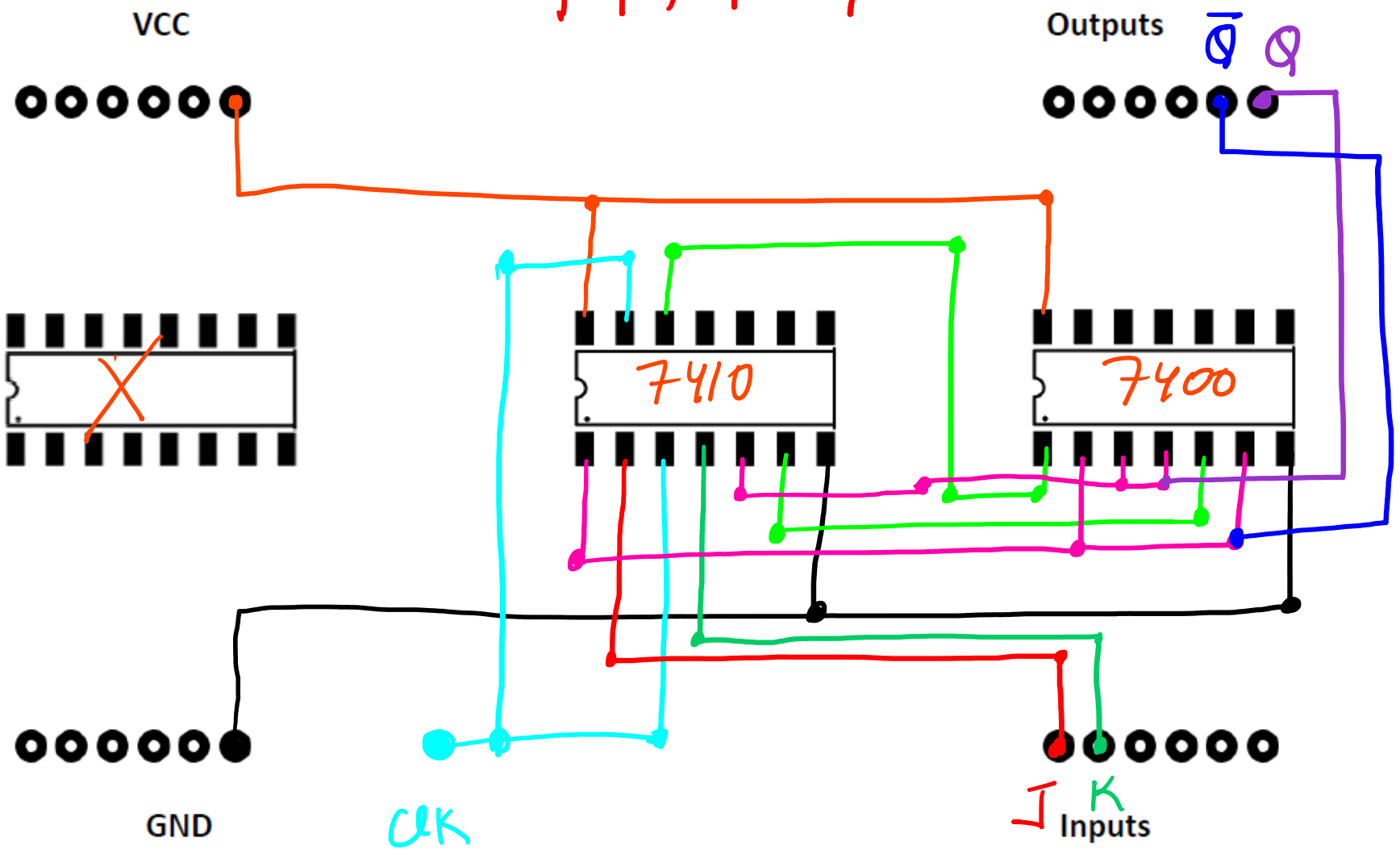
Pin configuration of ICs:







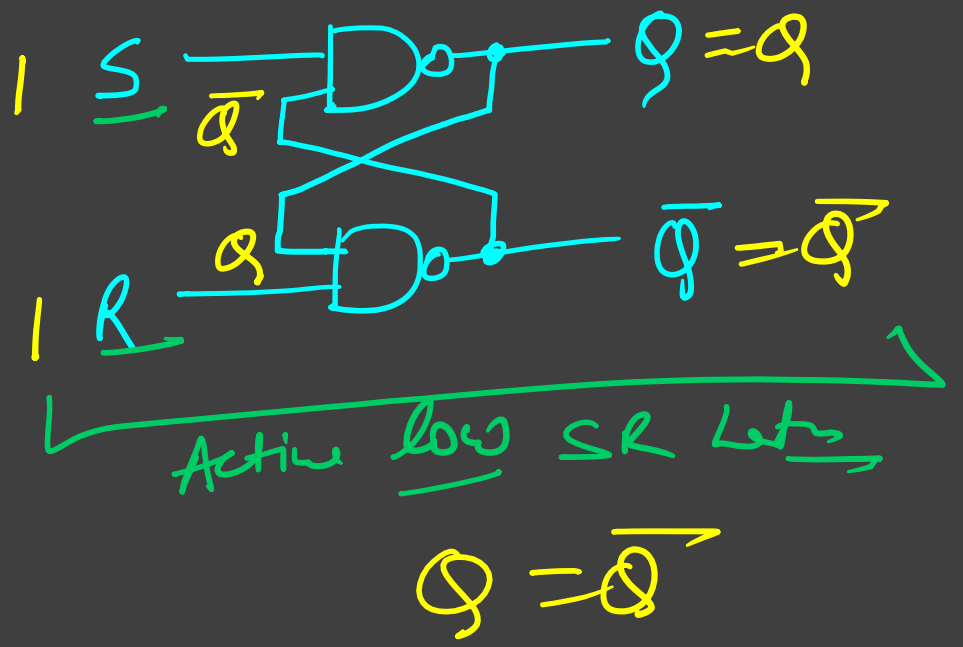
Draw Bread Board Connection diagram: JK flip flop using Gates. (7410, 7400)



Q: In the Given Circuit, at what value of SR the ckt shows invalid state

	S	R
A	0	0
B	0	1
C	1	0
D	1	1

No change



$Q = \overline{Q}$