ECE213: Digital Electronics

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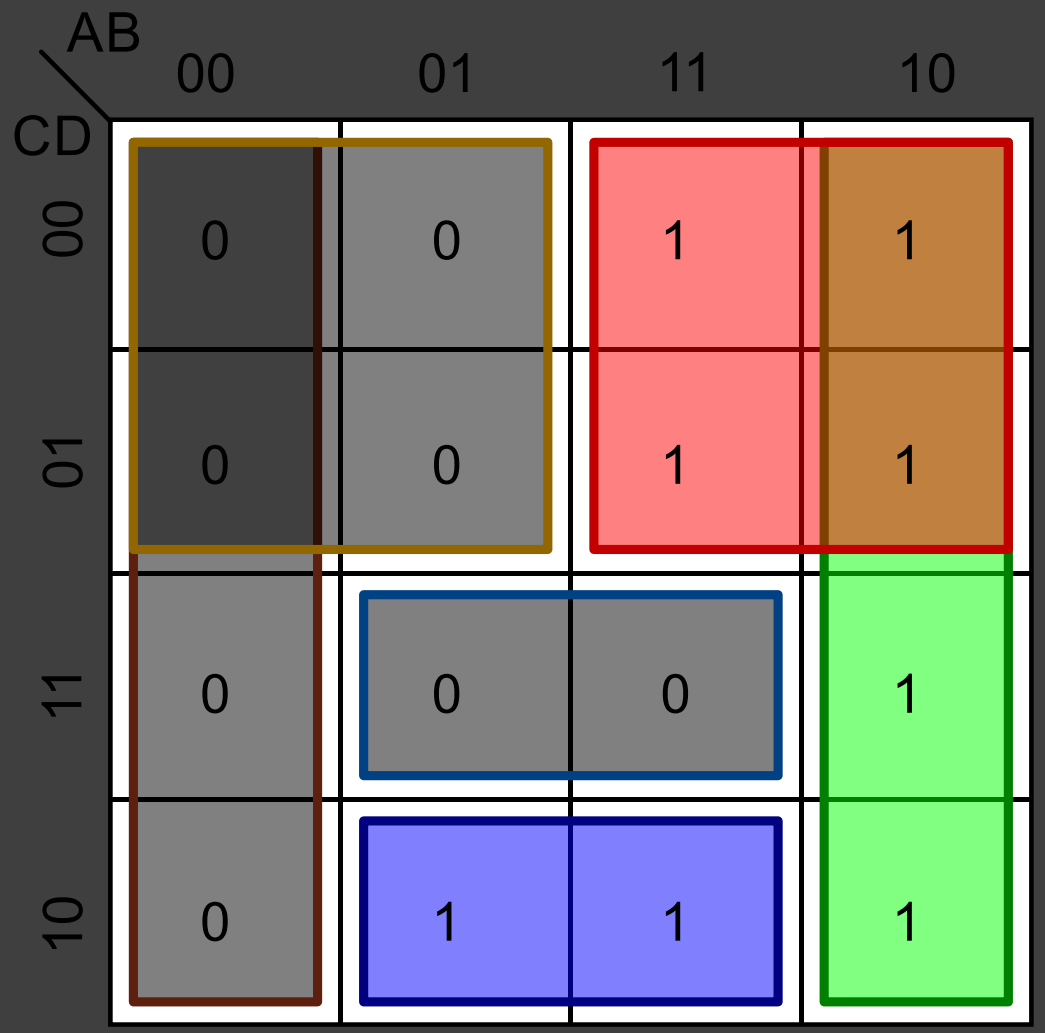
The Course Contents

Unit II

Combinational Logic System : Truth table, Basic logic operation, Boolean Algebra, Basic postulates, Standard representation of logic functions -SOP forms, Simplification of switching functions - K-map, Synthesis of combinational logic circuits, Logic gates, Fundamental theorems of Boolean algebra, Standard representation of logic functions POS forms

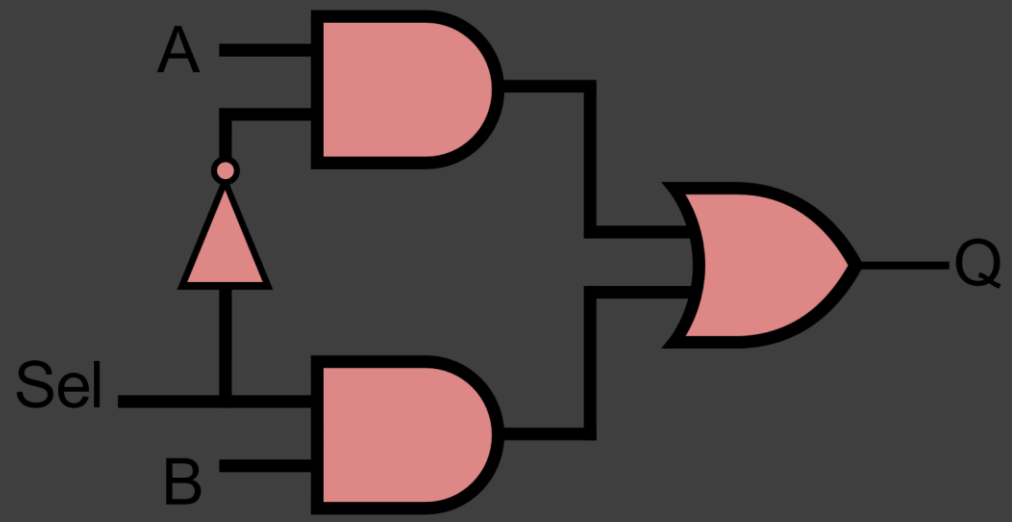


The Course Contents

Unit III

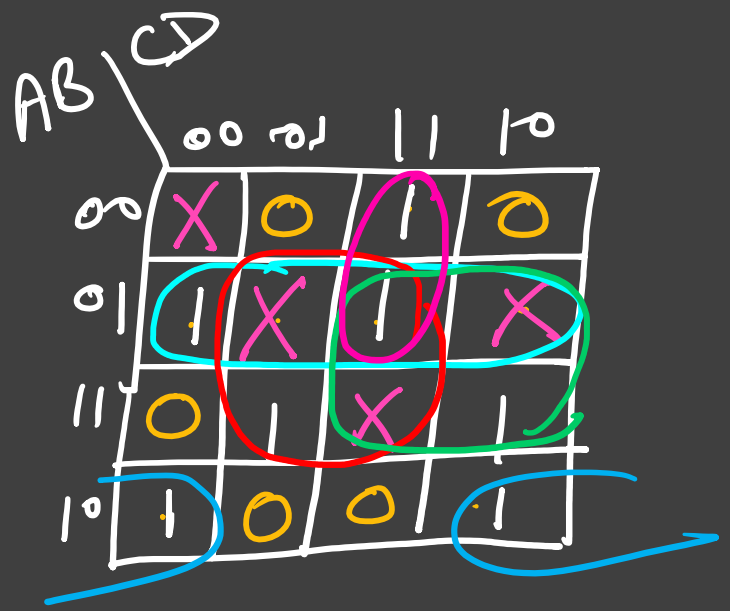
Introduction to Combinational Logic Circuits : Adders, Subtractors, Comparators, Multiplexers and Demultiplexers, Decoders, Encoders, Parity circuits

Introduction to Logic Families : Introduction to different logic families, Structure and operations of TTL, MOS and CMOS logic families



Don't Care

$$Y = \prod M(1, 2, 9, 11, 12) \cdot d(5, 6, 15)$$



$$Y = \bar{A}B + BD + BC + A\bar{B}\bar{D} + \bar{A}\bar{C}D$$

Combinational Logic System

Encoder and Decoder Circuits: Decoder

It is a combinational ckt which have n lin i/ps and 2^n lin o/p.

$n : 2^n$ decoder.

1:2
2:4
3:8
4:16
⋮

Basic

2:4 decoder

	MSB I_1	LSB I_0	Y_0	Y_1	Y_2	Y_3
0	0	0	1	0	0	0
1	0	1	0	1	0	0
2	1	0	0	0	1	0
3	1	1	0	0	0	1

Boolean eq.

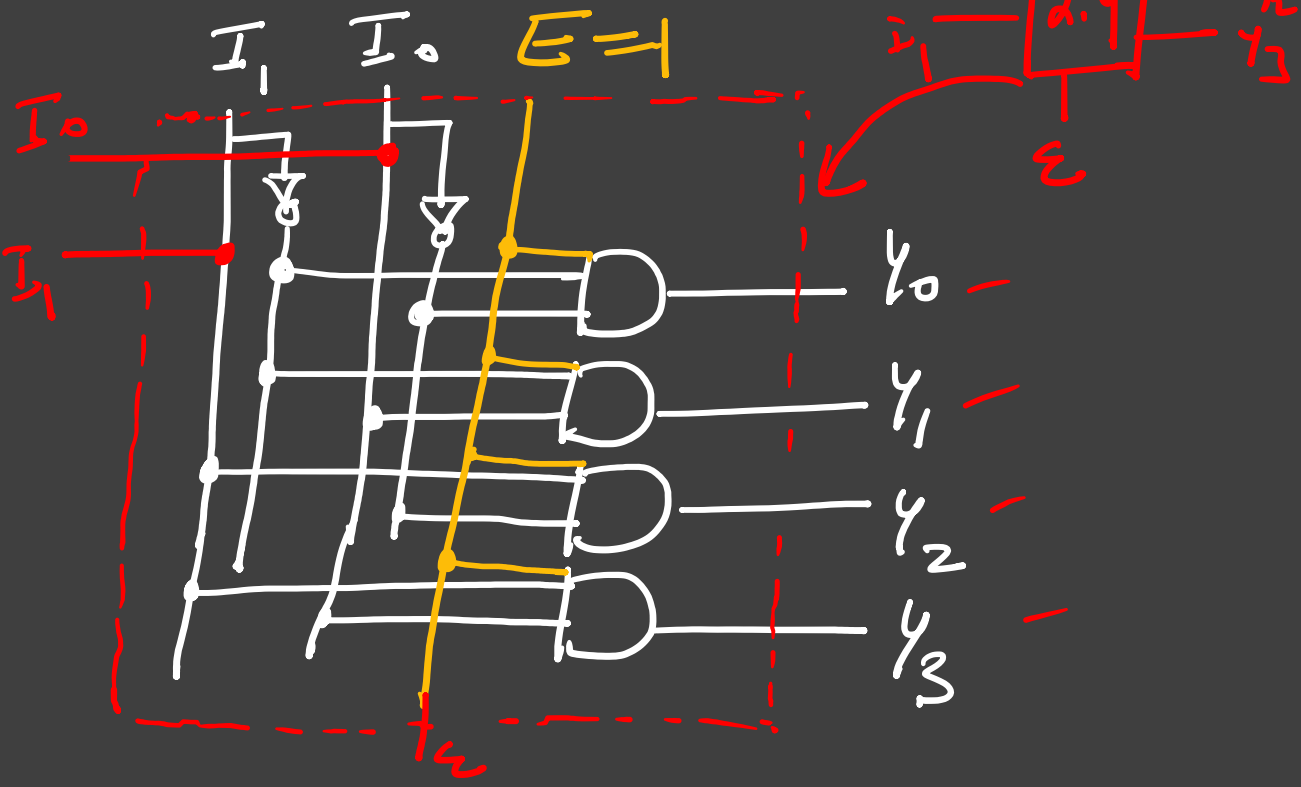
$Y_0 = \bar{I}_1 \bar{I}_0$

$Y_1 = \bar{I}_1 I_0$

$Y_2 = I_1 \bar{I}_0$

$Y_3 = I_1 I_0$

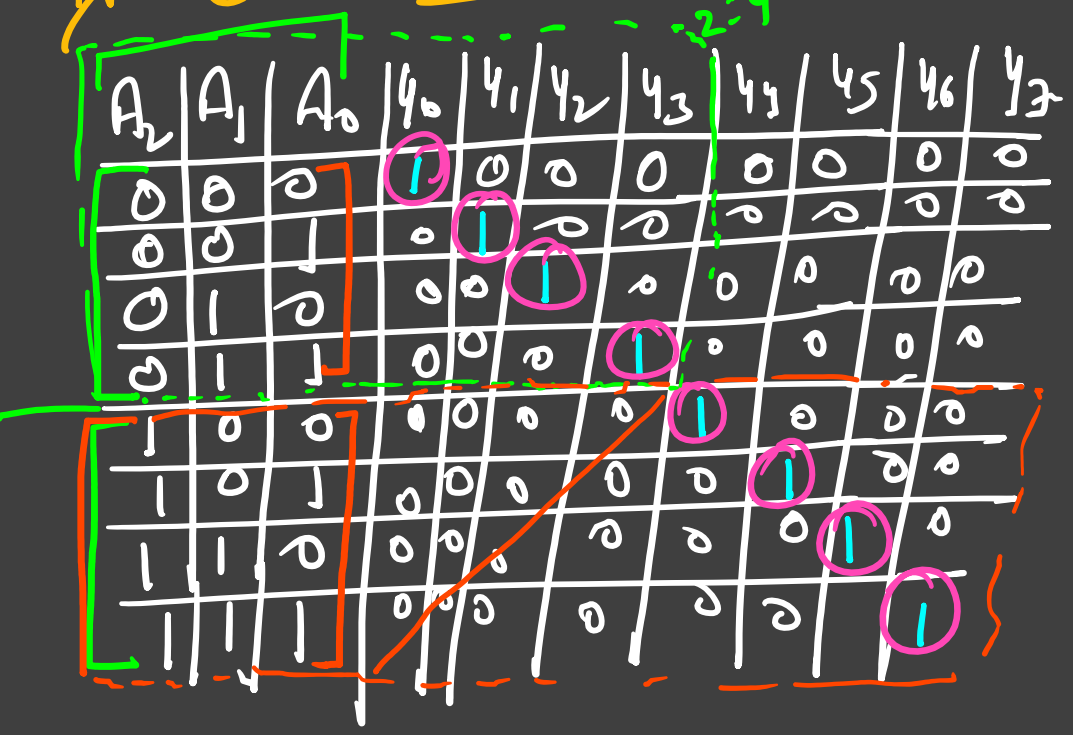
If we want to use one enable pin the ckt
- Enable is active high



Combinational Logic System

Encoder and Decoder Circuits: Decoder

★ 3:8 decoder (Active high)



$Y_0 = \bar{A}_2 \bar{A}_1 \bar{A}_0$

$Y_1 = \bar{A}_2 \bar{A}_1 A_0$

$Y_2 = \bar{A}_2 A_1 \bar{A}_0$

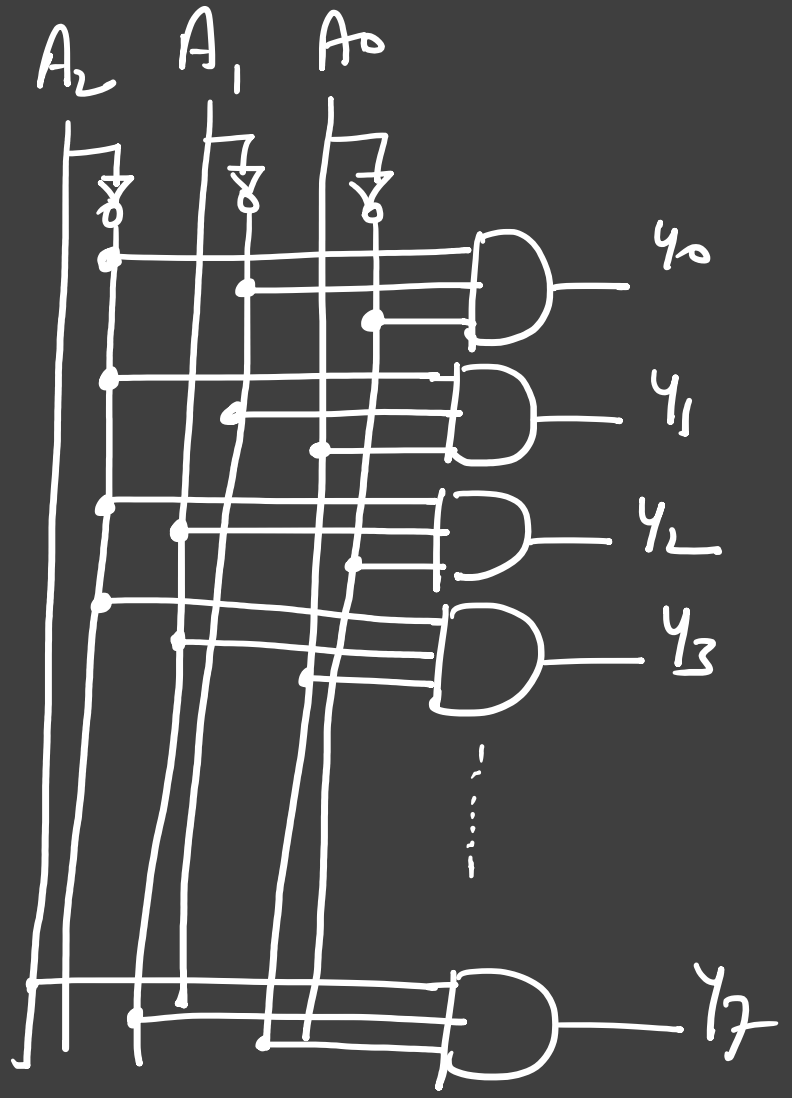
$Y_3 = \bar{A}_2 A_1 A_0$

$Y_4 = A_2 \bar{A}_1 \bar{A}_0$

$Y_5 = A_2 \bar{A}_1 A_0$

$Y_6 = A_2 A_1 \bar{A}_0$

$Y_7 = A_2 A_1 A_0$



Combinational Logic System

Encoder and Decoder Circuits: Decoder

4:16 Decoder

$A_3\ A_2\ A_1\ A_0$

$Y_0 = \overline{A_3}\,\overline{A_2}\,\overline{A_1}\,\overline{A_0}$

$Y_1 = \overline{A_3}\,\overline{A_2}\,\overline{A_1}\,A_0$

$Y_2 = \overline{A_3}\,\overline{A_2}\,A_1\,\overline{A_0}$

$Y_3 = \overline{A_3}\,\overline{A_2}\,A_1\,A_0$

$Y_4 = \overline{A_3}\,A_2\,\overline{A_1}\,\overline{A_0}$

$Y_5 = \overline{A_3}\,A_2\,\overline{A_1}\,A_0$

$Y_6 = \overline{A_3}\,A_2\,A_1\,\overline{A_0}$

$Y_7 = \overline{A_3}\,A_2\,A_1\,A_0$

$Y_8 = A_3\,\overline{A_2}\,\overline{A_1}\,\overline{A_0}$

$Y_9 = A_3\,\overline{A_2}\,\overline{A_1}\,A_0$

$Y_{10} = A_3\,\overline{A_2}\,A_1\,\overline{A_0}$

$Y_{11} = A_3\,\overline{A_2}\,A_1\,A_0$

$Y_{12} = A_3\,A_2\,\overline{A_1}\,\overline{A_0}$

$Y_{13} = A_3\,A_2\,\overline{A_1}\,A_0$

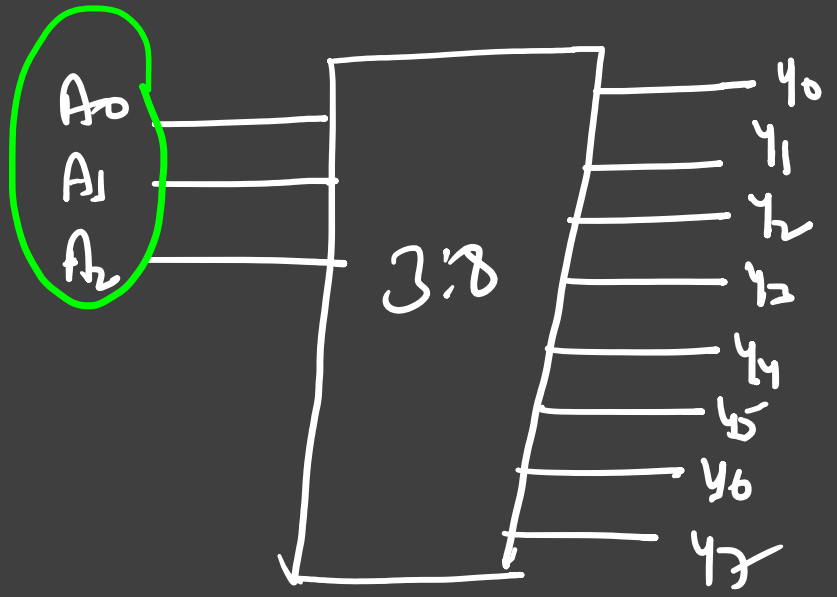
$Y_{14} = A_3\,A_2\,A_1\,\overline{A_0}$

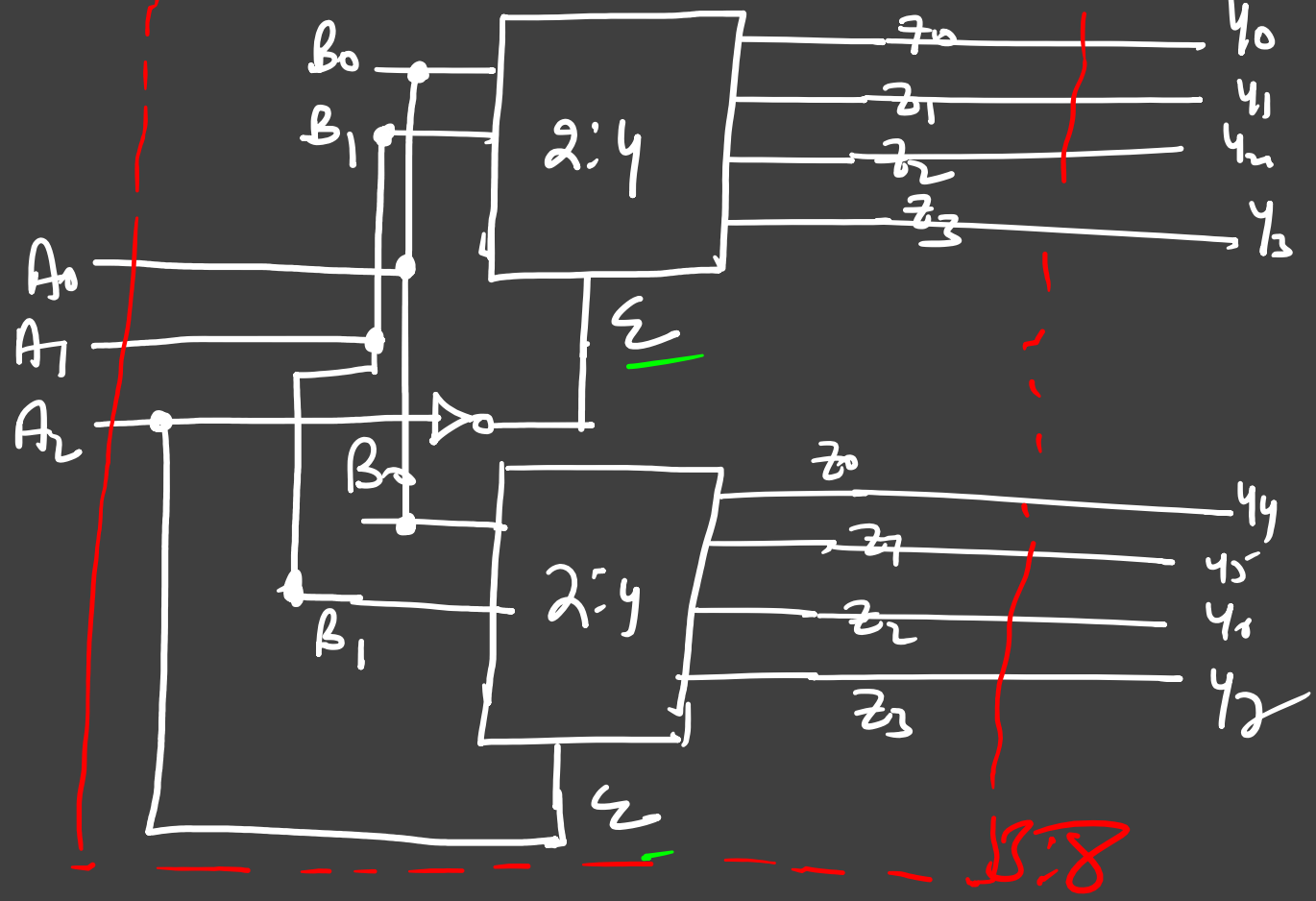
$Y_{15} = A_3\,A_2\,A_1\,A_0$

Combinational Logic System

Encoder and Decoder Circuits: Decoder Tree

Implement 3:8 decoder using 2:4 decoder





Combinational Logic System

Encoder and Decoder Circuits: Decoder Tree

☆ Implement the 4:16 Decoder using 1:2 dec.

Q: How many 1:2 dec. are required to impl. 4:16 dec.

A: No. of i/p = 4

No. of o/p = 2

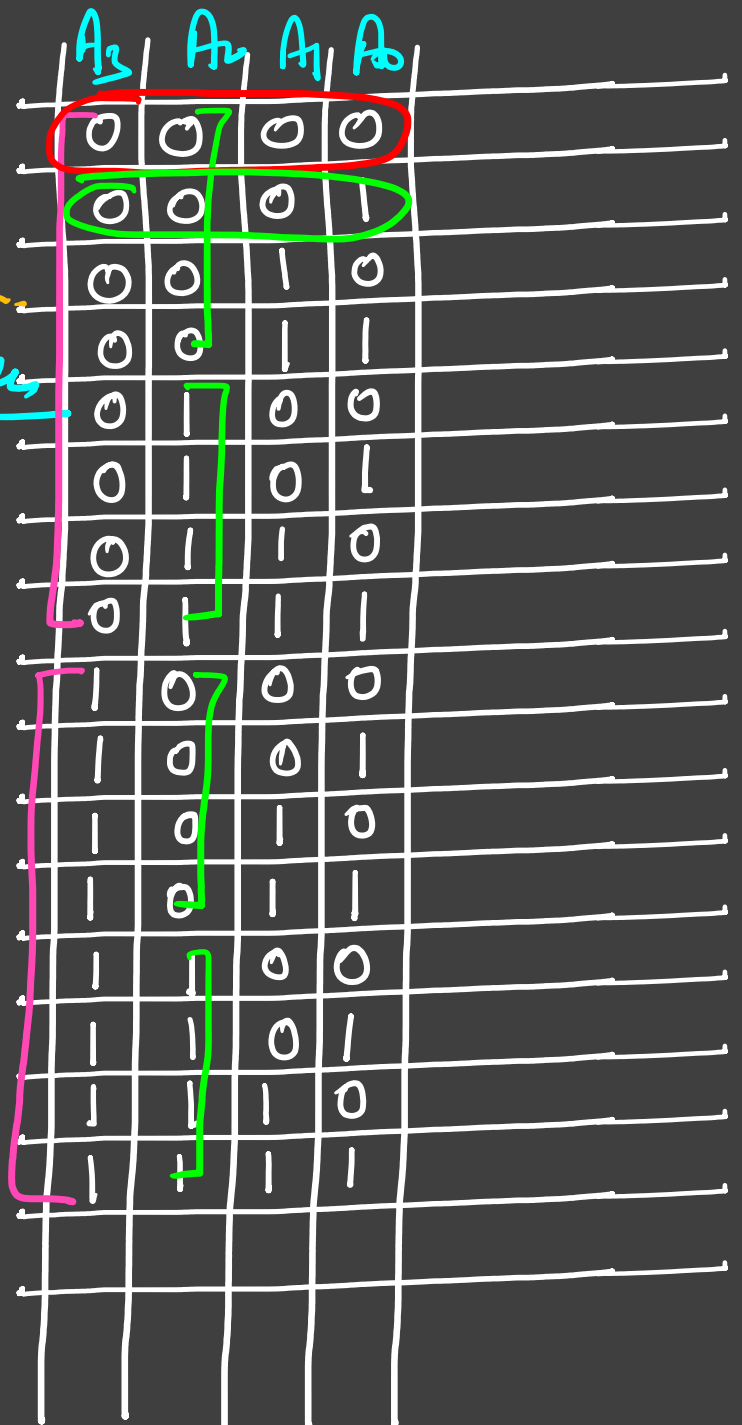
level / step 1 $\frac{16}{2} = 8$

level / step 2 $\frac{8}{2} = 4$

level / step 3 $\frac{4}{2} = 2$

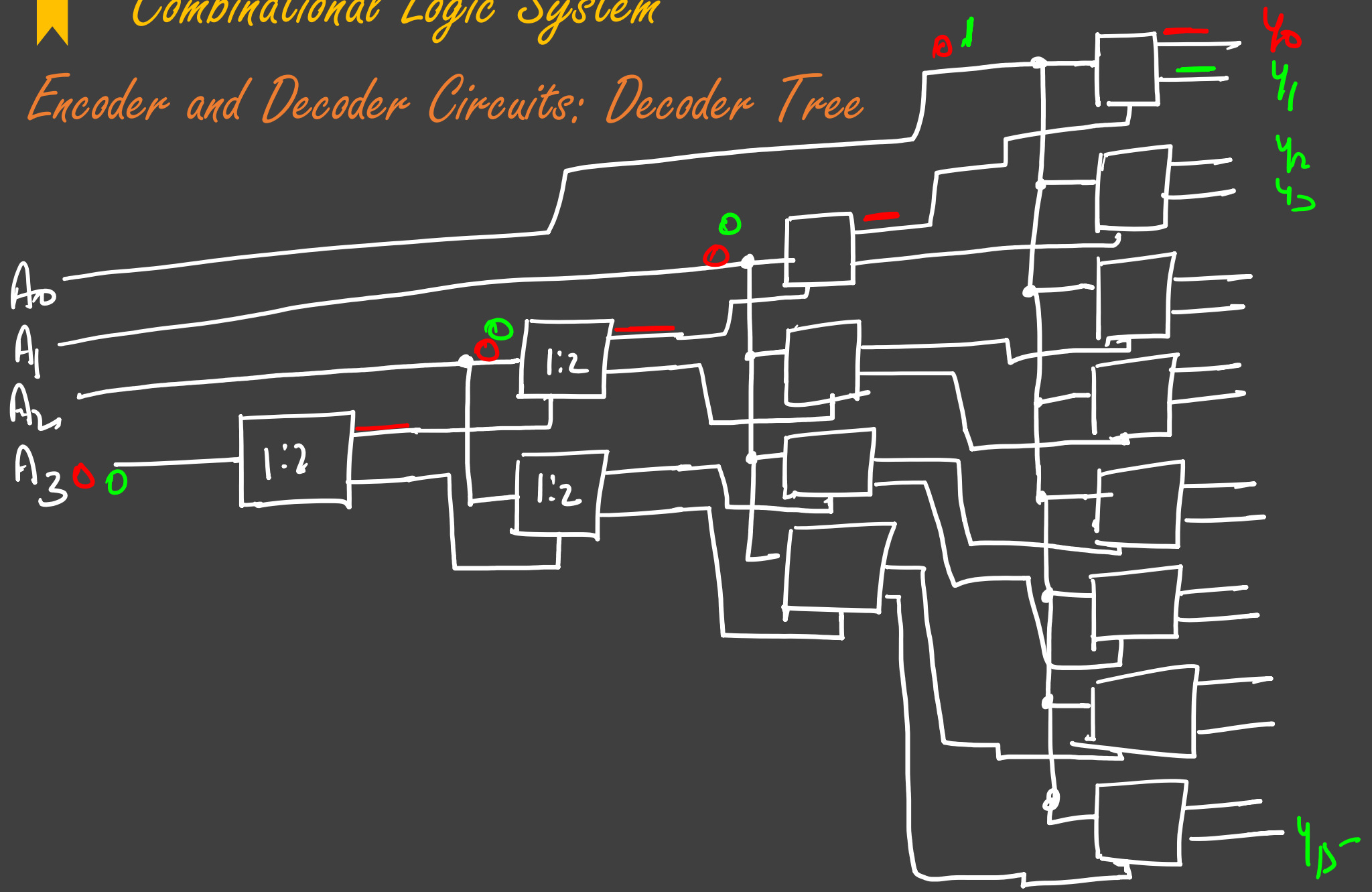
level / step 4 $\frac{2}{2} = 1$

15 dec.



Combinational Logic System

Encoder and Decoder Circuits: Decoder Tree

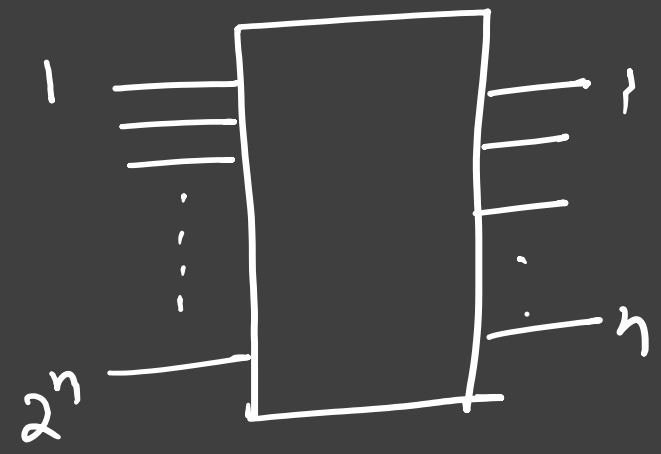


Combinational Logic System

Encoder and Decoder Circuits: Encoder

$n : 2^n$ is decoder

ip — op



$2^n : n$ is encoder

op — ip

$n=1$	$2:1$
$n=2$	$4:2$
$n=3$	$8:3$
$n=4$	$16:4$

D_1	D_0	y
0	0	
0	1	0
1	0	1
1	1	

Combinational Logic System

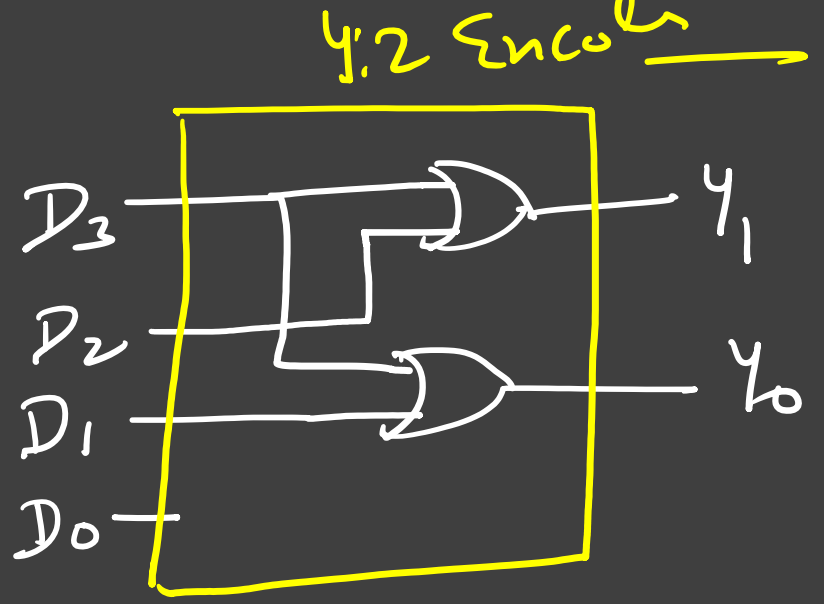
Encoder and Decoder Circuits: Encoder

Encoder 4:2

D_3	D_2	D_1	D_0	Y_0 (LSB)	Y_1 (MSB)	
0	0	0	1	0	0	0
0	0	1	0	1	0	1
0	1	0	0	0	1	2
1	0	0	0	1	1	3

$$Y_0 = D_1 + D_3$$

$$Y_1 = D_2 + D_3$$



Combinational Logic System

Encoder and Decoder Circuits: Encoder

★ 8:3 Encoder

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	0

I	Y_2	Y_1	Y_0
D_0	0	0	0
D_1	0	0	1
D_2	0	1	0
D_3	0	1	1
D_4	1	0	0
D_5	1	0	1
D_6	1	1	0
D_7	1	1	1

$$\begin{cases} Y_0 = D_1 + D_3 + D_5 + D_7 \\ Y_1 = D_2 + D_3 + D_6 + D_7 \\ Y_2 = D_4 + D_5 + D_6 + D_7 \end{cases}$$

OR

$2^8 = 256$

8 -

Combinational Logic System

Multiplexers and Demultiplexers

2:1 Mux

No. of I/P 2

No. of O/P 1

No. of Sel. lines 1

As the no. i/p increases

3-input

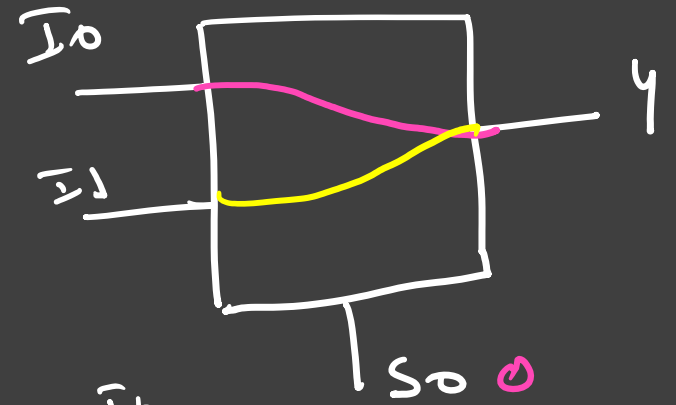
Multi $2^n : 1$

$n=1$	2:1
$n=2$	4:1
$n=3$	8:1
$n=4$	16:1

2^6

2^{11}

S_0	I_1	I_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



Y	$\bar{I}_1 I_0$	01	11	I_0
$\bar{S}_0$	0	1	1	0
S_0	0	0	1	1

$$Y = \bar{S}_0 I_0 + S_0 I_1$$

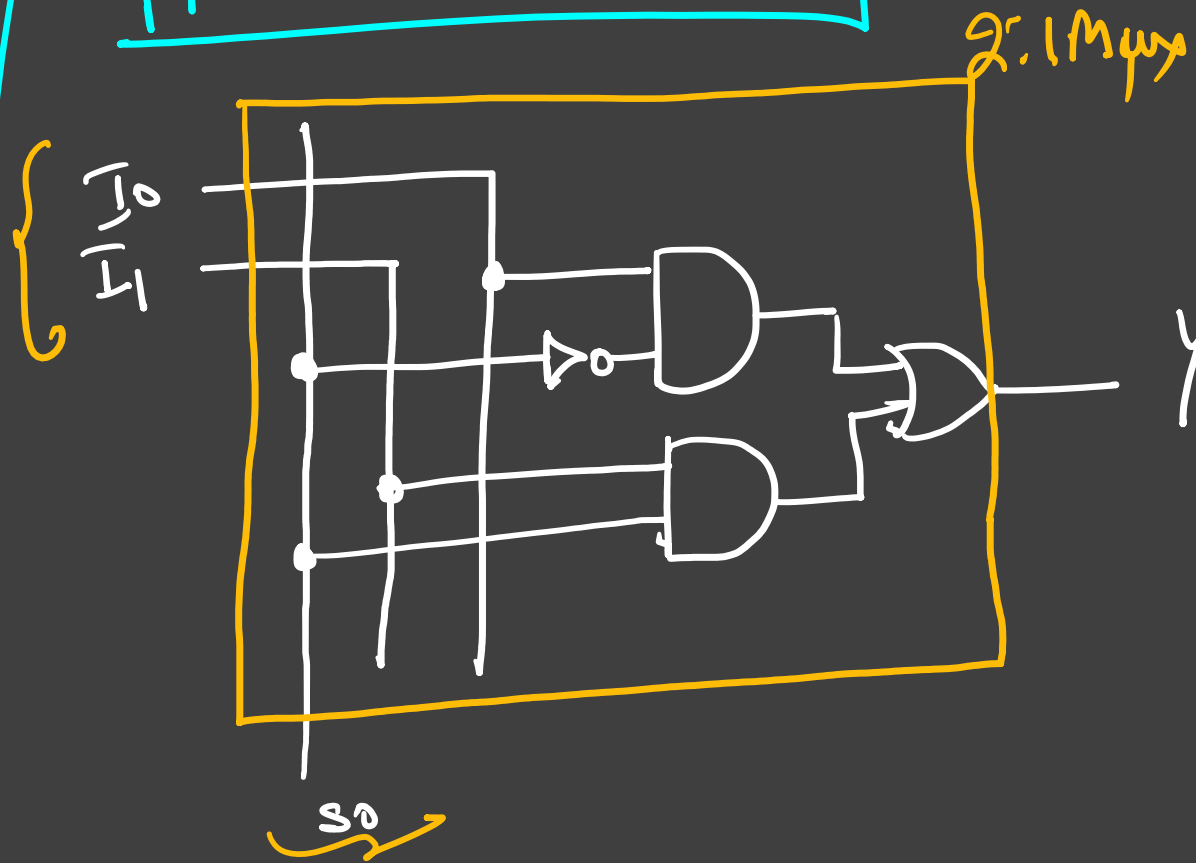
Combinational Logic System

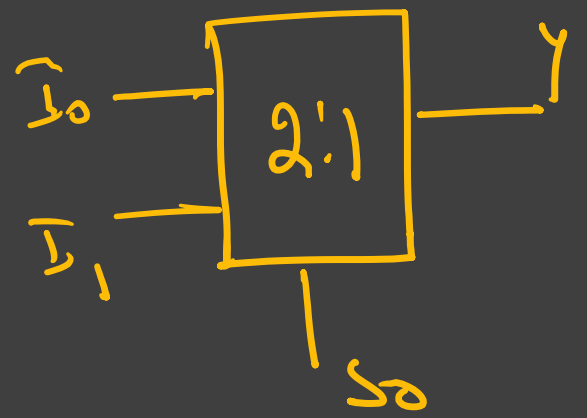
Multiplexers and Demultiplexers

2:1 Mux

S_0	Y
0	I_0
1	I_1

$$Y = \bar{S_0} I_0 + S_0 I_1$$





Combinational Logic System

Multiplexers and Demultiplexers

4:1 Mux

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

Q.1.5 Logic circuit of 4:1 Mux using the above eq.

Combinational Logic System

Multiplexers and Demultiplexers

★ **8:1 Mux**

$$Y = \bar{S}_2\bar{S}_1\bar{S}_0 I_0 + \bar{S}_2\bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3$$

$$+ S_2\bar{S}_1\bar{S}_0 I_4 + S_2\bar{S}_1 S_0 I_5 + S_2 S_1 \bar{S}_0 I_6 + S_2 S_1 S_0 I_7$$

★ **16:1 Mux**

Combinational Logic System

Multiplexers and Demultiplexers

A 32:1 Mux