

ECE213: Digital Electronics



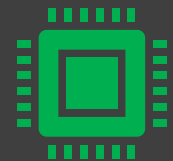
Ajmer Singh



9988921373



ajmer.17381@lpu.co.in



The Course Contents

Unit 1

Number Systems : Digital Systems, Data representation and coding, Logic circuits, Implementation of digital systems, Number Systems, Codes- Positional number system, Binary number system, Methods of base conversions, Binary arithmetic, Representation of signed numbers, Fixed numbers, Binary coded decimal codes, Gray codes, Error detection code, Parity check codes, octal number system, Hexadecimal number system, Error correction code, Hamming code, Octal arithmetic, Hexadecimal arithmetic, Floating point numbers

...	32	16	8	4	2	1
...	2^5	2^4	2^3	2^2	2^1	2^0
...	1	0	1	0	1	0
	Sixth digit	Fifth digit	Fourth digit	Third digit	Second digit	First digit

Value of digits in the "Binary numeral system"



The Course Contents

Unit II

Combinational Logic System : Truth table, Basic logic operation, Boolean Algebra, Basic postulates, Standard representation of logic functions - SOP forms, Simplification of switching functions - K-map, Synthesis of combinational logic circuits, Logic gates, Fundamental theorems of Boolean algebra, Standard representation of logic functions POS forms

AB		00	01	11	10
CD	00	0	0	1	1
	01	0	0	1	1
	11	0	0	0	1
	10	0	1	1	1

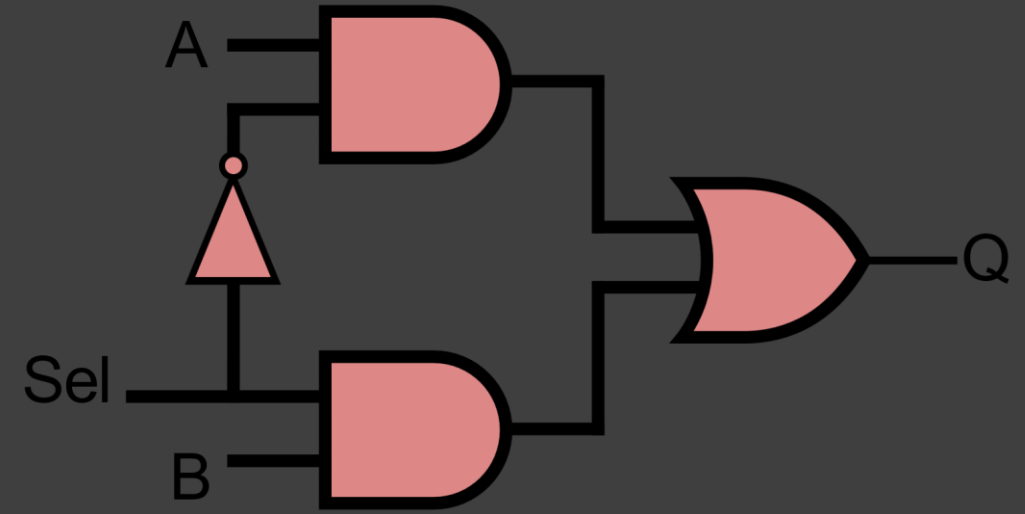


The Course Contents

Unit III

Introduction to Combinational Logic Circuits : Adders, Subtractors, Comparators, Multiplexers and Demultiplexers, Decoders, Encoders, Parity circuits

Introduction to Logic Families : Introduction to different logic families, Structure and operations of TTL, MOS and CMOS logic families



Tutorial

Ex $(AB.0C)_{16} = ()_2 = ()_8 = ()_{10}$

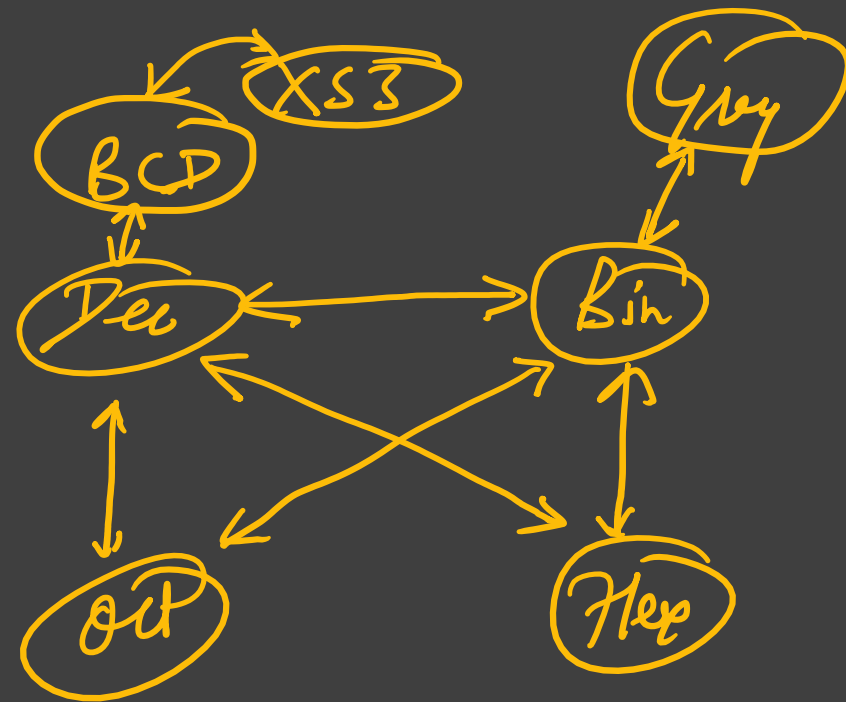
$$0(10/0/0/1/0000/1/00)_2$$

$$(253.030)_8$$

$$1\ 0\ 1\ 0\ 1\ 0\ 1\ 1\ .\ 0\ 0\ 0\ 0\ 1\ 1$$

$$128\ 64\ 32\ 16\ 8\ 4\ 2\ 1\ \frac{1}{2}\ \frac{1}{4}\ \frac{1}{8}\ \frac{1}{16}\ \frac{1}{32}\ \frac{1}{64}$$

$$128 + 32 + 8 + 2 + 1 + \frac{1}{32} + \frac{1}{64} = (171.046\dots)_{10}$$



Tutorial

Ex $(25)_{10} = (100)_b$

find b .

Sol.

$$25 = \begin{matrix} 1 & 0 & 0 \\ b^2 & b^1 & b^0 \end{matrix}$$

$$25 = b^2$$

$$\boxed{b = \pm 5}$$

$$\boxed{b = +5}$$

Ex $(51)_{10} = (123)_b$

$$51 = b^2 + 2b + 3$$

$$b^2 + 2b - 48 = 0$$

$$b = 6, -8$$

$$\boxed{b = 6}$$

$$(51)_{10} = (123)_6$$

Tutorial

Ex IEEE 754

$$(-27.125)_{10}$$

$$(11011.001)_2 = (27.125)_{10}$$

Normalization

$$\begin{array}{l} 11011.001 \times 2^0 \\ \leftarrow 1.1011001 \times 2^4 \end{array}$$

$$\begin{array}{r|rr} 2 & 27 & \\ \hline 2 & 13 & 1 \\ \hline 2 & 6 & 1 \\ \hline 2 & 3 & 0 \\ \hline & 1 & 1 \end{array}$$

$$\begin{array}{l} 0.125 \times 2 = .25 \quad 0 \\ .25 \times 2 = 0.5 \quad 0 \\ .5 \times 2 = 1.0 \quad 1 \end{array}$$

$$(4)_{10} = (100)_2$$

$$\begin{array}{r} 111111 \\ \hline 100 \end{array}$$

Sign 8-bit Exponent

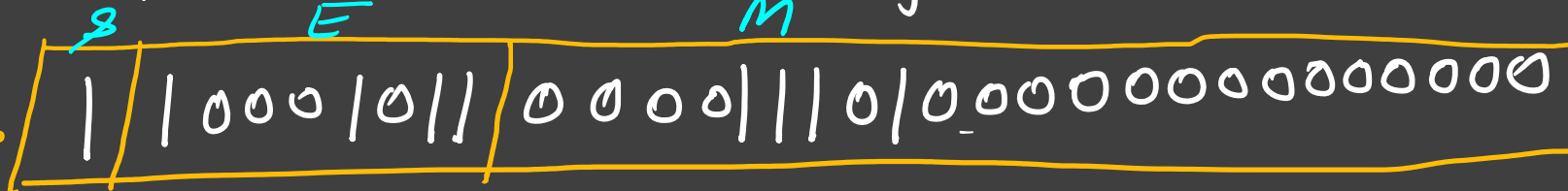
23-bit Mantissa



with 127 as bias

Tutorial

Ex The given IEEE 754 rep find the n



→ -ve

$$N = (-1)^s 1.M \times 2^{E-127}$$

$$= (-1)^1 1.00001110 \times 2^{12}$$

$$= (-1)^1 100001110000$$

\downarrow 4096
 \downarrow 2048
 \downarrow 1024
 \downarrow 512
 \downarrow 256
 \downarrow 128
 \downarrow 64
 \downarrow 32
 \downarrow 16
 \downarrow 8
 \downarrow 4
 \downarrow 2
 \downarrow 1

$$(-1) 4096 + 128 + 64 + 32 + 8$$

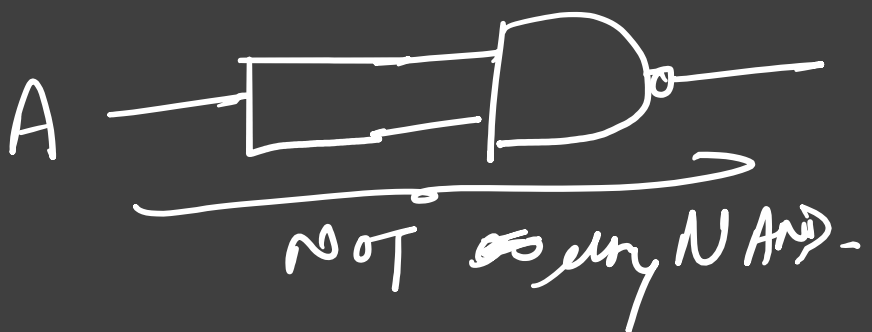
$$= -4328$$

$$\begin{array}{r}
 10001011 \\
 1111111 \\
 \hline
 0001100 \\
 \quad \quad \quad 12
 \end{array}$$

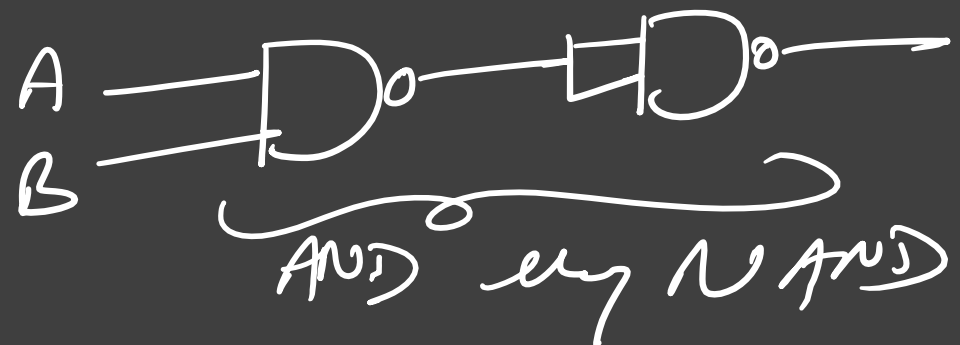
Tutorial

★ Universal Gate Implement the logic function using NAND Gate
 we know $Y_{NAND} = \overline{AB}$ — ①

① NOT using NAND
 $Y_{NOT} = \overline{A}$
 $Y_{NOT} = \overline{AA}$



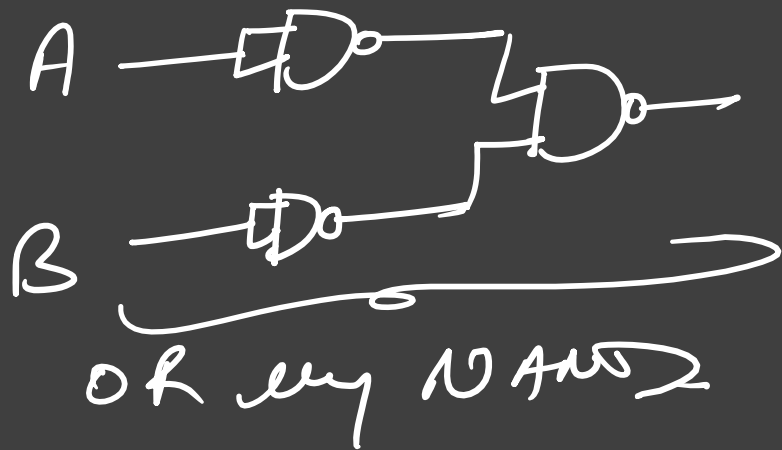
② AND using NAND
 $Y_{AND} = AB$
 $= \overline{\overline{AB}}$
 $= \overline{\overline{AB}}$



Tutorial

③ OR Gate using NAND

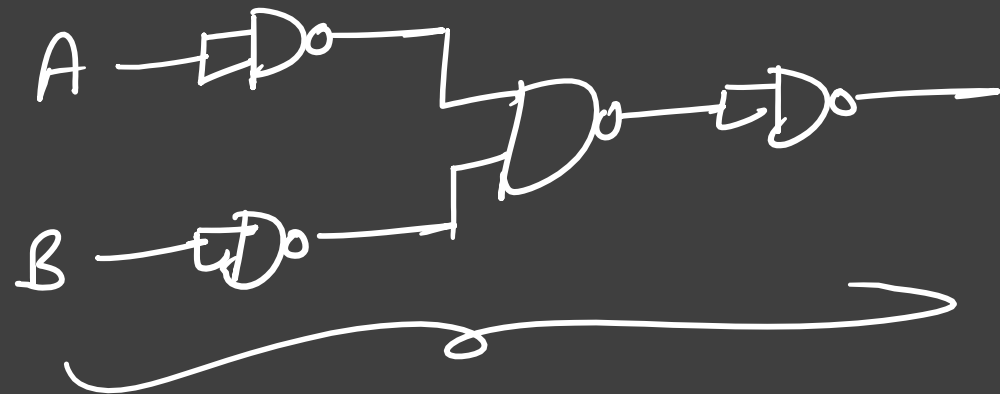
$$\begin{aligned} Y_{OR} &= A + B \\ &= \overline{\overline{A + B}} \\ &= \overline{\overline{A} \overline{B}} \end{aligned}$$



$$Y_{NAND} = \overline{AB}$$

④ NOR Gate using NAND

$$\begin{aligned} Y_{NOR} &= \overline{A + B} \\ &= \overline{\overline{\overline{A} \overline{B}}} \end{aligned}$$



Tutorial

⑤

XOR Gate using NAND

$$Y_{\text{XOR}} = A\bar{B} + \bar{A}B$$

$$= \overline{\overline{A\bar{B} + \bar{A}B}}$$

$$= \overline{\overline{A\bar{B}} \cdot \overline{\bar{A}B}}$$

$$Y_{\text{NAND}} = \overline{AB}$$

H.W. Find How to
represent XOR Gate using
only 4 NAND Gate

