ECE213: Digital Electronics

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The Course Contents

Unit V

Sequential Logic Circuits Applications : Registers: Operation of all basic Shift Registers, Counters: Design of Asynchronous and Synchronous counters, Ring counter and Johnson ring counter

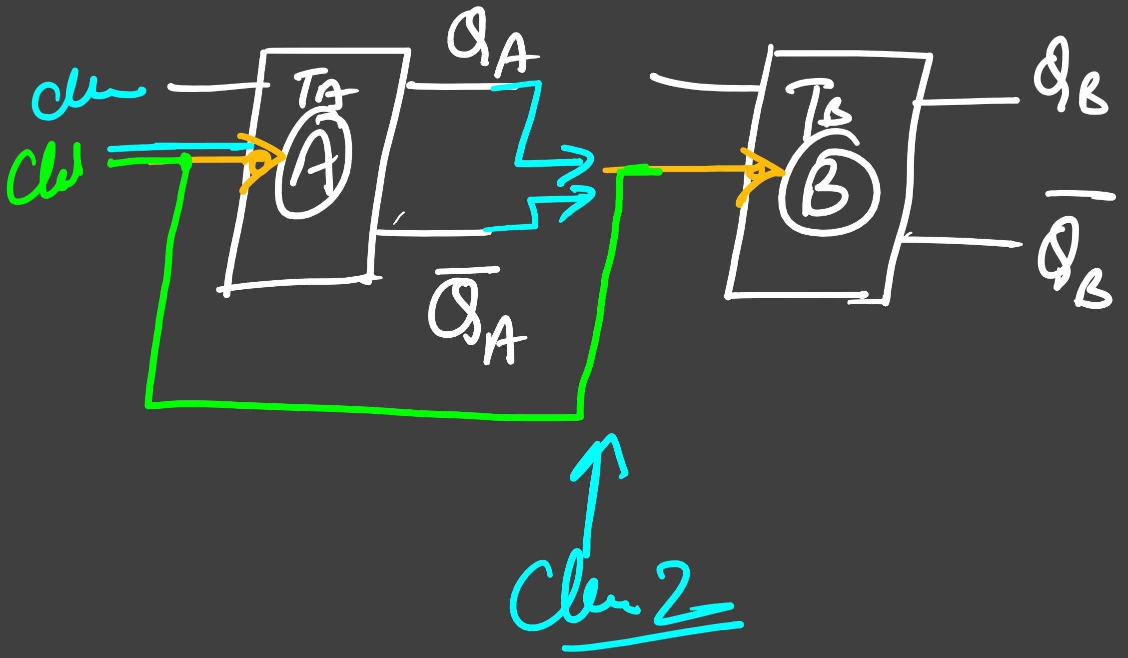
8 FF

8-bit
16-bit
32-bit

Sequential Logic Circuits Applications

Counters

- Asynchronous (Different clocks for diff FF)
- Synchronous (same clock for each FF)



★ Counter classification based on application

- → UP counter
- → Down Counter
- → up/down counter
- → Even Counter
- → odd Counter
- → Random Counter
- → MOD Counter

up

0
1
2
3
4
5
6
7
⋮

down

Q: To design n-bit Counter How many flip flop synchro

A: n

Sequential Logic Circuits Applications

Counters

3-bit
000
001
010
011
100
101
110
111

S.NO	Synchronous Counter	Asynchronous Counter
1	In synchronous counter, all flip flops are triggered with same clock simultaneously.	In asynchronous counter, different flip flops are triggered with different clock, not simultaneously.
2	Synchronous Counter is faster than asynchronous counter in operation.	Asynchronous Counter is slower than synchronous counter in operation.
3	Synchronous Counter does not produce any decoding errors.	Asynchronous Counter produces decoding error.
4	Synchronous Counter is also called Parallel Counter.	Asynchronous Counter is also called Serial Counter.
5	Synchronous Counter designing as well implementation are complex due to increasing the number of states.	Asynchronous Counter designing as well as implementation is very easy.
6	Synchronous Counter will operate in any desired count sequence.	Asynchronous Counter will operate only in fixed count sequence (UP/DOWN).
7	Synchronous Counter examples are: Ring counter, Johnson counter.	Asynchronous Counter examples are: Ripple UP counter, Ripple DOWN counter.
8	In synchronous counter, propagation delay is less.	In asynchronous counter, there is high propagation delay.

Sequential Logic Circuits Applications

Counters

★ How to design synchronous Counters

Step 1: Find the number of flip flop required as/per the application.

Step 2: Decide the type of FF (JK, T, SR, D), and make the excitation table of FF.

Step 3: Make the state diagram and state table of counter

Step 4: Mapping of Excitation table over State table

Step 5: Find the Boolean eqs. using K-map.

Step 6 Draw the logic diagram.

Sequential Logic Circuits Applications

CBA

Counters

Ex Design 3-bit syn. up Counter

Step 1: No. of FF = 3, Name to FF A, B, C, when A is LSB.

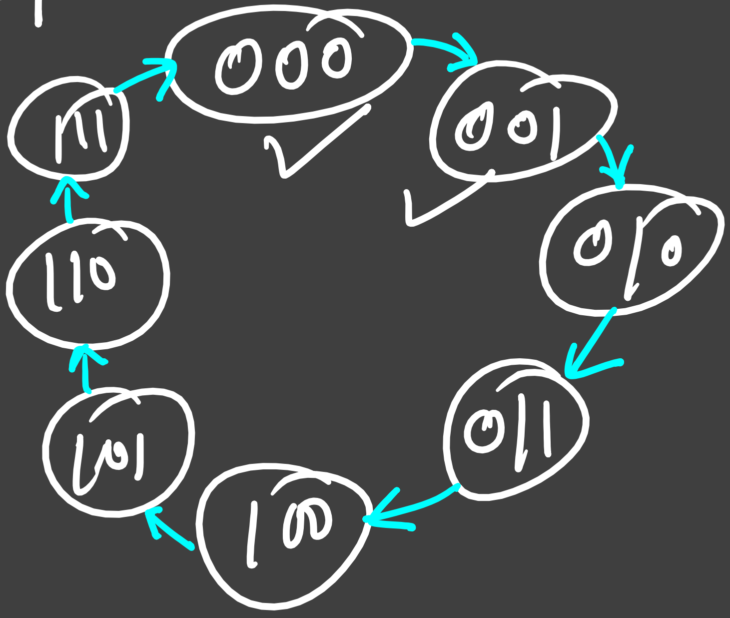
Step 2. Type of FF : JK

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Sequential Logic Circuits Applications

Counters

Step 3. State Diagram



★ State table

Map the excitation tables

Present Value			Next State								
Q_C	Q_B	Q_A	Q_C^+	Q_B^+	Q_A^+	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

Find $J_C, K_C, J_B, K_B, J_A, K_A$ in term of Q_C, Q_B, Q_A

Sequential Logic Circuits Applications

Counters

Steps for J_A

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$J_A = 1$

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	X	1	1	X
1	X	1	1	X

$K_A = 1$

For B

J_B

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$J_B = Q_A$

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	X	X	1	0
1	X	X	1	0

$K_B = Q_A$

For C

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_C = Q_BQ_A$

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	X	X	X	X
1	0	0	1	0

$K_C = Q_BQ_A$

Note if $J = K$ then JK becomes T FF