Combinational Circuits

- It is a connected arrangement of logic gates with a set of inputs and outputs.
- Combinational circuits are employed in digital computers for generating binary control decisions and for providing digital components required for data processing. HALF ADDER and FULL ADDER

Combinational Circuits

- No feedback paths
- No memory
- Combinational circuit is a connected arrangement of logic gates with set of inputs and outputs.
- Binary values of outputs are a function of binary combination of inputs.

Combinational Circuits

- In this, output depends only upon present input.
- Speed is fast.
- It is designed easy.
- There is no feedback between input and output.
- This is time independent.
- Elementary building blocks: Logic gates
- Used for arithmetic as well as boolean operations.
- Combinational circuits don’t have capability to store any state.
- As combinational circuits don’t have clock, they don’t require triggering.
- These circuits do not have any memory element.
- It is easy to use and handle.

Block Diagram –

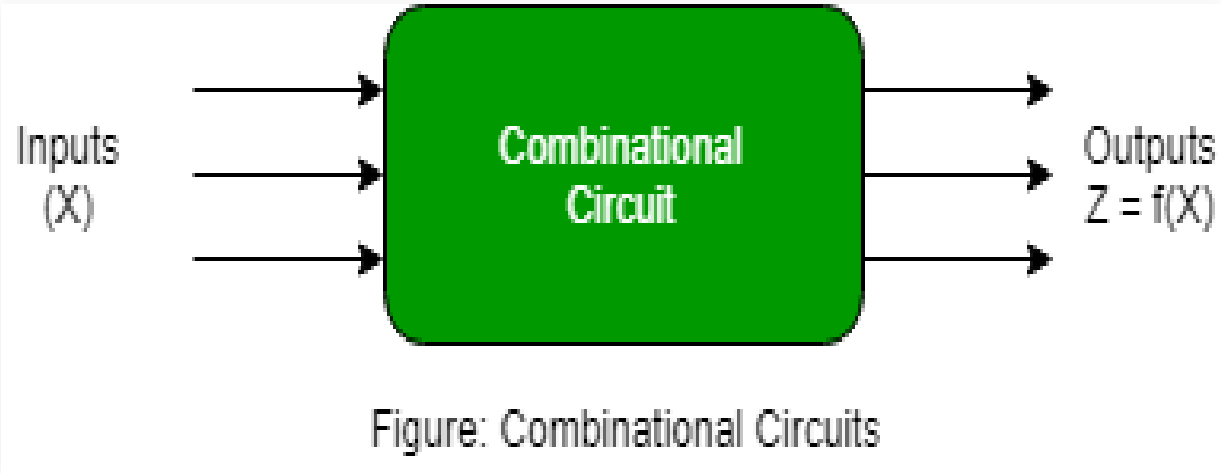


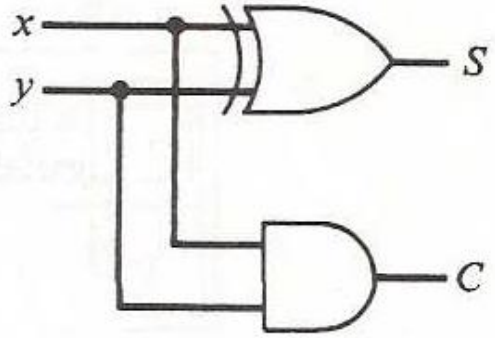
Figure: Combinational Circuits

HALF ADDER

- Performs arithmetic addition of two bits.
- Input variables are called as AUGEND and ADDEND
- Output Variables are SUM and CARRY

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

(a) Truth table



(b) Logic diagram

$$S = x'y + xy' = x \oplus y$$

$$C = xy$$

Figure 1-16 Half-adder.

FULL ADDER

- Performs arithmetic addition of three bits.
- Consists of three inputs and two outputs.

TABLE 1-2 Truth Table for Full-Adder

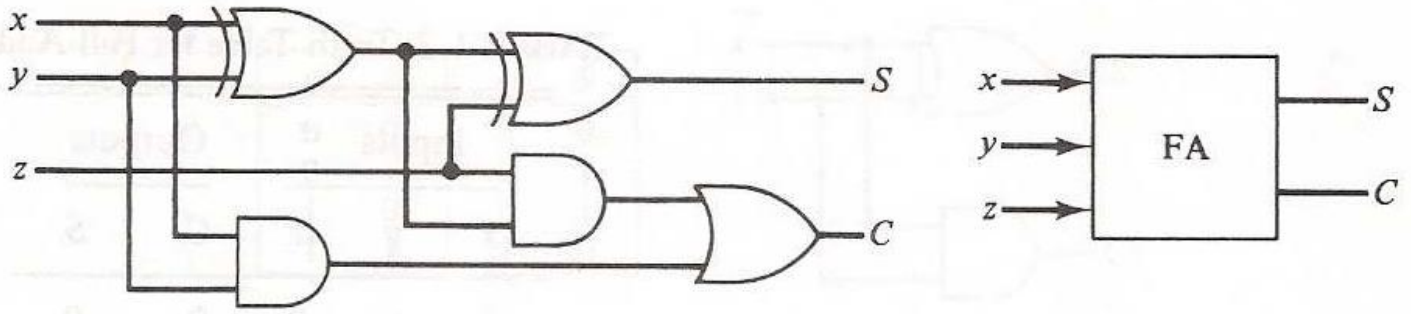
Inputs			Outputs	
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

FULL ADDER

$$S = x \oplus y \oplus z$$

$$C = xy + (x \oplus y)z$$

$$C = xy + (x'y + xy')z$$



(a) Logic diagram (b) Block diagram

Figure 1-18 Full-adder circuit.

Sequential Circuits

- Feedback paths exist
- Memory present
- 2 Types- Synchronous and Asynchronous
- Synchronous sequential circuits employ signals that effect storage elements only at discrete instants of time.
- Synchronization is achieved with help of device called clock.

Sequential Circuits

- **Asynchronous sequential logic** is not **synchronized** by a clock signal; the outputs of the **circuit** change directly in response to changes in inputs. The advantage of **asynchronous logic** is that it can be faster than **synchronous logic**, because the **circuit** doesn't have to wait for a clock signal to process inputs.

Sequential circuits

- **Sequential circuits** are those which are dependent on clock cycles and depends on present as well as past inputs to generate any output.

Block Diagram –

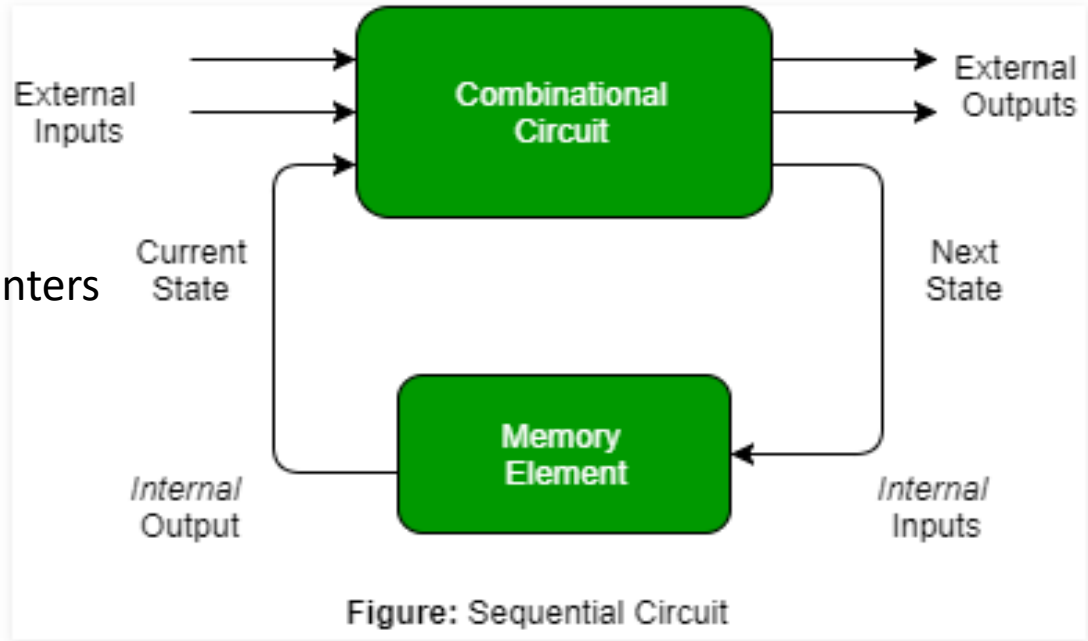


Figure: Sequential Circuit

Examples – Flip-flops, Counters

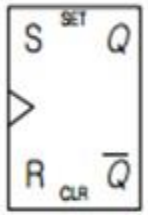
Sequential Circuit

- In this output depends upon present as well as past input.
- Speed is slow.
- It is designed tough as compared to combinational circuits.
- There exists a feedback path between input and output.
- This is time dependent.
- Elementary building blocks: Flip-flops
- Mainly used for storing data.
- Sequential circuits have capability to store any state or to retain earlier state.
- As sequential circuits are clock dependent they need triggering.
- These circuits have memory element.
- It is not easy to use and handle.

1-6 Flip-Flops

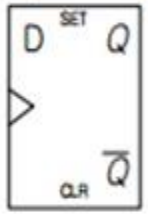
Combinational Circuit = Gate
Sequential Circuit = Gate + F/F

- Flip-Flop
  - The *storage elements* employed in clocked *sequential circuit*
  - A binary cell capable of storing one bit of information
- SR*(Set/Reset)* F/F



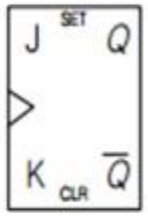
S	R	Q(t+1)	
0	0	Q(t)	no change
0	1	0	clear to 0
1	0	1	set to 1
1	1	?	Indeterminate

- D*(Data)* F/F



D	Q(t+1)	
0	0	clear to 0
1	1	set to 1

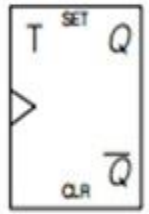
- "no change" condition
  1) Disable Clock
  2) Feedback output into input
- JK*(Jack/King)* F/F



J	K	Q(t+1)	
0	0	Q(t)	no change
0	1	0	clear to 0
1	0	1	set to 1
1	1	Q(t)'	Complement

- JK F/F is a refinement of the SR F/F
- The indeterminate condition of the SR type is defined in complement

- T*(Toggle)* F/F

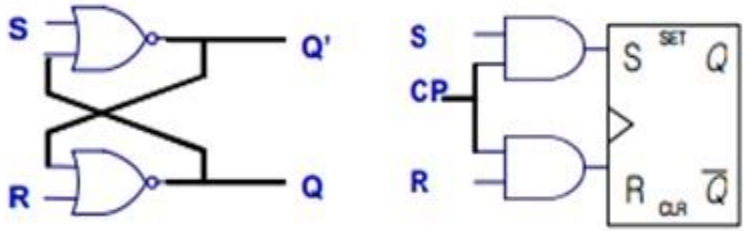


T	Q(t+1)	
0	Q(t)	no change
1	Q'(t)	Complement

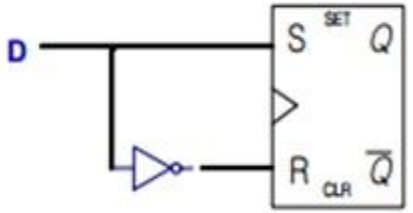
- T=1(J=K=1), T=0(J=K=0)

1-6 Flip-Flops

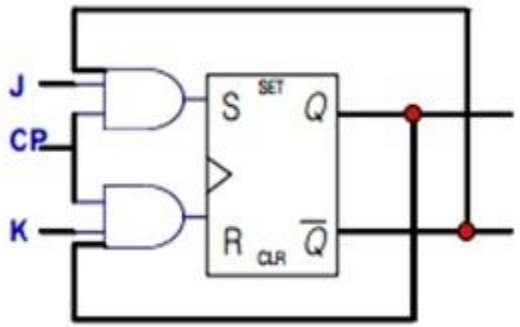
- SR*(Set/Reset)* F/F



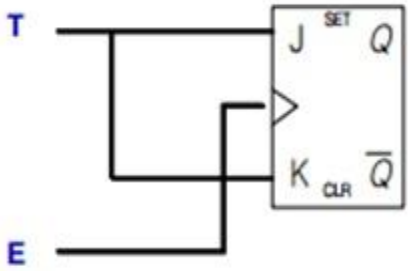
- D*(Data)* F/F



- JK*(Jack/King)* F/F

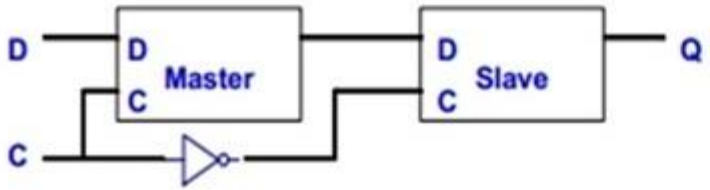


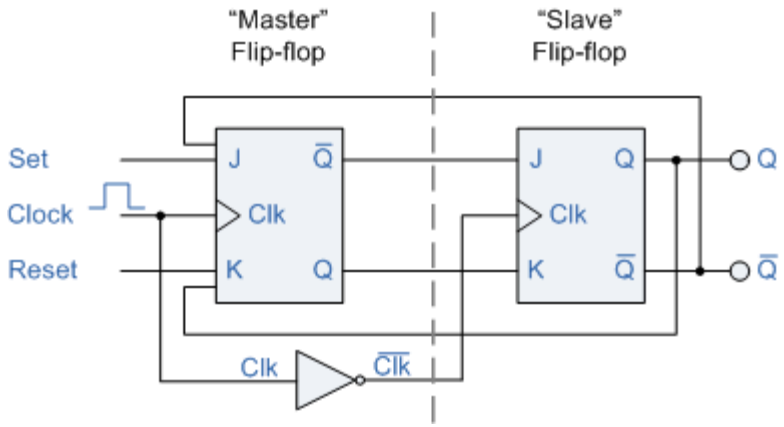
- T*(Toggle)* F/F

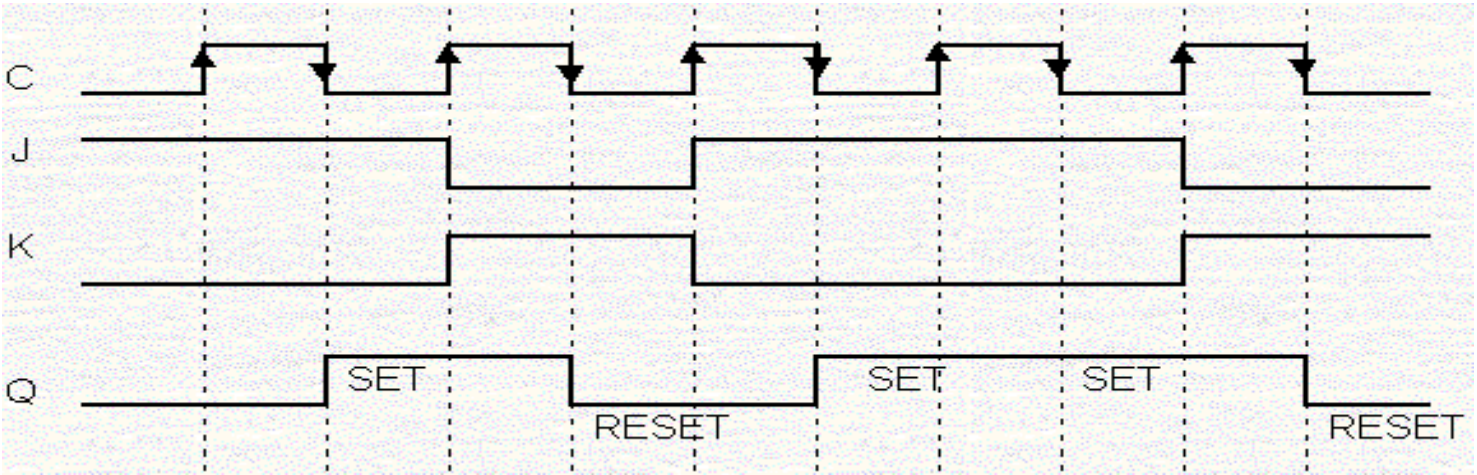


1-6 Flip-Flops

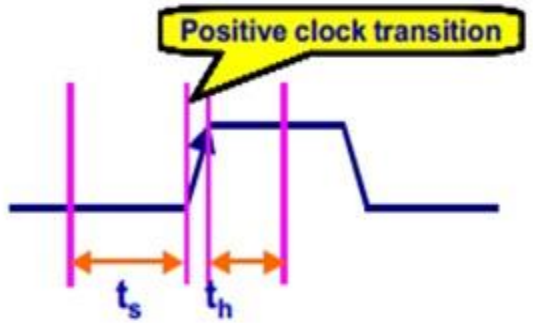
- Master – Slave D*(Data)* F/F







1-6 Flip-Flops



- Edge-Triggered F/F
  - State Change : *Clock Pulse*
    - Rising Edge(positive-edge transition)
    - Falling Edge(negative-edge transition)
  - Setup time(20ns)
    - minimum time that D input must remain at constant value before the transition.
  - Hold time(5ns)
    - minimum time that D input must not change after the positive transition.
  - Propagation delay(max 50ns)
    - time between the clock input and the response in Q
  - Master-Slave F/F

Master Slave flip flop are the cascaded combination of two flip-flops among which the first is designated as master flip-flop while the next is called slave flip-flop

Integrated Circuits

An IC is a small silicon semiconductors crystal called chip containing the electronic components for digital gates.

- Various gates are interconnected inside chip to form required circuit.
- Chip is mounted in ceramic/plastic container connected to external pin

Small scale Integration (SSI) : less than 10 gates

Medium Scale Integration(MSI) : between 10 to 200 gates (decoders, adders, registers)

Large Scale Integration(LSI) : between 200 and few thousands gates (Processors, Memory Chips)

Very Large Scale Integration (VLSI) : Thousands of gate within single package (Large Memory Arrays, Complex Microcomputer Chips)