Indian Institute of Information Technology, Allahabad

Assignment

"Low Power Design"

Submitted To:

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Submitted By:

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MEC2021040

Question:

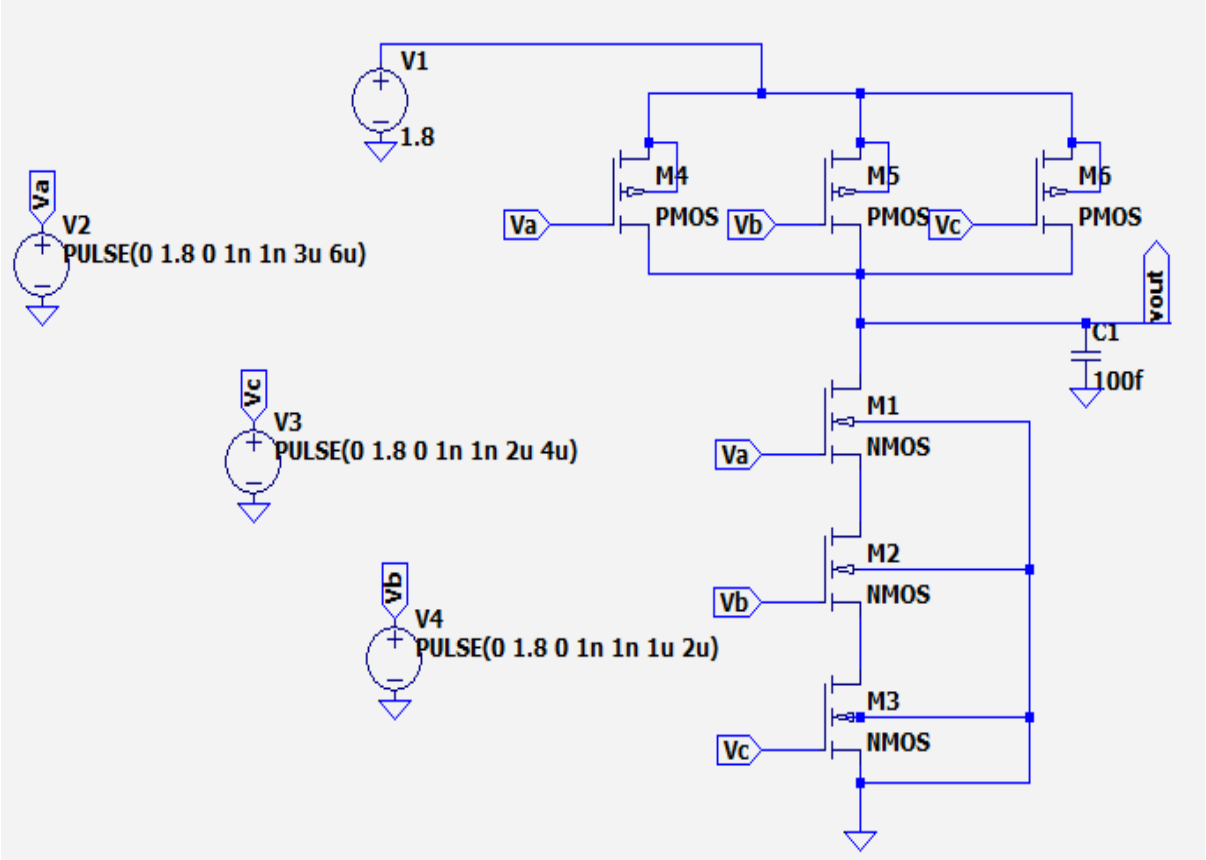
Design a 3-Input NAND or 3 – Input NOR.

1. Simulate & Compute the input pattern-dependent delay and leakage power (gate leakage, sub threshold leakage). Tabulate the results. Give the logical reasoning for the different values of delays, gate leakage & sub threshold leakage for each combination of inputs.

2. Compute the net power consumption. Make a diagram that should mention the contribution of each power component (dynamic, static, leakage).

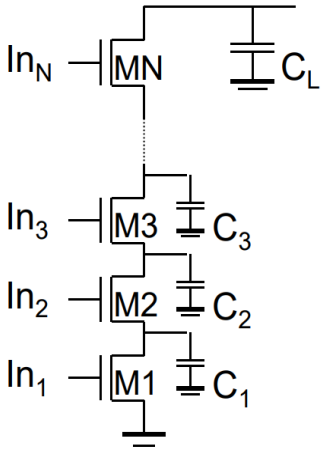
3. Optimize the design for optimal PDP and compute the PDP.

Designing of 3 Input NAND Gate:



W/L RATIO: (Optimized Circuit using Progressive Sizing)

- Progressive sizing



Distributed RC line

M1 > M2 > M3 > … > MN

(the FET closest to the *output* should be the smallest)

Can reduce delay by more than 20%; decreasing gains as technology shrinks

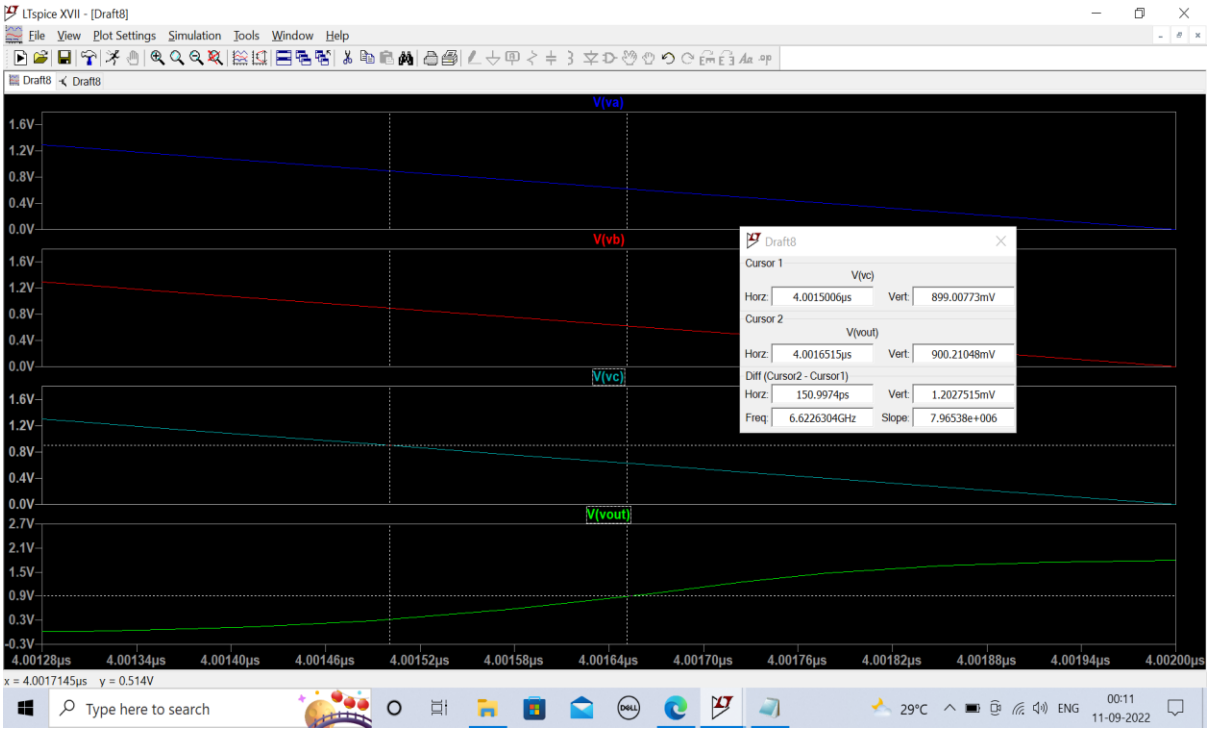
The sizing for NAND gate using PTM 90nm Technology file

SPICE NETLIST:

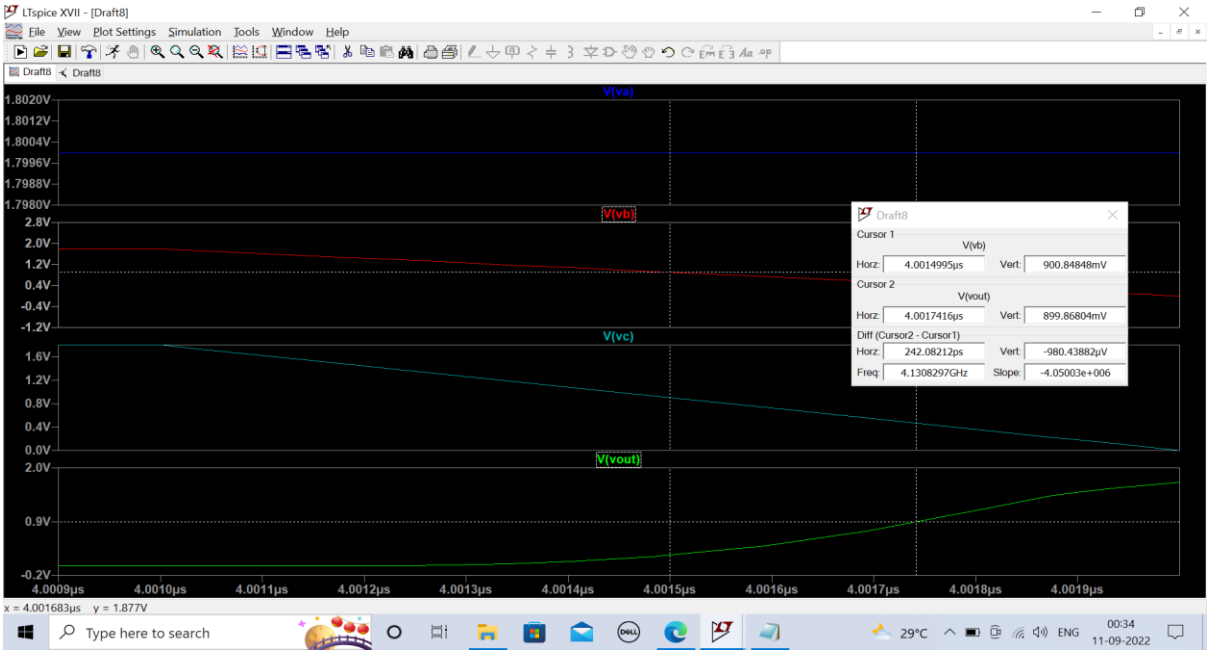
```
* C:\Users\vrake\OneDrive\Desktop\New folder\Draft8.asc
M1 vout Va N002 0 NMOS l=180n w=360n
M2 N002 Vb N003 0 NMOS l=180n w=540n
M3 N003 Vc 0 0 NMOS l=180n w=900n
M4 N001 Va vout N001 PMOS l=180n w=1440n
M5 N001 Vb vout N001 PMOS l=180n w=1440n
M6 N001 Vc vout N001 PMOS l=180n w=1440n
V1 N001 0 1.8
V2 Va 0 PULSE(0 1.8 0 1n 1n 3u 6u)
V3 Vc 0 PULSE(0 1.8 0 1n 1n 2u 4u)
V4 Vb 0 PULSE(0 1.8 0 1n 1n 1u 2u)
C1 vout 0 100f
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\vrake\OneDrive\Documents\LTspiceXVII\lib\cmp\standard.mos
.model  NMOS NMOS  level = 54
+version = 4.0          binunit = 1           paramchk= 1           mobmod  = 0
+capmod  = 2            igcmod  = 1           igbmod  = 1           geomod  = 1
+diomod  = 1            rdsmod  = 0           rbodymod= 1           rgatemod= 1
+permod  = 1            acnqsmod= 0           trnqsmod= 0
+tnom    = 27           toxe    = 2.05e-9     toxp    = 1.4e-9      toxm    = 2.05e-9
+dtox    = 0.65e-9      epsrox  = 3.9         wint    = 5e-009      lint    = 7.5e-009
+ll      = 0            wl      = 0           lln     = 1           wln     = 1
+lw      = 0            ww      = 0           lwn     = 1           wwn     = 1
+lwl     = 0            wwl     = 0           xpart   = 0           toxref  = 2.05e-9
+xl      = -40e-9
+vth0    = 0.397        k1      = 0.4         k2      = 0.01        k3      = 0
+k3b     = 0            w0      = 2.5e-006    dvt0    = 1           dvt1    = 2
+dvt2    = -0.032       dvt0w   = 0           dvt1w   = 0           dvt2w   = 0
+dsub    = 0.1          minv    = 0.05        voffl   = 0           dvtp0   = 1.2e-009
```

Pattern Dependent Delay for Different Inputs:

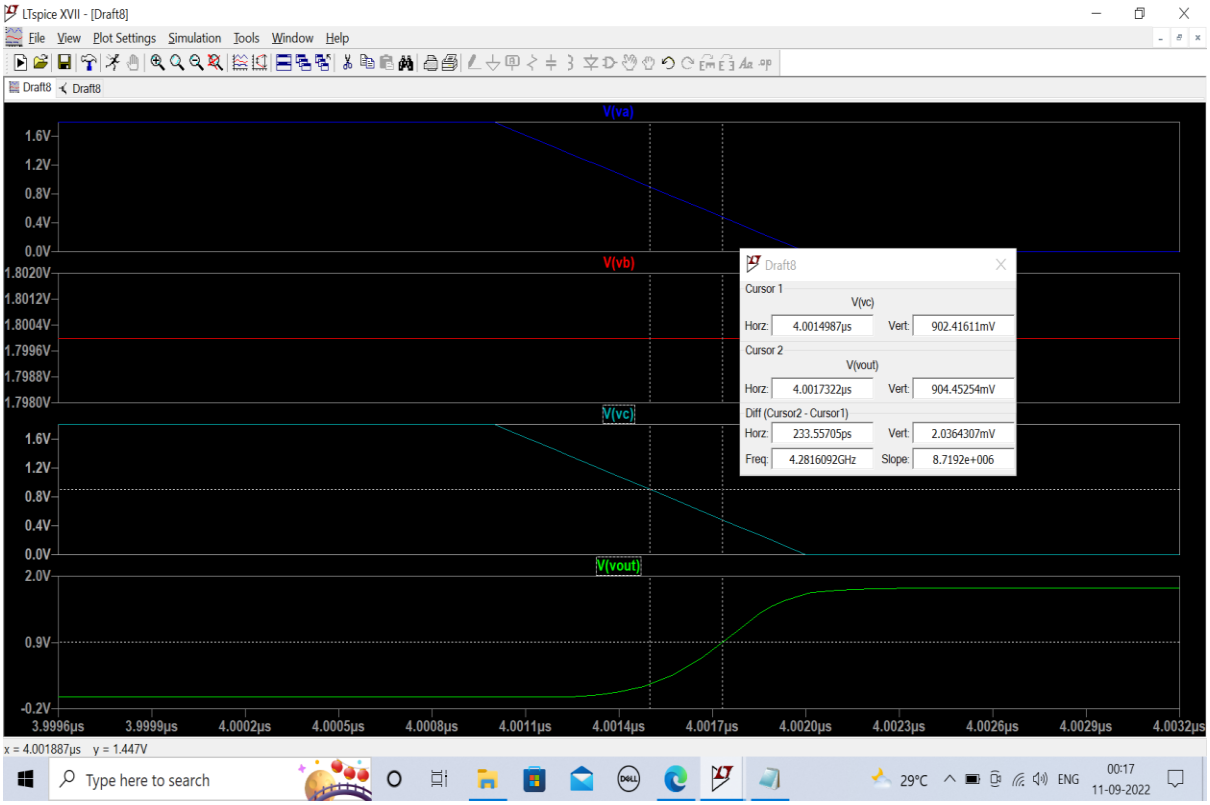
1. For I/P (0, 0, 0)



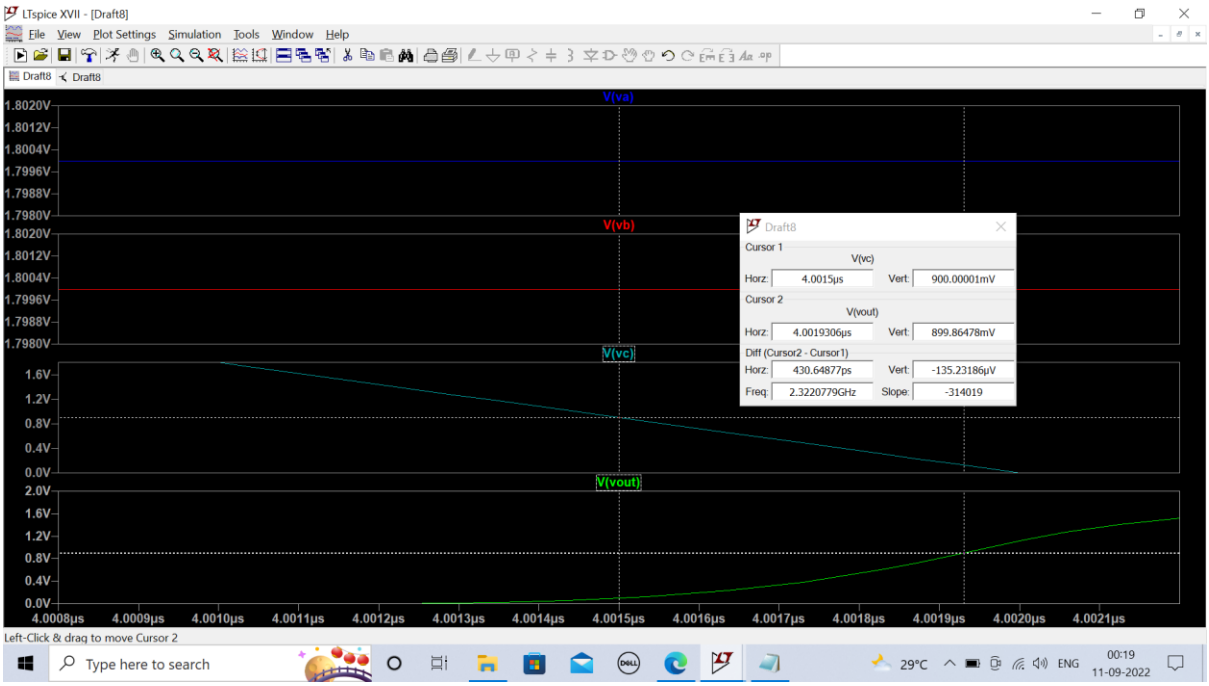
2. For I/P (0, 0, 1)



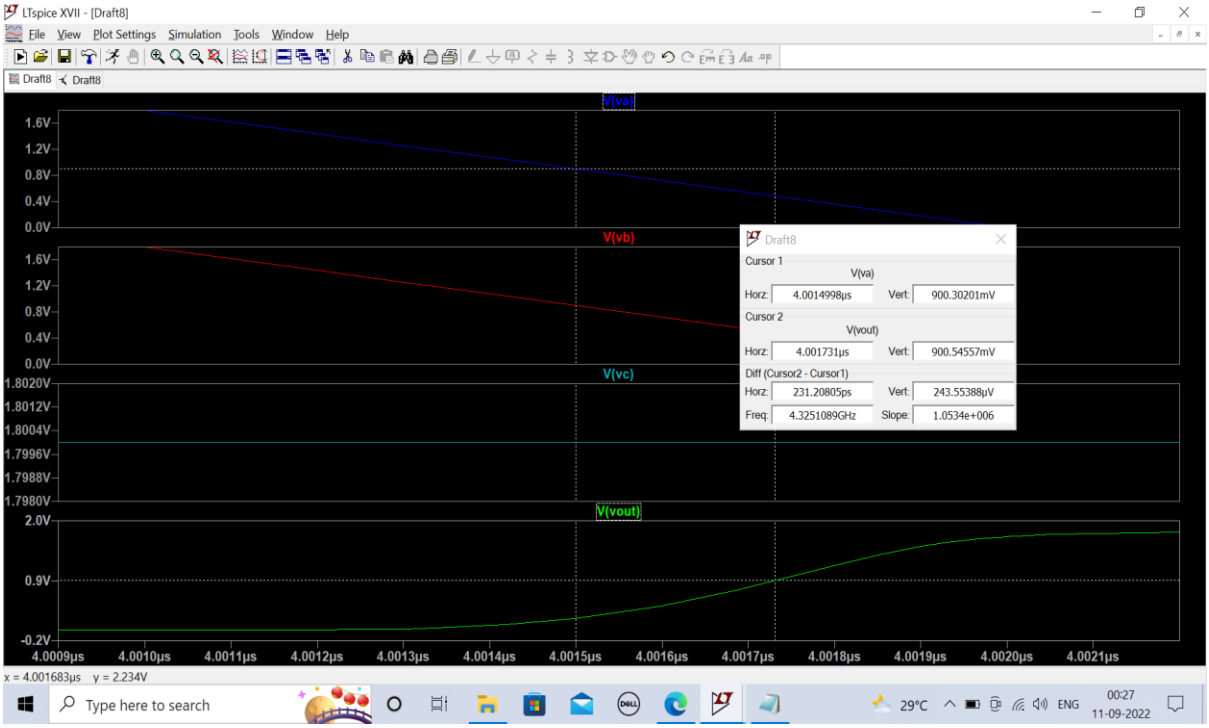
3. For I/P (0, 1, 0)



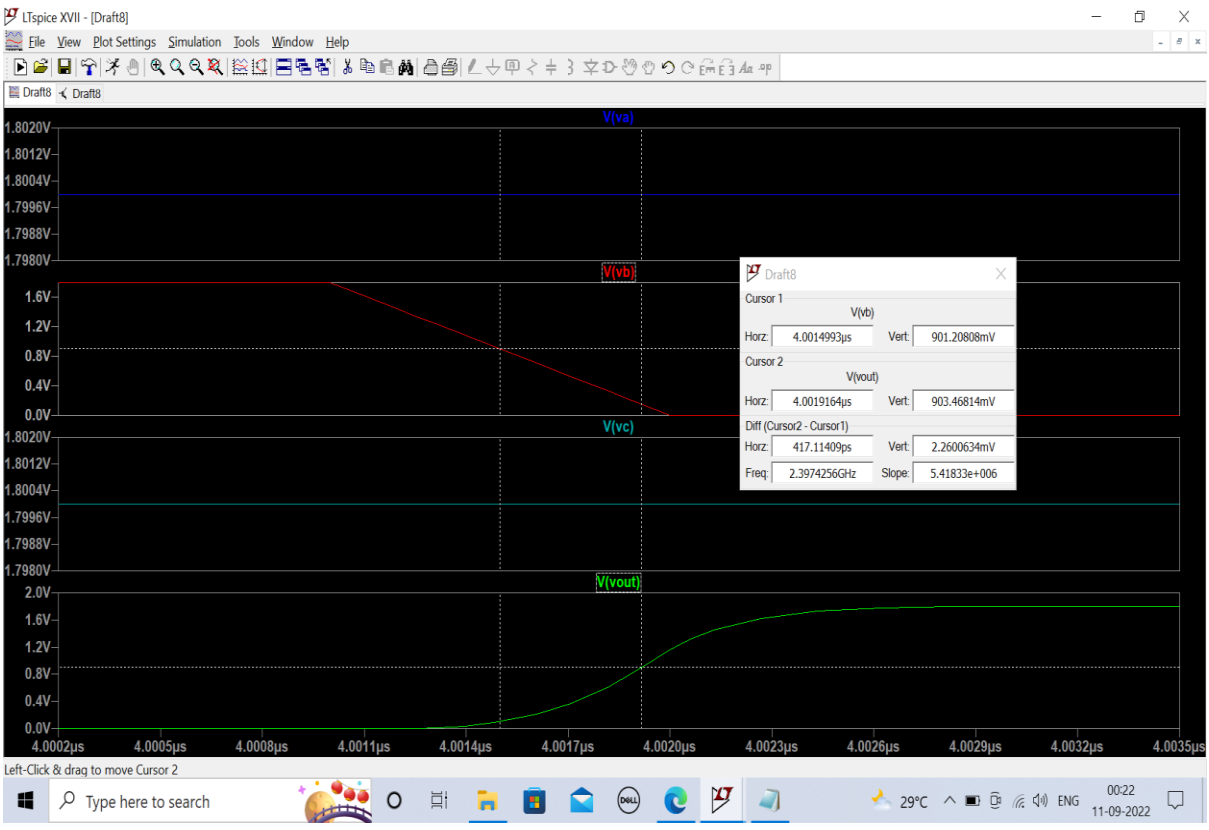
4. For I/P (0, 1, 1)



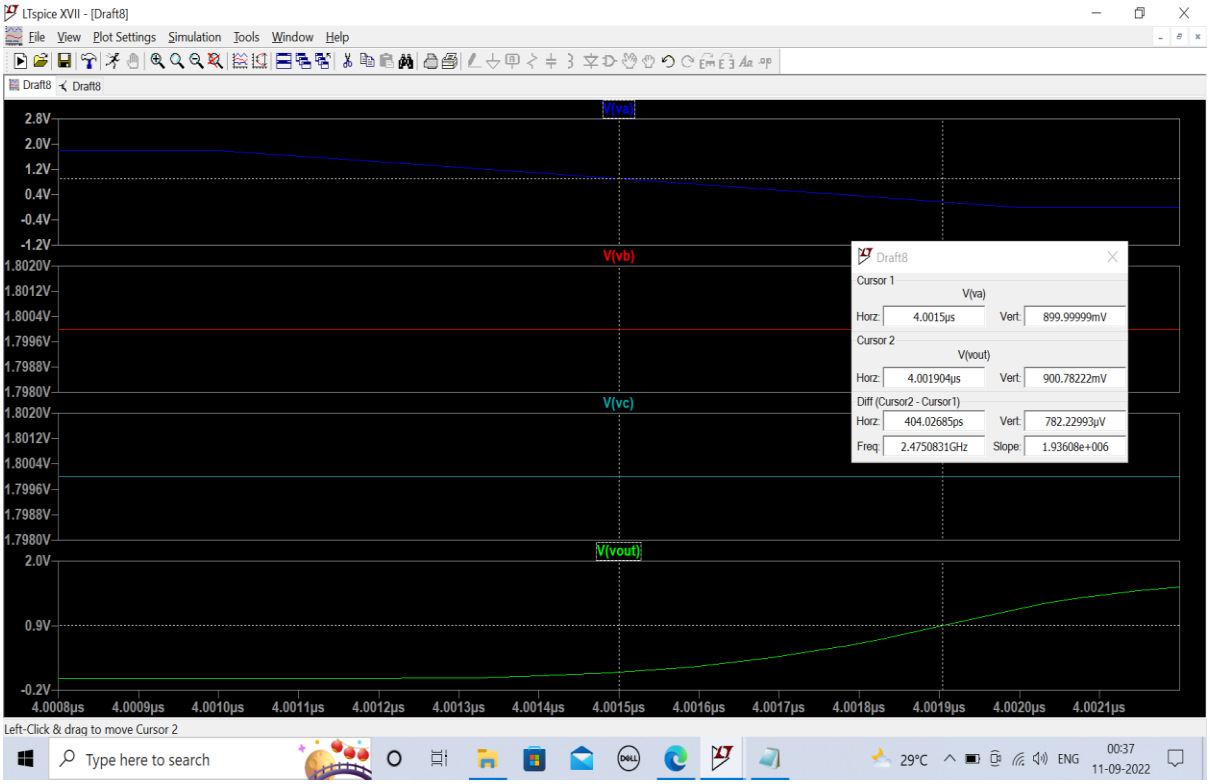
5. For I/P (1, 0, 0)



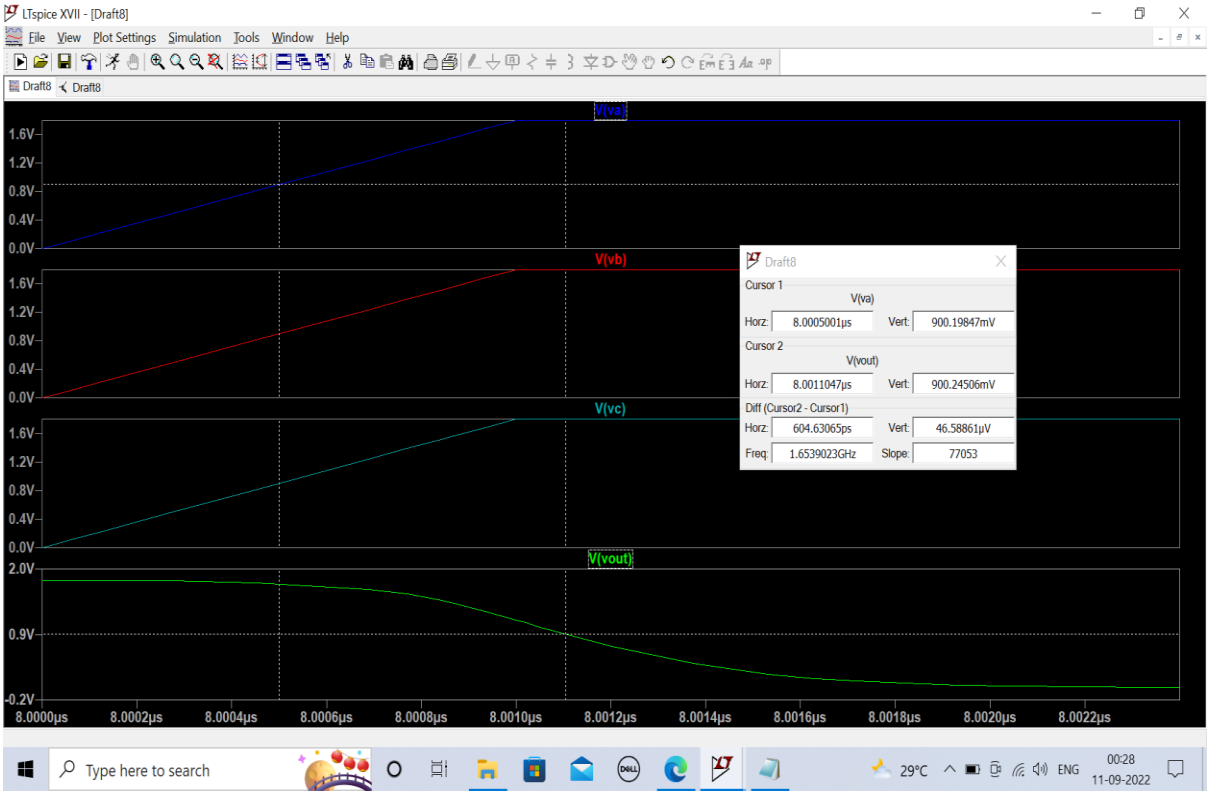
6. For I/P (1, 0, 1)



7. For I/P (1, 1, 0)



8. For I/P (1, 1, 1)



Pattern Dependent Delay for different Input Supply Voltage:

The total standby current is equal to the sum of Isub through the PMOS transistors and I gate through the NMOS transistors. However, for input states where at least one input is low and the gate output is high, Isub through turned-off transistors and I gate through turned-on transistors combine at internal stack nodes. Isub and I gate are therefore interdependent in these cases, and must be analyzed simultaneously.

Delay is dependent on the pattern of inputs

- 1st order approximation of delay:

  T propagation delay ≈ 0.69*R effective* CL

- R effective depends on the input pattern

S. No.	Input Voltage (Vc, Vb, Va)	Output Delay (Pico second)
1	0 0 0	150.99
2	0 0 1	242.08
3	0 1 0	233.55
4	0 1 1	430.64
5	1 0 0	231.20
6	1 0 1	417.11
7	1 1 0	404.02
8	1 1 1	604.63

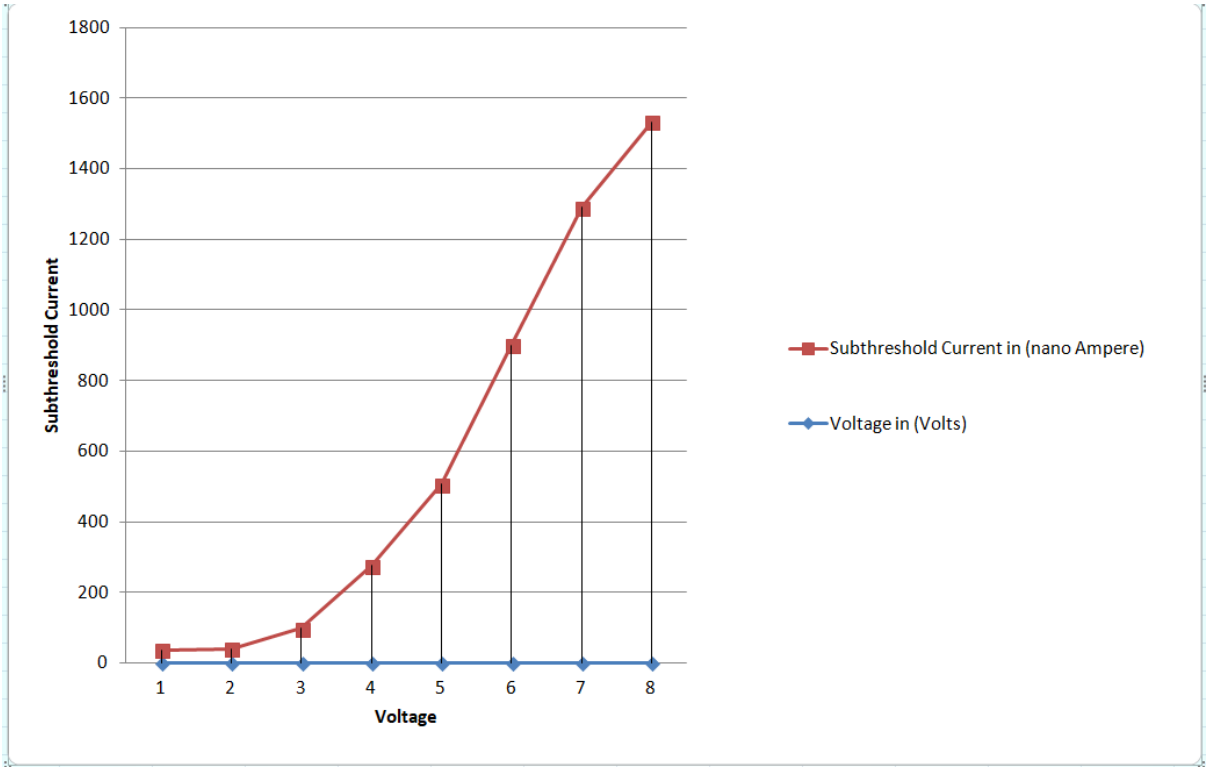
Sub-threshold Current:

Sub-threshold current is the current between the source and drain of a MOSFET when the transistor is in sub-threshold region, or weak-inversion region, that is for gate-to-source voltages below the threshold voltage.

Table for Sub-threshold voltage versus increase in input voltage:

1	Voltage in (Volts)	Subthreshold Current in (nano Ampere)
2	0.1	36.44
3	0.2	40.61
4	0.25	97.61
5	0.3	275.53
6	0.33	505.93
7	0.36	899.11
8	0.38	1289.5
9	0.39	1532.2

Graph for Sub-threshold voltage versus increase in input voltage:



Power Calculations:

Sources of power dissipation

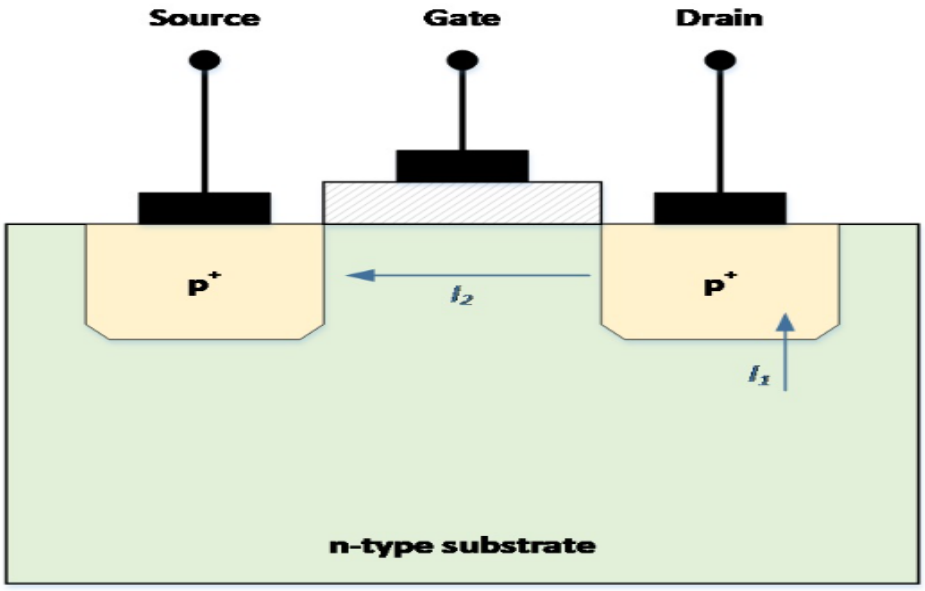
The power consumed in a VLSI circuit can be broadly classified into two types – Static power dissipation and Dynamic power dissipation.

1. Static Power

Static power is the power consumed when there is no circuit activity or you can say, when the circuit is in quiescent mode. In the presence of a supply voltage, even if we withdraw the clocks and don't change the inputs to the circuit, the circuit will still consume some power, called the static power consumption.

It is mainly due to the leakage currents that flow, when the transistor is in off-state. There are many types of leakage currents, however in the diagram below I have shown only two common leakage currents.

Reverse bias leakage current flows when the junction diodes within the transistors are reverse biased. Similarly sub-threshold leakage current flows from drain to source through the channel, when $V_{GS} \sim V_{th}$ [V_{th} is the threshold voltage of the transistor]. Typically the leakage power dissipation in a transistor is inversely proportional to its threshold voltage.



I_1 = Reverse Bias current
I_2 = Subthreshold current

Pattern Dependent Gate Current and Sub threshold current:

However, an undesirable leakage current can flow between the drain and the source. The MOSFET current observed at Vgs < Vt is called the sub-threshold current. This is the main contributor to the MOSFET off-state current, I off. continuous down-scaling of the device size has lead to very thin gate oxides, the leakage current that can flow from the channel to the gate comes into the order of the sub-threshold leakage current and the gate cannot be considered as an ideally insulated electrode anymore.

I/P Pattern (Vc,Vb,Va)	**Ig** (Gate Leakage) (nA)	**Isub** (Sub-threshold Current) (nA)	**Is** (total static current) (nA)	**Power**(static) **Vdd*Is** (nW)	**PDP** (power delay product) (nW*pSec)
0 0 0	0	0	0	0	0
0 0 1	0	0.505	0.505	0.909	220.05
0 1 0	1.29	0.505	1.795	3.23	754.36
0 1 1	8.68	1.01	9.69	17.442	7511.22
1 0 0	58	0.505	58.505	105.30	24346.2
1 0 1	57	1.01	58.01	104.418	43550.45
1 1 0	92	1.01	93.01	167.41	67636.98
1 1 1	114	1.5	115.5	207.9	125702.5

Total Average Static Power: 75.82nW

In general, the worst-case and best-case leakage states of common CMOS gates behave differently when both I sub and I gate are considered compared to Isub alone. Table showed that when only Isub is considered, the worst-case leakage state for NAND structures occurs when all inputs are high as the PMOS devices leak in parallel and sum.

For NOR structures, the reverse is true: all inputs set to low causes all NMOS devices to leak concurrently in parallel. For these two cases, we now include I gate. In NAND gates with all inputs tied high, the NMOS devices in the pull-down stack all exhibit worst-case I gate which adds to the large Isub of the PMOS devices to create a large total leakage current.

In the NOR gate with all inputs set to low, the PMOS devices have Vgd=Vgs=Vdd but since PMOS devices show very small I gate, the overall impact *will* be small. Meanwhile, the parallel pull-down devices exhibit only reverse edge direct tunnelling which is negligible. As a result of these trends, we find that the *range* of total leakage current across states is broadened for NAND gates and compressed for NORs.

Dynamic Power Calculation:

2. Dynamic Power

Dynamic power is the power consumed when the circuit is in operation, which means we have applied supply voltage, applied clock and changing the inputs.

It is mainly due to the dynamic currents, such as capacitance currents (switching power) and short-circuit currents (short-circuit power) as described below –

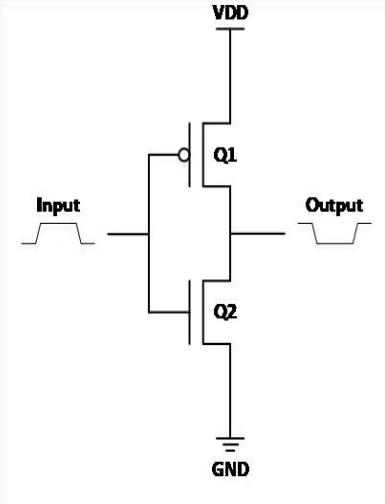
2.1. Switching power dissipation

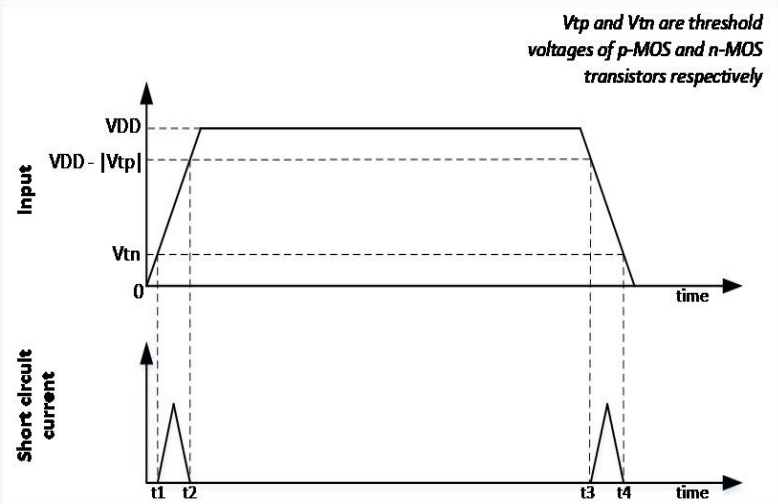
This is due to the charging and discharging of total load, which includes the output capacitors and other parasitic capacitors. At a very high level, we can say the switching power dissipation, $P_{dynamic} = \alpha.(V_{dd})^2.C_L.f$, where –

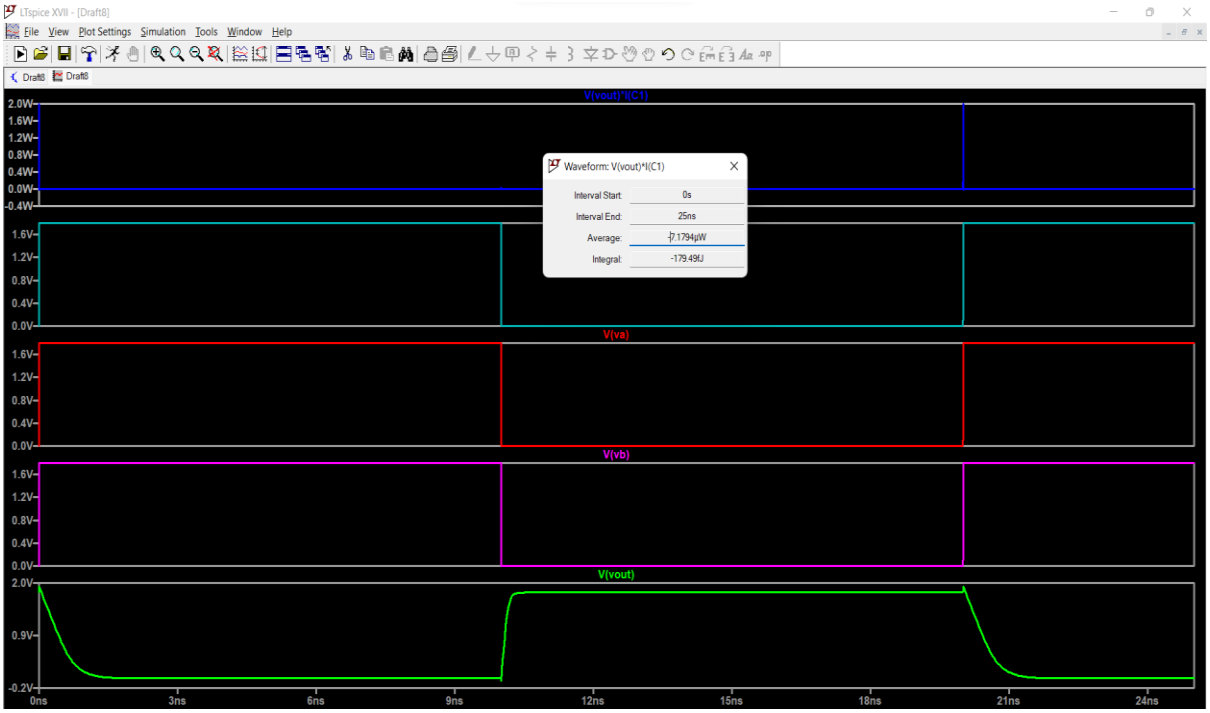
α = switching activity
V_{dd} = supply voltage
C_L = total load capacitance
f = frequency of operation

2.2. Short-circuit power dissipation

As the input changes slowly, there will be certain duration of time for which some of the transistor(s) in the pull-up network and pull-down network are turned 'ON' simultaneously, forming a short-circuit path from VDD to GND.







Total dynamic power: 7.17/14 = **512nW**

Dynamic power (theoretical calculation):

$P_{(dynamic)} = \alpha*(Vdd^2)*f*C_L$

$= (7/64)*(1.8)^2*100*10^6*100*10^{-15}$

$= 3.54\mu$ W

Comparison between Static and Dynamic Power: