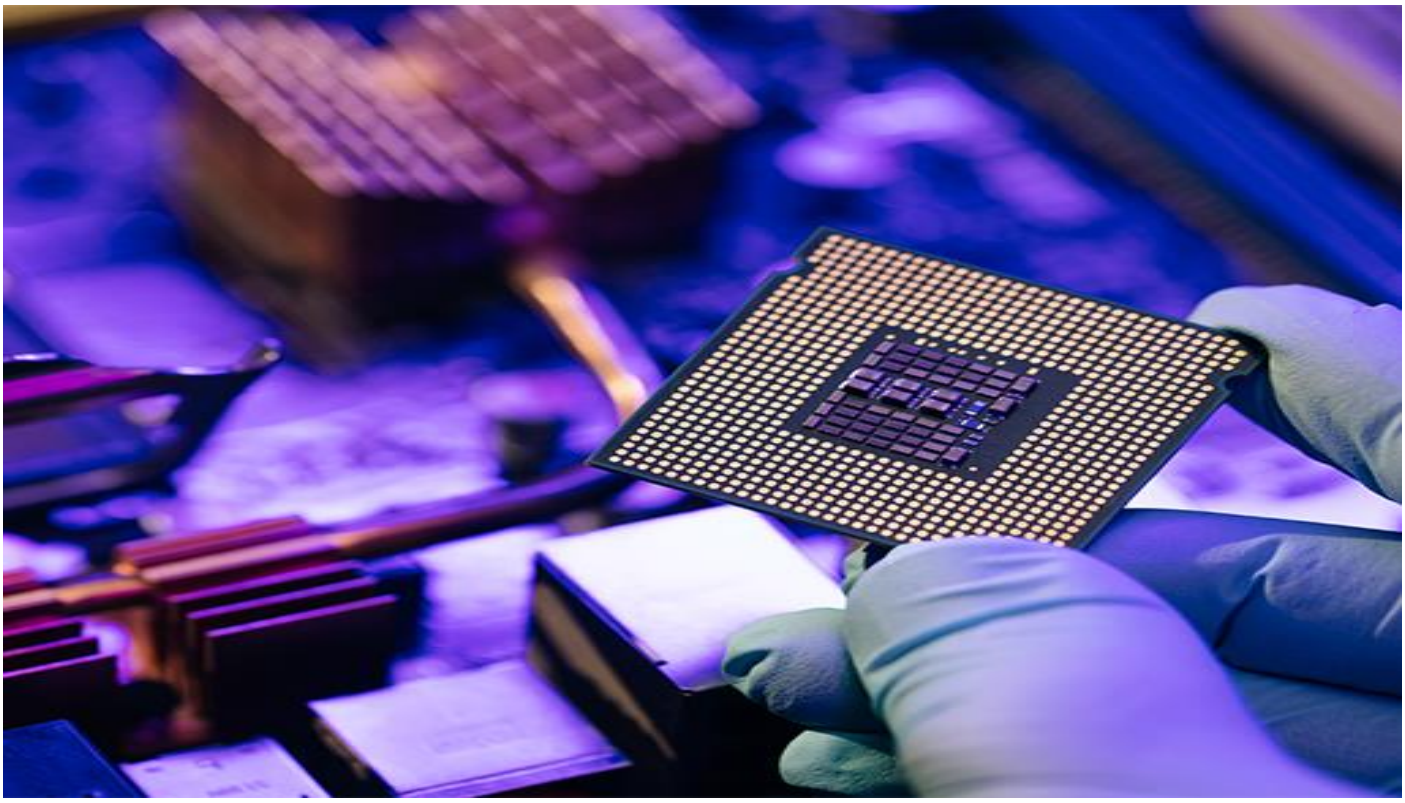
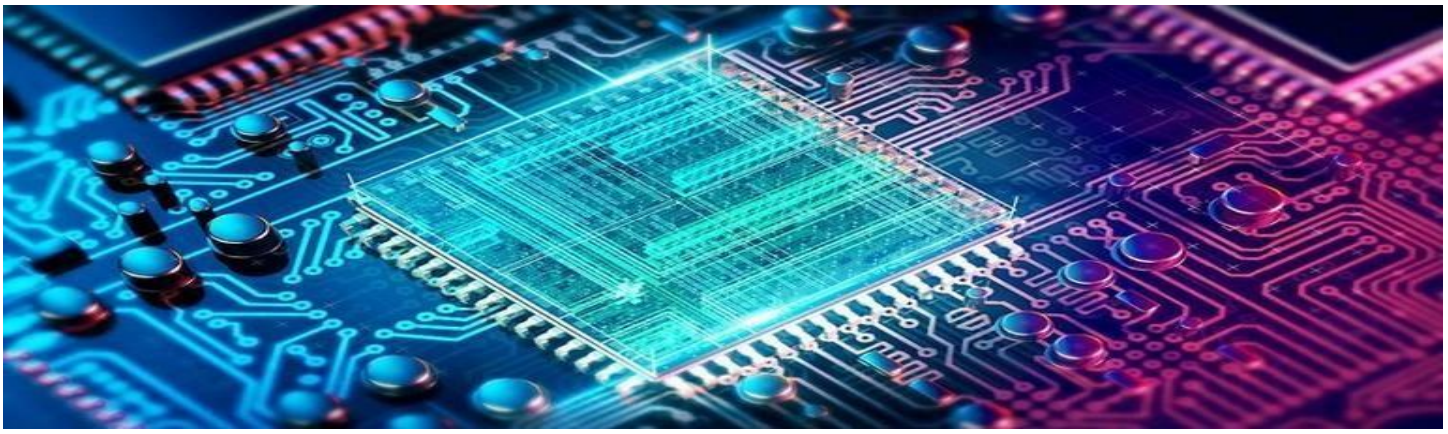


REPORT ON,

"CADENCE EXPERIMENTS"

SUBMITTED BY:

SHREE RAKSHA B N [BU21EECE0100552]



VLSI refers to the process of creating an integrated circuit (IC) by combining thousands or even millions of transistors onto a single chip. It's a pivotal technology in modern electronics manufacturing.

VLSI technology is the backbone of various electronic devices and systems, **its applications include,**

1. Microprocessors and microcontrollers
2. Memory chips (RAM, ROM, flash memory)
3. Digital signal processors (DSPs)
4. Application-specific integrated circuits (ASICs)
5. System-on-Chip (SoC) designs
6. Integrated circuits for telecommunications, networking, automotive, aerospace, and consumer electronics.

Front-end design, also referred to as RTL (register-transfer level) design, is the process of using high-level design languages like Verilog or VHDL to create a functional model of the system. Determining the system's logical behaviour and functional requirements, including inputs and outputs, data flow, and overall architecture, is the main goal of this design phase. Ensuring that the system will fulfil its functional requirements and specifications is largely dependent on the front-end design phase. Thefront-end design phase ends when the design is verified to meet the functional specifications and is finished.

The process of converting an RTL design into a physical layout that can be fabricated onto a chip is called **back-end design**, sometimes referred to as physical design. During this stage of the design process, the various components on the chip are placed and routed, and the design is optimized for power, performance, and other constraints. Ensuring that the design's physical implementation satisfies the system's performance, power, and other requirements is largely dependent on the back-end design phase.

The **Cadence tool** is a software suite used for designing and testing of system-on-chip (SoC) and integrated circuits (ICs). It provides a user-friendly interface for implementing, simulating, and testing complex analog, digital, and mixed-signal designs.

- **The key features of Cadence:**

1. **User Interface**: Cadence provides a customizable GUI that supports a wide range of tasks, from circuit design to simulation to implementation.

2. **Circuit Design**: Cadence uses a schematic-driven approach to design circuits, allowing designers to easily create and connect components, build hierarchies, and manage design variants.

3. **Simulation**: Cadence includes a suite of simulation tools that enable designers to verify their designs at various stages of the development process. It supports both analog and digital simulations with flexible and comprehensive analysis features.

4. **Layout Design**: Cadence allows designers to lay out the circuit in the physical domain using its layout editor. It supports hierarchical design, design rule checking (DRC), layout-versus-schematic (LVS), and extraction of parasitics.

5. **Design for Manufacturability (DFM):** Cadence provides a suite of tools for designing for manufacturability, including lithography simulation, stress management, and yield optimization.

6. **Integration:** Cadence can be integrated with other EDA tools, including HDL simulators, synthesis tools, and testbench generation tools.

Aim: To implement

1. Schematic and DC Simulation of a Resistive Voltage Divider

2. Schematic and Transient Analysis of a First Order RC Circuit

3. Study and Simulation of Operating Regions of a MOSFET

4. Schematic, Symbol and Simulation of a CMOS Inverter

5. Layout, DRC, LVS of a CMOS Inverter

6. Hierarchical Schematic and Simulation of a NAND, XOR, 1-biFulader

7. Schematic and Simulation of a D-Flip Flop

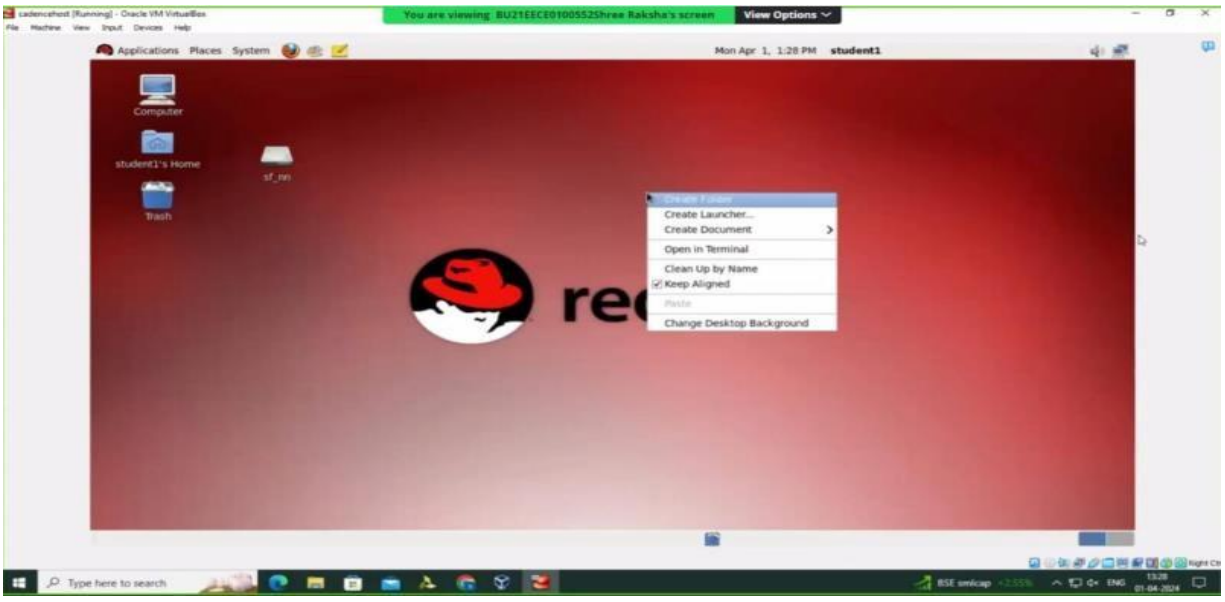
Apparatus: PC with Oracle VM virtual box.

Procedure:

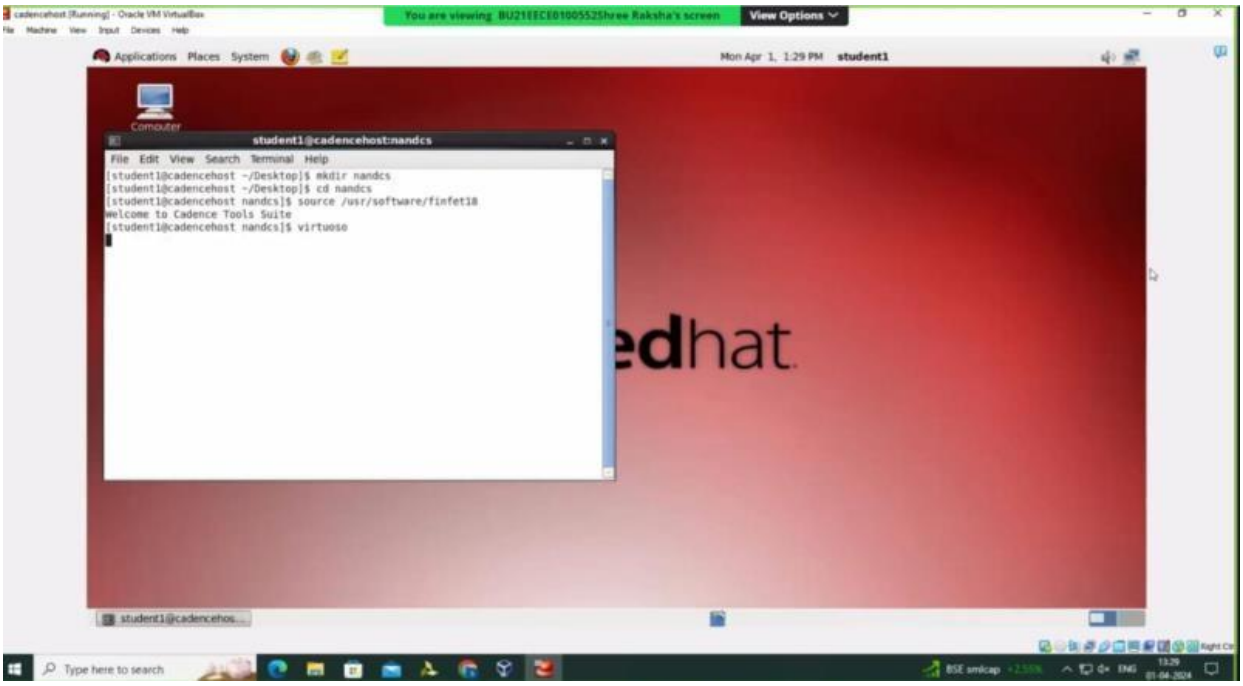
STEPS TO IMPLEMENT EXPERIMENT IN CADENCE VIRTUOSO TOOL

STEP-1: LIBRARY CREATION

- Open oracle VM virtual box.
- Click on start.
- Right click on workspace, select open in terminal.



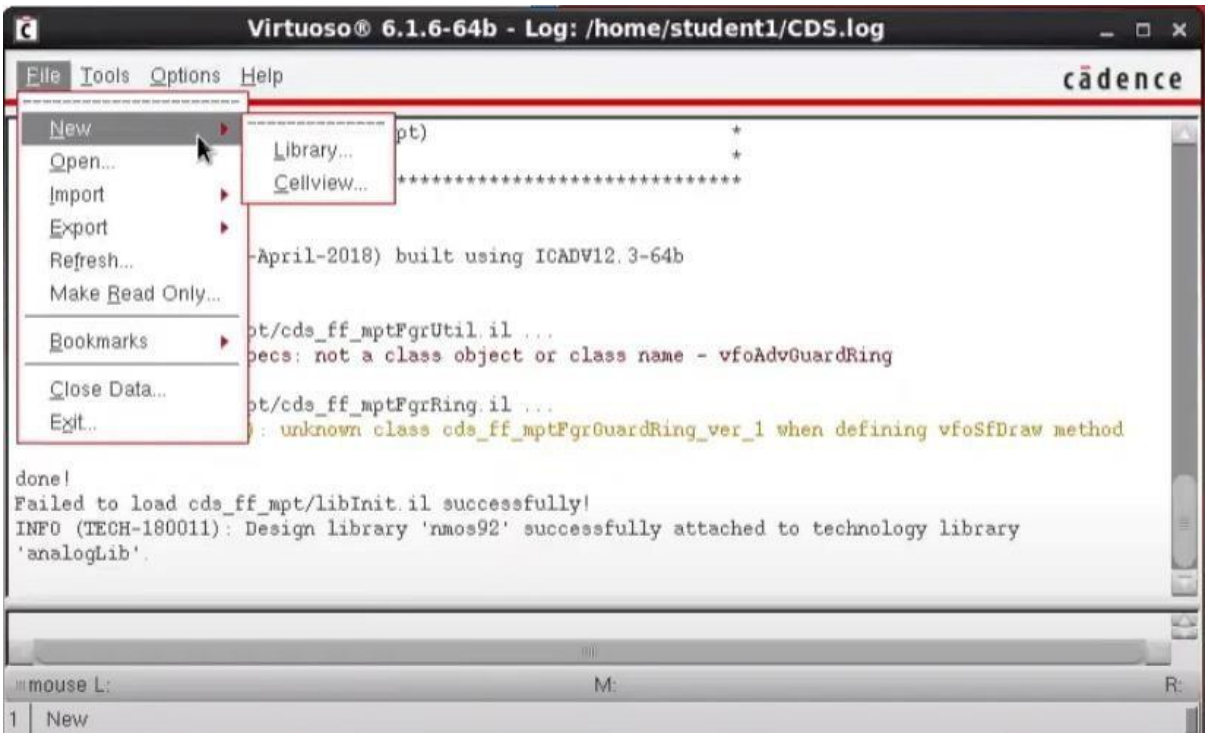
- Type the commands,



- Explanation the commands typed in the terminal:

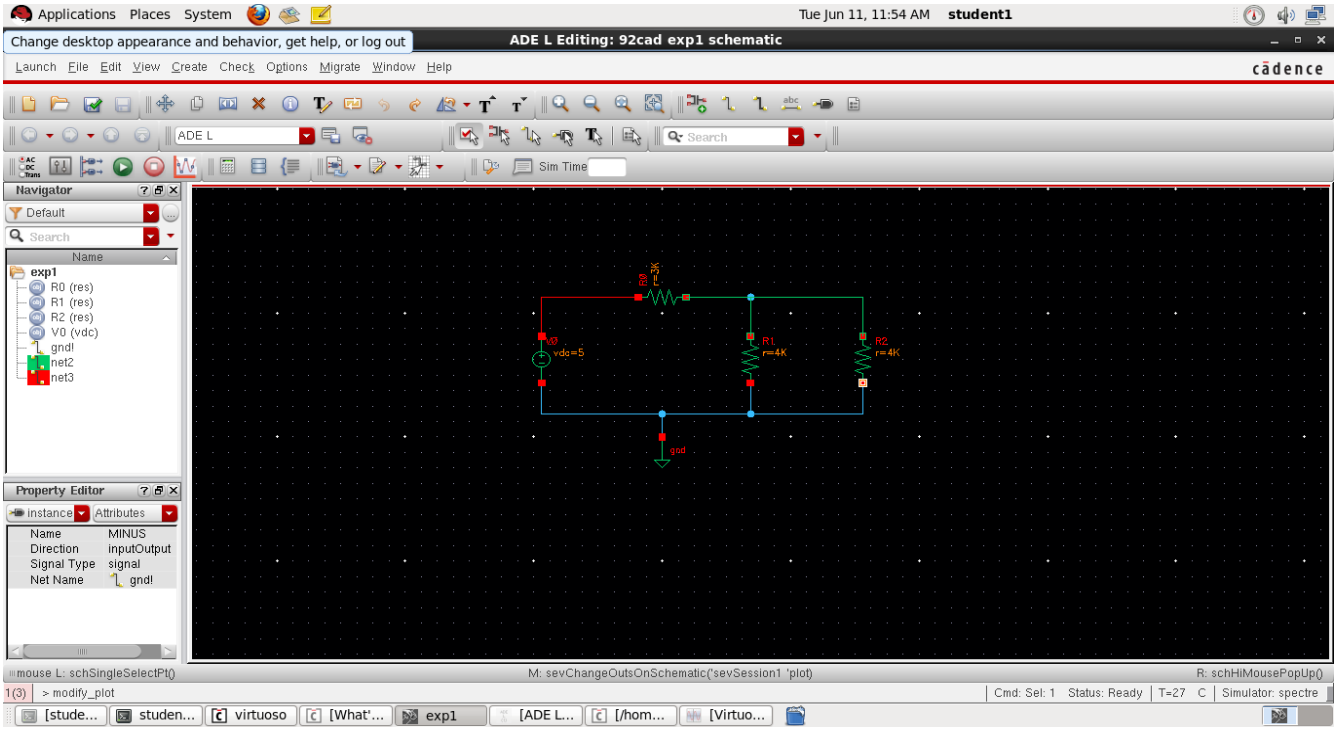
- **mkdir:** This command is used to create a new directory (folder) within the current directory.
- **cd:** Short for "change directory," this command is used to navigate between directories.
- **Source /usr/software/finfet18:** refers to a directory path where certain files or resources related to the Finfet18nm technology node are stored. Cadence provides design tools and solutions for integrated circuit (IC) design, and finfet technology is a type of transistor design used in modern semiconductor manufacturing processes.
- **virtuoso:** Virtuoso is a widely-used tool within Cadence for electronic design automation (EDA). It's primarily used for designing and simulating integrated circuits (ICs) and electronic systems. It includes various modules for schematic capture, layout editing, simulation, and more.
- Virtuoso tab appears
- In virtuoso tab
    - Tools>File>New>Library>select Attach to existing technology>Ok.

- Give any name. Select Attach to an existing technology library> Select analogLib>ok.

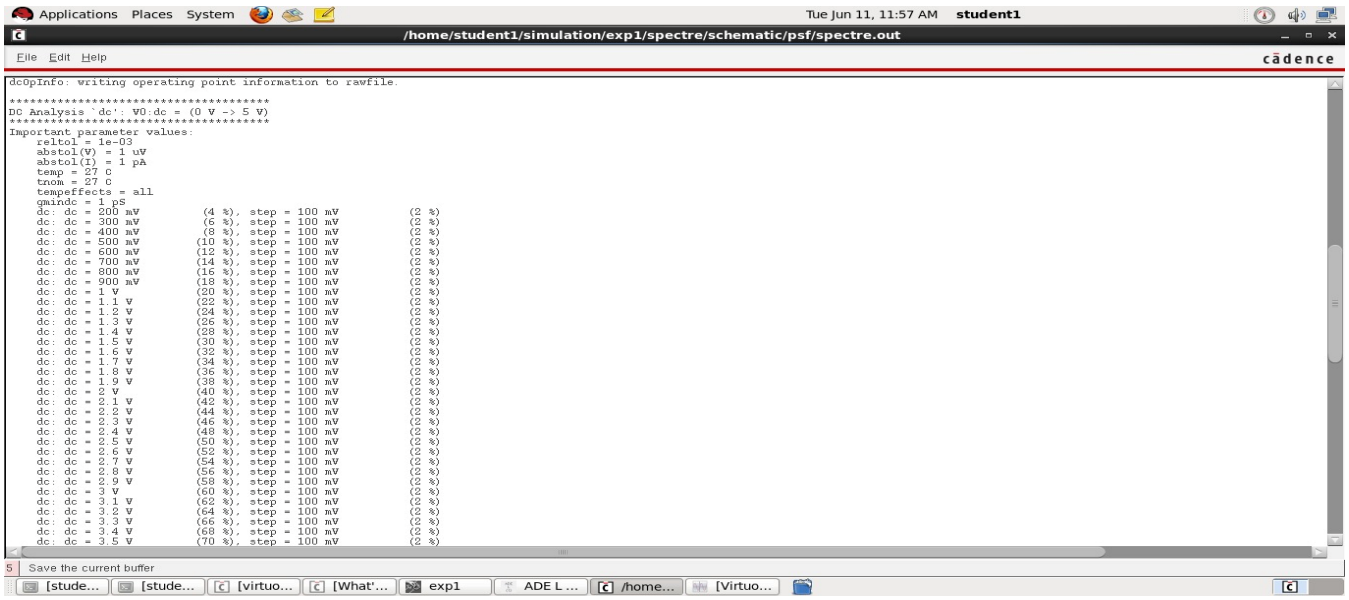

Virtuoso® 6.1.6-64b - Log: /home/student1/CDS.log
File Tools Options Help
cadence
New
Open...
Import
Export
Refresh...
Make Read Only...
Bookmarks
Close Data...
Exit...
Library...
Cellview...
pt) *
*
****
-April-2018) built using ICADV12.3-64b
pt/cds_ff_mptFgrUtil.il ...
pecs: not a class object or class name - vfoAdvGuardRing
pt/cds_ff_mptFgrRing.il ...
: unknown class cds_ff_mptFgrGuardRing_ver_1 when defining vfoSfDraw method
done!
Failed to load cds_ff_mpt/libInit.il successfully!
INFO (TECH-180011): Design library 'nmos92' successfully attached to technology library
'analogLib'.
mouse L:
M:
R:
1
New

EXP 1: SCHEMATIC AND DC SIMULATION OF A RESISTIVE VOLTAGE DIVIDER

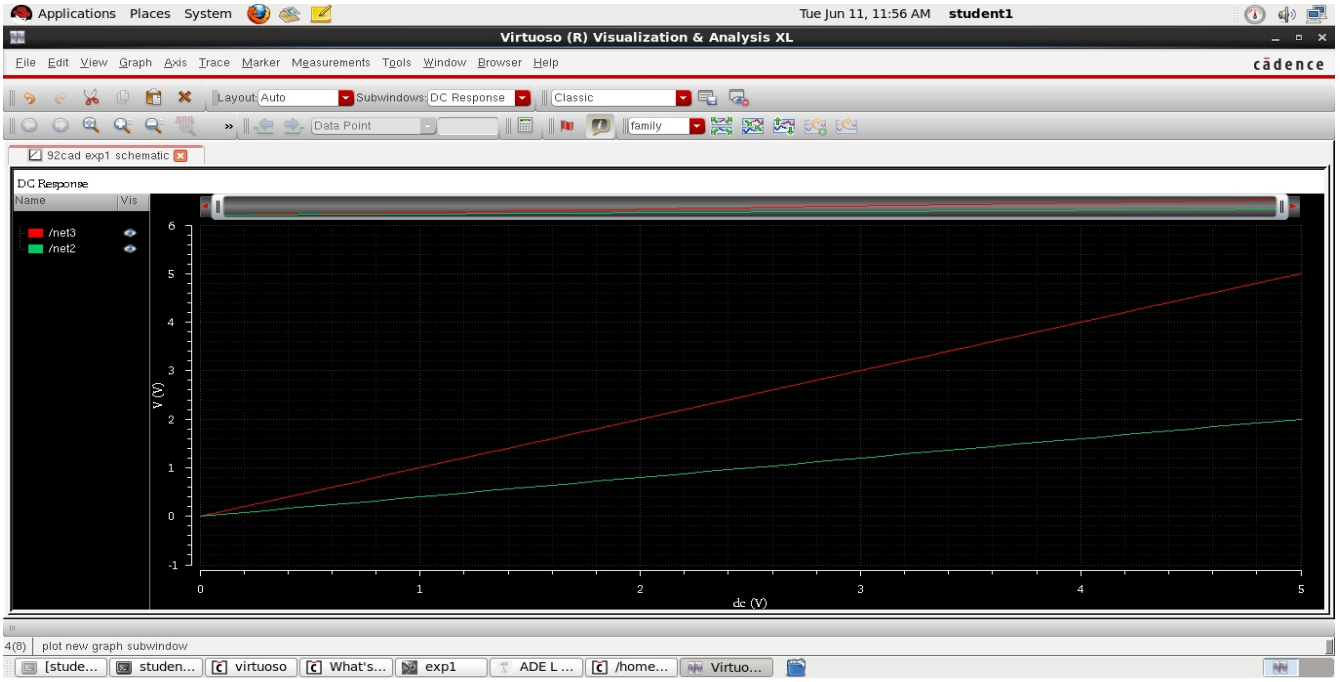
- File>New>cell view named voltage_divider
- Workspace opens> click on create instance > select the components.
- Add resistors R1 and R2, voltage source Vdc, and ground gnd
- Connect the circuit as shown in the figure,



- Launch ADE L and Configure DC Analysis
- Select Vout as output net and run simulation
- Values of a desired output



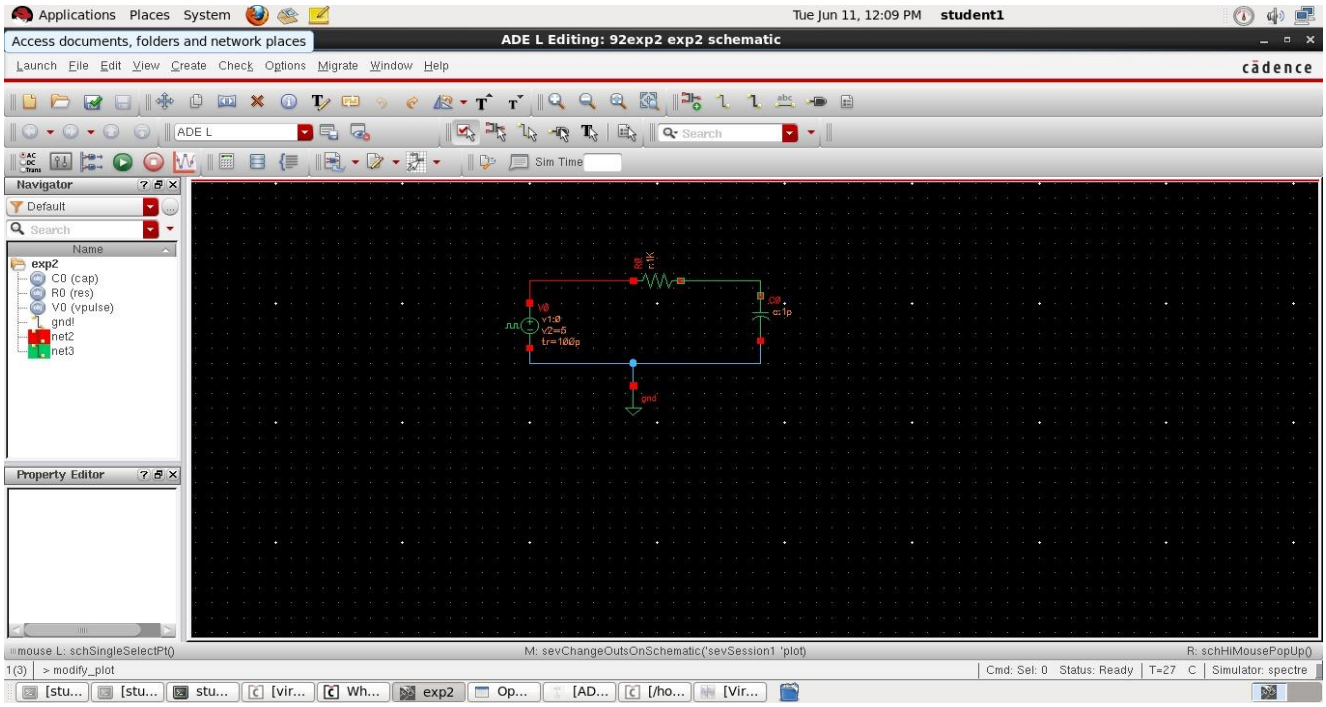
- Graph and final Result of the DC Simulation



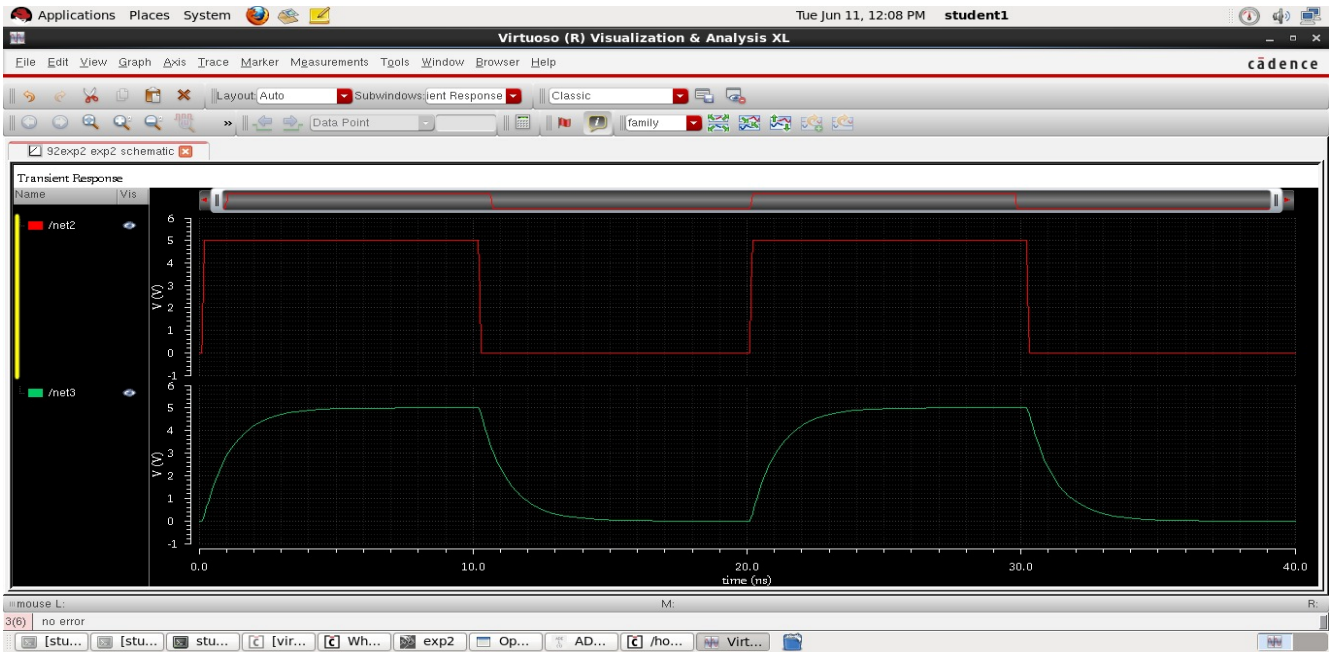
Conclusion: The schematic and DC Simulation of a resistive voltage divider were successfully implemented.

EXP 2: SCHEMATIC AND TRANSIENT ANALYSIS OF A FIRST ORDER RC CIRCUIT

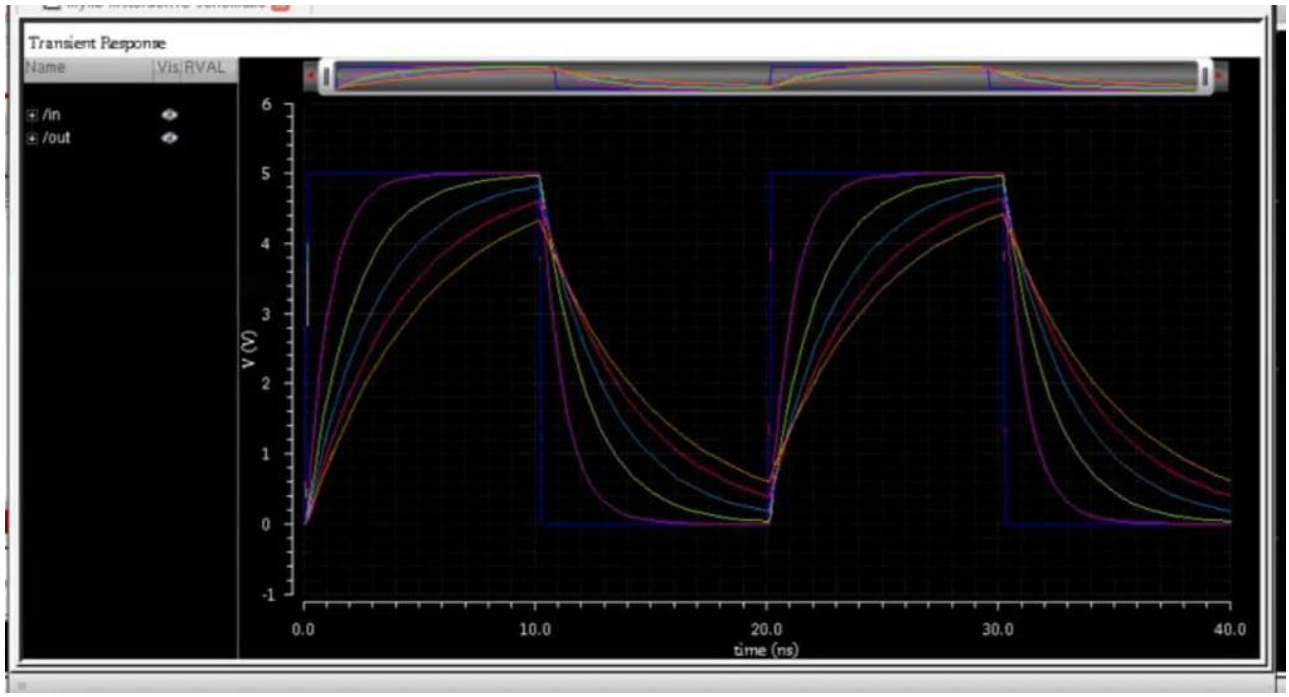
- File>New>cell view named rc_circuit
- Add a resistor R, a capacitor C, pulse voltage source Vpulse, ground Gnd
- Workspace opens> click on create instance > select the components.
- Connect the circuit as shown in the figure,



- Launch ADE L and configure Transient Analysis with a stop time of 2ms
- Select Vout as the output net and Run simulation
- Graph obtained



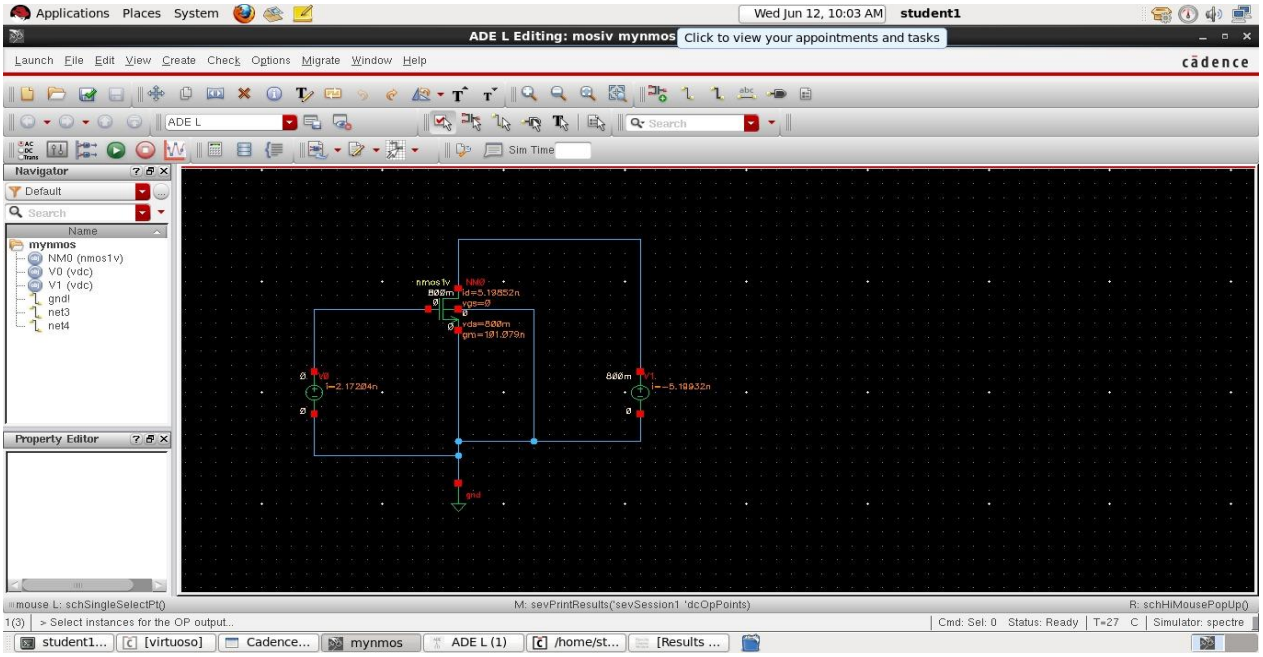
- Graph Final Results

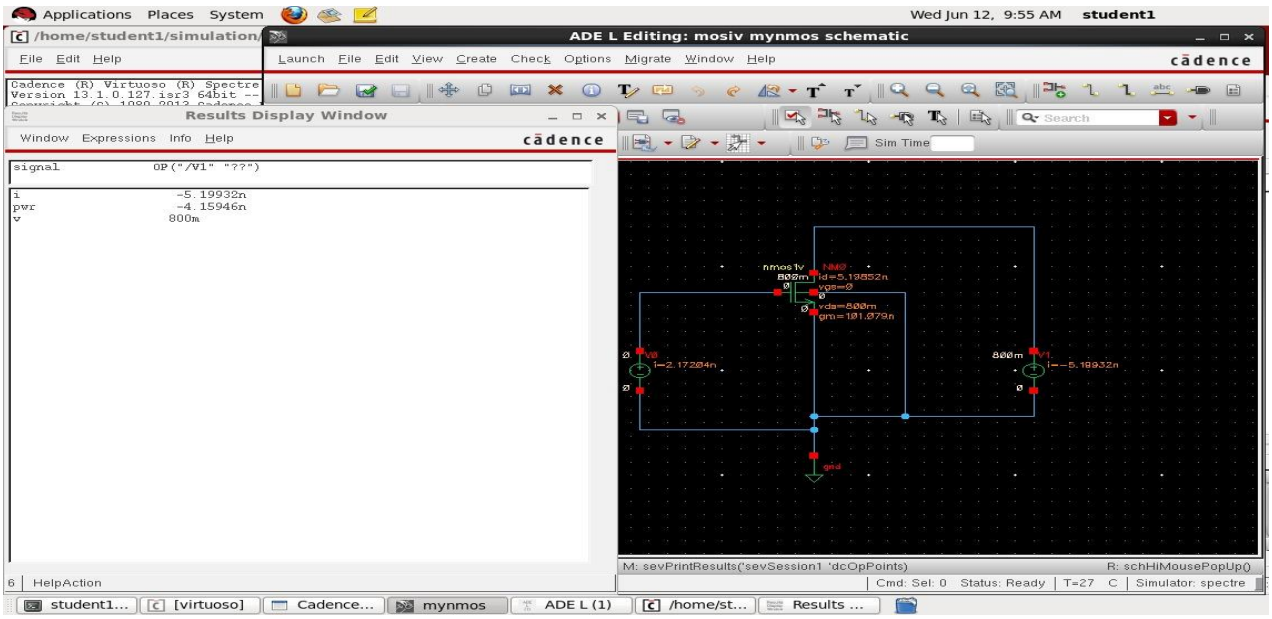


Conclusion: The schematic and transient analysis of a frist-order RC circuit were Successfully implemented.

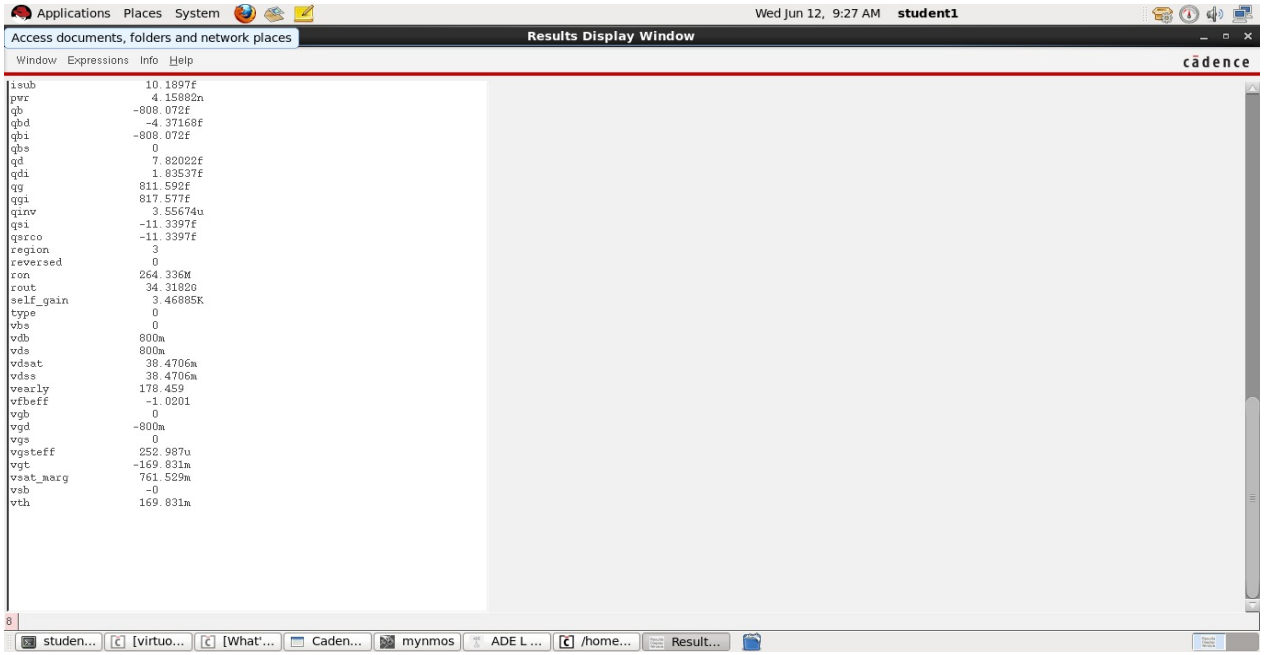
EXP 3: STUDY AND SIMULATION OF OPERATING REGIONS OF A MOSFET

- File>New>cell view named mosfet_study
- And a NMOS Transistor, a DC voltage source VDC, and ground Gnd to the schematic.
- Connect the components as per the MOSFET test circuit and name the wires appropriately.
- Workspace opens> click on create instance > select the components.
- Connect the circuit as shown in the figure,



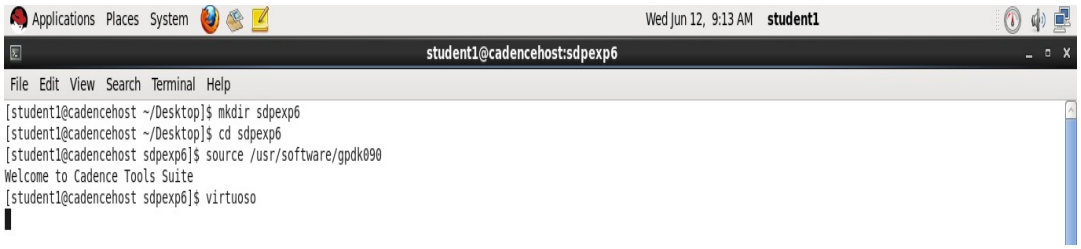


- Launch ADE L and configure DC Analysis
- Select IDE as the output net
- Connect the components as per the MOSFET test circuit and name the wires appropriately.
- Obtained values

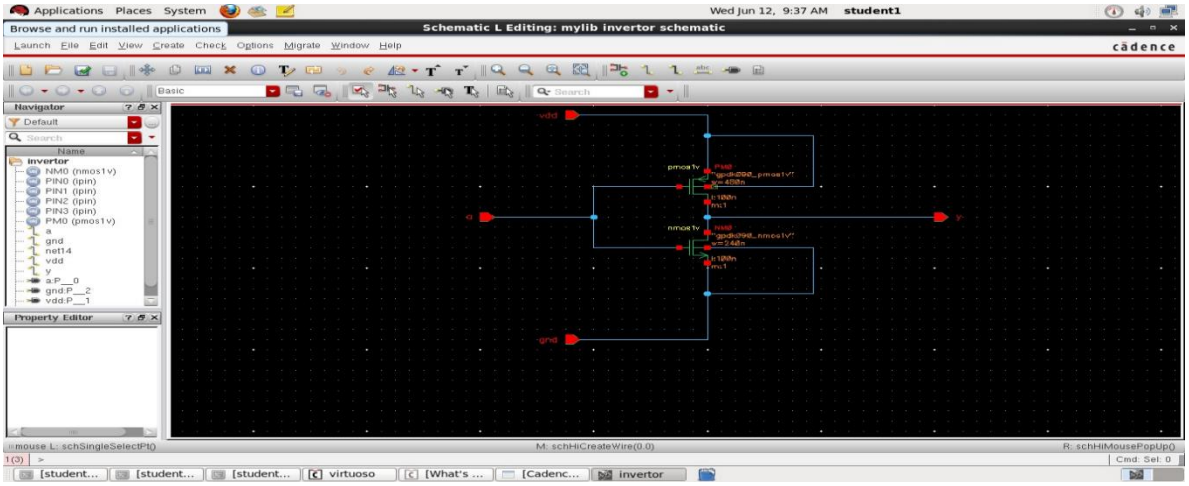


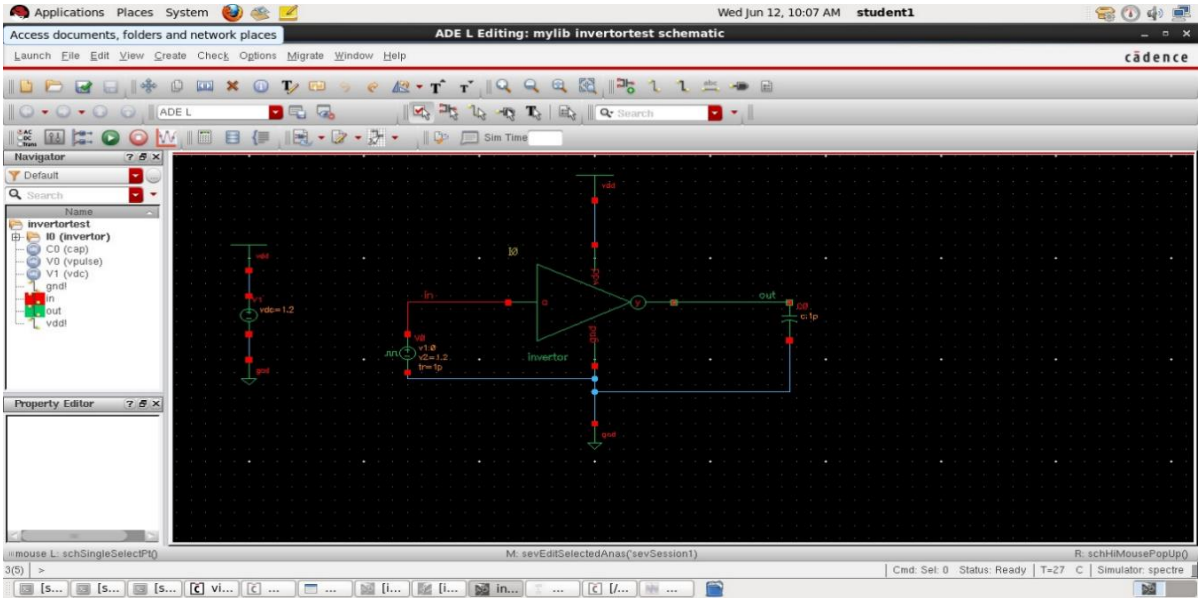
Conclusion: The study and simulation of the operating regions of a MOSFTE were successfully implemented. The simulation of a desired output.

EXP 4 & 5: SCHEMATIC, SYMBOL AND SIMULATION OF A CMOS INVERTER AND LAYOUT, DRC, LVS OF A CMOS INVERTER

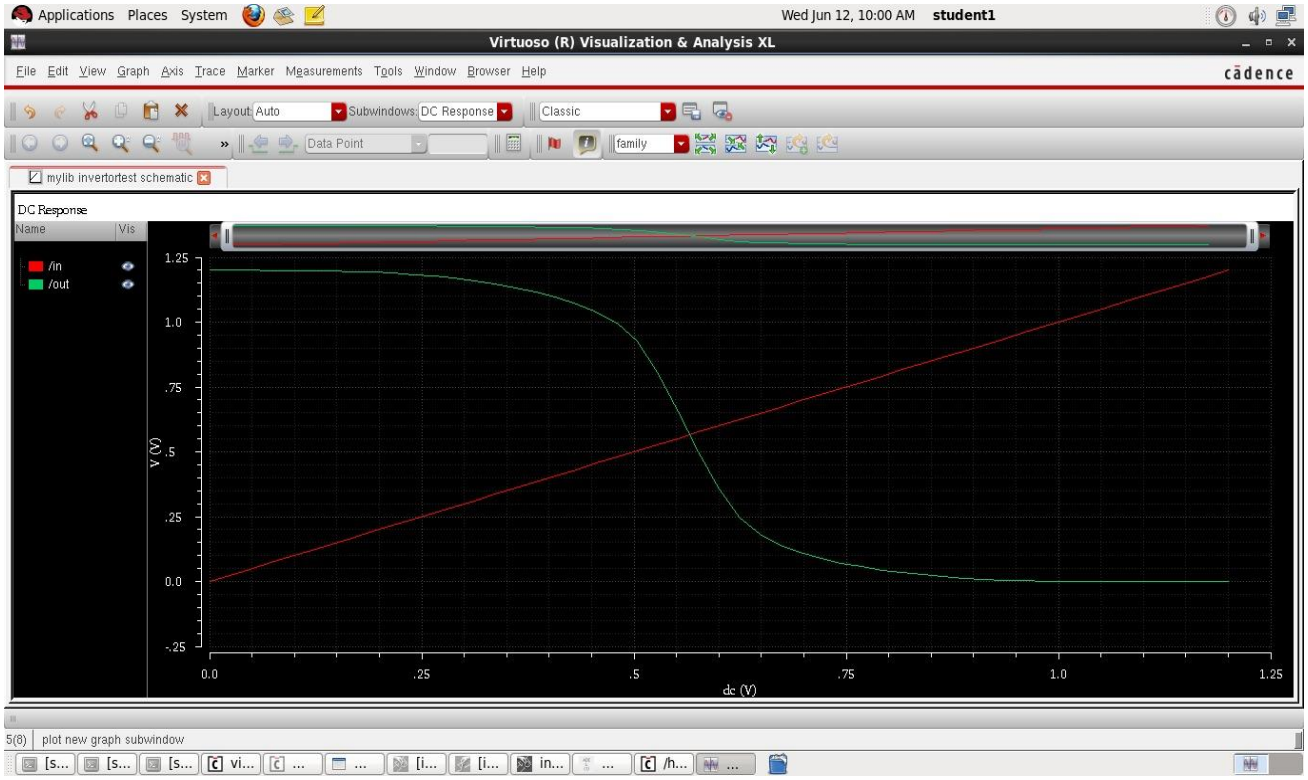


- File>New>cell view named as cmos_inverter
- Add an NMOS transistor, a PMOS transistor, a DC Voltage source VDC, and ground GND to the schematic
- Connect the components as per the CMOS Inverter circuit and name the wires aappropriately
- Workspace opens> click on create instance > select the components.
- Connect the circuit as shown in the figure,

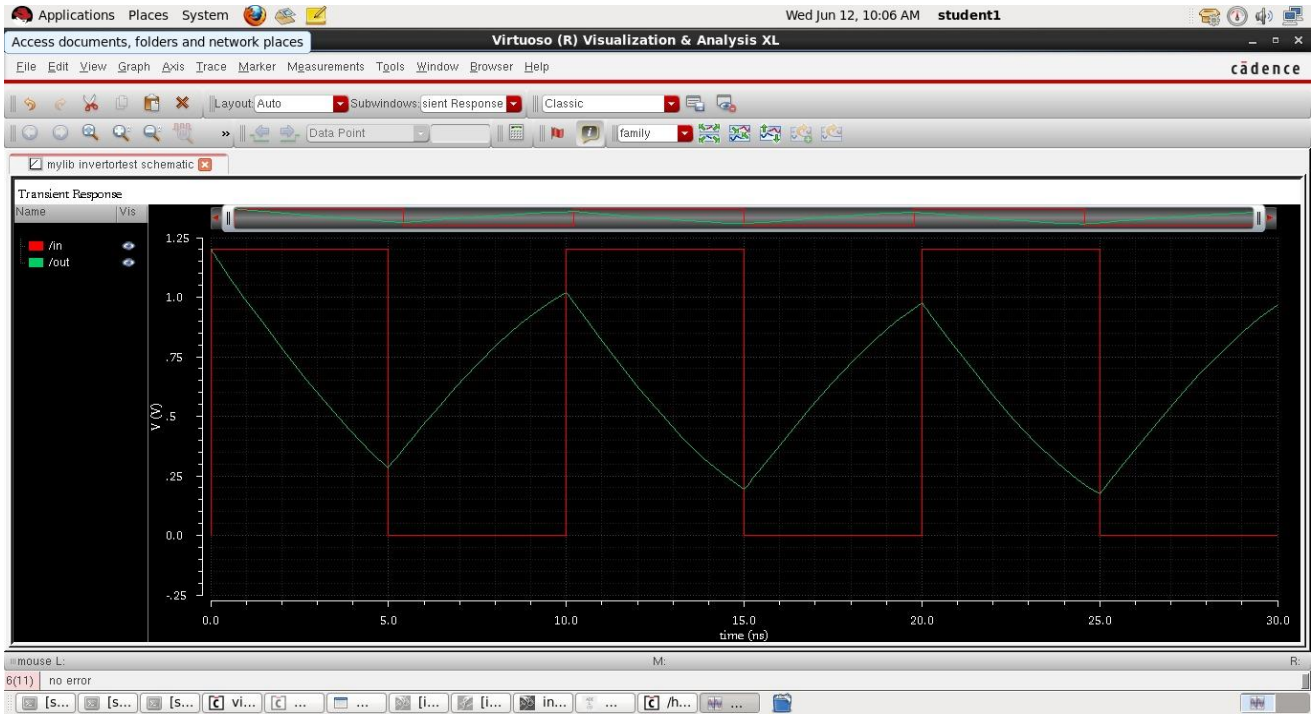


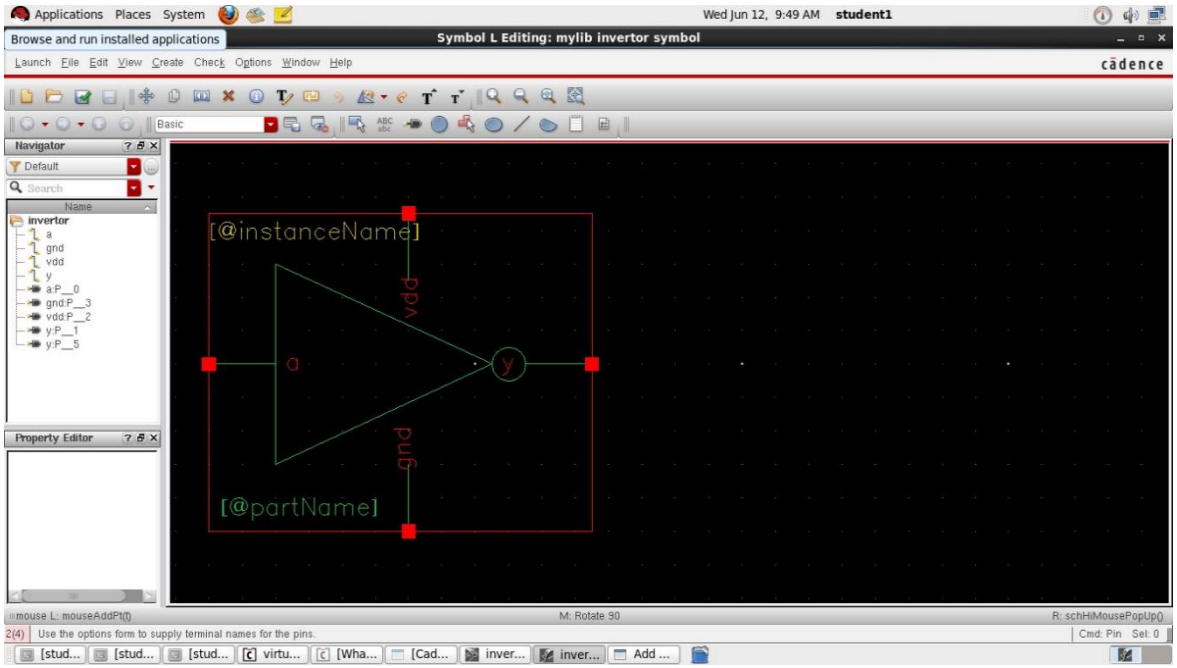


- Launch ADE L and configure Transient Analysis with a Stop time of 100ns
- Select Vout as the output net.
- Run the simulation and view the output graphs.
- Graph for DC Response

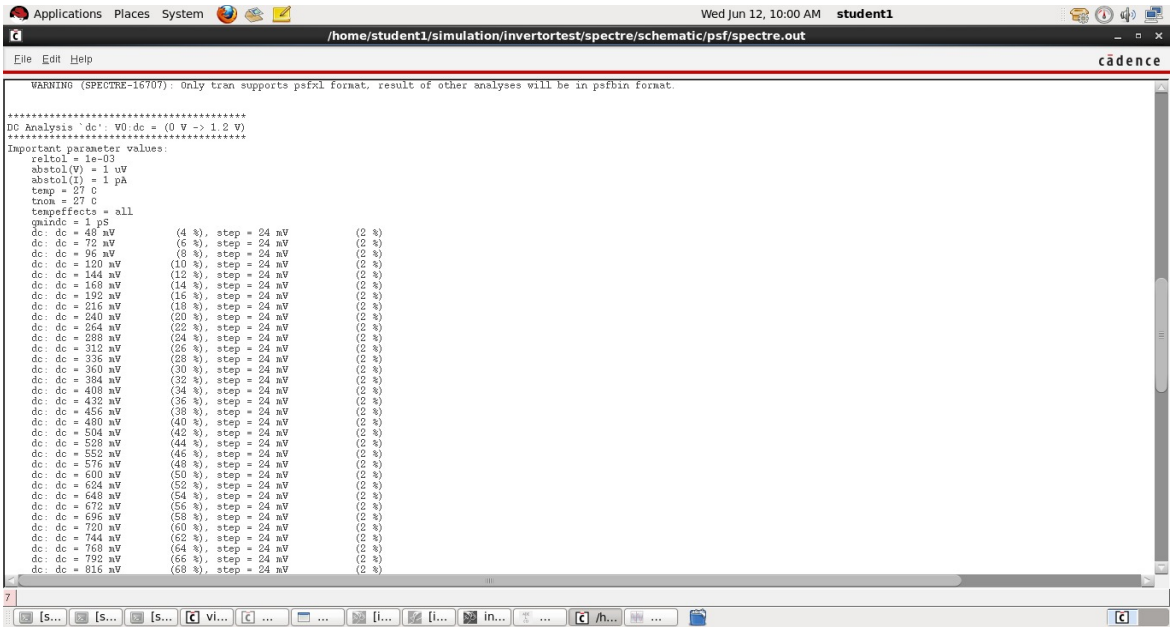


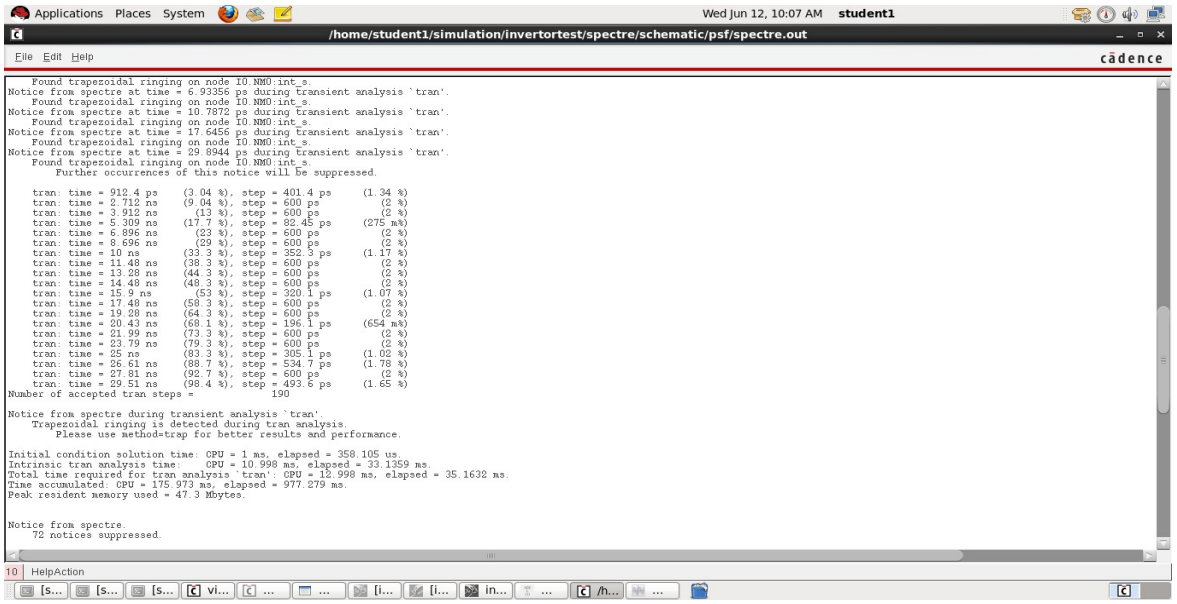
- Graph for Transient Response



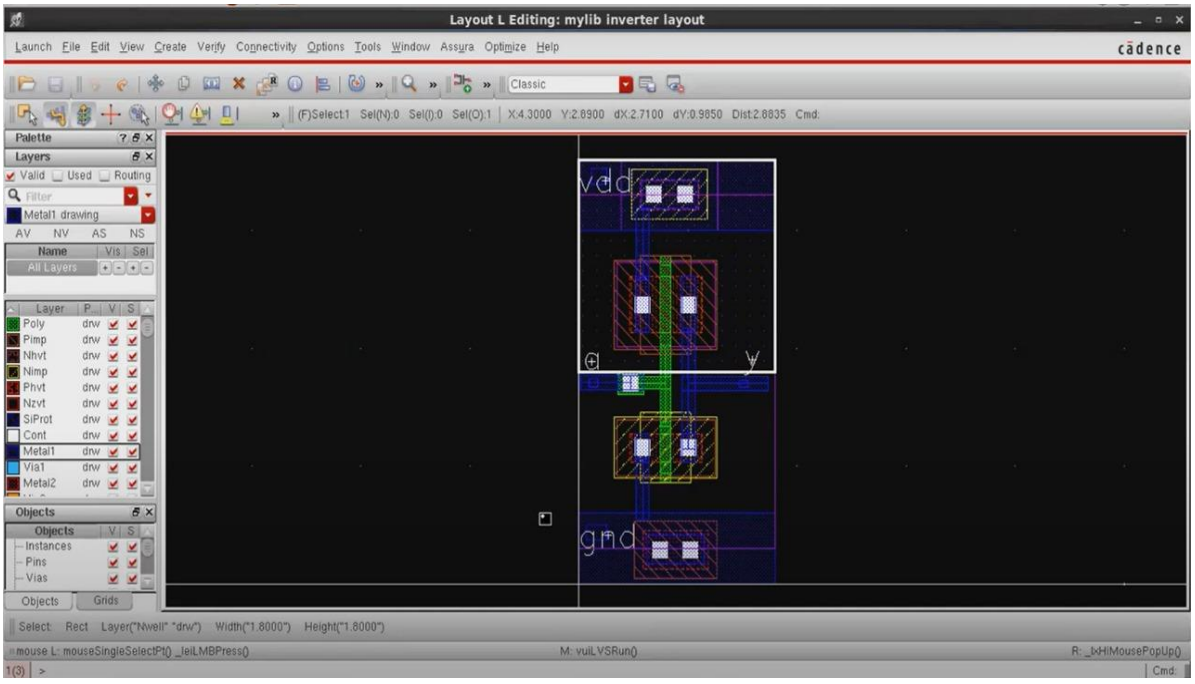


- Values for a desired output





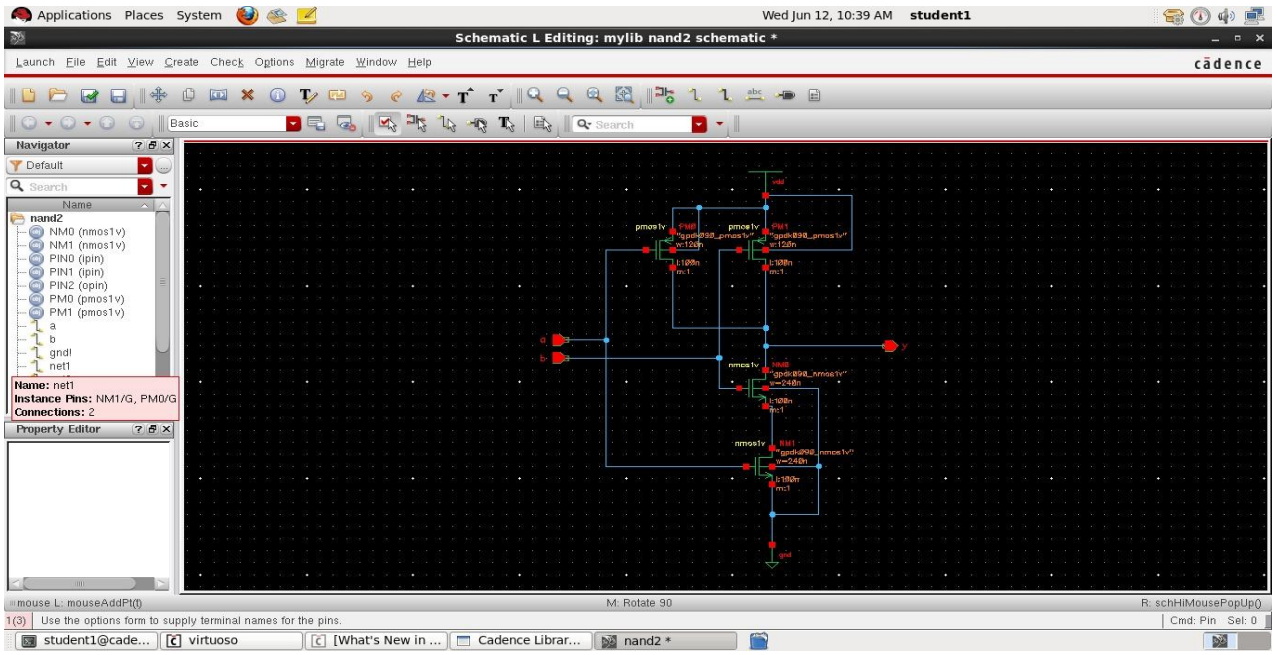
Layout, DRC, LVS of a CMOS Inverter



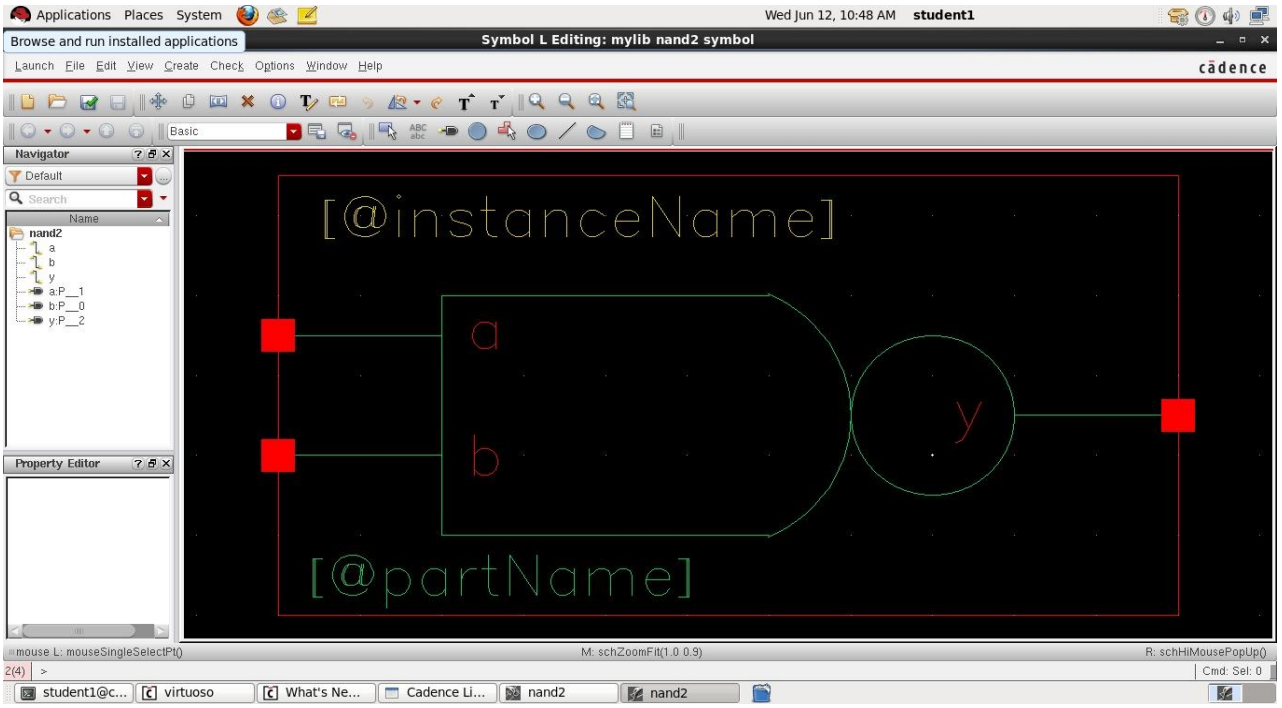
CONCLUSION: The schematic and Simulation of a CMOS Inverter and the layout DRC, and LVS checks, ensuring that the layout matches the schematic.

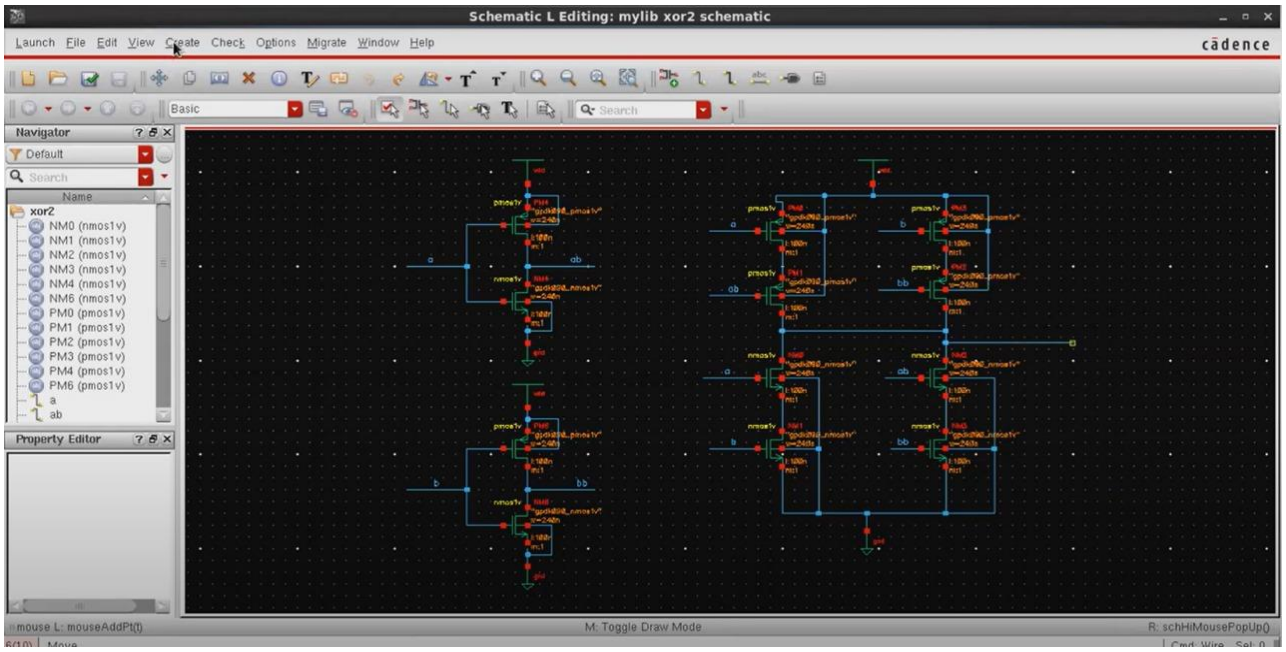
EXP 6: Hierarchical Schematic and Simulation of a NAND, XOR, and 1-bitFulladder

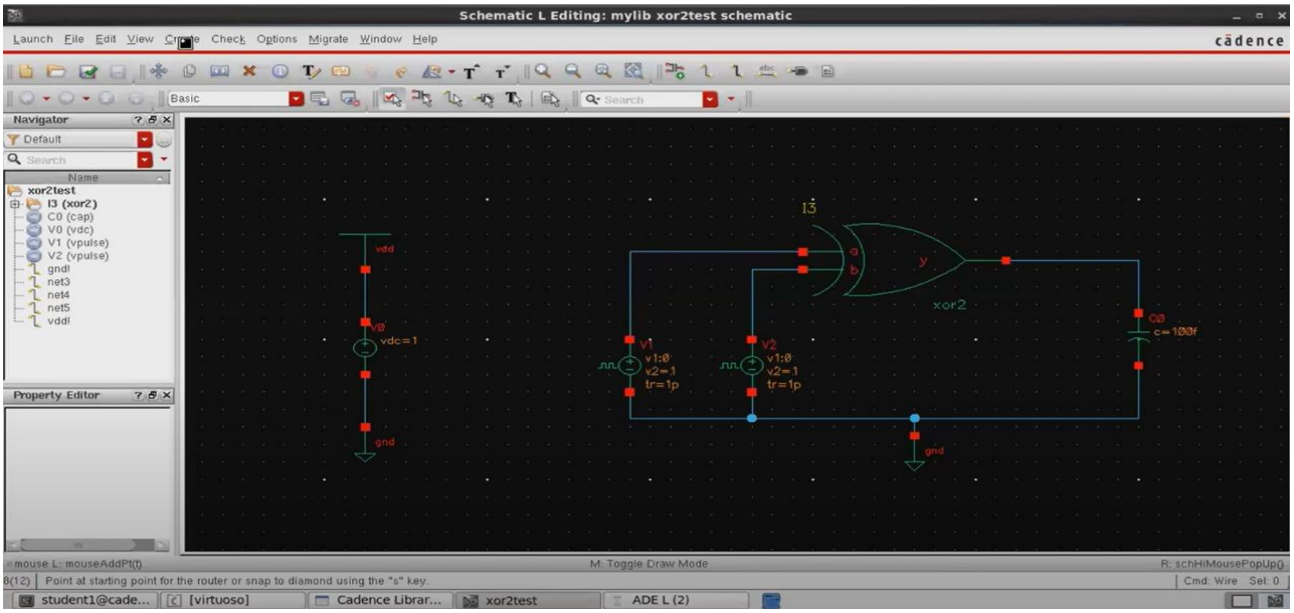
- File>New>cell view named as nand_gate, xor_gate, and full_adder.
- Add the necessary components NMOS and PMOS transistors and connect them as per the logic circuits for NAND, XOR, and full adder.
- Workspace opens> click on create instance > select the components.
- Connect the circuit as shown in the figure

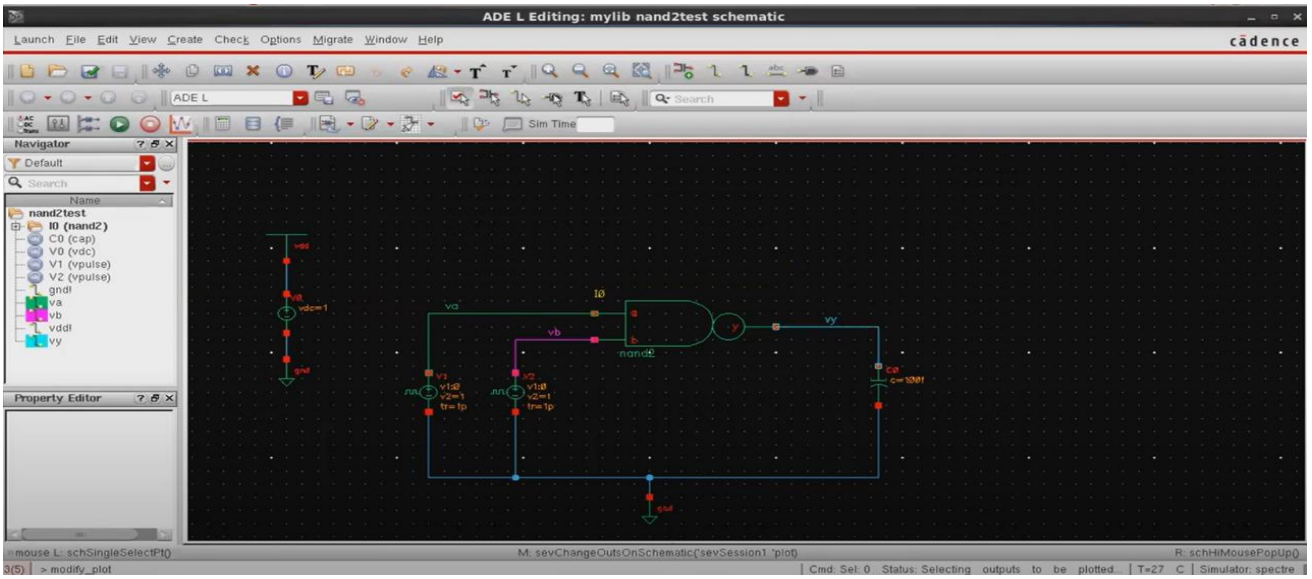


- Create symbols for each logic gate from the schematic views.

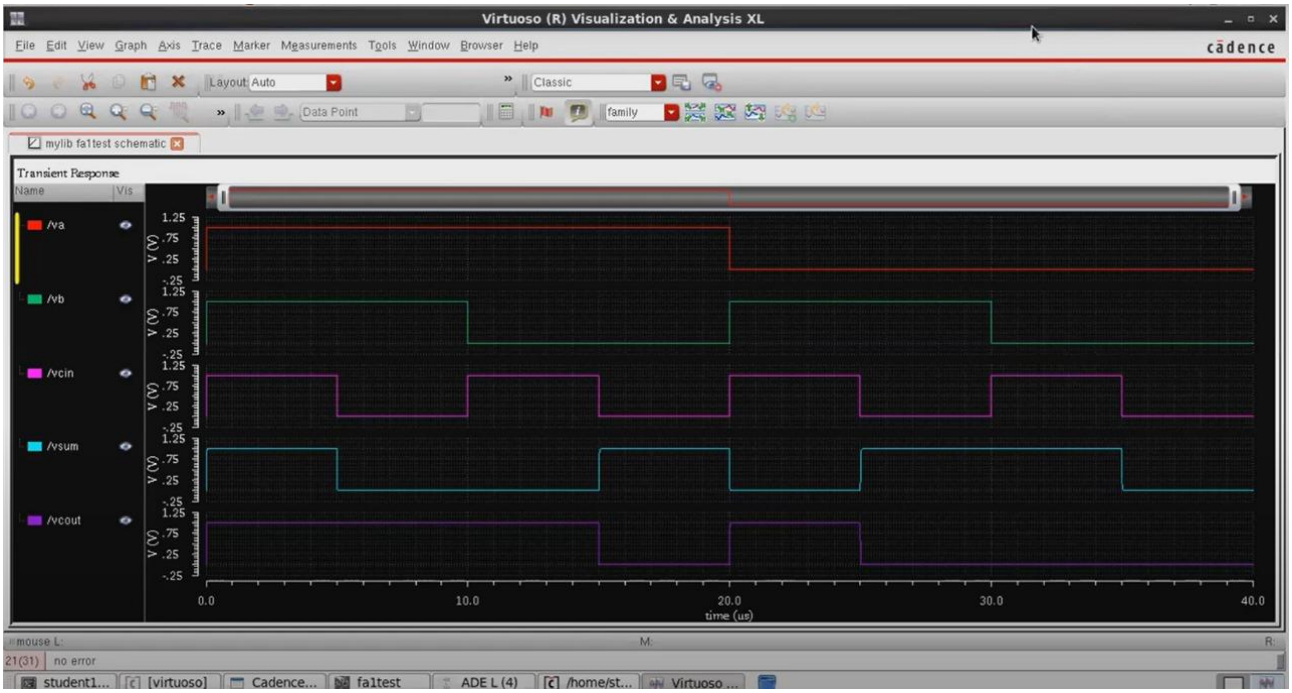


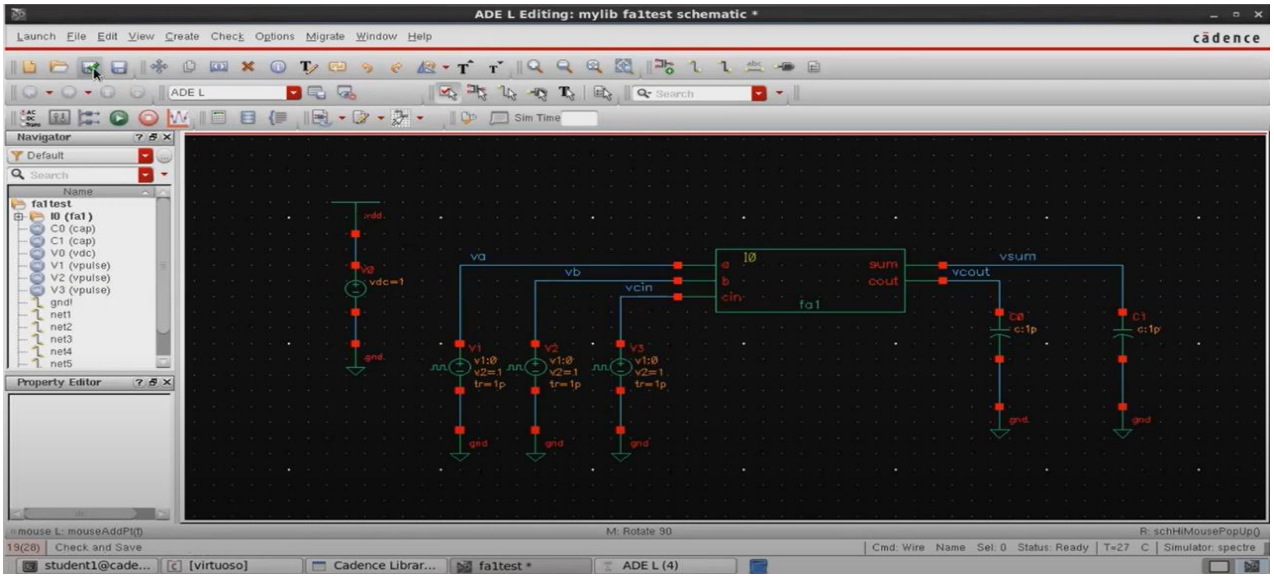

Schematic L Editing: mylib xor2 schematic
Launch File Edit View Create Check Options Migrate Window Help
cadence
Navigator
Default
Name
xor2
NM0 (nmos1v)
NM1 (nmos1v)
NM2 (nmos1v)
NM3 (nmos1v)
NM4 (nmos1v)
NM6 (nmos1v)
PM0 (pmos1v)
PM1 (pmos1v)
PM2 (pmos1v)
PM3 (pmos1v)
PM4 (pmos1v)
PM6 (pmos1v)
a
ab
Property Editor
mouse L: mouseAddPt(t)
M: Toggle Draw Mode
R: schHiMousePopUp()

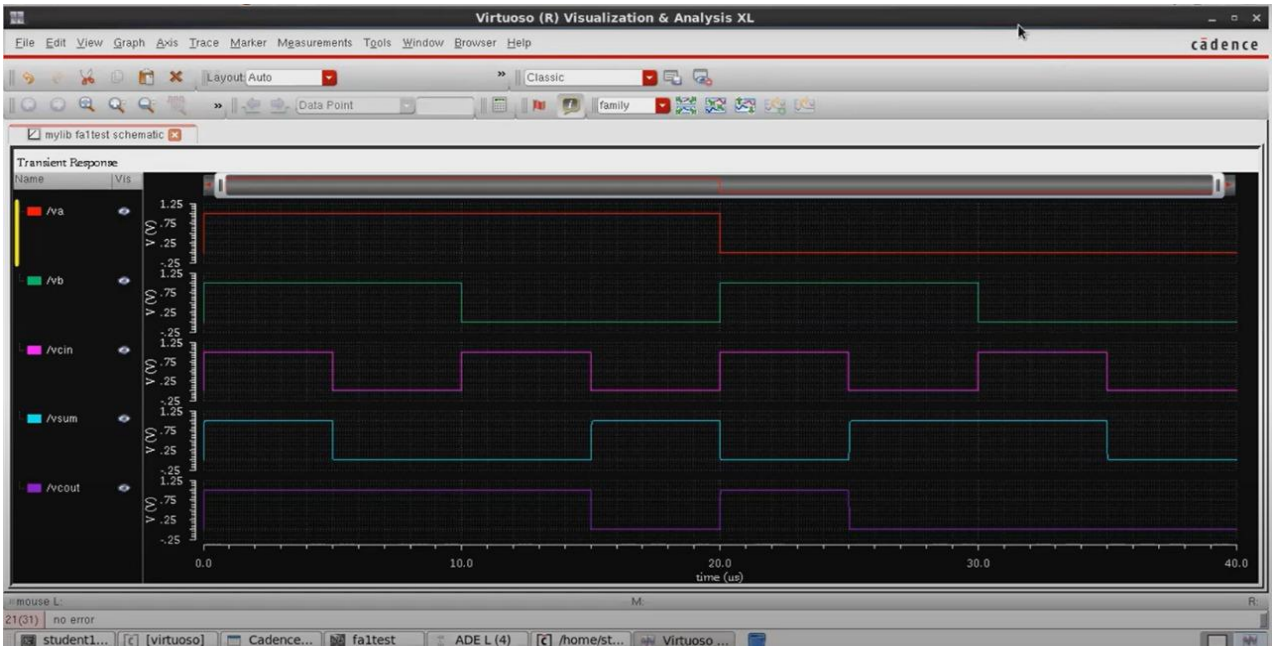

Schematic L Editing: mylib xor2test schematic
Launch File Edit View Create Check Options Migrate Window Help
cadence
Navigator
Default
Name
xor2test
I3 (xor2)
C0 (cap)
V0 (vdc)
V1 (vpulse)
V2 (vpulse)
gnd!
net3
net4
net5
vdd!
Property Editor
I3
xor2
V0
vdc=1
V1
v1:0
v2=1
tr=1p
V2
v1:0
v2=1
tr=1p
C0
c=100f
vdd
gnd
mouse L: mouseAddPt(t)
M: Toggle Draw Mode
R: schHiMousePopUp()
Point at starting point for the router or snap to diamond using the "s" key.
Cmd: Wire Sel: 0
student1@cade...
[virtuoso]
Cadence Librar...
xor2test
ADE L (2)


ADE L Editing: mylib nand2test schematic
Launch File Edit View Create Check Options Migrate Window Help
cadence
ADE L
Sim Time
Navigator
Default
Name
nand2test
I0 (nand2)
C0 (cap)
V0 (vdc)
V1 (vpulse)
V2 (vpulse)
gnd!
va
vb
vdd!
vy
Property Editor
I0
nand2
V0
vdc=1
V1
v1:0
v2=1
tr=1p
V2
v1:0
v2=1
tr=1p
C0
c=100f
vdd
gnd
mouse L: schSingleSelectPt()
M: sevChangeOutsOnSchematic('sevSession1 'plot)
R: schHiMousePopUp()
> modify_plot
Cmd: Sel: 0 Status: Selecting outputs to be plotted. T=27 C Simulator: spectre

- Launch ADE L and configure the appropriate analysis (Transient or DC)
- Select the output nets and run the simulations.
- View the output graphs to verify the functionality.







Conclusion: The hierarchical schematics and simulations for the NAND Gate, XOR Gate, and 1-bit full adder were successfully implemented.