The report is based on Hardware Assignment 1 of the COL-215 course, which is regarding a single digit seven segment display….

COL-215

SINGLE DIGIT SEVEN SEGMENT DISPLAY

Hardware Assignment 1

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CONTENTS

INTRODUCTION

- In this assignment, we are designing and implementing a circuit that takes a 4-bit hexadecimal number as input from the switches on the Basys3 board and displays the same on a seven-segment display.
- We also create a testbench to simulate the code providing the four bits of the digit as inputs to the circuit.
- The designing is done on Vivado software using VHDL.

PROBLEM DESCRIPTION

- Design a combinational circuit that takes a single 4-bit hexadecimal or decimal digit input from the switches and produces a 7-bit output for the seven-segment display of Basys3 FPGA board.

THEORY

SEVEN SEGMENT DECODER

- A basys3 board has 4 seven-segment displays i.e. each display consists of seven individual segments which can be turned on or off independently from each other so as to represent varied alpha-numeric data by their combination.
- Each individual display consists of seven segment which have a common anode and their own cathodes.
- For a segment, when the anode is set to ACTIVE (=0) and cathode is INACTIVE (=1), it turns on.
- On the contrary, for any other combination of anode-cathode state, the segment remains off.

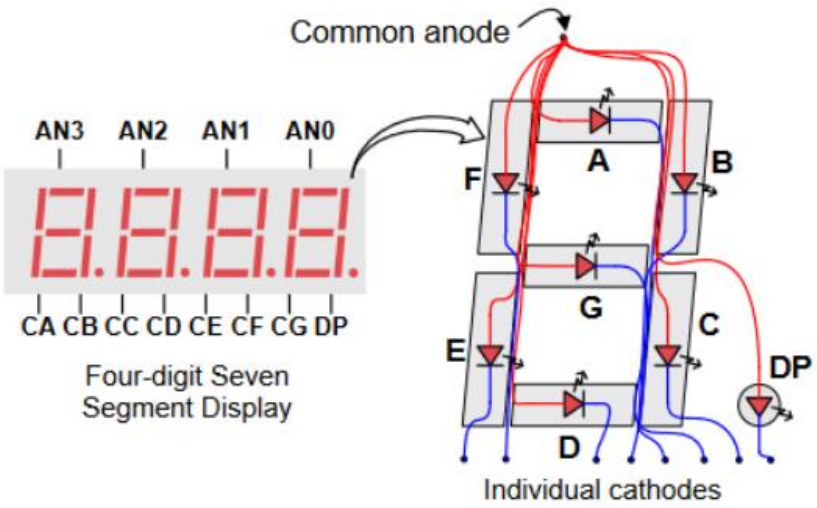


Figure 1: Pin details for 7 seven display on Basys 3 board

DESGIN DECISIONS

FINDING THE COMBINATIONAL LOGIC USING TRUTH TABLE

- We represented the input bits in form ABCD, where A represents the msb and D lsb. The output for each of the seven segments is represented by o1,o2,o3,o4,o5,o6,o7; the variables a0,a1,a2,a3 represent Anode.
- The expressions for all oi's were generated using the truth table and K-maps.
- The truth table is as follows:

TRUTH TABLE

A	B	C	D	O1	O2	O3	O4	O5	O6	O7
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	1	1	1	1	1	0	1
1	0	1	1	0	0	1	1	1	1	1
1	1	0	0	1	0	0	1	1	1	0
1	1	0	1	0	1	1	1	1	0	1
1	1	1	0	1	1	0	1	1	1	1
1	1	1	1	1	0	0	0	1	1	1

NOTE: On basys3 board, anode and cathode are ACTIVE LOW PINS. Thus, an output of 1 will be treated as Inactive (=Off) and an output of 0 will be treated as active for (=On).

K-MAPS AND COMBINATIONAL LOGICS

O1 = NOT ((NOT A AND C) OR (B AND C) OR (NOT A AND B AND D) OR (NOT B AND NOT D) OR (A AND NOT D) OR (A AND NOT B AND NOT C));

AB / CD	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	1	0	1	1
10	1	1	0	1

O2 = NOT ((NOT A AND NOT B) OR (NOT A AND NOT C AND NOT D) OR (A AND NOT C AND D) OR (A AND C AND NOT D) OR (NOT B AND NOT C) OR (NOT A AND C AND D));

AB / CD	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	0	1	0	1
10	1	1	0	1

O3 = NOT ((A AND NOT B) OR (NOT C AND D) OR (NOT A AND B) OR (NOT A AND NOT C) OR (NOT A AND D));

AB / CD	00	01	11	10
00	1	1	1	0
01	1	1	1	1
11	0	1	0	0
10	1	1	1	1

O4 = NOT ((C AND NOT D) OR (NOT B AND C) OR (B AND NOT C AND D) OR (A AND NOT D) OR (NOT B AND NOT D));

AB / CD	00	01	11	10
00	1	0	1	1
01	0	1	0	1
11	1	1	0	1
10	1	0	1	1

O5 = NOT ((C AND NOT D) OR (A AND B) OR (A AND C) OR (NOT B AND NOT D));

AB / CD	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	1	1	1	1
10	1	0	1	1

O6 = NOT ((NOT C AND NOT D) OR (B AND NOT D) OR (A AND NOT B AND D) OR (A AND C AND D) OR (NOT A AND B AND NOT C));

AB / CD	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	1	0	1	1
10	1	1	1	0

O7 = NOT ((A AND NOT B) OR (C AND NOT D) OR (A AND D) OR (NOT A AND B AND NOT C) OR (NOT B AND C));

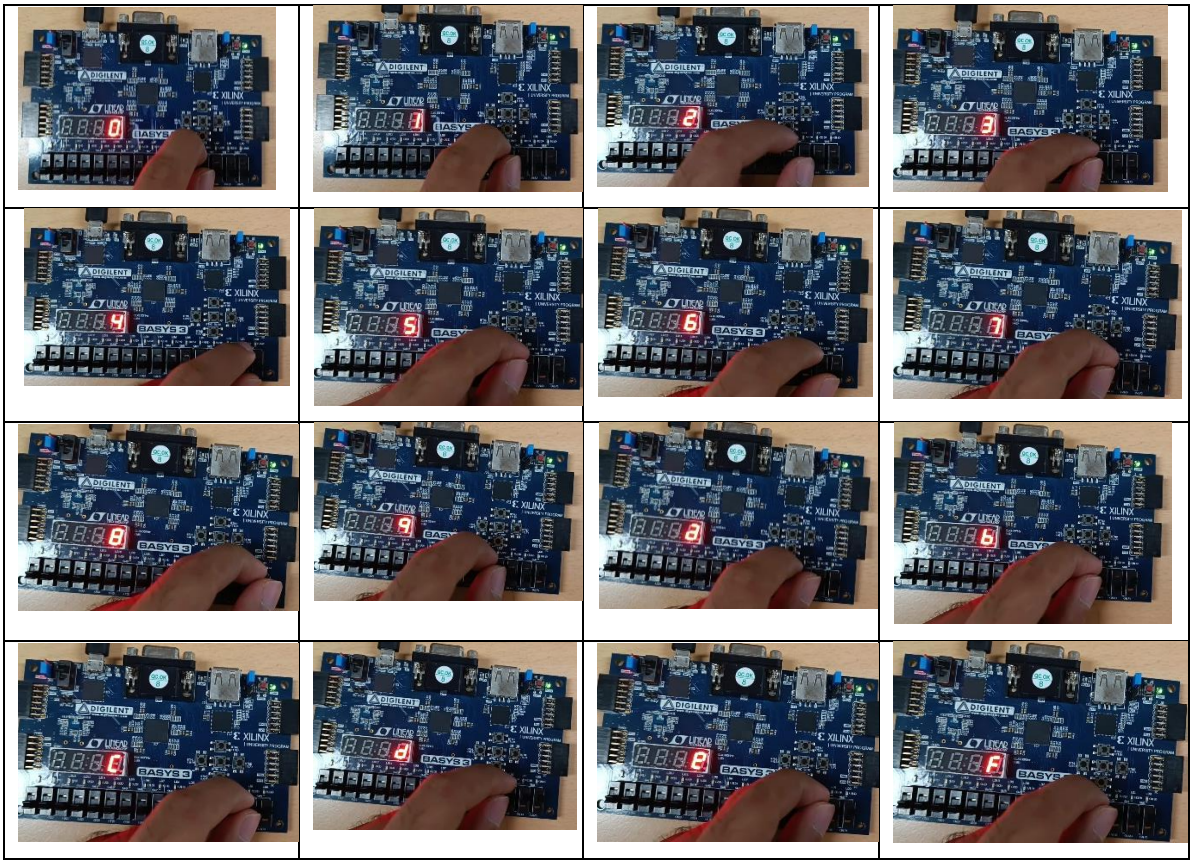
AB / CD	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	0	1	1	1
10	1	1	1	1

ANODES

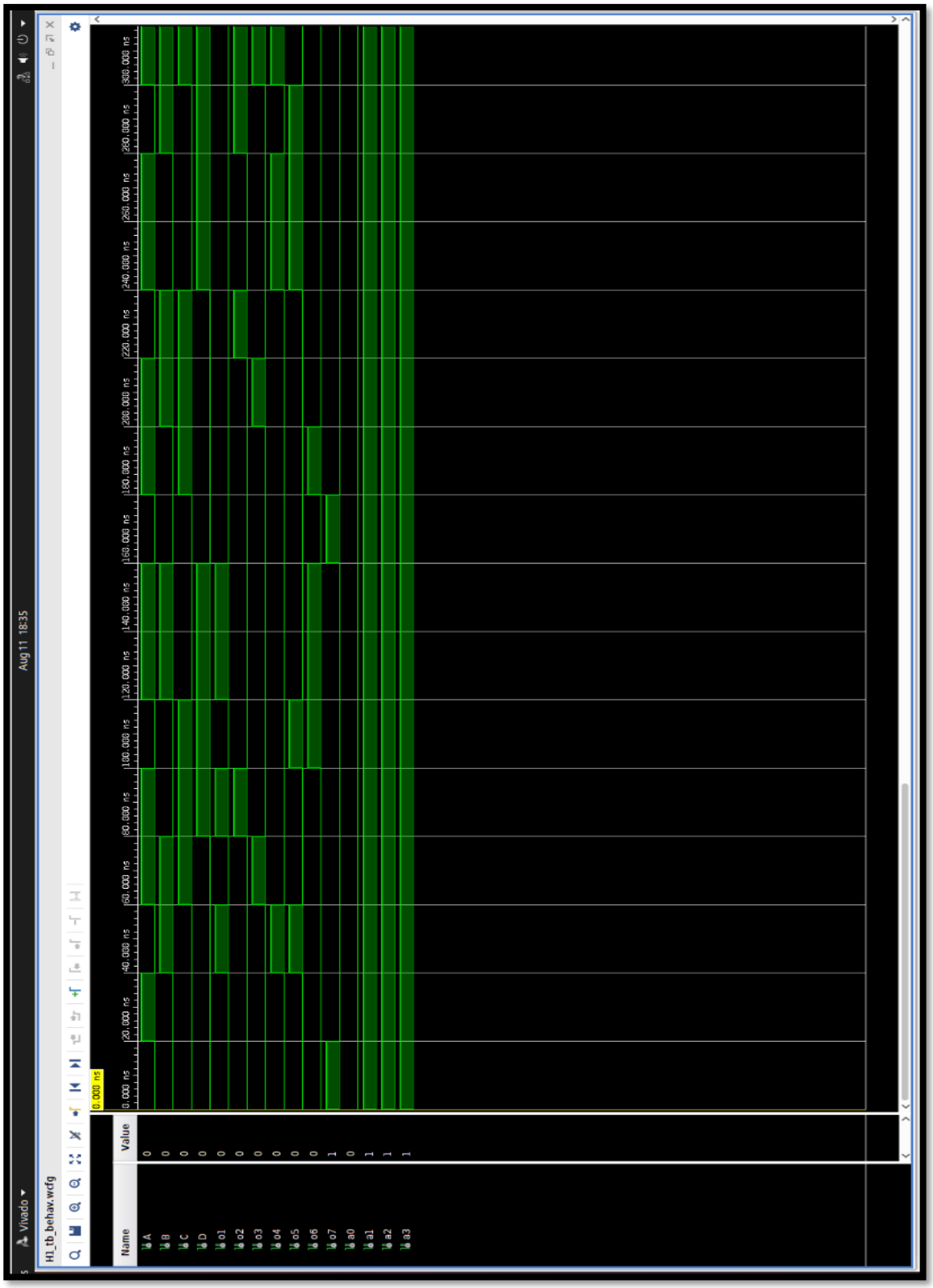
To keep one anode on and others off, we set three anodes to a contradiction and the remaining one to a tautology.

RESULTS

- The 16 characters of the hexadecimal number system were successfully displayed on a single seven segment display of the basys3 board.
- Remaining three displays remained off during the process.
- Synthesis, implementation and simulation of the code was successful.
- Below are the snapshots of individual characters



SIMULATION SNAPSHOT



SYNTHESIS REPORT

- The link to the complete synthesis report is shared below:

  https://drive.google.com/file/d/1JvLCRvd7fgfo5rBDDql1gn6P4l4OVyGk/view?usp=drive_link

- Particular screenshots are included below:

SLICE LOGIC

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	4	0	0	20800	0.02
LUT as Logic	4	0	0	20800	0.02
LUT as Memory	0	0	0	9600	0.00
Slice Registers	0	0	0	41600	0.00
Register as Flip Flop	0	0	0	41600	0.00
Register as Latch	0	0	0	41600	0.00
F7 Muxes	0	0	0	16300	0.00
F8 Muxes	0	0	0	8150	0.00

MEMORY(BRAM)

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	50	0.00
RAMB36/FIFO*	0	0	0	50	0.00
RAMB18	0	0	0	100	0.00

DSP

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	90	0.00

REMARKS AND CONCLUSION

- In this assignment, we thus learnt how to operate the displays on the bsys3 board and display using a 7 segment display. We learnt about the designing of such displays, their anode/cathode design, the .vhd codes for same and driving the circuit using K-maps and combinational logic.