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CS281
W2

4.1

Consider the following instruction:
Instruction:
AND Rd,Rs,Rt
Interpretation:
Reg[Rd] = Reg[Rs] AND Reg[Rt]

4.1.1

[5] <§4.1> What are the values of control signals generated by the control in Figure 4.2 for the above instruction?

As a result of the instruction provided, the values of the signals would reflect the values represented by this format.

opcode	extsel	bsrc	opsel	memw	regw	wbsrc	regdst	pcsrc
ALU	-----------	reg	func	false	true	ALU	rd	pc+4

An AND instruction uses an ALU opcode meaning the BSrc will look to the registry and the OpSel will retrieve information to tell the ALU that it is to AND. There's no need to modify the memory for this operation so it is left unchanged, But since it will write back to the registry eventually at rd RegW is left as true. WBSrc will take the output from the ALU, RegDst is set to rd, and PCSrc is only PC+4 because there are no jumps performed during the operation.

4.1.2

[5] <§4.1> Which resources (blocks) perform a useful function for this Instruction?

The resources or blocks that perform useful functions during the execution of the instruction given are the PC, ALU, MUX, Instruct Memory, and the registers.

As the program counter increases with the completion of the instruction, the Instruction Memory, alu, and the mux use the code sent to decide what to do with the information that is either in the registries, or what information to put in which registry. There is no use for jumping during this instruction so that is not used.

4.1.3

[10] <§4.1> Which resources (blocks) produce outputs, but their outputs are not used for this instruction? Which resources produce no outputs for this Instruction?

In the instruction provided the branch produces outputs. The branch's output is not used by the AND instruction. The data memory does not produce any output as a result of this instruction.

4.7

In this exercise we examine in detail how an instruction is executed in a single-cycle datapath. Problems in this exercise refer to a clock cycle in which the processor fetches the following instruction word:

10101100011000100000000000010100

.

Opcode = 101011 = sw

Assume that data memory is all zeros and that the processor's registers have the following values at the beginning of the cycle in which the above instruction word is fetched:

R0	0
R1	–1
R2	2
R3	–3
R4	–4
R5	10
R6	6
R8	8
R12	2
R31	–16

4.7.1

[5] <§4.4> What are the outputs of the sign-extend and the jump "Shift Left 2" unit (near the top of Figure 4.24) for this instruction word?

Sign extend = 15:0 of the instruction = 00000000000000000000000000010100
Out of the jump for shift left 2 = 25:0 = 0001100010000000000001010000

4.7.2

[10] <§4.4> What are the values of the ALU control unit's inputs for this Instruction?

The ALU control unit's input for this instruction would be 0010 as the opcode from this code is 101011 telling us we are working with a sw operation, Knowing then that this code loads and stores add the ALUOp had to be 00.

4.7.3

[10] <§4.4> What is the new PC address after this instruction is executed?
Highlight the path through which this value is determined.

The new PC address after the instruction is executed is PC+4.

Once the instruction is started
pc is sent to be added with 4 (PC+4)
This is then sent to a mux
It moves past the mux as a result of the Branch control settings currently set
This is then sent to another mux
It moves past the mux as a result it not being a jump instruction
Now what has gone through this is set as the PC so instead of it being PC it is now PC+4

4.7.4

[10] <§4.4> For each Mux, show the values of its data output during the execution of this instruction and these register values.

WrReg Mux: 3
ALU Mux: 16
Mem-ALU Mux: 0
Branch Mux: PC+4
Jump Mux: PC+4

4.7.5

[10] <§4.4> For the ALU and the two add units, what are their data input
Values?

ALU: 2 and 16
Add - PC+4: PC and 4
Add - Branch: PC+4 and 16x4

4.7.6

[10] <§4.4> What are the values of all inputs for the "Registers" unit?

readReg1: 2
readReg2: 3
WriteReg: 3
WriteData: 0

RegWrite: 1

Li I-Type instruction single-cycle datapath diagram, description, control signal values(table)

Lui I-Type instruction single-cycle datapath diagram, description, control signal values(table)

jal J-Type instruction single-cycle datapath diagram, description, control signal values(table)

jr R-Type instruction single-cycle datapath diagram, description, control signal values(table)