LogicGreen Technologies Co., LTD

8-bit LGT8XM

RISC Microcontroller with In-System Programmable FLASH Memory

LGT8F88P

LGT8F168P

LGT8F328P

Data book

Version 1.0.4

Applications

Motor-driven

automation and

control home appliances

Functional Overview

- **High performance and low power consumption 8 Place LGT8XM Kernel**
- **advanced RISC Architecture**

  131 Instruction, 80% More than a single cycle execution

  32x8 General purpose working registers

  32MHz Up work 32MIPS Efficiency in the implementation

  Internal single-cycle multiplier (8x8)
- **Non-volatile program and data memory space**

  32Kbytes On-chip online programming **FLASH** Program Memory

  2Kbytes Internal data **SRAM**

  Programmable E2PROM Analog interface, support byte access new

  program encryption algorithms to ensure user safety codes
- **Peripheral Controller**

  Two independent prescaler 8 Bit timer, output compare mode support

  Two independent prescaler 16 Bit timers, support for input capture and output compare

  internal 32KHz Can be calibrated **RC** Oscillator real-time counter function

  Supports up to 9 road PWM Output, three complementary set of programmable dead-band control

  12 aisle 12 Bit high-speed ADC (**ADC)**

  - Optional internal, external reference voltage
  - Programmable Gain (X1 / 8/16/32) Differential amplifier input channels
  - Automatic threshold voltage monitoring mode

  Two analog comparators (**AC)** And support from ADC Extended input channels

  internal 1.024V / 2.048V / 4.096V ± 1% May be calibrated reference voltage source

  One 8 Bit programmable **DAC** , It may be used to generate a reference voltage

  source programmable watchdog timer (**WDT**) Programmable synchronous /

  asynchronous serial interface (**USART / SPI**) Synchronous Peripheral Interface

  (**SPI),** Programmable master / slave mode of two-wire serial interface (**TWI),** compatible

  I2C Master-slave mode

  16 Digit arithmetic acceleration unit (**DSC)** , Direct support 16 Bit data access access
- **Special Function Processor**

  SWD Double-chip debug / production interrupt source and an external interface I / O Change interrupt

  support the built-in power-on reset circuit (**POR**) And programmable low voltage detection circuit (**LVD**)

  Built-in 1% Can be calibrated 32MHz RC Oscillator frequency output Built-in support 1% Can be

  calibrated 32KHz RC Oscillator external support 32.768KHz as well as 400K ~ 32MHz Crystal Input

  6x High current push-pull drive IO Support high-speed PWM application

- **I / O And Packaging:** QFP48 / 32L, SSOP20L
- **Low power consumption:** 1uA@3.3V
- **working environment**

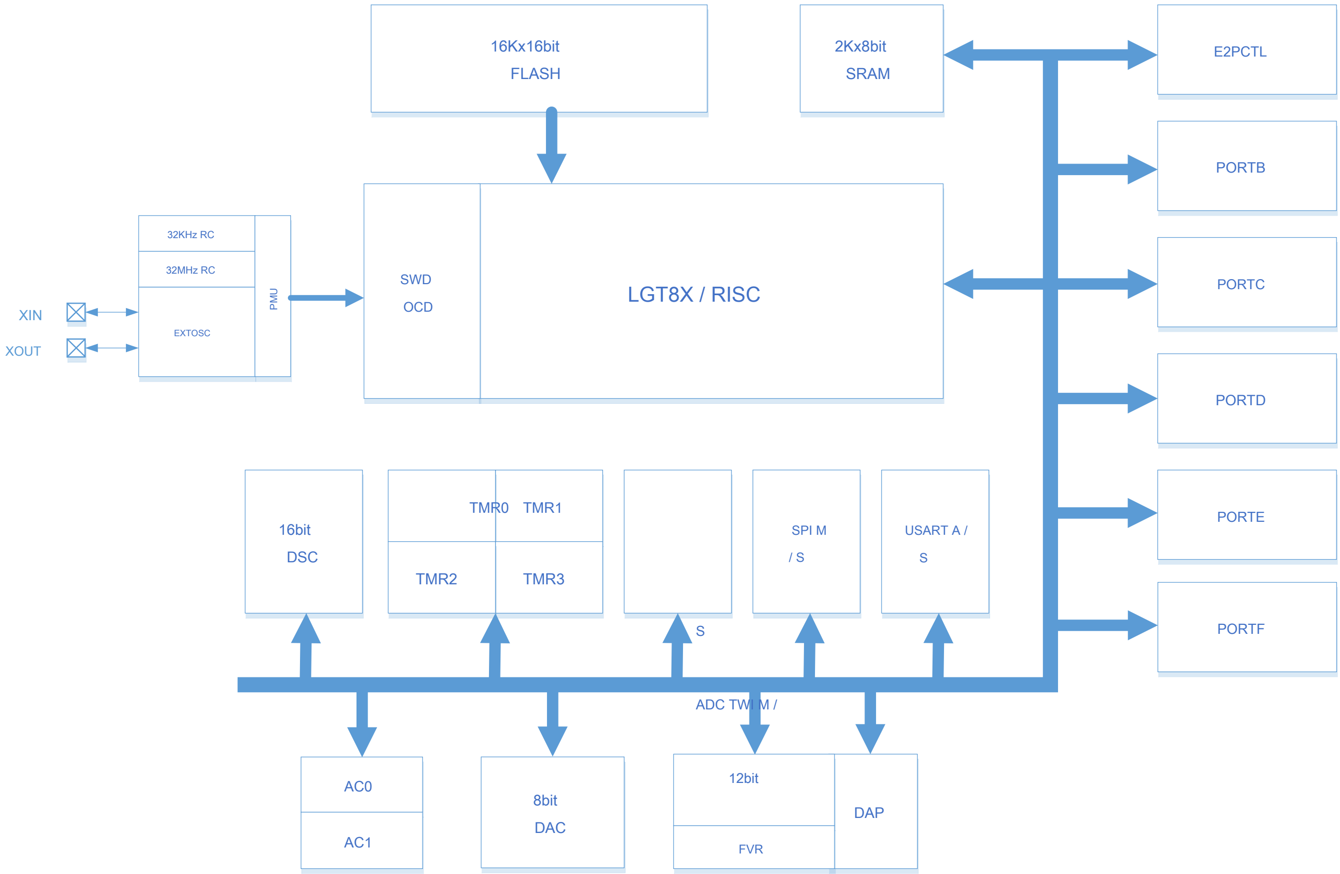
  Operating Voltage: 1.8V ~ 5.5V

  working frequency: 0 ~ 32MHz

  Operating temperature: - 40C ~ + 85C HBM

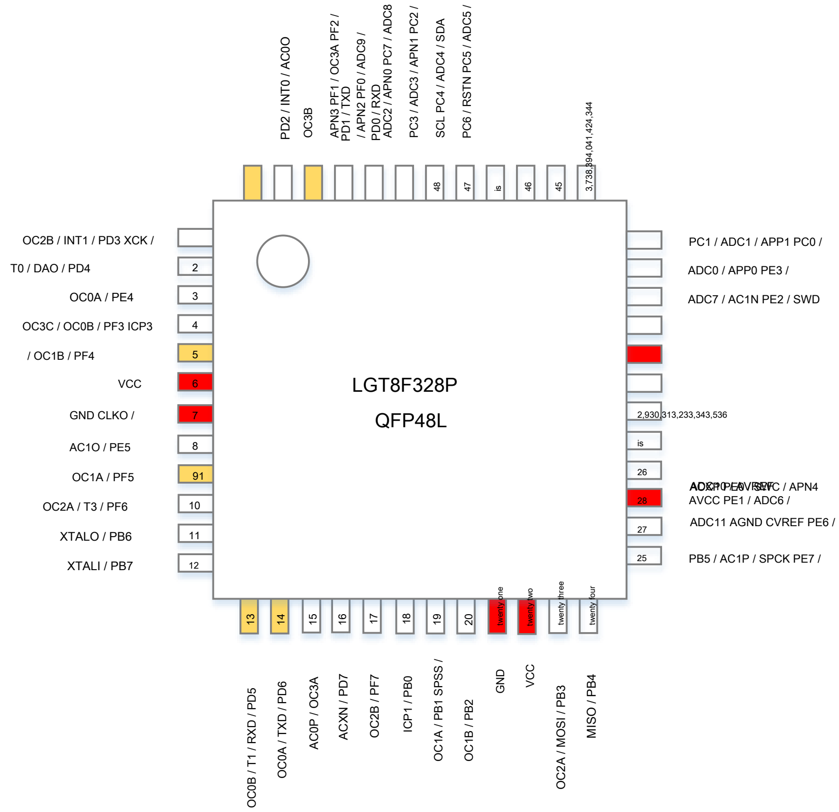
  ESD: > 4KV

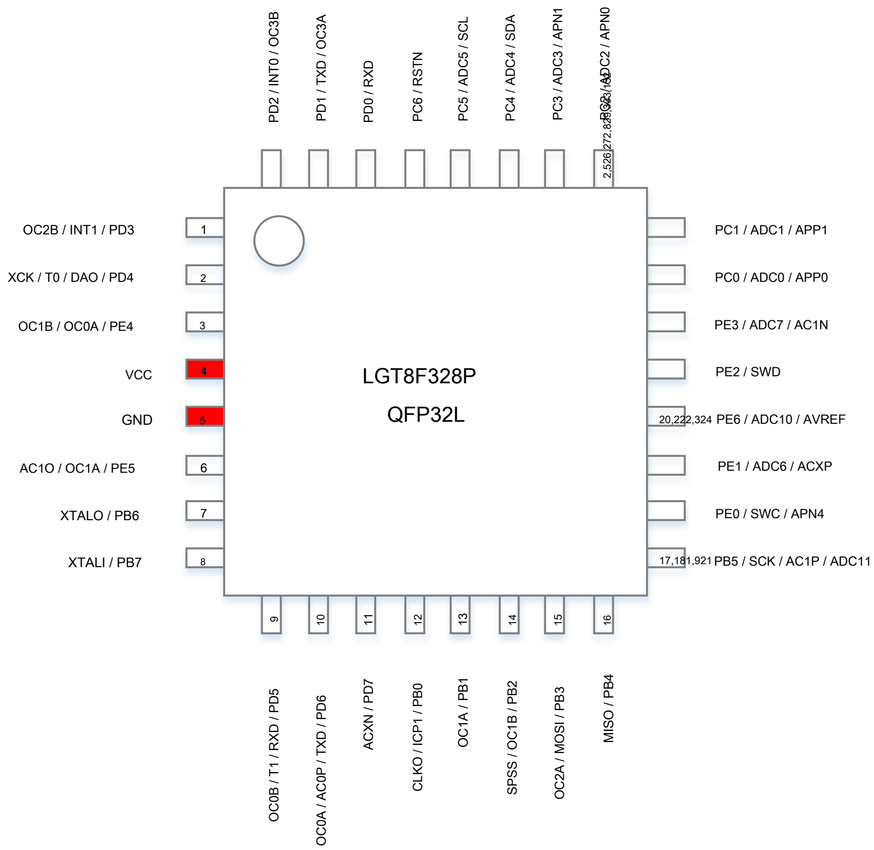
system framework

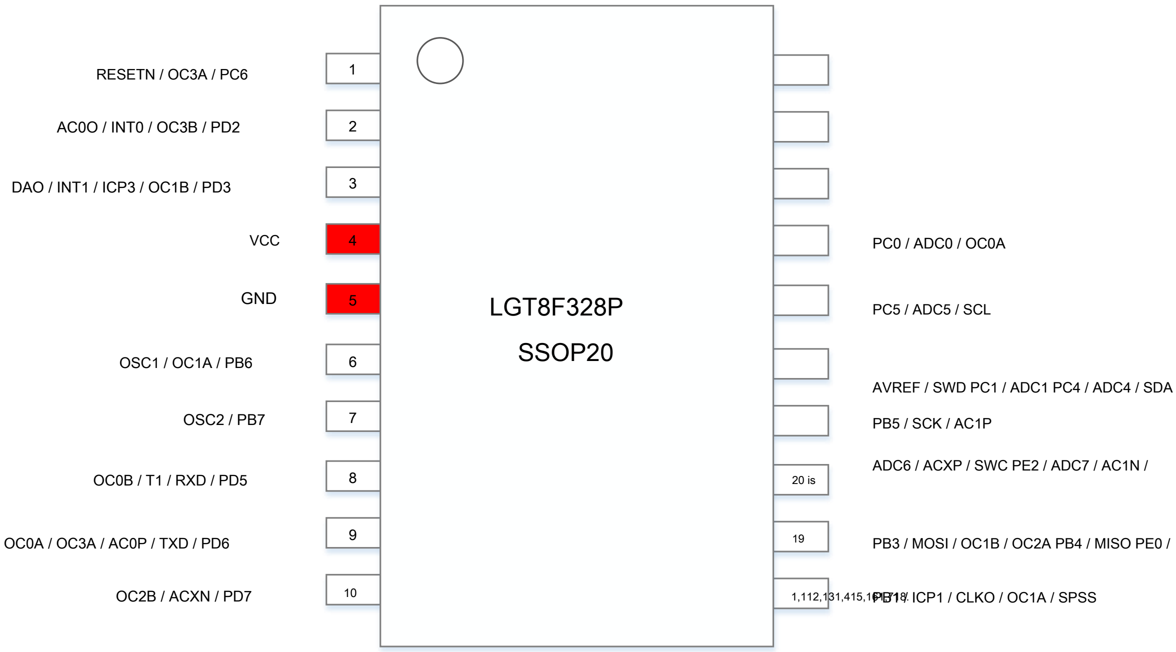


Module Name	Module features
SWD	Debug module, while achieving online debugging and ISP Features
LGT8X	8bit high performance RISC Kernel
E2PCTL	data FLASH Access Interface Controller
PMU	Power management module, Responsible for managing the transition between the system status
PORTB / C / D / E / F	General-purpose programmable input and output ports
DSC	16 Digit arithmetic acceleration unit
ADC DAP IVREF	8 aisle 12 Bit ADC programmable gain differential amplifier 1.024V / 2.048V / 4.096V Internal Reference
AC0 / 1	Analog comparator
TMR0 / 1/2/3	8/16 Bit timer / counter, PWM Controller
WDT	Reset Watchdog module
SPI M / S	Master-slave SPI Controller
TWI M / S	Master-Slave two-wire interface controller, compatible I2C protocol
USART	Synchronous / Asynchronous Serial Transceiver
DAC	8 Bit DAC

Package defined






RESETN / OC3A / PC6
AC0O / INT0 / OC3B / PD2
DAO / INT1 / ICP3 / OC1B / PD3
VCC
GND
OSC1 / OC1A / PB6
OSC2 / PB7
OC0B / T1 / RXD / PD5
OC0A / OC3A / AC0P / TXD / PD6
OC2B / ACXN / PD7
1
2
3
4
5
6
7
8
9
10
LGT8F328P
SSOP20
20 is
19
PC0 / ADC0 / OC0A
PC5 / ADC5 / SCL
AVREF / SWD PC1 / ADC1 PC4 / ADC4 / SDA
PB5 / SCK / AC1P
ADC6 / ACXP / SWC PE2 / ADC7 / AC1N /
PB3 / MOSI / OC1B / OC2A PB4 / MISO PE0 /
PB1 / ICP1 / CLKO / OC1A / SPSS

Pin Description

LGT8FX8P Series package, QFP48L All package lead pin. Other packages are in QFP48 On the basis of multiple internal I / O Bound to produce a pin. Special care configure the pin direction. The following table lists a variety of package pins binding information:

QFP48	QFP32	SSOP20	Function Description
01	**01**	**03**	PD3 / INT1 / OC2B * PD3: Programmable port D3 INT1: External interrupt input 1 OC2B: Timer 2 Compare Match Output B
02	**02**		PD4 / DAO / T0 / XCK PD4: Programmable port D4 DAO: internal DAC Export T0: Timer0 External clock input XCK: USART Transmit clock
03	**03**	**-**	PE4 / 0C0A * PE4: Programmable port E4 OC0A: Timer 0 Compare Match Output A
04	**-**	**-**	PF3 / OC3C / OC0B * PF3: Programmable port F3 OC3C: Timer 3 Compare Match Output C OC0B: Timer 0 Compare Match Output B
05	**03**	**03**	PF4 / OC1B * / ICP3 PF4: Programmable port F4 OC1B: Timer 1 Compare Match Output B ICP3: Timer 3 Capture input
06	**04**	**04**	VCC
07	**05**	**05**	GND
08	**06**	**-**	PE5 / AC1O / CLKO * PE5: Programmable port E5 C1O: Analog comparator AC1 Export CLKO: System clock output
09		**06**	PF5 / OC1A * PF5: Programmable port F5 OC1A: Timer 1 Compare Match Output A
10	**-**	**-**	PF6 / T3 / OC2A * PF6: Programmable port F6 T3: Timer 3 External clock input OC2A: Timer 2 Compare Match Output A
11	**07**	**06**	PB6 / XTALO PB6: Programmable port B6 XTALO: Crystal IO Output port

12	08	07	PB7 / XTALI PB7: Programmable port B7` XTALI: Crystal IO Input port
13	09	08	PD5 / RXD * / T1 / OC0B PD5: Programmable port D5 RXD: USART Receiving data (optional) T1: Timer 1 External clock input OC0B: Timer 0 Compare Match Output B
14	10	09	PD6 / TXD * / OC0A PD6: Programmable port D6 TXD: USART Data transmission (optional) OC0A: Timer 0 Compare Match Output A
15			AC0P / 0C3A AC0P: Analog comparator 0 Positive input OC3A: Timer 3 Compare Match Output A
16	11	10	PD7 / ACXN PD7: Programmable port D7 ACXN: Analog comparator 0/1 Public negative input
17	-		PF7 / OC2B PF7: Programmable port F7 OC2B: Timer 2 Compare Match Output B
18	12	11	PB0 / ICP1 PB0: Programmable port B0 ICP1: Timer 1 Capture input
19	13		PB1 / OC1A PB1: Programmable port B1 OC1A: Timer 1 Compare Match Output A
20	14	12	PB2 / OC1B / SPSS PB2: Programmable port B2 OC1B: Timer 1 Compare Match Output B SPSS: SPI Slave Chip Select Mode
twenty one	-	-	GND
twenty two	-	-	VCC
twenty three	15	12	PB3 / MOSI / OC2A PB3: Programmable port B3 MOSI: SPI Master Out / Slave OC2A: Timer 2 Compare Match Output A
twenty four	16	13	PB4 / MISO PB4: Programmable port B4 MISO: SPI A host input / output slave
25	17	14	PB5 / SPCK / AC1P PB5: Programmable port B5 SPCK: SPI Clock signal AC1P: Analog comparator 1 Positive input

26	-	-	PE7 / ADC11 PE7: Programmable port E7 ADC11: ADC Analog input channels 11
27	-	-	AVCC: Internal analog circuit power supply
28	18	15	PE0 / SWC / APN4 PE0: Programmable port E0 SWC: SWD Debug interface clock APN4: Differential amplifier inverting input channels 4
29	19		PE1 / ADC6 / ACXP PE1: Programmable port E1 ADC6: ADC Analog input channels 6 ACXP: Analog comparator 0/1 Public input positive terminal
30	20	16	PE6 / ADC10 / AVREF PE6: Programmable port E6 ADC10: ADC Analog input channels 10 AVREF: ADC External Reference
31	-	-	CVREF: ADC An external reference voltage output for only 0.1uF Filter capacitor
32	-	-	AGND: The internal analog circuitry
33	twenty one	16	PE2 / SWD PE2: Programmable port E2 SWD: SWD Debug interface cable
34	twenty two		PE3 / ADC7 / AC1N PE3: Programmable port E3 ADC7: ADC Analog input channels 7 AC1N: Analog comparator negative input
35	twenty three	17	PC0 / ADC0 / APP0 PC0: Programmable port C0 ADC0: ADC Analog input channels 0 APP0: Positive input of the differential amplifier channels 0
36	twenty four	18	PC1 / ADC1 / APP1 PC1: Programmable port C1 ADC1: ADC Analog input channels 1 APP1: Positive input of the differential amplifier channels 1
37	25	-	PC2 / ADC2 / APN0 PC2: Programmable port C2 ADC2: ADC Analog input channels 2 APN0: Differential amplifier inverting input channels 0
38	26	-	PC3 / ADC3 / APN1 PC3: Programmable port C3 ADC3: ADC Analog input channels 3 APN1: Differential amplifier inverting input channels 1

39	27	19	PC4 / ADC4 / SDA PC4: Programmable port C4 ADC4: ADC Analog input channels 4 SDA: I2C Data line controller
40	28	20	PC5 / ADC5 / SCL PC5: Programmable port C5 ADC5: ADC Analog input channels 5 SCL: I2C The controller clock line
41	29	1	PC6 / RESETN PC6: Programmable port C6 RESETN: External reset input
42	-	-	PC7 / ADC8 / APN2 PC7: Programmable port C7 ADC8: ADC Analog input channels 8 APN2: Differential amplifier inverting input channels 2
43	-	-	PF0 / ADC9 / APN3 PF0: Programmable port F0 ADC9: ADC Analog input channels 9 APN3: Differential amplifier inverting input channels 3
44	30	-	PD0 / RXD PD0: Programmable port D0 RXD: USART Receiving input data
45	31	-	PD1 / TXD PD1: Programmable port D1 TXD: USART Data transmission output
46		1	PF1 / OC3A PF1: Programmable port F1 OC3A: Timer 3 Compare Match Output A
47	32	2	PD2 / INT0 / AC0O PD2: Programmable port D2 INT0: External interrupt input 0 AC0O: Analog comparator 0 Export
48			PF2 / OC3B PF2: Programmable port F2 OC3B: Timer 3 Compare Match Output B

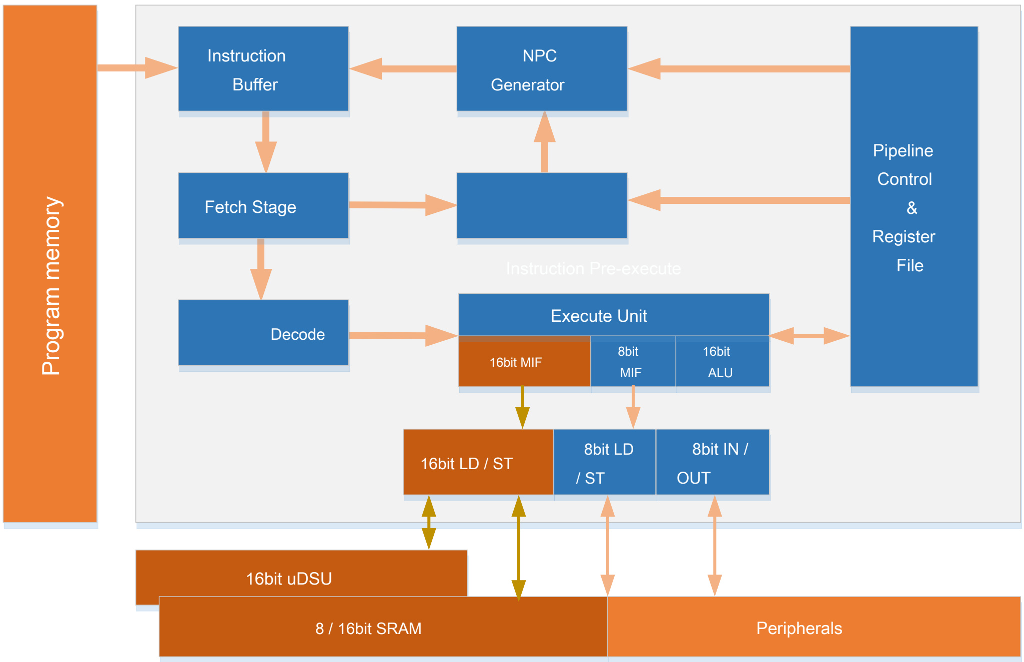
LGT8XM Kernel

- Low-power design
- high efficiency RISC Architecture
- 16 Place LD / ST Extension (uDSU dedicated)
- 130 Instructions, which 80% More than a single cycle
- Embedded In-Circuit Debugger (OCD) stand by

Outline

This chapter describes LGT8XM Core architecture and function. The kernel is MCU Brain, responsible for ensuring the correct implementation of the program, so the kernel must be able to perform accurate calculations, control peripherals and handle a variety of interrupts.

LGT8XM Kernel structure



In order to achieve greater efficiency and parallelism, LGT8XM Core uses Harvard architecture - Separate program and data buses. Through an optimized two instruction execution pipeline, the pipeline two pipeline is possible to reduce the number of invalid instructions, reduces the FLASH Views program memory, thus reducing power consumption of the core operation. Simultaneously LGT8XM Increased core before the instruction cache fetch stage (this can be cached simultaneously 2 Instructions), by the pre-execution module instruction fetch cycle further reduces the FLASH Program memory access frequency; by extensive testing, LGT8XM Can be reduced by about architecture than other similar kernel 50% Correct FLASH Access, greatly reducing the operating power consumption of the system.

LGT8XM Kernel has 32 More 8 General purpose working registers bit high-speed access (Register file) , Contributes to a single cycle of arithmetic and logic (ALU) . Under normal circumstances, ALU Two operands from the arithmetic average of general purpose working registers, ALU The result of the operation also written to the register file in one cycle.

32 A working register by 6 For paired together constituting a three 16 Bit registers, may be used for indirect addressing address pointers, and to access an external memory FLASH Program space. LGT8XM Single-cycle support 16 Bit arithmetic operations, greatly improves the efficiency of indirect addressing. LGT8XM These three special kernel 16 Bit registers is named X, Y, Z Register, will be described in detail later.

ALU Supported between the arithmetic logic operation between the register and the constant register, a single register may be operational in ALU In execution. ALU After the completion of the operation, the influence on the calculation result of the kernel state of the update to the state register (SREG) .

Program flow is controlled by conditional and unconditional jumps / call implementation, it can be addressed to the program area. most
LGT8XM Instructions 16 Bit. Each corresponding to a program address space 16 Position or 32 Bit LGT8XM instruction.

After the kernel interrupt response or subroutine calls, the return address (PC) It is stored in the stack. Stack is allocated in the system general data SRAM And therefore limited only by the size of the stack system SRAM The size and usage. All applications support interrupt or subroutine call, you must first initialize the stack pointer register (SP) , SP able to pass IO Space access. data
SRAM able to pass 5 Different addressing mode access. LGT8XM The internal storage space are mapped to a unified linear address space. For details, please refer to the introduction of the storage section.

LGT8XM A flexible core includes an interrupt controller, the interrupt function via a global state register interrupt enable bit. All interrupts have a separate interrupt vector. Interrupt priority and interrupt vector address corresponding relationship, the smaller the interrupt address, the higher the priority of the interrupt.

I / O Space contains 64 One can IN / OUT Instruction register direct addressing space. These control registers real kernel and the status register, SPI And other I / O Control function peripherals. This part of the space by IN / OUT
Direct access instruction, the address may be mapped to the data memory space accessed through them (0x20 - 0x5F) . In addition,
LGT8FX8P Also contains extended I / O Space, they are mapped to the data storage space 0x60 - 0xFF Here only use
ST / STS / STD as well as LD / LDS / LDD Instruction accesses.

To enhance the LGT8XM Core computing power Instruction increased prevalence line 16 Bit LD / ST Extension. this 16 Place
LD / ST Expand cooperation 16 Digital arithmetic acceleration unit (uDSU) Work to achieve efficient 16 Bit data operations. Concurrent kernel also increased RAM Spatial 16 Bit access capability. therefore 16 Place LD / ST Can be extended uDSU, RAM Transfer between the working register and 16 Bits of data. For details, refer " Digital arithmetic accelerator " chapter.

An arithmetic logic unit (ALU)

LGT8XM It contains an internal 16 Bit arithmetic logic unit, can be completed in one cycle 16 An arithmetic operation data. Efficient ALU versus 32 It is connected to general purpose working registers. To complete the arithmetic logic operation between the two registers or register with immediate data in one cycle. ALU Divided into three operations: arithmetic, logic, and bit operations. Simultaneously ALU Hardware multiplier section also includes a single-cycle can be achieved within a period of two 8 Direct register bit signed or unsigned operation. Refer to the instruction set of the detail portion.

Status Register (SREG)

Status register is mainly due to the implementation of the last preserved ALU Operation on the generated result information. The flow of information for controlling execution. It is a status register ALU Update operation is completely finished, so that the dispensed using a separate comparison instruction result is a more compact and efficient code. The status register does not automatically saved and restored in response to interrupts and exits from the interrupt, which requires software to be realized.

SREG Register Definition

SREG System status register								
address: 0x3F (0x5F)				Defaults: 0x00				
Bit	7	6	5	4	3	2	1	0
Name	I	T	H	S	V	N	Z	C
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[0]	C	The carry flag indicates arithmetic or logic operation results in a carry Refer INSTRUCTIONS						
[1]	Z	Zero flag indicating the result of an arithmetic or logic operation is zero, refer to the instruction description section						
[2]	N	Negative flag indicating arithmetic or logic operation produces a negative number, please refer to the instruction described Said portion						
[3]	V	Overflow flag, two's-complement operation result indicates overflow, refer to the instructions described Said portion						
[4]	S	Sign bit, equivalent to N versus V XOR operation result, specific instructions refer to the description section						
[5]	H	Half Carry Flag, in BCD Useful in the operation, it indicates a half-byte Operations produced into Place						
[6]	T	Temporary, bit copy (BLD) And bit memory (BST) Instructions for use, T Bit position as a temporary storage for temporarily storing the value of a general register bit. Refer to command description section						
[7]	I	Global interrupt enable bit, this bit must be set to 1 In order to enable the kernel interrupt response events. Different interrupt sources are controlled by independent control bits. Global interrupt enable bit is the interrupt signal control entered the final barrier kernel. I Interrupt vector bit is automatically cleared by hardware in response to the kernel, in the interrupt return instruction (RETI) After automatically set. I Bit can also be used SEI with CLI Instruction changes, refer to the instruction description section						

General purpose working registers

The general purpose registers LGT8XM Instruction set architecture optimization. In order to achieve efficiency and flexibility needed to execute the kernel, LGT8XM Internal general purpose working registers to support what several access modes:

- One 8 Read a bit at the same time 8 Bit write operation
- Two 8 Read a bit at the same time 8 Bit write operation
- Two 8 Read a bit at the same time 16 Bit write operation
- One 16 Read a bit at the same time 16 Bit write operation

LGT8XM General purpose working registers

	7 0	Addr.	
	R0	0x00	
	R1	0x01	
	R2	0x02	
	…		
	R13	0x0D	
	R14	0x0E	
General purpose working registers	R15	0x0F	
	R16	0x10	
	R17	0x11	
	…		
	R26	0x1A	X Register Low Byte
	R27	0x1B	X High byte register
	R28	0x1C	Y Register Low Byte
	R29	0x1D	Y High byte register
	R30	0x1E	Z Register Low Byte
	R31	0x1F	Z High byte register

Most instructions can directly access to all of the general-purpose working registers, they are also the most single-cycle instruction. As shown above, each register address corresponds to a data memory space, these general purpose registers are mapped into the data storage space. As soon as they do not really exist in SRAM But such storage unified organization mapped to visit them a lot of flexibility. X / Y / Z Index register pointer can be used as any general purpose registers.

X / Y / Z register

register R26 ... R31 It can be combinations of two, three configuration 16 Bit registers. These three 16 Bit register used primarily to access the address pointer indirection, X / Y / Z Register structure as follows:

	15 XH	XL 0
X register	7 0	7 0
	R27 (0x1B)	R26 (0x1A)

	15 YH	YL 0
Y register	7 0	7 0
	R29 (0x1D)	R28 (0x1C)

	15 ZH	ZL 0
Z register	7 0	7 0
	R31 (0x1F)	R30 (0x1E)

In the different addressing modes, These registers are used as a fixed offset, the auto-increment and auto-decrement of the address pointer described details, refer to the instruction portion.

Stack Pointer

Stack is used to store temporary data, local variables and subroutine return address and interrupt calls. Of particular note is not designed to stack grows from high addresses to low addresses. Stack pointer register (SP) Always points to the top of the stack. Stack pointers to data SRAM Where physical space, where he stored subroutine call or interrupt must stack space. PUSH Instruction will make the stack pointer is decremented.

Stack SRAM The location must perform or interrupt the correct setting is enabled by software before the subroutine. Generally the stack pointer is initialized to point SRAM The highest address. The stack pointer must be set to high SRAM Start address. SRAM Address map data storage system, refer to system data storage section.

Stack Pointer instructions

instruction	Stack Pointer	description
PUSH	increase 1	Data pushed onto the stack
CALL ICALL RCALL	increase 2	Interrupts or subroutine calls the return address onto the stack
POP	cut back 1	Data taken from the stack
RET RETI	cut back 2	Interrupt or subroutine call out the return address from the stack

Assigned by the stack pointer I / O Two spaces 8 Bit register configuration. The actual length of the implementation-dependent with system stack pointer. in LGT8XM Some chip architecture, the data space is so small that only SPL Addressing can meet the need, in this case, SPH Register will not occur.

SPH / SPL Stack Pointer Register Definition

SPH / SPL Stack pointer register	
SPH: 0x3E (0x5E) SPL: 0x3D (0x5D)	Defaults: RAMEND
SP	SP [15: 0]
R / W	R / W
Bit Definitions	
[7: 0]	SPL Low stack pointer 8 Place
[15: 8]	SPH Stack Pointer High 8 Place

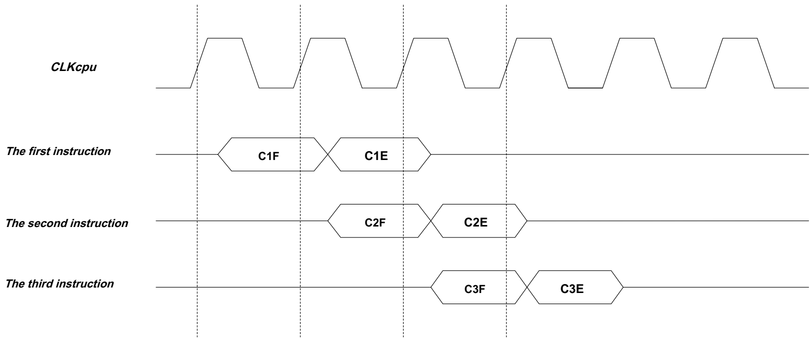
Instruction Execution Timing

This section describes the general concept of sequence execution. LGT8XM Kernel by the kernel clock (CLKcpu) Drive, the clock is directly derived from the system clock source selection circuit.

The following figure shows the instructions on the Harvard architecture and the fast access register file concept basis pipelined execution timing. This is the

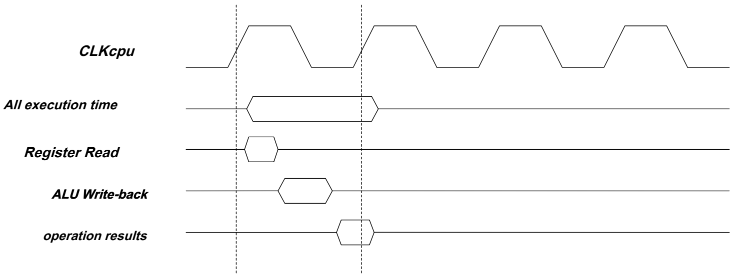
Have access to the kernel 1MIPS / MHz Guarantee the physical execution efficiency.

As can be seen from the figure, while the second instruction will read out during execution of the first instruction. When entering the second instruction execution



During the row, while the third will read instructions. So throughout the implementation period, you do not need to spend extra period of reading instruction, the pipeline from the point of view, to achieve efficiency every Monday execute an instruction.

The following figure shows the access sequence of general purpose working registers, in one cycle, ALU Operation uses two registers as operands, and during this period the ALU Execution result into the destination register.



Reset and Interrupt Handling

LGT8XM Support for multiple interrupt sources. These and a reset interrupt vector corresponding to a single program space vector entry program. In general, all the interrupts have a separate control bits. When the control bit is set and enabled kernel after the global interrupt enable bit kernel in order to respond to the interrupt.

The lowest default program space reserved for the reset and interrupt vector area. LGT8FX8P A complete list of supported interrupts refer to interrupts introduce chapters. This list also determines the priority levels of the different interrupts. The lower the interrupt vector address, the corresponding interrupt priority is higher. Reset (RESET) It has the highest priority, followed by INT0 - External Interrupt Request 0.
Interrupts can be redefined to any of the start address of the vector table (except for the reset vector) 256 Starting at byte aligned, need MCU Control Register (MCUCR) middle IVSEL Bits and IVBASE Vector base register achieve.

When the kernel response, the global interrupt enable flag I Hardware will be automatically cleared. Users can be I Bit enables the realization of nested interrupts. So any disruption that ensued will interrupt the current interrupt service routine. I Bit in the interrupt return instruction (RETI) After automatically set, the normal interrupt response can be followed.

A kind of basic types of interrupts. The first type is triggered by an event, the event interrupt set interrupt flag. After interruption for this, the kernel interrupt request, the current PC Value is a direct replacement for the actual interrupt vector address, perform the corresponding interrupt service routine, while the hardware interrupt flag is automatically cleared. Interrupt flag can also write to the location of the interrupt flag 1 Clear. If the interrupt occurs, the interrupt enable bit is cleared, the interrupt flag will still be set to record interrupt events. Wait until after the interrupt is enabled, the record interrupt event will be an immediate response. Similarly, if an interrupt occurs, the Global Interrupt Enable bit (SERG.I) Is cleared, the corresponding interrupt flag will be set to record interrupt events, etc.

The global interrupt enable bit is set, the interrupt will be recorded in order to perform in accordance with the priority.

The second type is interrupted when an interrupt condition persists, the response has been interrupted. Such interruptions do not need to interrupt flag. If the interrupt condition disappears before the interrupt is enabled, the interrupt will not get a response.

when LGT8XM Kernel from the interrupt service routine exits, execution flow returns to the main program. After performing one or several instructions in the main program, in order to respond to other requests pending interrupts.

Note that the system status register (SREG) It does not automatically save after entering the interrupt service, will not automatically resume after returning from the interrupt service. It must be responsible for handling the software.

When CLI After the instruction to disable interrupts, the interrupt will be banned immediately. in CLI So that occur after the instruction interrupts do not get a response. And even CLI Simultaneous interrupt instruction is executed, it will not be acknowledged. The following example shows how to use CLI Avoid interrupting upset EEPROM Write timing:

Interrupt response time

LGT8XM Kernel optimized for interrupt response so that any interruption in 4 Obtained in response to certain system clock cycles. 4 After the system clock cycles, enter the interrupt service routine execution cycle. At this 4 Internal clock, before the interruption

PC Value is pushed onto the stack, the system performs the process flow goes to the interrupt service routine corresponding to the interrupt vector. If an interrupt occurs during a multi-cycle instruction execution, the kernel will ensure the proper execution of the current instruction is completed. If an interrupt occurs in the system is in sleep state (SLEEP) , Interrupt response requires additional 4 Clock cycles. This increases the clock cycle synchronization cycle for wake-up from sleep mode operation selected. Detailed description of sleep mode, please refer to the relevant sections of power management.

Need to return from the interrupt service routine 2 Clock cycles. At this 2 Clock cycles, PC Restored from the stack, the stack pointer plus 2 And automatically enable global interrupt control bit.

The storage unit

Outline

This chapter describes LGT8FX8P Series of different internal storage units. LGT8XM Architecture supports two main types of internal storage space, namely data storage and program memory space. LGT8FX8P Interior also contains data FLASH May be implemented inside the controller EEPROM Data storage interfaces. In addition, LGT8FX8P The system also includes a special memory unit for storing system configuration information and the global chip device number (GUID) .

LGT8FX8P Series chip contains LGT8F88P / 168P / 328P Four different models; four models of peripherals, and is fully compatible packaging, the difference is FLASH Internal program memory space and data SRAM The following table compares the clear description of the LGT8FX8P Different series chip memory configurations:

DEVICE	FLASH	SRAM	E2PROM	Interrupt vector
LGT8F88P	8KB	1KB	2KB	1 Instruction words
LGT8F168P	16KB	1KB	4KB	2 Instruction words
LGT8F328P	32KB	2KB	It can be configured to 0K / 1K / 2K / 4K / 8K (versus FLASH shared)	2 Instruction words

LGT8F328P No separate internal analog for E2PROM Interface FLASH Space; means for simulation E2PROM The storage space program FLASH Sharing, the user depending on the application needs, to select the appropriate configuration.

Since the analog E2PROM Interface uses unique realization, the system requires twice the program FLASH Space simulation E2PROM Storage space, such as for LGT8F328P , When you configure a 1KB of E2PROM Space, there will be 2KB Bytes of program space is reserved, the rest 30KB of FLASH Space for storing programs.

LGT8F328P program FLASH versus E2PROM Shared configuration table:

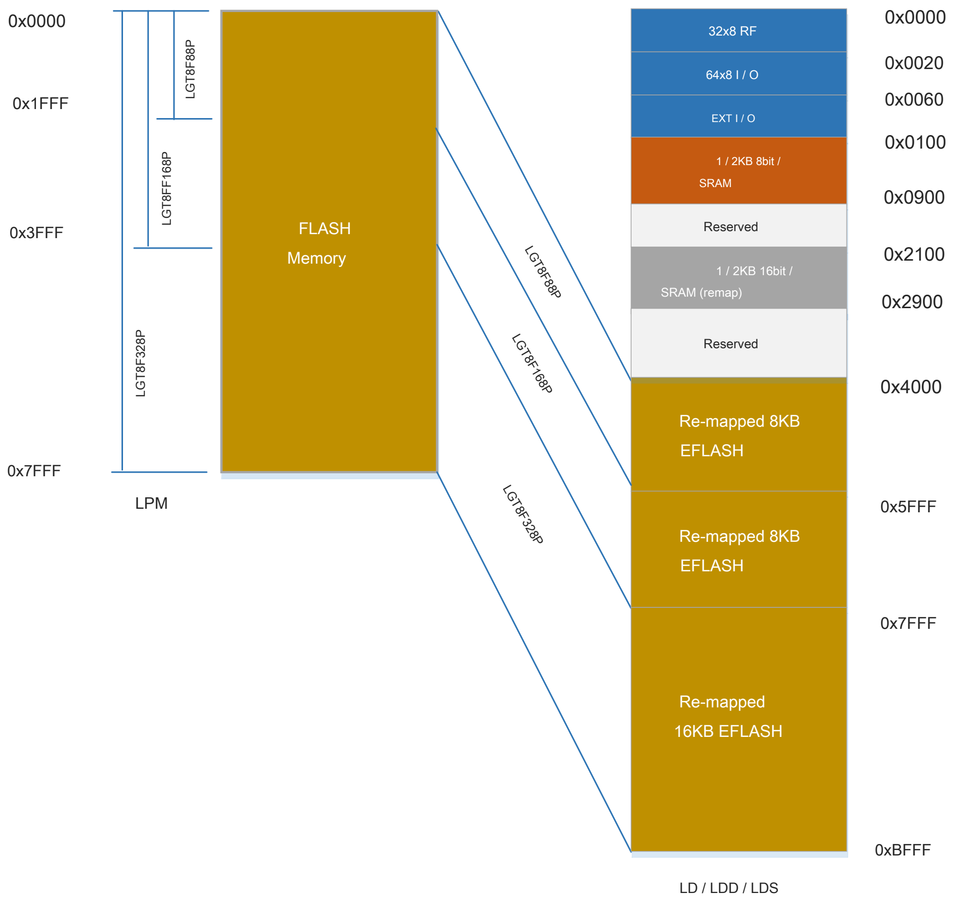
DEVICE	FLASH	E2PROM
LGT8F328P	32KB	0KB
	30KB	1KB
	28KB	2KB
	24KB	4KB
	16KB	8KB

System Programmable FLASH Program storage unit

LGT8FX8P Internal microcontrollers include 8K / 16K / 32K Byte on-chip programmable line FLASH A program storage unit.

program FLASH To ensure that at least 100,000 Or more of erase cycles. LGT8FX8P Internal integration FLASH Interface controller can be implemented in system programming (ISP) And since the upgrade functions of the program. Specific implementation details, please refer to the chapter on FLASH Description of the controller interface portion.

You can also program space LPM Instructions direct access (read), this feature can be achieved constant find application-related table. Simultaneously FLASH Program space is mapped to data memory space within the system, the user can also use LD / LDD / LDS To achieve FLASH Access to space. Program space is mapped to data memory space 0x4000 In the beginning of the address range. As shown below:



SRAM The data storage unit

LGT8FX8P Family of microcontrollers is a relatively complex microcontroller, which supports a plurality of different types of peripherals, which peripherals are allocated in the controller 64 More I / O Register space. Directly through IN / OUT Instruction accesses. Other peripheral control register allocation 0x60 ~ 0xFF Region, since this space is mapped into the data memory space, only through ST / STS / STD as well as LD / LDS / LDD And other commands access.

LGT8FX8P System data storage space from 0 Start address, the general purpose working registers are mapped file, I / O Space for expansion I / O Space and internal data SRAM space. initial 32 Bytes corresponding to the address LGT8XM Kernel 32
General purpose working registers. The following 64 Addresses can be achieved through IN / OUT Direct access to the standard instruction I / O space. Then the 160 Addresses is an extension I / O Space, the next step is up to 2K Bytes of data SRAM . From 0x4000 To begin 0xBFFF End of this space, mapped FLASH A program storage unit.

Within the system 1K / 2K byte SRAM They are respectively mapped to two spaces. From 0x0100 To begin 0x0900 This is the end of the space to the kernel 8 The width of the read bit bytes. From 0x2100 To begin 0x2900 This area is ended 16 Bit access space width. system RAM It is mapped to 0x2100 Mainly used for upper address begins with uDSU Module work to achieve efficient 16 Bit data storage. In programming, the ordinary 8 Addressing variable bit address plus 0x2000 Offset to switch to 16 Bit access mode.

System Support 5 Different addressing modes can cover the entire data space: Direct access Indirect access band offset, indirect access, front access to decrement indirect access address, the access address increment indirect access. General purpose working registers R26 To R31 Indirect address pointer for access. Indirect addressing can access the entire data storage space. With indirect access to the offset address can be addressed to Y / Z Near the base address register 63 Address space.

When using the support auto-increment / decrement register indirect access mode, the address register X / Y / Z Will automatically decrement / increment by hardware access occurs before / after. Refer to the instruction set description section.

16 Bit register X / Y / Z And the associated automatic addressing mode (increasing, decreasing), in 16 Lower extended mode also has a very important role. 16 Bit extended mode can be used LD / ST The increment / decrement mode, with automatic variable increment, decrement addressing. This mode when an arithmetic operation of the array, will be very effective. Please refer to the specific implementation " Digital arithmetic accelerator (uDSU) " The relevant sections.

Common I / O register

LGT8FX8P of I / O There are three common space I / O register GPIOR2 / 1/0 , These three registers can be used IN / OUT Access instruction, for storing user-defined data.

Peripheral register space

I / O Detailed definition of space, see LGT8FX8P Data Sheet " Registers Overview " chapter.

LGT8FX8P So peripherals are assigned to I / O space. all I / O Address space can be LD / LDS / LDDD as well as ST / STS / STD Instruction accesses. Data access is through 32 General purpose working registers transfer. in 0x00 ~ 0x1F between I / O Instruction register can be addressed via bit SBI with CBI access. In these registers, a bit value may be used a SBIS with SBIC Instruction detection, process control program to execute. Refer to the instruction set description section.

When IN / OUT Instruction Access I / O When the register must be addressed 0x00 ~ 0x3F Address between. When LD or ST Instruction Access I / O When space must pass I / O Space unified data mapping space in the system memory map address access (plus 0x20 Offset). Some other assignments in the extended I / O Peripheral register space (0x60 ~ 0xFF) , Can only use ST / STS / STD with LD / LDS / LDD Instruction accesses.

For compatibility with future devices, reserved bits must be written in the write operation 0 . You can not be reserved I / O Write operation is performed on the space.

Some registers include a state flag that needs to be written 1 It can be cleared. have to be aware of is, CBI with SBI Command supports only specific bits, CBI / SBI It can only work on registers containing such status flags. In addition, CBI / SBI Command can only work in 0x00 To 0x1F Registers this address range.

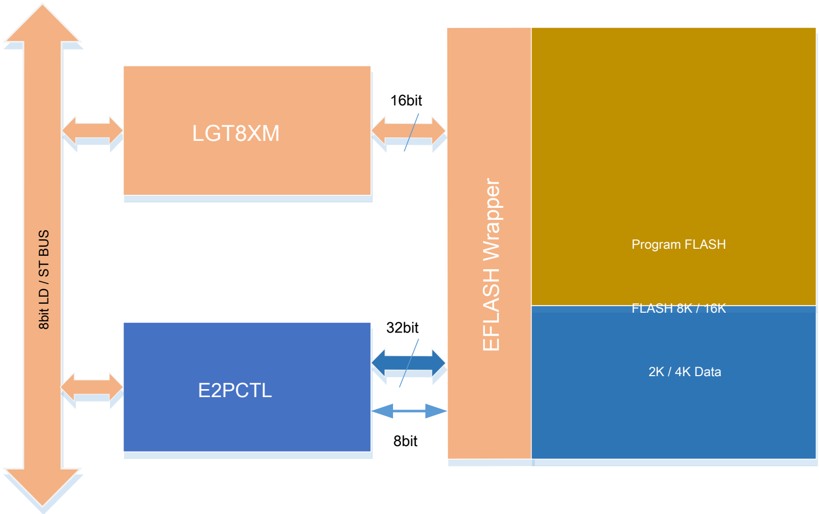
FLASH Controller (E2PCTL)

LGT8FX8P Internally integrates a flexible and reliable EFLASH Read-write controller, the system may utilize existing data FLASH Memory, read and write access for byte of storage space, to achieve a similar E2PROM Storage applications; E2PROM Interface using flash analog equalization algorithm, data can be FLASH Life cycle improve 1 Times or so, to ensure 100,000 Or more of erase cycles.

E2PCTL The controller also realized the FLASH Online program space erase operation can be achieved through software online from

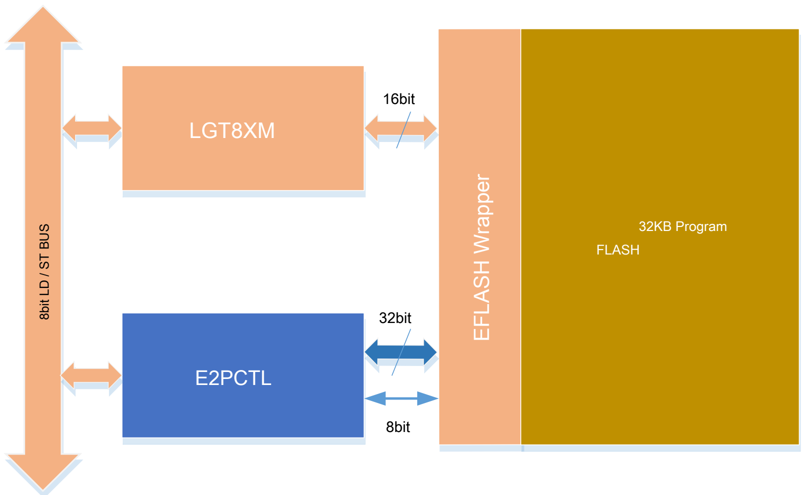
Dynamic firmware upgrade function. by FLASH Controller Access Program FLASH Space program, supports only Page Erase (1024 Byte) and 32 Read and write access bit width.

LGT8F88D / 168D E2PCTL FIG controller architecture



E2PCTL simulation E2PROM Function to access data FLASH When the space can support 8 Position, 32 Write bit width. Access program FLASH When space, support and page erase 32 Bit data read and write. due to LGT8FX8P internal FLASH The minimum storage unit 32 Position, it is recommended use 32 Bit access, especially for write operations. 32 Read and write operations not only efficient bit access, but also conducive to the protection of FLASH Endurance memory cell.

LGT8F328P E2PCTL FIG controller architecture



LGT8F328P No extra internal data FLASH. therefore, LGT8XM Core and E2PCTL Share internal 32K byte FLASH storage. Users can, will 32K byte FLASH Space is divided into program space and data space. By configuring E2PCTL The controller may set the analog E2PROM The size of the space. E2PCTL Use paging mode analog E2PROM Logic algorithm page (1K Bytes). Therefore simulation 1K Byte E2PROM Space, need to occupy 2K Byte FLASH Space, and so on, to achieve 4K Byte E2PROM , Take up 8K Byte

FLASH space. Specific implementations, please refer to E2PCTL Description of the algorithm implementation.

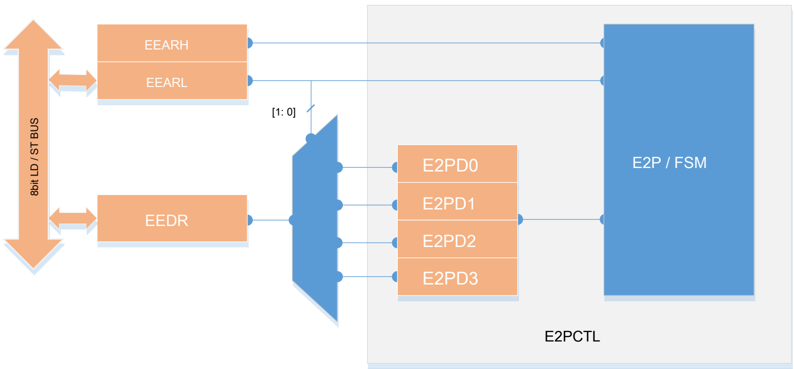
E2PCTL Data register

E2PCTL There are internal controller 4 Bytes of data cache (E2PD0 ~ 3) ,this 4 The composition of the final byte cache access FLASH Spatial 32 Bit data interface.

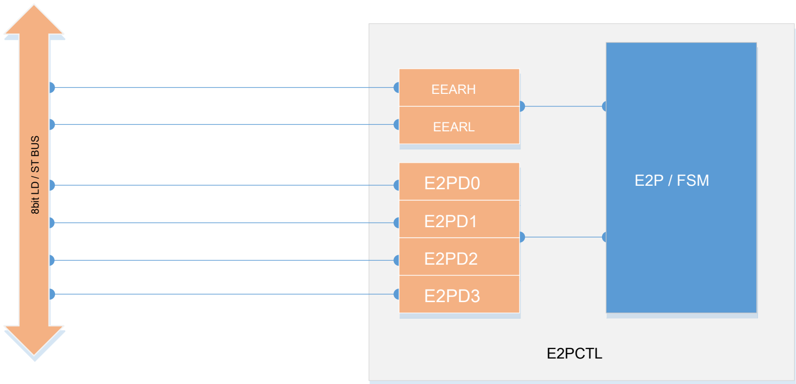
when E2PCTL Controller operates in byte read and write mode, EEDR As an interface to read and write bytes of data, E2PCTL more EEARL [1: 0] Address information to load data into the correct data cache, and according to the current FLASH Padded data destination further three bytes of data, The final will be a combination of full 32 Bit data updates to FLASH in.

when E2PCTL work at 32 When the bit read-write mode, At this point you can still use EEDR Data register as a common interface through EEARL [1: 0] As the internal address addressing data cache, a full read and write 32 Bit data. In addition, use may also be directly mapped to the data cache IO Direct access to the register space (E0 ~ 3) .

E2PCTL work at 8 Bit byte data write mode access a schematic view:



E2PCTL work at 32 Data read-write mode bit access word schematic:



Byte mode for downward compatibility LGT8FX8D Byte-write mode. LGT8FX8P Built-in FLASH for 32 Bit interface width, using 32 Bit reads and writes will write efficiency and FLASH The Endurance bring great benefits, it is recommended to use 32 Bit read-write mode.

E2PCTL simulation E2PROM Interface algorithm

we know, FLASH The memory must be erased before writing, and erasing operation is in units of pages. LGT8FX8P Internal FLASH A memory page size is 1K byte. Therefore, in order to update a data byte page, the data also need to be erased entire page, and then update the target address data, and other page while restoring bytes of data, the entire operation not only time consuming, It also brings the risk of data loss due to unexpected power.

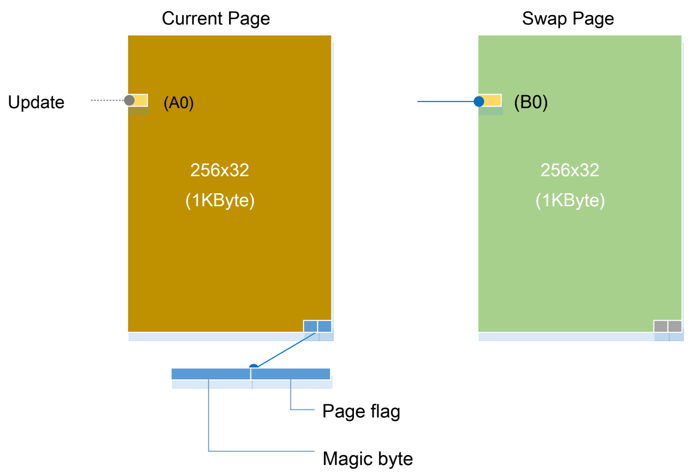
E2PCTL Internal use of paging algorithm simulation E2PROM . Page mode switching algorithm can guarantee the implementation of a page erase, not because of power failure and other unforeseen circumstances result in the loss of the original data. As well as exchange algorithm 2 A page space

Using mutually exchanged alternately, Also increases simulation E2PROM Life space.

In terms of efficiency, E2PCTL The controller implements a continuous data update mode, the update data is reduced by repeated brought rewritable process.

In terms of realization, E2PCTL Managed separately for each page, and a page was last occupied 2 Bytes as an information page states. In use the user is greater than 1K of E2PROM When the simulation space, we need to pay attention to address cross 1K Special treatment space. Because each 1K The last space 2 Bytes reserved for E2PCTL Use, the user can not this 2 Bytes of space for proper read and write.

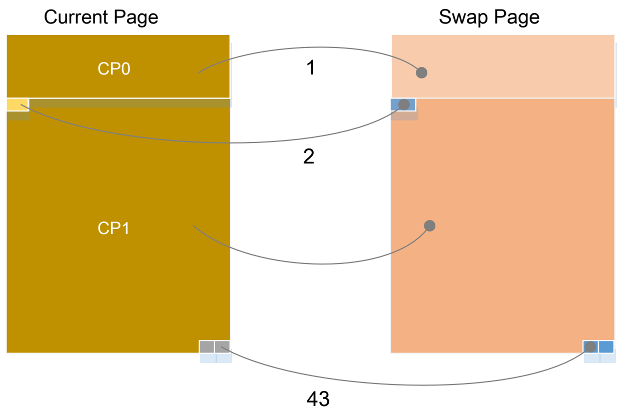
The figure below shows E2PCTL Based schematic page exchange algorithm:



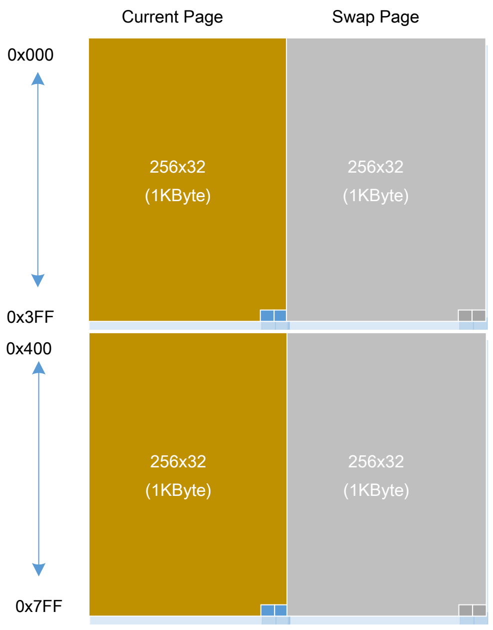
as the picture shows, E2PCTL internal use 2 Pages simulate a page size E2PROM space. These two pages are marked as a current page, in addition to the exchange page. E2PCTL Use the last page 2 Bytes of memory page information. When we need to update one byte page, such as the image above A0 byte. First of all, we do not erase the current page, but the page erase exchange. Then the current page is divided into 3 A part of the operation. The first is A0 Before the data, this has become part of our space CP0 ,Afterwards A0 After the data, this part of space CP1 . E2PCTL Based on user configuration, CP0 Copying data corresponding to the address corresponding to the page switching, and then need to update the data written to the address corresponding to the page switching (B0) And finally copy CP1 To exchange data page.

After the completion of the operation, the data exchange has been completed, but does not update the page status. Therefore, if power failure occurs before or other abnormalities, because this update operation is not complete, and before the data is not destroyed, to ensure data integrity. If everything goes well, E2PCTL Will be at CP1 Finally, the updated page status page for exchanging data written information before the exchange of the page, to realize replace face to face page. Since then, the exchange page becomes the current page.

E2PCTL Page exchange process shown below (1-> 2-> 3-> 4) :



When the system configuration E2PROM Simulation space is greater than 1K Time, E2PCTL Or to the page for the smallest unit to achieve E2PROM Simulation algorithm space. For example, if you configure 2K of E2PROM Area, in fact, E2PCTL It will take up 4 Pages (4K)Space. among them 2 It is a set of pages, a page size for the analog E2PROM space.



Note that the user-configured 2K Byte E2PROM Space is not continuous, because the end of each page 2 Bytes will be used to save the page state information.

E2PCTL Continuous programming mode

Because by E2PCTL Updates will lead to the exchange page, the page will exchange process for exchanging page erase, page erase not only time consuming, but also will increase FLASH The loss of life. therefore E2PCTL Increases sequential write mode. In the continuous write mode, the user can continuously update E2PROM Area, only in the last consecutive addresses, will perform paging operations, applications that require continuous updating a block of data, Continuous mode more effective.

Continuous programming mode E2PCTL Control register ECCR of SWM Bit. After the continuous mode is enabled, the subsequent write operation to write data directly on the switch corresponding to the page address, in SWM Mode, the write operation is not performed CP0 / 1 Area data copy operation. Before writing the last byte, software SWM Prohibit continuous mode, and then write, then E2PCTL Will perform a complete CP0 / 1 The copy operation and update status information page.

E2PCTL Read and write FLASH Program Space

by E2PCTL The controller can be achieved on the program FLASH Read and write access to space. And simulation E2PROM The difference is that by E2PCTL The program FLASH Access to space requires full software control. Proceed as follows:

1. Erase the target page, you need to first erase data before updating the target page, the page address EEAR To register

   Out. Correct FLASH Page erase command and control, please refer to EECR Defined register;
2. programming FLASH Space must be 32 Bit is the smallest unit. by E2PD0 ~ 3 Setting data;
3. By the destination address EEAR Given register, the address EEAR [1: 0] It will be ignored;

by E2PCTL Literacy program FLASH Space, can be achieved online updates (IAP) Function, in some field applications require custom update update application data and the need for the product, very useful.

E2PCTL Interface operation process

E2PCTL The controller works primarily through 4 Registers implemented, respectively, E2PCTL Control Status Register EECR , ECCR ; Data register EEDR (E2PD0 ~ E2PD3) And address register EEAR (EEARL / EEARH) .

ECCR Register sets E2PCTL Working conditions, required in most states E2PCTL Set before the completion of the work, this process is generally implemented in a system initialization. ECCR Register SWM Write bit enables the continuous mode, the control bit needs to be set in a continuous operation during the write.

EECR For controlling the operation type selection register, to select an operation instruction, such as setting the read, erase command.

EEDR Register for 8 Byte mode interface, E2PD0 ~ 3 For 32 Write bit mode operation;

EEAR Register sets read and write target address, page address is also used to set the page erase operations. Page address is the page-bit units have been aligned, the page size is 1K Byte, note EEAR Specified address is a byte address.

by E2PCTL Access Interface FLASH Program space:

by E2PCTL Interface can be achieved on FLASH Read, write and erase program space. Correct FLASH Supports only reading and writing space 32 Bit access width. Page erase operation to position the unit, the size of each page 1K byte(256x32) .

Write FLASH Before the program space, First page erase the destination address is located. E2PCTL write FLASH Space program does not support continuous mode, Users need in order to complete the write operation. The following is a rewritable FLASH Program space process:

1. program FLASH Page Erase

- Set up EEAR [14: 0] To be erased target page address, the program FLASH One size 1K Bytes, EEAR [14:10] The page address, EEAR [9: 0] Set as 0
- Set up EEPM [3: 0] = 1X01 ,among them EEPM [2] Can be set 0 or 1
- Set up EEMPE = 1 , Simultaneously EEPE = 0
- Within four cycles, provided EEPE = 1 ,starting program FLASH Erase Procedure

2. program FLASH Program operation

- write E2PD0 ~ 3 ,ready 32 Bit programming data
- Set up EEAR As the destination address, the address is here 4 Byte alignment
- Set up EEPM [3: 0] = 1X10 , among them EEPM [2] Can be set 0 or 1
- Set up EEMPE = 1 ,Simultaneously EEPE = 0
- Within four cycles, provided EEPE = 1 ,start up FLASH Programming Process

by E2PCTL Access Interface E2PROM Simulated space:

E2PCTL Analog controller E2PROM Data access interface logic FLASH space. simulation E2PROM stand by 8 Position, 16 Bits and 32 Data read and write access bit width. 8 Byte mode E2PROM Better compatibility with the interface. 32 Bit mode and will help improve storage efficiency FLASH Of life, and therefore 32 Bit reads and writes for the proposed read-write mode. E2PROM Analog interface supports continuous write mode, the need to update multiple consecutive address data applications, the obvious advantages, is recommended.

for LGT8F88P / 168P ,data FLASH Independent storage space. Without going through ECCR And enable register configuration FLASH Data space. LGT8F328P And no independent data FLASH Space data FLASH And procedures FLASH shared 32K byte FLASH space. Need ECCR Enabling data register FLASH Partition function, and by ECCR Register ECS [1: 0] Bit configuration data FLASH the size of. The configuration takes effect, use other methods and LGT8F88P / 168P the same.

FLASH The controller in the realization E2PROM Interface, the interior has been achieved automatically erased when the necessary data FLASH The logic, EPROM Erase command is optional, this command is only used when the user needs to perform individually erased.

EECR Register control FLASH Erase / write timing, including program FLASH with E2PROM . The particular type of operation required by EECR Register EEPME with EEPM [3: 0] set up. Correct E2PROM Read operation is relatively simple, after setting a good destination address and patterns, write EERE Will come into target address corresponding 32 Bit data read FLASH An internal controller, the user can EEDR Read byte register interest. FLASH The controller does not implement the program FLASH Read space, the user can easily use LPM Or by program FLASH At unified mapping space using address data

LD / LDD / LDS Instruction read.

1.8 Bit mode, programming E2PROM

- To set the target address EEARH / L register
- To set up new data EEDR register
- Set up EEPM [3: 1] = 000 , EEPM [0] Can be set 0 or 1
- Set up EEMPE = 1 , Simultaneously EEPE = 0
- Within four cycles, provided EEPE = 1

When the setting is completed, FLASH The controller will start the programming operation, the programming period CPU It will remain on the current instruction address, will continue to run until after the operation is completed. During programming, if the data needs to be erased FLASH , FLASH The controller will start erasing process automatically.

2.32 Bit mode, programming E2PROM

- by E2PD0 ~ 3 ,ready 32 Bit data
- To set the target address EEARH / L register. Note that this is byte-aligned address, FLASH Controller with EEAR [15: 2] As access FLASH the address of.
- Set up EEPM [3: 1] = 010 , EEPM [0] Can be set 0 or 1
- Set up EEMPE = 1 , Simultaneously EEPE = 0
- Within four cycles, provided EEPE = 1

3.8 Bit mode, Reading E2PROM

- To set the target address EEARH / L register
- Set up EEPM [3: 1] = 000
- Set up EERE = 1 start up E2PROM Read
- wait 2 Cycles (two execution NOP operating)
- Data corresponding to the target address is updated to EEDR register

4.32 Bit mode, Reading E2PROM

- Set up EEARH / L As the destination address, the address is 4 Byte alignment
- Set up EEPM [3: 1] = 010 Open 32 Bit interface mode
- Set up EERE = 1 ,start up E2PROM Read
- wait 2 A system clock cycle (execution of two NOP instruction)

E2PCTL Analog access E2PROM Space, support continuous programming mode, continuous mode to access an application needs to update data blocks are very efficient, but also help to improve FLASH Life. Continuous mode supports only programming 32 Data programming operation bit width.

Continuous access mode ECCR Register SWM Bit. SWM When enabled, followed by E2PCTL Write simulation E2PROM Space in the continuous operation mode programming. In successive programming mode, E2PCTL The controller automatically feed the data processing in the case where the target address. However, if occurs in a continuous feed during the programming mode, programming the controller in a continuous process, not automatically CP0 / 1 Data exchange area, it will not update the page information.

When programmed to continuously before the last operation, by clearing SWM Close continuous bit programming mode, then the non- SWM The last time the programming operation mode start after the end of the programming, E2PCTL Will automatically CP0 / 1 Copying data exchange area to the page, and the page update exchange, making the currently active page, thus completing the entire successive programming operation.

5. Process successive programming mode:

1. by ECCR Configuration Data FLASH The size and enable SWM Place
2. use 32 Bit mode simulation program E2PROM region
3. If this is not the last operation, go back to step 2 Under a continuing program data
4. If you reach the last program, first by SWM Prohibit successive programming mode, then step 2 of

   Operational processes completion of the last program

E2PCTL Efficient FLASH Data Management

E2PCTL In addition to programming the controller to achieve a continuous mode, can also ECCR Register CP0 / 1 Bits of data exchange paging process replication independent control. ECCR Register CP0 / 1 Exchange processes are used to control page for the current page CP0 / 1 Area data exchange operation. Clear CP0 / 1 Position, in the paging procedure does not exchange data area corresponding to the current page. An efficient management method provided in this section, will use this feature.

in FLASH Data update process, the most time-consuming operation occurs in the exchange page erase procedure. Therefore, we can address one kind of data management method to minimize the number of page erase, both to improve programming efficiency, life loss can be reduced.

Here we provide a reference algorithm for block-based data management application:

1. Assume that the user data is only a complete data block, data block size 4 Integer number of bytes;
2. Data update will update every time a complete data block
3. In addition to the block information storing user data, Also you need to store a block management information

Under the above three conditions, we can take full advantage E2PCTL Continuous programming mode and automatic paging mechanism to achieve a high efficiency FLASH Data management methods.

Since the data is updated each time a data block is the same size, and each block data structure is stored in the address information points to the next block of data, we can update the data every time in order of address programming FLASH Without making CP0 / 1 Data replication. And because every time the update data to a region has been erased, Page Erase does not occur.

When the last piece of data is written, at which point the configuration information back to the starting address of a data area of the page. This occurs after the data write operation, E2PCTL It will start the process of erasing a page, and update the currently active page.

FLASH Protection operation

in case VCC Voltage is low, FLASH The erase operation may occur error because the voltage is too low.

FLASH / Data erase operation error at low pressure may be provided by two reasons. First, the normal FLASH Erase operation requires a minimum operating voltage, this voltage is lower than the operation will fail and result in data errors. The second reason is the kernel operating at a certain frequency, it requires a minimum voltage requirement, when this voltage is below, the instruction execution error will result, so that FLASH Operating errors occur.

By following simple ways to avoid similar problems:

When the supply voltage is low, the system enters the reset state. This low-voltage detection circuit can be arranged inside (VDT) achieve. in case VDT Detecting the current operating voltage is lower than the set threshold, VDT Will output a reset signal. in case VDT Threshold can not meet the needs of the application, can be considered an additional external reset circuit.

Register Description

FLASH Address Register - EEARH / EEARL

EEARH / EEARL		
EEARH: 0x22 (0x42) EEARL: 0x21 (0x41)	Defaults: 0x0000	
bits	EEAR [15: 0]	
R / W	R / W	
Bit Definitions		
[7: 0]	EEARL EFLASH / E2PROM Access address low 8 Bit.	
[14: 8]	EEARH EFLASH / E2PROM Access Address High 7 Place	
[15]	-	Are reserved

When E2PCTL Controller Access Program FLASH When the region, EEAR [14: 2] Used to access 4 Byte aligned entire program space. EEAR [1: 0] Only access to the data register EEDR Use. For details, please refer to the following on EEDR Description data register. E2PCTL Controller Support 8/16/32 Bit mode, no matter what kind of model, here EEAR Are byte aligned address.

FLASH Data Register - EEDR / E2PD0

EEDR / E2PD0 - FLASH / E2PROM Data register 0		
EEDR / E2PD0: 0x20 (0x40)	Defaults: 0x00	
bits	EEDR [7: 0]	
R / W	R / W	
Bit Definitions		
[7: 0]	EEDR E2PD0	E2PCTL Data register 16/32 When the bit pattern, used to access the least significant byte

FLASH Data Register - E2PD1

E2PD1 - E2PCTL Data register 1	
E2PD1: 0x5A	Defaults: 0x00
bits	E2PD1 [7: 0]

R / W	R / W
Bit Definitions	
[7: 0]	E2PD1 16 When the bit pattern for storing 16 High-bit data 8 Place 32 When used to store the low bit pattern 16 High-bit data 8 Place

FLASH Data Register - E2PD2

E2PD2 - FLASH Data register 2	
E2PD2: 0x57	Defaults: 0x00
Bits	E2PD2 [7: 0]
R / W	R / W
Bit Definitions	
[7: 0]	E2PD2 32 When the bit pattern for storing high 16 Low-bit data 8 Place

FLASH Data Register - E2PD3

E2PD3 - FLASH Data register 3	
E2PD3: 0x5C	Defaults: 0x00
Bits	E2PD3 [7: 0]
R / W	R / W
Bit Definitions	
[7: 0]	E2PD3 32 When the bit pattern for storing high 16 High-bit data 8 Place

FLASH Mode Control Register - ECCR

ECCR - FLASH / E2PROM Configuration Register								
ECCR: 0x36 (0x56)					Defaults: 0x0C			
bits	WEN	EEN	ERN	SWM	CP1	CP0	ECS1	ECS0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
The initial value	0	0	0	0	1	1	0	0

Bit Definitions		
[7]	WEN	ECCR Write enable control modification ECCR Before, you must first WEN write 1 And then 6 Within a periodic update ECCR Contents of the register
[6]	EEN	E2PROM Enabled, only LGT8F328P effective 1 :Enable E2PROM Simulation, will from 32KFLASH Reserved some space 0 : Disabled E2PROM simulation, 32KFLASH All for program space
[5]	ERN	write 1 Reset E2PCTL Controller
[4]	SWM	Continuous write mode for simulation E2PROM Controller Operation
[3]	CP1	Page exchange CP1 Regional enable control
[2]	CP0	Page exchange CP0 Regional enable control
[1: 0]	ECS [1: 0]	E2PROM Configuration space 00 : 1KB E2PROM, 30KB program FLASH 01 : 2KB E2PROM, 28KB program FLASH

		10 : 4KB E2PROM, 24KB program FLASH 11 : 8KB E2PROM, 16KB program FLASH

FLASH Access Control Register - EECR

EECR - FLASH / E2PROM Control register								
EECR: 0x1F (0x3F)				Defaults: 0x00				
bits	EEPM3	EEPM2	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
The initial value	0	0	0	0	0	0	0	0
Bit Definitions								

Bits	Name	[3]	[2]	[1]	[0]	Mode Description
[7: 4]	EEPM [3: 0]	EFLASH / EPROM Access mode control bits				
		0	0	0	x	8 Bit mode read / write E2PROM (default)
		0	0	1	x	16 Bit mode read / write E2PROM
		0	1	0	x	32 Bit mode read / write E2PROM
		1	x	0	0	E2PROM Erase (optional)
		1	x	0	1	program FLASH Erased (page erase)
		1	x	1	0	program FLASH program
		1	x	1	1	Reset FLASH / E2PROM Controller

[3]	EERIE	FLASH / E2PROM Ready interrupt enable control. write 1 Enable write 0 Prohibited. when EEPE After the hardware is automatically cleared, E2PROM Ready interrupt valid. in EPROM During operation, this will not generate an interrupt
[2]	EEMPE	FLASH / E2PROM Programming operation enable control bit EEMPE For control EEPE Is valid, when at the same time set EEMPE for 1 , EEPE for 0 After, in four cycles after setting EEPE for 1 Will start the programming operation. Otherwise invalid programming operation. After four cycles, EEMPE It is automatically cleared
[1]	EEPE	FLASH / E2PROM Programming operation enable bit
[0]	EERE	E2PROM Read enable bit, data valid after two periodic

Common I / O register- GPIOR2

GPIOR2 - Common I / O register 2	
GPIOR2: 0x2B (0x4B)	Defaults: 0x00
Bits	GPIOR2 [7: 0]
R / W	R / W
The initial value	0x00
Bit Definitions	
[7: 0]	GPIOR2 Common I / O register 2 For storing a user-defined data

Common I / O register- GPIOR1

GPIOR1 - Common I / O register 1		
GPIOR1: 0x2A (0x4A)		Defaults: 0x00
Bits	GPIOR1 [7: 0]	
R / W	R / W	
The initial value	0x00	
Bit Definitions		
[7: 0]	GPIOR1	Common I / O register 1 For storing a user-defined data

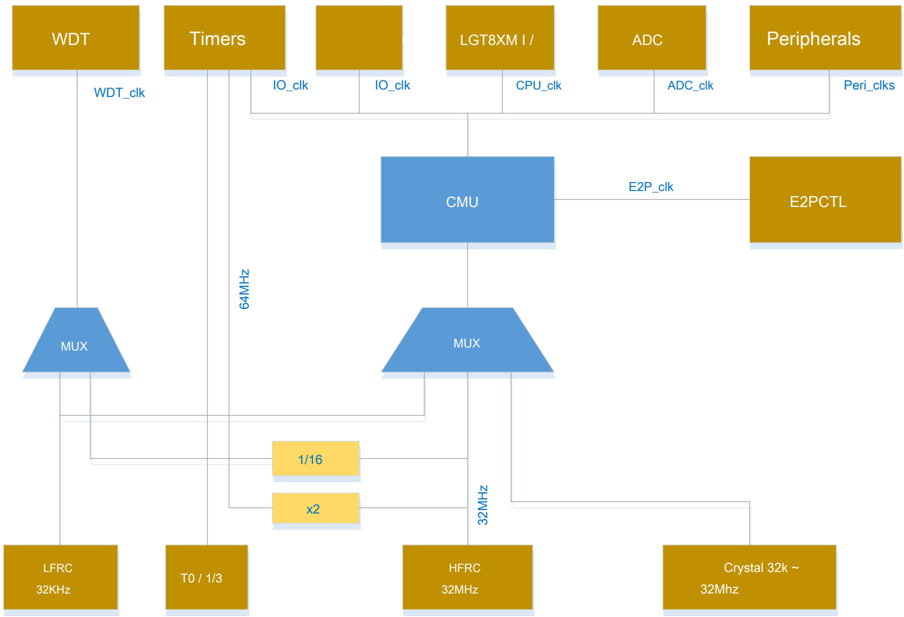
Common I / O register- GPIOR0

GPIOR0 - Common I / O register 0		
GPIOR0: 0x1E (0x3E)		Defaults: 0x00
Bits	GPIOR0 [7: 0]	
R / W	R / W	
The initial value	0x00	
Bit Definitions		
[7: 0]	GPIOR0	Common I / O register 0 For storing a user-defined data

System Clock and Configuration

System Clock Distribution

LGT8FX8P Support for multiple clock input. The system can operate in three main clock sources, each of the internal 32KHz Can be calibrated RC Oscillator, internal 32MHz Can be calibrated RC And an external oscillator 400KHz ~ 32MHz Crystal input. The figure below shows LGT8FX8P Clock distribution system, CMU The center of the clock management is responsible for dividing the system clock, the clocks generated independently for different clock control module and the like. General applications, not all of the clocks do not operate simultaneously, in order to reduce power consumption, depending on the power management system of the sleep mode, the clock is not used to close the module. Specific operation details, please refer to the relevant sections of power management.



CPU_clk

For driving LGT8XM Kernel and SRAM Operation. Such drive general purpose working registers, status registers, etc.

CPU After the clock is stopped, the kernel will not continue to execute instructions and calculation. Execution system SLEEP After the instruction into the sleep mode the core clock will be turned off.

Peri_clk

Most peripheral modules for driving, such as timer / counter, SPI , USART Wait. IO Clock is also used to drive an external interrupt module. When the peripheral clock is stopped due to sleep, some peripherals may be part of the work in the wake of the system clock or a separate asynchronous mode. such as TWI The address recognition can wake up most of the sleep mode, when the address recognition part of the work in asynchronous mode.

E2P_clk

E2P_clk A clock for generating FLASH Interface access timing. E2P_clk Generating access E2PCTL access FLASH The timing of the interface. E2P_clk Fixed from the inside 32MHz HFRC Oscillator 32 Divider (1MHz) . If you need to use E2PCTL Internal program module to read and write FLASH Or data FLASH Space, need to be able to advance inside 32MHz Oscillator.

Asy_clk

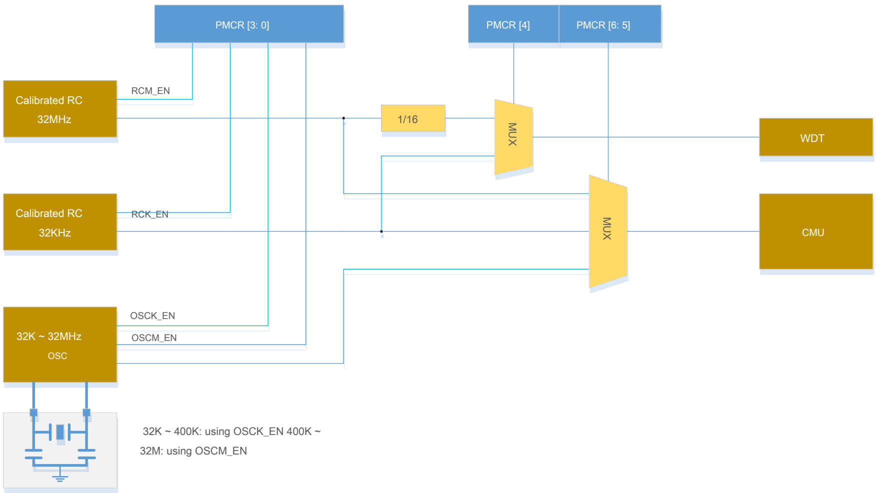
Asynchronous timer clock. Timer / counters can be used as an external clock or crystal oscillator (32.768K) drive. This independent clock mode, the system can handle the sleep mode, the timer keeps running.

WDT_clk

Internal watchdog timer clock source, may be configured to select the internal 32KHz LFRC Oscillator, or from within 32MHz HFRC of 16 Divider (2MHz). After the system, watchdog default clock source 32KHz LFRC Oscillator.

Clock source selection

LGT8FX8P stand by 4 Input clock sources, the user can PMCR Register achieve clock source can be controlled, and to complete the handover of the master clock. Here is PMCR FIG control structure:



LGT8FX8P internal OSC The oscillator can operate at high frequency and low frequency modes, the user needs to control the actual size of the interior of the external oscillator OSC Oscillator operates in the correct mode. The same internal RC Oscillator is also divided into two kinds of high and low frequencies. PMCR Lowest register 4 Four bits for controlling the clock source. Control relationship is as follows:

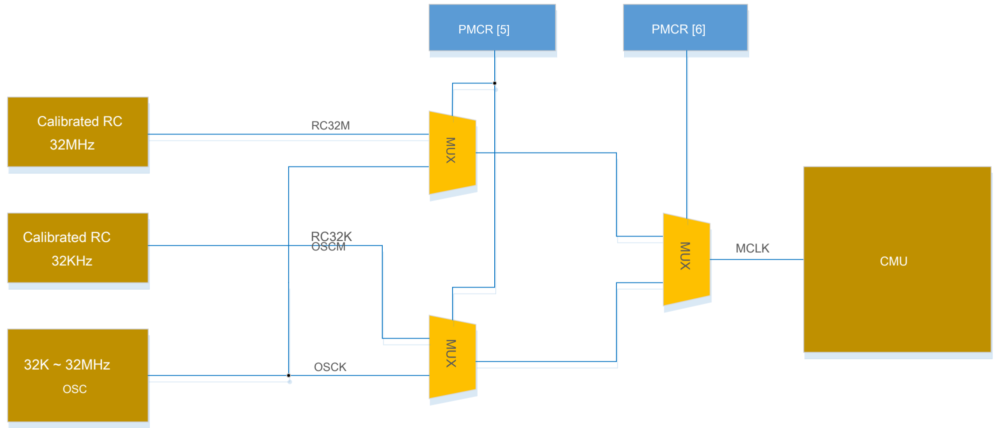
PMCR	Of the clock source
PMCR [0]	32MHz RC Enable control, 1 Enable, 0 shut down
PMCR [1]	32KHz RC Enable control, 1 Enable, 0 shut down
PMCR [2]	400K ~ 32MHz OSC Mode is enabled, 1 Enable, 0 shut down
PMCR [3]	32K ~ 400K OSC Mode is enabled, 1 Enable, 0 shut down

LGT8FX8P After the power system, is used by default 32MHz RC As the system clock source, clock source core at 8 Divider (4MHz) . Users can set PMCR And a system register prescaler register (CLKPR) Change the default configuration.

If the user needs to change the primary clock source configured, ensure that the clock before switching after switching the clock source in a stable operation state. It is necessary prior to switching the master clock source, by PMCR [3: 0] Enabling the desired clock source, and to wait until after a stable clock switching.

When the user switches to an external master clock oscillator, although the user is enabled external crystal, but does not rule configuration errors or due to failure of the crystal oscillator can not cause vibrating. If the switching to the external crystal at this point, the system will stop working after the handover. Therefore, in view of the reliability of the system, it is recommended to open the watchdog timer to prevent such problems from the perspective of software design.

After the clock is enabled and waiting for stabilization, by PMCR [6: 5] Switching the master clock. among them PMCR [5] Selects internal RC And an external crystal oscillator, PMCR [6] For selecting the low-speed and high-speed clock source clock source.



Master clock source selection:

PMCR [6]	PMCR [5]	Master clock source
0	0	internal 32MHz RC Oscillator (default)
0	1	external 400K ~ 32MHz Fast Crystal
1	0	internal 32KHz RC Oscillator
1	1	external 32K ~ 400KHz Low-speed oscillator

Timing Clock Source Control

To protect PMCR Register unexpected modification of PMCR Modifications of the register needs to be strictly specified installation sequence. PMCR MSB register (PMCR [7]) For implementing timing control. Users modify PMCR Before other bits, you must first of all to PMCR [7] Put 1 At home 1 After the operation 6 Within a period of change PMCR Other registers. 6 After a period of PMCR Direct modification will fail.

Below to switch to the external high frequency oscillator, for example, lists the suggested steps:

(1) Enable clock source

- Set up PMCR [7] = 1
- Within a period of six set PMCR [2] = 1 , An external high speed mode to enable the external oscillator
- Waiting for an external crystal oscillator is stable (wait time varies due to different crystal, general us Level can wait)

(2) Switching the primary clock source

- Set up PMCR [7] = 1
- Within a period of six set PMCR [6: 5] = 01 The system operates automatically switches to the external oscillator clock
- Performs several NOP Operation, to improve the stability (optional)

[NOTE]: In the above switching operation of the master clock, the system clock to ensure that the current normal operation, after switching to the external crystal, it can be closed before the interior RC Oscillator.

System Clock Prescaler

LGT8FX8P An internal system clock prescaler, the clock may be pre-divisor register (CLKPR) Control. This function can be used when the system does not require very high processing power, reducing the system power consumption. Prescaler setting is valid for the system clock source support. Clock Prescaler can affect the implementation of the core clock and the synchronization peripherals.

When switching between different clock prescaler is provided, the system clock prescaler ensure no burrs in the handover process, to ensure that it will not have a high frequency of the intermediate state. Division switching is executed immediately after the register is changed into effect, a maximum of 2-3 After a period of the current system clock, the system clock is switched to a new frequency-divided clock.

To avoid misuse of the clock divider register of CLKPR The modifications must also follow a special timing process:

- Set clock prescaler change enable bit (CLKPCE) for 1 , CLKPR So other bits 0
- Within four cycles, write the desired value CLKPS ,Simultaneously CLKPCE write 0

Before changing the clock frequency prescaler register, Need to disable interrupt function, in order to ensure a complete write timing can be.

Respect to the main clock prescaler register CLKPR The specific definition, please refer to the part of this section describes the register.

internal RC Oscillator calibration

LGT8FX8P It contains two internal calibration RC Oscillator, after calibration, can be reached ± 1% Less accuracy. among them 32MHz RC The default clock for the system to work.

LGT8FX8P Pre-production, internal 32MHz HFRC with 32KHz LFRC We are calibrated, and the calibration value writing system configuration information region. Power system during the calibration values will be read into the internal register, the register achieve RC Frequency of recalibration.

Calibration register is located IO Address space, the user program can read and write. For applications with special needs frequency, the output frequency can be adjusted by modifying the internal oscillator calibration register mode. To modify the calibration information register does not change the factory configuration, the system re-configuration or a user initiated power-bit reload operation, the calibration register will return to the factory settings.

Register Definition

32MHz HFRC Oscillator Calibration Register - RCMCAL

RCMCAL - 32MHz HFRC Calibration Registers		
RCMCAL: 0x66	Default: factory configuration	
Bits	RCCAL [7: 0]	
R / W	R / W	
Bit Definitions		
[7: 0]	RCCAL	After the power system, it will be the value of the register configuration information System RC Calibration values for change.

32KHz RC Oscillator Calibration Register - RCKCAL

RCKCAL - 32MHz RC Calibration Registers	
RCKCAL: 0x67	Default: factory settings
Bits	RCKCAL [7: 0]
R / W	R / W
Bit Definitions	
[7: 0]	RCKCAL The calibration values is written RCKCAL Register completed 32KHz RC Oscillator Calibration

Clock Source Register Management - PMCR

PMCR - Clock Source register management								
PMCR: 0xF2				Defaults: 0x03				
Bits	PMCE	CLKFS / CLKSS	WCLKS	OSCKEN	OSCMEN	RCKEN	RCMEN	
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	

Bit Definitions		
[0]	RCMEN internal	32MHz RC Oscillator Enable Control, 1 Enable, 0 Ban
[1]	RCKEN internal	32KHz RC Oscillator Enable Control, 1 Enable, 0 Ban
[2]	OSCMEN External	high frequency crystal oscillator enable control, 1 Enable, 0 Ban
[3]	OSCKEN External	enable control low frequency oscillator, 1 Enable, 0 Ban
[4]	WCLKS	WDT Clock source selection, 0 - Select the internal 32MHz HFRC Oscillator 16 Divide 1 - internal 32KHz LFRC Oscillator
[5]	CLKSS	Master clock source selection control to select the clock source type, the reference clock source selection portion
[6]	CLKFS	Master clock source frequency controlled clock frequency selection type, a reference clock source selection portion
[7]	PMCE	PMCR Change enable control register bits. Change PMCR Position before the other, this bit must first be set, and then set the value of the other bits in the four cycles.

Master clock prescaler register - CLKPR

CLKPR - Master clock prescaler register								
CLKPR: 0x61				Defaults: 0x03				
Bits	WCE	CKOEN1	CKOEN0	-	PS3	PS2	PS1	PS0
R / W	R / W	R / W	R / W	-	R / W	R / W	R / W	R / W

Bit Definitions						
[3: 0]	CLKPS	Clock select bit prescaler				
		PS3	PS2	PS1	PS0	Frequency division parameter
		0	0	0	0	1
		0	0	0	1	2
		0	0	1	0	4
		0	*0*	*1*	*1*	*8(default allocation)*

		0	1	0	0	16
		0	1	0	1	32
		0	1	1	0	64
		0	1	1	1	128
		1	0	0	0	256
		Other values				Retention
[4]	-	Are reserved				
[5]	CKOEN0 Set the system clock is in PB0 Pin output					
[6]	CKOEN1 Set the system clock is in PE5 Pin output					
[7]	WCE	Change clock prescaler clock changing control CLKPR Before the other bits of the register, you must first be provided separately CKWEN for 1 , Then in four cycles after the system, to set the other bits. After four cycles, CKWEN Automatically cleared.				

Power Management

Outline

Sleep mode by turning off the system clock and a clock module, so as to reduce system power consumption. LGT8FX8P Provides a very flexible controller module and a sleep mode, the user can use to achieve the best low-power configuration.

LGT8FX8P Upon entering the sleep mode, and does not automatically close analog functional modules, such as ADC , DAC ,Comparators (AC) , A low voltage reset module (LVD) And so on, depending on the application software to be required, before entering into sleep off unneeded analog functions, and to restore the correct state after a system wake-up.

LGT8FX8P It supports multiple sleep modes, including ADC A noise eliminating mode for eliminating ADC Part of the digital conversion process ADC Supply disturbances. In addition, other power control modes are divided into five categories:

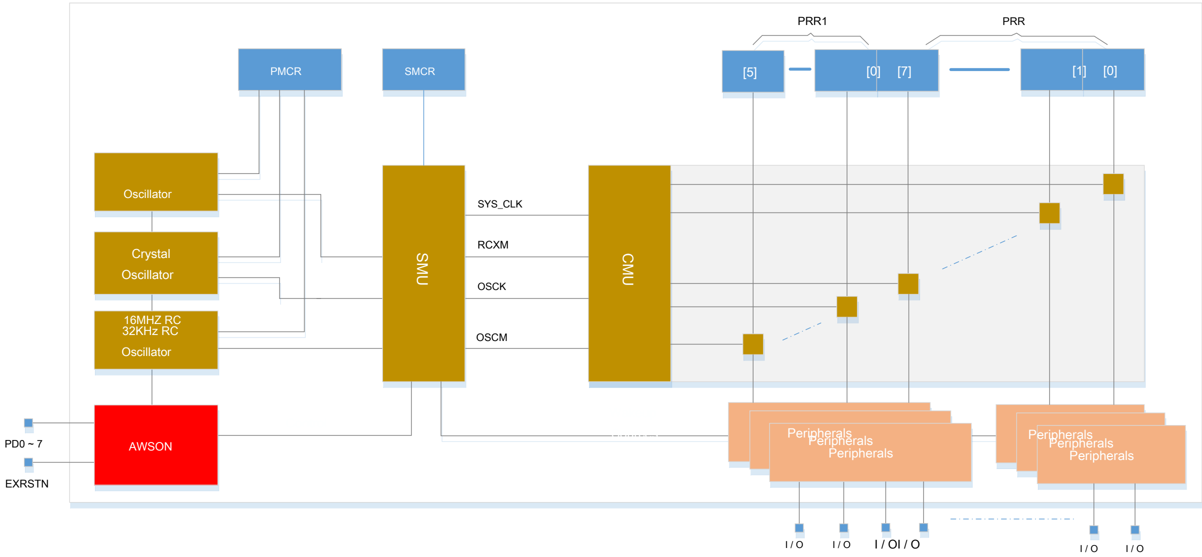
Sleep Mode	Function Description
Idle mode (IDLE)	Just close core clock, other peripheral modules work properly, all valid interrupt sources can be the kernel to wake up
Power-saving mode (Save)	versus DPS0 The same pattern, Save Mode and LGT8FX8D Compatibility
Power-down mode (DPS0)	versus Save The same model to support wakeup sources include: • All pin change • Watchdog Timer wake • Asynchronous mode TMR2 wake
Power-down mode (DPS1)	Close all the external oscillator, Supports wakeup sources include: • All external pin level change • External Interrupt 0/1 • Work on 32K LFRC Watchdog Timer
Power-down mode (DPS2)	Closed core power, Lowest power mode wakeup options supported include: • External reset • PORTD Pin Change • LPRC Timed wake-up (128ms / 256ms / 512ms / 1s) It should be noted, from DPS2 Wake-up process with the same power-on reset

LGT8FX8P Support Deep Sleep DPS2 In this mode, the internal LDO Is powered down, the kernel registers, and all peripheral controllers SRAM Etc. is powered down, Where the data will not be maintained. FLASH The storage unit will be in a powered down state, DPS2 System to achieve minimum power consumption mode. Power-down mode via port D (PORTD)
Pin change wake-up, you can choose 5 Level timing wake. For wake DPS2 Timers because it does not support the calibration accuracy 15% So, only suitable for the timed wake-up low accuracy applications.

System from DPS2 Wake-up, Will first open LDO This is the same process and power-on process. Perform a full chip power-on reset startup, loading configuration information, and the address of the reset vector from the program.

except DPS2 Than the other modes, the internal power supply will not, in the sleep process, all registers and information RAM Data will not be lost. After the wake, the kernel continues from the last instruction before sleep.

Power management system diagram:



As shown in FIG, LGT8FX8P Mainly through sleep-mode controller (SMU) And a clock management unit (CMU) Control power consumption of the entire system. From the power-saving level, we can put into power 4 Levels:

The first level is by PRR Operation clock control register module, the clock is not used to close the module, power-saving operation of the system dynamics. Under normal circumstances, this level can save power consumption is not obvious.

The second stage is the primary clock source by switching to the low frequency clock, and a clock source module is not closed, and other analog modules used, this mode can be substantially obtained very substantial operating power consumption of the system and sleep power consumption.

The third level is to enter into power-down mode by the system (DPS1) , DPS1 Mode LGT8FX8P Polar standby power consumption can be obtained from the power down mode wake-up, the software can MCUSR Reading the status register before reset.

The fourth level is a power-down mode (DPS2) This kernel mode turns off the power, can achieve the lowest system power consumption. Due to the closure of the core power, All data will be lost in this mode. Immediately perform a power-on reset process after wake-up, the system starts running again from the reset vector.

AWSON Power Management

versus LGT8FX8D Compared to power-down mode DPS2 A new power mode. DPS2 Mode used for applications with higher power requirements of dormancy. enter DPS2 After, the system only maintains a static module (AWSON) In working condition, other circuits are in full power-down state.

AWSON Module is dedicated to the responsible DPS2 Sleep and wake-up control mode, AWSON Modules mainly by IO Wake-up control logic, and a low power consumption LPRC composition. Software can IOCWK Register and DPS2R Register to achieve AWSON control.

IOCWK Register controls PD0 ~ 7 Level change wake-up function. DPS2R Register controls DPS2 Mode and LPRC Function mode. Please refer to the end of this particular section Register Definition section.

use DPS2 Former mode, software settings IOCWK Enable needed wakeup IO Or by DPS2R Register enables LPRC And configure the timed wake-up period, and then by DPS2R Register DPS2EN Enable bit DPS2 mode. After the setup is complete, the software required by SMCR Register Set DPS2 Sleep mode, then execute SLEEP Command goes to sleep.

Sleep mode and wake-up source

LGT8FX8P stand by 5 Species sleep mode, the user can select the appropriate sleep mode according to application requirements. SMCR Register contains control set the sleep mode is performed SLEEP After instructions, the core enters sleep mode. In order to obtain a more ideal sleep power consumption, the kernel is recommended before entering Sleep mode, turn off all clocks and analog modules are not used. But note that the wake-up source to generate some of the need to work the clock, if you need to use this type of wake-up source, keep working condition-related clock source.

Sleep mode and wake-up:

Sleep Mode	Effective Clock				Wake-up source							
	Core clock	The peripheral clock	ADC	Asynchronous Clock	Pin Change	External Interrupt 0/1	TWI Address Matching	TMR2 Interrupt	End of Conversion ADC PD	Watchdog overflow	Peripheral Interrupt	Level change
Idle mode (IDLE)		X	X	X	X	X	X	X	X	X	X	X
ADC Noise suppression			X	X	X	X	X	X	X	X		X
Power-saving mode (SAVE)				X	X	X	X	X		X		X
Power-down mode (DPS0) (With RC32K)				X	X	X		X		X		X
Power-down mode (DPS1) (Without RC32K)				X	X	X		X				X
Power-down mode (DPS2) (Without LDO)												X

If you need to enter more than 5 Kind of sleep mode, SMCR middle SE Bit must be set 1 , To enable a sleep mode control. And then executing a SLEEP Command can be. SMCR middle SM0 / 1/2 For selecting various sleep modes. Specific information, refer to the following description.

in MCU The next is in sleep mode, if the wake-up source is active, MCU Will be 4 After wake cycles, we continue to execute instructions. If the interruption remains active, the interrupt will also respond immediately, the interrupt service routine. If the SLEEP Mode system reset has occurred, MCU Also it will wake up and start the reset vector.

when MCU In Power / Off Mode, the system can be interrupted by external INT0 / 1 Wake up, wake up after MCU From sleep Position before continuing execution.

Idle mode (IDLE)

when SM2 ... 0 Set as 000 ,carried out SLEEP Instruction, MCU Enter IDLE mode, IDLE Kernel mode will shut off the clock work, in addition to the other peripherals are working properly.

IDLE Mode via external interrupt and internal interrupts wake. If you do not use comparator, and ADC As a wakeup source, it is recommended to turn it off.

IDLE Close kernel mode because only the clock running, it does not significantly reduce power consumption. IDLE Mode, the kernel will stop execution and instruction fetch, the program can be reduced internal FLASH The operating power consumption.

but IDLE Wake-up mode has a relatively flexible manner, the user can acquire a more desirable system operation by reducing the power consumption of the master clock, and turning off unneeded modules.

ADC Noise Reduction

when SM2 ... 0 Set as 001 ,carried out SLEEP Instruction, MCU enter ADC Noise suppression mode. In this mode, the kernel and most of the peripherals will stop working, ADC ,External Interrupt, TWI Address match, WDT And operating in asynchronous clock mode, timer / counter 2 They can work properly.

ADC Noise has been mainly used as a model ADC Transformation provides a good working environment. Reduce high frequency interference digital to analog conversion module. After entering this mode, ADC Save automatically starts sampling conversion, the converted data to ADC After the data register, ADC End of Conversion interrupt MCU From ADC Wake-up mode noise.

Power-saving mode (Save)

when SM2 ... 0 Set as 010 ,carried out SLEEP Instruction, MCU Enter Save mode. In this mode, the system will shut off all the work of the clock module. This mode due to the closure of all the work the clock module, it can only be awakened by an asynchronous mode, external interrupts, TWI Address matching and operate at independent clock source mode WDT Wake-up signal can be generated in this mode.

This model can turn off all modules except that of the master clock source. To achieve more desirable operating power consumption, it is recommended herein before entering mode, the system will be switched to the internal clock master 32K RC Or external 32KHz Low frequency oscillator, then it is not used to close off the source clock and an analog module.

Power-down mode DPS0

when SM [2: 0] Set as 110 ,carried out SLEEP Instruction, MCU Will enter into DPS0 mode. enter DPS0 After, in addition to internal 32KHz RC , The other clock sources are closed. This mode can be interrupted by external INT0 / 1 Wake up; if enabled WDT Interrupt function, can also WDT Achieve timing wake.

Power-down mode DPS1

when SM [2: 0] Set as 011 ,carried out SLEEP Instruction, MCU Will enter into DPS1 mode. enter DPS1 After all clock sources are closed systems. This model can be used IO Level change, the watchdog wake.

Power-down mode DPS2

Set up SM [2: 0] for 111 And by DPSR2 Register DPS2EN Enable AWSON Module, execution SLEEP After entering the command DPS2 mode. enter DPS2 After the mode, the system power off the core. So register and RAM Data will be lost. From DSP2 Wake-up process with the same power-on reset process.

DPS2 Mode, Since the closed core voltage, the register information is lost, so the control status of the ports will all return to the input state, all IO The output drive and pull-up control will be closed.

FLASH Power control and fast wake-up

When the system is SLEEP After mode, the kernel will not continue executing instructions, then you can choose to close FLASH Power, in order to obtain lower power consumption standby. This function can be MCUCR Register FPDEN Position control is realized;

In power-down mode, The system can use external interrupt or WDT Wake-up, in order to filter out possible interference of the external signal, an internal wake-up circuit comprises a filter circuit can be configured, the user can select the appropriate filter width according to the needs. Filter circuit can be arranged MCUCR Register FWKPEN achieve.

MCUCR [FWKPEN] Filter width control:

FWKPEN	Filter Width
0	260us (default)
1	32us

Register Description

Sleep Mode Control Register - SMCR

SMCR - Sleep Mode Control Register								
SMCR: 0x33 (0x53)				Defaults: 0x00				
Bits				SM2	SM1	SM0	SE	
R / W	-			R / W	R / W	R / W	R / W	
Bit Definitions								
[0]	SE	Sleep mode enable control bit, is set to 1 After execution SLEEP Instructions, the core will enter the sleep mode. SE Bit can protect the system into sleep mode unexpectedly. After the wake, it is recommended immediately clear SE Bit.						
[3: 1]	SM	Sleep Mode Select						
		SM2	SM1	SM0 Mode	Description			
		0	0	0	IDLE mode			
		0	0	1	ADC Noise Reduction			
		0	1	0	Save mode			
		0	1	1	DPS1 mode			
		1	1	0	DPS0 mode			
		1	1	1	DPS2 mode			
		Others			Are reserved			
[7: 4]	-	Are reserved						

Saving Control Register - PRR

PRR - Power control register								
PRR: 0x64					Defaults: 0x00			
PRR	PRTWI	PRTIM2	PRTIM0	-	PRTIM1	PRSPI	PRUART0	PRADC
R / W	R / W	R / W	R / W	-	R / W	R / W	R / W	R / W
Bit Definitions								
[0]	PRADC	Set as 1 ,shut down ADC Controller Clock						
[1]	PRUART0	Set as 1 ,shut down USART0 The clock module						
[2]	PRSPI	Set as 1 ,shut down SPI The clock module						
[3]	PRTIM1	Set as 1 Disables the timer / counter 1 Clock						
-	-	Are reserved						
[5]	PRTIM0	Set as 1 Disables the timer / counter 0 Clock						
[6]	PRTIM2	Set as 1 Disables the timer / counter 2 Clock						
[7]	PRTWI	Set as 1 ,shut down TWI The clock module						

Saving Control Register - PRR1

PRR1 - Power control register 1								
PRR1: 0x65				Defaults: 0x00				
PRR1			PRWDT	-	PRTIM3	PREFL	PRPCI	-
R / W			R / W	-	R / W	R / W	R / W	-

Bit Definitions		
[0]	-	Are reserved
[1]	PRPCI	Set as 1 , Off the external pin interrupt module and the external clock change
[2]	PREFL	Set as 1 ,shut down FLASH Clock Interface Controller
[3]	PRTIM3	Set as 1 ,shut down TMR3 Clock controller
[4]	-	Are reserved
[5]	PRWDT	Set as 1 ,shut down WDT Counter Clock
[7: 6]	-	Are reserved

MCU Control Register - MCUCR

MCUCR - MCU Control register								
MCUCR: 0x35 (0x55)				Defaults: 0x00				
MCUCR	FWKEN	FPDEN EXRFD		PUD	IRLD	IFAIL	IVSEL	WCE
R / W	R / W	R / W	R / W	R / WW / O		R / O	R / W	R / W

Bit Definitions		
[0]	WCE	MCUCR Update Enable bit, update MCUCR Before, you first need to set this bit, and then 6 Completed within a period MCUCR Update registers
[1]	IVSEL	Interrupt Vector Select bit, this location 1 After the interrupt vector address will be based IVBASE Mapped to the new value of the register address
[2]	IFAIL	The system failed to load configuration bits flag, 0 = By checking the configuration information 1 = Failed to load configuration information
[3]	IRLD	write 1 The reload the system configuration information
[4]	PUD	Pull on the global disable bit 0 = Pull-up control to enable global 1 = Close all IO The pull-up resistor
[5]	EXRFD	External reset filtering disable bit 0 = Enable External reset (190us) The digital filter 1 = Disable external reset of the digital filter circuit
[6]	FPDEN	Flash Power / down Enable Control 0 :system SLEEP Rear FLASH Remain powered 1 :system SLEEP Rear FLASH Power outage
[7]	FWKEN	Fast wake-up mode enable control, only Power / Off Mode is active 0 : 260us Filter delay 1 : 32us Filter delay

PD Group level change wakeup control register - IOCWK

IOCWK - PD Group level change wakeup control register								
IOCWK: 0xAE					Defaults: 0x00			
Bits	IOCD7	IOCD6	IOCD5	IOCD4	IOCD3	IOCD2	IOCD1	IOCD0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	IOCWK	Put 1 Corresponding bit, enabling PD group IO The pin change wake-up function						

DPS2 Mode Control Register - DPS2R

DPS2R - DPS2 Mode control register								
DPS2R: 0xAF					Defaults: 0x00			
Bits	-	-	-	-	DPS2E	LPRCE	TOS1	TOS0
R / W	-	-	-	-	R / W	R / W	R / W	R / W
Bit Definitions								
[1: 0]	TOS	LPRC Timed wake-up settings: 00 = 128ms 01 = 256ms 10 = 512ms 11 = 1s						
[2]	LPRCE	LPRC Enable Control 0 = Disable LPRC Timer 1 = Enable LPRC Timer						
[3]	DPS2E	DPS2 Mode enable control bit 0 = Disable DPS2 mode 1 = Enable DPS2 mode						
[7: 4]	-	Retention						

System reset control

Outline

After a reset, all I / O Register will be set to their initial values, the program begins at the reset vector. LGT8FX8P The interrupt vector address, you must use a RJMP - Relative jump instruction to jump to the reset handler. If the program is useless to use interrupt is not enabled interrupt source, interrupt vector will not be used, the interrupt vector area can be used to store the user's program code.

After the reset is effected, all I / O Port immediately into their initial state. most I / O Initialization state is entered and close off the internal pullup. Analog input function I / O Also initialized to digital I / O Features.

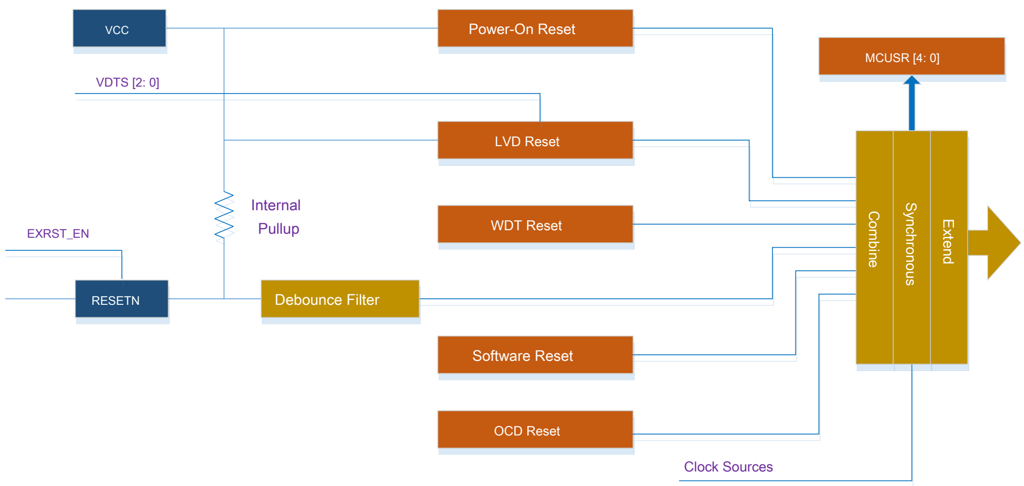
When the reset becomes inactive, LGT8FX8P Internal timer counter started for broadening reset. Broadening the width of the reset signal used to ensure the system power supply and clock modules into a stable state.

Reset sources

LGT8FX8P Total supports six sources of reset:

- POR: internal low pressure system when the operating voltage POR Module reset threshold, the reset valid.
- External reset: low pulse on the external reset pin of the chip constant width, the external reset is asserted.
- Reset Watchdog: Watchdog module after, if the watchdog timer expires, the system will reset.
- Low voltage reset: LGT8FX8P It has an internal low-voltage detection module (LVD) , When the system power is below LVD Setting the reset threshold, MCU It will also be reset.
- Software Reset: LGT8FX8P Internal reset register trigger a dedicated software, the user can be reset at any time by the register MCU .
- OCD Reset: OCD Reset is issued debugger module for direct reset MCU Kernel.

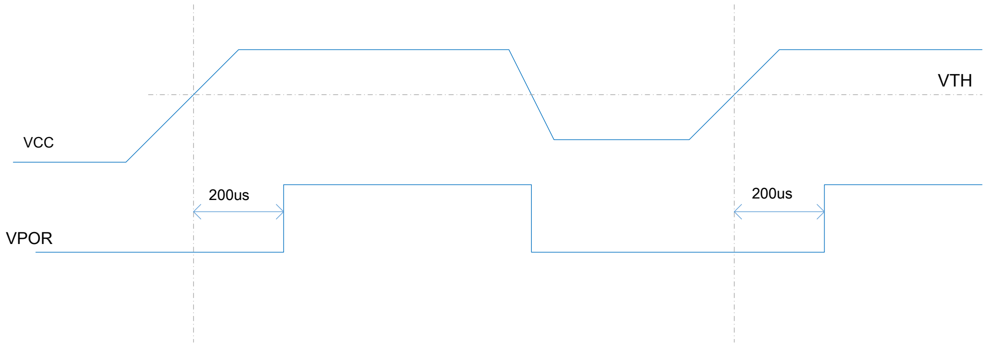
Reset System structure:



Power-On Reset

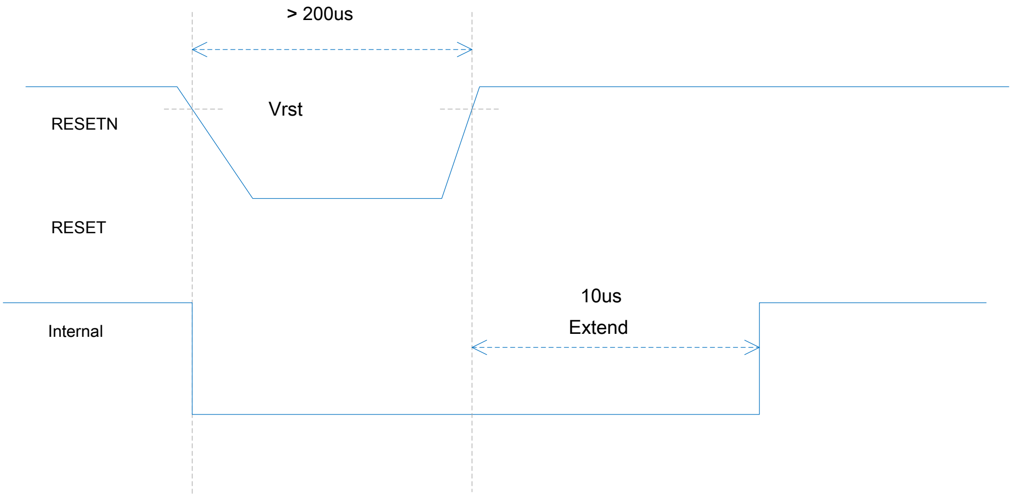
Power-on reset signal is generated internally by the voltage detection circuit. When the system power supply (VCC) Below detection threshold, the power-on reset signal is active. Power-on reset detection threshold, refer to the portion of electrical parameters.

On reset circuitry to ensure that the chip in the reset state during power-on, can be run from a known stable state After power. Power-on reset signal inside the chip will be broad exhibition counter, to ensure that after power inside the various analog blocks, such as RC Oscillator to enter the steady-state operation.



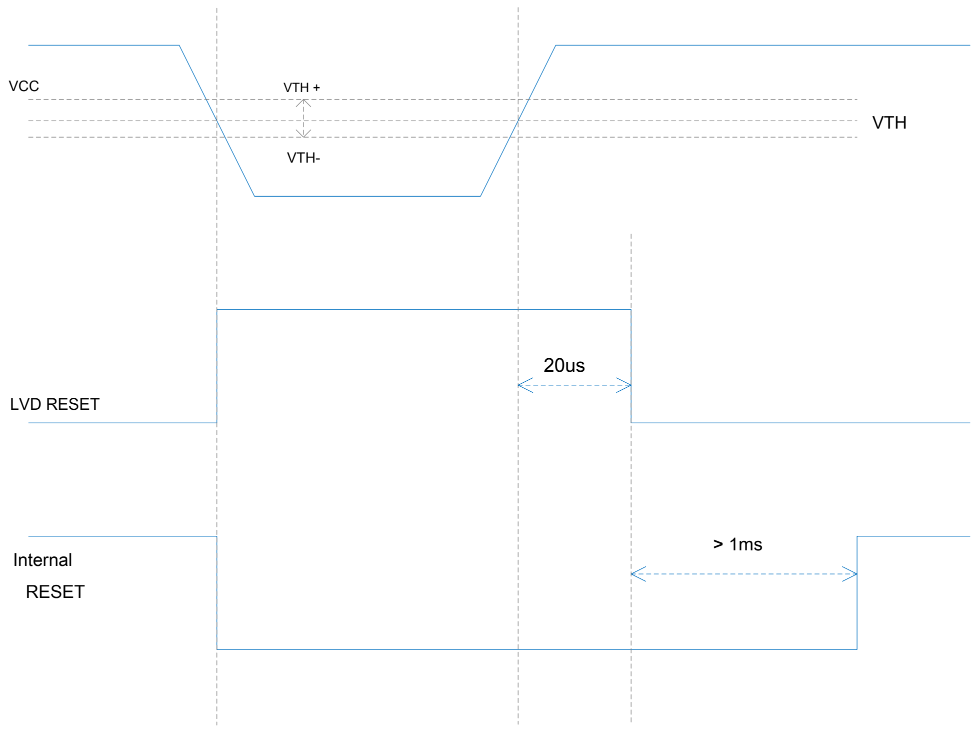
External reset

In the external reset pin (RSTN) Applying a low level on the external reset immediately effective. Greater than a width of the low minimum reset pulse width requirement. External reset is asynchronous reset, even if there is no clock chip, external reset will still be able to reset the chip. LGT8FX8P The external reset pin also can be used as general-purpose I / O use. After the chip is powered on, The default as an external reset function. Users can register configuration, external reset function off the pin, so that can be used as an ordinary I / O use. Please refer to the specific use IOCR Description section of the register.



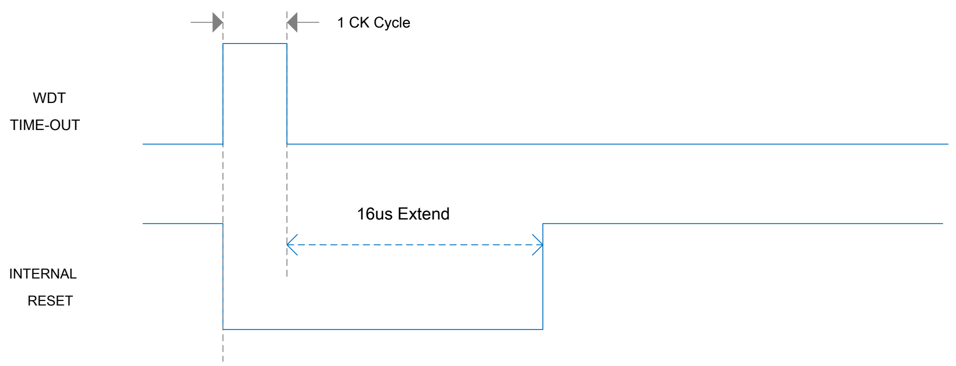
Low-voltage detection (LVD) Reset

LGT8FX8P Internal comprises a programmable low voltage detector (LVD) Circuit. LVD The same is detected VCC Voltage variation, but different from the power reset is LVD Voltage threshold detector may be selected. The user can directly operate VDTCR Register selection between different voltage threshold. LVD A voltage detection circuit having ± 10mV ~ ± 50mV Hysteresis characteristics for filtering VCC Jitter voltage. when LVD When enabled, if VCC The reset voltage drops to the set threshold, LVD Reset effective immediately. when VCC After reset is increased above the threshold, resetting the internal circuit starts to expand, will continue to stretch at least a reset 1 millisecond.



Watchdog reset

When the watchdog timer overflows, if the Watchdog system reset function, the system will generate a reset signal period immediately. General watchdog reset signal will be inside the wide delay counter exhibition. The detailed operation of the watchdog controller, see Details of the test section below.



Software reset, OCD Reset

Software reset is by operation of the user VDTCR Sixth register trigger, a software reset and watchdog reset timing is completely similar. The internal reset signal broadening 16us .

OCD Reset unit generated by the internal chip debugger, OCD Reset is normally controlled by the debugger, the user can not trigger software OCD Reset.

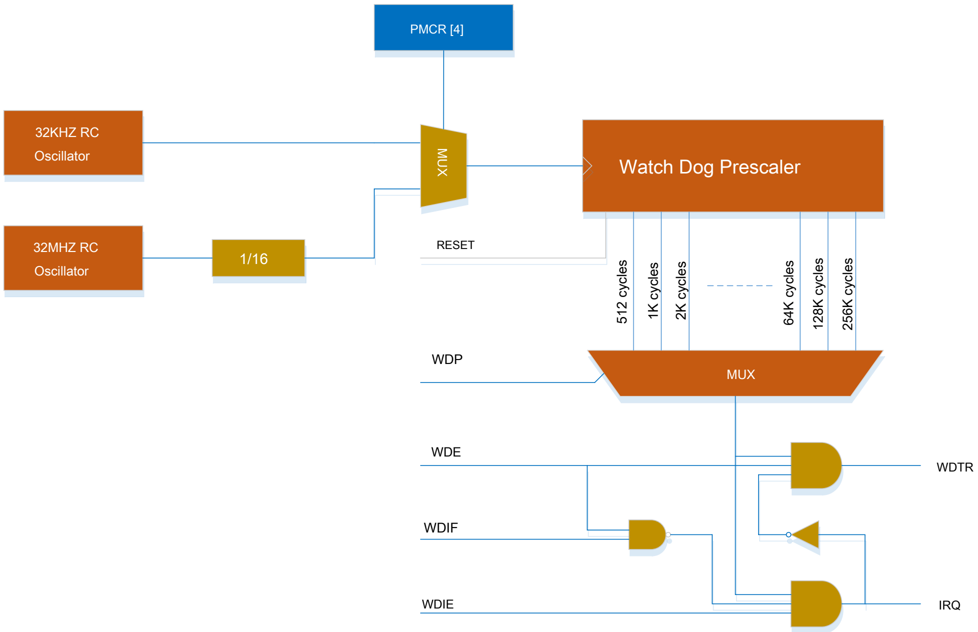
Watchdog Timer

- Optional internal clock 32KHz RC Or internal 32MHz RC of 16 Divider (2MHz)
- Supports interrupt mode, reset mode and reset interrupt mode
- Timer expires maximum to 8 second

LGT8FX8P Interior contains an enhanced watchdog timer (WDT) Module. WDT Timer operation clock can be internal 32KHz RC Oscillator, or internal 32MHz RC Oscillator 16 Divider. WDT After the counter overflows, an interrupt may be output or a system reset signal. In normal use, the software needed to perform a

WDR - Watchdog Timer Reset instruction restart until the counter overflows. If the system does not even execution WDR instruction, WDT It will generate an interrupt or system reset.

A configuration diagram of the watchdog timer as shown below:



In interrupt mode, WDT Generates an interrupt request signal overflow. You can use this as a wake-up signal interrupt sleep mode, it can be used as a general system timer uses. For example, you can use this interrupt an operation execution time limit, terminate one of the tasks in the current overflow. In the reset mode, WDT Generating a system reset signal immediately after the counter overflows. The most typical use is to prevent system crashes or running out. The third mode is reset interrupt mode, interrupt and reset combines two functions. First, the system will respond WDT

Interrupt function exits WDT After the interrupt routine, and immediately switched to reset mode. This feature can save support some of the more critical parameter information before reset.

to prevent WDT Was accidentally disabled, shut down WDT The operation must be carried out in accordance with the timing of a strictly defined. The following code describes how to disable the watchdog timer. The following example assumes that interrupt has been disabled, so that the entire operation process will not be interrupted.

Enable watchdog and closing operation example code:

Assembly code

```
WDT_OFF:
    ; Turn off global interrupt
    CLI
    ; Reset watchdog timer
    WDR
    ; Clear WDRF in MCUSR
    IN r16, MCUSR
    ANDI r16, ~ (1 << WDRF)
    OUT MCUSR, r16
    ; Write logical one to WDCE and WDE
    ; Keep old Prescaler setting to prevent unintentional time-out
    LDS r16, WDTCSR
    ORI r16, (1 << WDCE) | (1 << WDE)
    STS WDTCSR, r16
    ; Turn off WDT
    LDI r16, (0 << WDE)
    STS WDTCSR, r16
    ; Turn on global interrupt
    SEI
    RET
```

C Language code

```
void WDT_OFF (void) {

    __disable_interrupt ();
    __watchdog_reset ();
    / * Clear WDRF in MCUSR * /
    MCUSR & = ~ (1 << WDRF);
    / * Write logical one to WDCE and WDE * /
    / * Keep old Prescaler setting to prevent unintentional time-out * /
    WDTCSR | = (1 << WDCE) | (1 << WDE);
    / * Turn off WDT * /
    WDTCSR = 0x00;
  __enable_interrupt ();}
```

[Use suggestions]

in case WDT Was accidentally enabled, such as program running, the chip will be reset, but WDT In still enabled. If the user code does not address WDT This will result in a reset cycle. To avoid this situation, the user software clears the watchdog reset flag in the initialization process (WDRF) with WDE Control bit.

The following code describes how to change the value of the watchdog timer timeout.

Assembly code

```
WDT_TOV_Change:
    ; Turn off global interrupt
    CLI
    ; Reset watchdog timer
    WDR
    ; Start timed sequence
    LDS r16, WDTCSR
    ORI r16, (1 << WDCE) | (1 << WDE)
    STS WDTCSR, r16
    ; - Got for cycles to set the new value from here -; Set new
    time-out value = 64k cycles
    LDI r16, (1 << WDE) | (1 << WDP2) | (1 << WDP0)
    STS WDTCSR, r16
    ; - Finished setting new value, used 2 cycles; Turn on
    global interrupt
    SEI
    RET
```

C Language code

```
void WDT_TOV_Change (void) {

    __disable_interrupt ();
    __watchdog_reset ();
    / * Start timed sequence * /
    WDTCSR | = (1 << WDCE) | (1 << WDE);
    / * Set new time-out value = 64K cycles * /
    WDTCSR | = (1 << WDE) | (1 << WDP2) | (1 << WDP0);
  __enable_interrupt ();}
```

【Instructions for use】

Change WDP Before configuration bits, it is recommended to reset the watchdog timer. Because changes WDP Bit to relatively small time-out period is likely to cause the watchdog timeout reset.

Register Definition

Low voltage detection (LVD) Control Register - VDTCR

VDTCR - LVD Control register								
VDTCR: 0x62				Defaults: 0x00				
Bits	WCE	SWR	- VDTS2		VDTS1	VDTS0 VDREN VDTEN		
R / W	R / WW / R		- R / W		R / W	R / W	R / W	R / W
Bit Definitions								

[0]	VDTEN	Low-pressure detecting module enable control, 1 Enable, 0 Ban
[1]	VDREN Low voltage reset enable control function, 1 Enable, 0 Ban	
[4: 2]	VDTS	Low voltage detection threshold configuration bits 000 = 1.8V 001 = 2.2V 010 = 2.5V 011 = 2.9V 100 = 3.2V 101 = 3.6V 110 = 4.0V 111 = 4.4V
[5]	-	Are reserved
[6]	SWR	Soft Reset Enable bit, this bit is cleared to generate a software reset
[7]	WCE	VDTCR Enable users to change the value of the change in VDTCR Before the value of the register, you must first write this bit 1 , After the 6 Clock cycles, change VDTCR The value of the other bits. After four cycles WCE Automatically cleared of VDTCR Register update operation is invalid.

IO Register Function Multiplexing - PMX2

PMX2 - IO Register Function Multiplexing								
PMX2: 0xF0				Defaults: 0x00				
Bits	WCE	STSC1	STSC0	-	-	XIEN	E6EN	C6EN
R / W	R / W	R / W	R / W	-	- R / W		R / W	R / W
Bit Definitions								

0	C6EN	PC6 Pins default reset, this bit is set 1 External reset function is disabled, the reset function is disabled, PC6 It can be used as an ordinary I / O use
1	E6EN	PE6 The default function as an analog input pin, setting this bit 1 , Closes the analog input, this pin can be used as GPIO use
2	XIEN	External clock input enable control
4: 3	-	Are reserved
5	STSC0	Low-speed oscillator start control
6	STSC1	High-speed crystal startup control
7	WCE	IOCR Enable users to change the value of the change in IOCR Before the value of the register, you must first write this bit 1 ,in

		After 6 Clock cycles, change IOCR The value of the other bits. After four cycles WCE Automatically cleared of IOCR Register update operation is invalid.

MCU Status Register - MCUSR

MCUSR - IO Special Function Registers Control								
MCUSR: 0x34 (0x54)				Defaults: 0x00				
Bits	SWDD	-	PDRF	OCDRF	WDRF	BORF	EXTRF	PORF
R / W	R / W	-	R / W	R / W	R / W	R / W	R / W	R / W

Bit Definitions		
[0]	PORF	Power-on reset flag, write 0 Clear
[1]	EXTRF	External reset flag, power-on reset automatically cleared, or write 0 Clear
[2]	BORF	Detection reset, power-on reset automatically cleared, or write 0 Clear
[3]	WDRF	Watchdog reset flag, power-on reset automatically cleared, or write 0 Clear
[4]	OCDRF	OCD Debugger reset flag, power-on reset automatically cleared, or write 0 Clear
[5]	PDRF	From Power / off Wake-up signs, detailed description please refer to the power management section.
[6]	-	Are reserved
[7]	SWDD	SWD Interface disable bit. write 1 Will be closed SWD interface. SWD After the interface is down, and will not be able to debug ISP operating. If the user program closed SWD Interface, power down process by RESET Way as to prohibit the operation of internal procedures, and then debug ISP operating. SWD After closing the interface, SWD Occupied by two I / O Interface can be used as general-purpose I / O use. To avoid SWDD Misuse, users need to first update in SWDD Within four cycles after a write bit SWDD To take effect.

[Use suggestions]:

To be more accurate and effective use of the reset flag information, it is recommended that users try to read the pre-reset flag in the initialization process and then cleared.

Watchdog Control Status Register - WDTCSR

WDTCSR - WDT Control and status registers								
address: 0x60					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	WDIF	WDIE	WDP3	WDTOE	WDE	WDP2	WDP1	WDP0
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
[7]	WDIF	WDT Interrupt flag. when WDT Work in the interrupt mode and an overflow occurs will set WDIF Bit. when WDT Interrupt enable bit WDIE for "1" And the Global Interrupt When set, WDT An interrupt is generated. carried out WDT Will be cleared when the interrupt WDIF Bit of WDIF Write bit "1" Also clears the bit.
[6]	WDIE	WDT Interrupt enable control bit. When set WDIE Bit "1" When, and Global Interrupt set, WDT Interrupt is enabled.

		When set WDIE Bit "0" Time, WDT Interrupts are disabled. WDIE Bit and WDE Together determine the watchdog-bit mode, as shown in the following table.

WDE	WDIE	mode	After the action overflow
0	0	stop	no
0	1	Interrupt Mode	Interrupt
1	0	Reset mode	Reset
1	1	Reset interrupt Reset Mode	Interrupt

[5]	WDP3	WDT Prescale factor selection control section 3 Bit. WDP [3] with WDP [2: 0] composition WDT Select bit prescale factor WDP [3: 0] , To set WDT The time-out period.
[4]	WDTOE	WDT Close enable control bit. When should WDE When cleared, WDTOE Bit to be set, otherwise WDT It will not be closed. when WDTOE After the bit is set, hardware will 4 After four clock cycles cleared WDTOE Bit.
[3]	WDE	WDT Enable control bit. When set WDE Bit "1" Time, WDT It is enabled. When set WDE Bit "0" Time, WDT Prohibited. only at WDTOE When the bit WDE In order to be cleared. To turn has enabled the WDT , Must operate in accordance with the following sequence: 1. At the same time set WDTOE with WDE Bit, even if WDE It has been set in the closed Before beginning operation also must WDE Bit is written "1" ; 2. In the following 4 Clock cycles, for WDE Bit is written "0" . This turns off WDT . when WDE Bit "1" And WDT Overflow bit is set and reset WDT Reset system flag WDRF (lie in MCUSR register). when WDRF Will be set when the bit in the set state WDE Bit. So to be cleared WDE Bit must be cleared WDRF Bit.
[2: 0]	WDP	WDT Prescale factor selection control. To set WDT The time-out period. Recommended WDT When the count is not changed WDP Values change during the counting WDP The value will produce unpredictable WDT overflow.

Watchdog prescaler selection list:

WDP3	WDP2	WDP1	WDP0	Watchdog timer overflow number of cycles	32KHz clock	2MHz clock
0	0	0	0	2K cycles	64ms	1ms
0	0	0	1	4K cycles	128ms	2ms
0	0	1	0	8K cycles	256ms	4ms
0	0	1	1	16K cycles	512ms	8ms
0	1	0	0	32K cycles	1s	16ms
0	1	0	1	64K cycles	2s	32ms
0	1	1	0	128K cycles	4s	64ms
0	1	1	1	256K cycles	8s	128ms
1	0	0	0	512K cycles	16s	256ms
1	0	0	1	1024K cycles	32s	512ms

1	0	1	0	Are reserved
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Interrupts and Interrupt Vector

- 28 Interrupt sources
- Programmable starting address vector

LGT8F88P / 168P / 328P The interruption is basically the same resources, the main difference is: LGT8F88P The interrupt vector is 1 Instruction Word (16 Bit), and LGT8F168P / 328P The interrupt vector is 2 Instructions.

LGT8F88P Interrupt vector list

LGT8F88P Interrupt vector list:

Numbering	Vector address	Interrupt source signals	Interrupt Source Description
1	0x0000	RESET	External reset, power-on reset, a watchdog reset, SWD Debug reset, low voltage reset
2	0x0001	INT0	External Interrupt Request 0
3	0x0002	INT1	External Interrupt Request 1
4	0x0003	PCI0	Interrupt pin level 0
5	0x0004	PCI1	Interrupt pin level 1
6	0x0005	PCI2	Interrupt pin level 2
7	0x0006	WDT	Watchdog overflow interrupt
8	0x0007	TC2 COMPA	Timer 2 Compare match A Interrupt
9	0x0008	TC2 COMPB	Timer 2 Compare match B Interrupt
10	0x0009	TC2 OVF	Timer 2 Overflow
11	0x000A	TC1 CAPT	Timer 1 Input Capture interrupt
12	0x000B	TC1 COMPA	Timer 1 Compare match A Interrupt
13	0x000C	TC1 COMPB	Timer 1 Compare match B Interrupt
14	0x000D	TC1 OVF	Timer 1 Overflow
15	0x000E	TC0 COMPA	Timer 0 Compare match A Interrupt
16	0x000F	TC0 COMPB	Timer 0 Compare match B Interrupt
17	0x0010	TC0 OVF	Timer 0 Overflow
18	0x0011	SPI STC	SPI Serial transfer end interrupt
19	0x0012	USART RXC	USART RX Complete
20	0x0013	USART UDRE	USART Data Register Empty
twenty one	0x0014	USART TXC	USART End of Transmit Interrupt
twenty two	0x0015	ADC	ADC Conversion end interrupt
twenty three	0x0016	EE_RDY	EEPROM Ready interrupt
twenty four	0x0017	ANA_COMP	Analog comparator 0 Interrupt
25	0x0018	TWI	Two-wire serial interface interrupt
26	0x0019	ANA_COMP1	Analog comparator 1 Interrupt
27	0x001A	-	Retention
28	0x001B	PCI3	Interrupt pin level 3
29	0x001C	PCI4	Interrupt pin level 4
30	0x001D	TC3_INT	Timer 3 Interrupt

LGT8F168P / 328P Interrupt vector list

LGT8F168P / 328P Interrupt vector list:

Numbering	Vector address	Interrupt source signals	Interrupt Source Description
1	0x0000	RESET	External reset, power-on reset, a watchdog reset, SWD Debug reset, low voltage reset
2	0x0002	INT0	External Interrupt Request 0
3	0x0004	INT1	External Interrupt Request 1
4	0x0006	PCI0	Interrupt pin level 0
5	0x0008	PCI1	Interrupt pin level 1
6	0x000A	PCI2	Interrupt pin level 2
7	0x000C	WDT	Watchdog overflow interrupt
8	0x000E	TC2 COMPA	Timer 2 Compare match A Interrupt
9	0x0010	TC2 COMPB	Timer 2 Compare match B Interrupt
10	0x0012	TC2 OVF	Timer 2 Overflow
11	0x0014	TC1 CAPT	Timer 1 Input Capture interrupt
12	0x0016	TC1 COMPA	Timer 1 Compare match A Interrupt
13	0x0018	TC1 COMPB	Timer 1 Compare match B Interrupt
14	0x001A	TC1 OVF	Timer 1 Overflow
15	0x001C	TC0 COMPA	Timer 0 Compare match A Interrupt
16	0x001E	TC0 COMPB	Timer 0 Compare match B Interrupt
17	0x0020	TC0 OVF	Timer 0 Overflow
18	0x0022	SPI STC	SPI Serial transfer end interrupt
19	0x0024	USART RXC	USART RX Complete
20	0x0026	USART UDRE	USART Data Register Empty
twenty one	0x0028	USART TXC	USART End of Transmit Interrupt
twenty two	0x002A	ADC	ADC Conversion end interrupt
twenty three	0x002C	EE_RDY	EEPROM Ready interrupt
twenty four	0x002E	ANA_COMP	Analog Comparator Interrupt
25	0x0030	TWI	Two-wire serial interface interrupt
26	0x0032	ANA_COMP1	Analog comparator 1 Interrupt
27	0x0034	-	Retention
28	0x0036	PCI3	Interrupt pin level 3
29	0x0038	PCI4	Interrupt pin level 4
30	0x003A	TC3_INT	Timer 3 Interrupt

LGT8FX8P The reset vector address from 0x0000 Begin execution. In addition to the reset vector, the other by the vector address can be MCUCR Register IVSEL as well as IVBASE Register redirected to 512 Byte-aligned start address.

Interrupt vector processing

The following code is only LGT8F88P For example, reset and interrupt vectors for explaining the programming, for reference only:

Examples of assembly code - LGT8F88P		
address	Code	Explanation
0x000	RJMP RESET RJMP	Reset Vector
0x001	EXT_INT0 RJMP	External Interrupt 0
0x002	EXT_INT1 RJMP PCINT0	External Interrupt 1
0x003	RJMP PCINT1 RJMP	Pin Change Interrupt 0
0x004	PCINT2 RJMP WDT RJMP	Pin Change Interrupt 1
0x005	TIM2_COMPA RJMP	Pin Change Interrupt 2
0x006	TIM2_COMPB RJMP	Watchdog timer interrupt timer 2 Compare
0x007	TIM2_OVF RJMP	match A Group interrupt timer 2 Compare match
0x008	TIM1_CAPT RJMP	B Group interrupt timer 2 Overflow interrupt
0x009	TIM1_COMPA RJMP	timer 1 Capture interrupt timer 1 Compare
0x00A	TIM1_COMPB RJMP	match A Group interrupt timer 1 Compare match
0x00B	TIM1_OVFR RJMP	B Group interrupt timer 1 Overflow interrupt
0x00C	TIM0_COMPA RJMP	timer 0 Compare match A Group interrupt timer 0
0x00D	TIM0_COMPB RJMP	Compare match B Group interrupt timer 0 Overflow
0x00E	TIM0_OVF RJMP SPI_STC	
0x00F	RJMP USART_RXC RJMP	
0x010	USART_UDRE RJMP	
0x011	USART_TXC RJMP ADC	SPI Transmission complete interrupt
0x012	RJMP EE_RDY RJMP	USART Reception completion interrupt
0x013	ANA_COMP RJMP TWI	USART Data Register Empty
0x014	NOP NOP RJMP PCI3	USART Send complete interrupt
0x015		ADC Conversion Complete Interrupt
0x016		EEPROM Ready Interrupt Controller
0x017		Comparator Interrupt
0x018		TWI Reserved interrupt controller
0x019		addresses are reserved address pin
0x01A		change interrupt 3
0x01B;		
0x01C (**RESET :)**	LDI r16, high (RAMEND)	Set the stack pointer to start the main program RAM The
0x01D	OUT SPH, r16 LDI	top address
0x01E	r16, low (RAMEND) OUT	
0x01F	SPL, r16 SEI	
0x020		Enable global interrupt
0x021		

Register Definition

MCU Control Register - MCUCR

MCUCR - MCU Control register								
MCUCR: 0x35 (0x55)				Defaults: 0x00				
MCUCR	FWKEN	FPDEN	EXRFD	PUD	IRLD	IFAIL	IVSEL	WCE
R / W	R / W	R / W	R / W	R / WW / O		R / O	R / W	R / W

Bit Definitions		
[0]	WCE	MCUCR Update Enable bit, update MCUCR Before, you first need to set this bit, and then 6 Completed within a period MCUCR Update registers
[1]	IVSEL	Interrupt Vector Select bit, this location 1 After the interrupt vector address will be based IVBASE Mapped to the new value of the register address
[2]	IFAIL	The system failed to load configuration bits flag, 0 = By checking the configuration information 1 = Failed to load configuration information
[3]	IRLD	write 1 The reload the system configuration information
[4]	PUD	Pull on the global disable bit 0 = Pull-up control to enable global 1 = Close all IO The pull-up resistor
[5]	EXRFD	External reset filtering disable bit 0 = Enable External reset (190us) The digital filter 1 = Disable external reset of the digital filter circuit
[6]	FPDEN	Flash Power / down Enable Control 0 :system SLEEP Rear FLASH Remain powered 1 :system SLEEP Rear FLASH Power outage
[7]	FWKEN	Fast wake-up mode enable control, only Power / Off Mode is active 0 : 260us Filter delay 1 : 32us Filter delay

Interrupt Vector Address Register - IVBASE

IVBASE - Interrupt Vector Address Register		
IVBASE: 0x75	Defaults: 0x00	
IVBASE	IVBASE [7: 0]	
R / W	R / W	
Bit Definitions		
[7: 0]	IVBASE	in case IVSEL for 1 Interrupt vector (except for the reset vector) will IVBASE Base address 512 Remapping bytes on a page. Interrupt vector base address is mapped to: (IVBASE << 8) + table 1 Corresponding vector address

External Interrupt

- 2 External interrupt sources
- Level or edge-triggered interrupts can be configured
- Wake-up source can be used in sleep mode

Outline

External interrupted by INT0 with INT1 Pin trigger. As long as the external interrupt is enabled, even if it 2 Configured as an output pin can also trigger an interrupt. This software can be used to generate an interrupt. External interrupts may be rising and falling edge or level-triggered, the external interrupt control register EICRA To configure. When the external interrupt is enabled and configured as level triggered (only INT0 with INT1 When the pin), as long as the pin is low, the interrupt will have been produced. INT0 with INT1 Rising or falling edge triggers an interrupt pin needs IO Clock work, and INT0 with INT1 Low pin triggers an interrupt is asynchronous detection. In addition to the idle mode, sleep mode under other IO The clock is stopped. Therefore, this 2 It can be used as external interrupt wake-up source in other sleep modes other than Idle mode.

If the level of the trigger level as a wake-up interrupt source in the power saving mode, the change must be held for some time to wake up MCU To reduce MCU Sensitivity to noise. The required level must be maintained long enough time for the MCU The end of the wake-up process, then the trigger level interrupts.

Register Definition

Register List

register	address	Defaults	description
EICRA	0x69	0x00	External Interrupt Control Register A
EIMSK	0x3D	0x00	External interrupt mask register
EIFR	0x3C	0x00	External Interrupt Flag Register

External Interrupt Control Register A- EICRA

EICRA **- External Interrupt Control Register A**								
address: 0x69				Defaults: 0x00				
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	ISC11	ISC10	ISC01	ISC00
R / W	-	-	-	- R / W		R / W	R / W	R / W

Bit	Name	description
7: 4	-	Reservations.
3	ISC11	INT1 Pin interrupt trigger control bit high.
2	ISC10	INT1 Pin interrupt trigger control bit low. When the global interrupt set and GICR The respective control bit interrupt mask register is set when the external interrupt 1 by INT1 Pin excited. See table describes interrupt trigger mode. Prior to edge detection MCU First sampling INT1 Level on the pin. If the selected edge trigger or level trigger changes in the way, that last longer than 1 A system clock cycle pulse will trigger an interrupt. Shorter pulses are not guaranteed to trigger an interrupt. If you choose low

		Level trigger, then the low level must be held until the completion of the current instruction execution will trigger an interrupt.
1	ISC01	INT0 Pin interrupt trigger control bit high.
0	ISC00	INT0 Pin interrupt trigger control bit low. When the global interrupt set and GICR The respective control bit interrupt mask register is set when the external interrupt 0 by INT0 Pin excited. See table describes interrupt trigger mode. Prior to edge detection MCU First sampling INT0 Level on the pin. If the selected edge trigger or level trigger changes in the way, that last longer than 1 A system clock cycle pulse will trigger an interrupt. Shorter pulses are not guaranteed to trigger an interrupt. If you select a low level interrupt level must be held until the completion of the current instruction execution will trigger an interrupt.

External Interrupt 1 The table below trigger.

External Interrupt 1 Trigger control

ISC1 [1: 0]	description
0	External pin INT1 Low trigger
1	External pin INT1 Rising or falling edge trigger
2	External pin INT1 Falling edge
3	External pin INT1 Rising edge triggered

External Interrupt 0 The table below trigger.

External Interrupt 0 Trigger control

ISC0 [1: 0]	description
0	External pin INT0 Low trigger
1	External pin INT0 Rising or falling edge trigger
2	External pin INT0 Falling edge
3	External pin INT0 Rising edge triggered

External Interrupt Mask Register - EIMSK

***EIMSK* - External interrupt mask register**								
address: 0x3D					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	INT1	INT0
R / W	-	-	-	-	-	- R / W		R / W
Bit	Name description							
7: 2	-	Retention						
1	INT1 External pin 1 Interrupt enable control bit. When set INT1 Bit "1" When, and Global Interrupt set, external pin 1 Interrupts are enabled, wake-up function is enabled. even if INT1 Pin is configured as an output pin corresponding change in level occurs, an interrupt will be generated. When set INT1 Bit "0" When the external pin 1 Interrupts are disabled, wake-up function is also disabled.							

0	INT0	External pin 0 Interrupt enable control bit. When set INT0 Bit "1" When, and Global Interrupt set, external pin 0 Interrupts are enabled, wake-up function is enabled. even if INT0 Pin is configured as an output pin corresponding change in level occurs, an interrupt will be generated. When set INT0 Bit "0" When the external pin 0 Interrupts are disabled, wake-up function is also disabled.

External Interrupt Flag Register - EIFR

EIFR - External Interrupt Flag Register								
address: 0x3C					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	INTF1	INTF0
R / W	-	-	-	-	-	- R / W		R / W

Bit	Name	description
7: 2	-	Reservations.
1	INTF1	External pin 1 Interrupt flag. When the edge-triggered external pin 1 Interrupted, INTF1 It is set. When the low level triggered external pins 1 When the interrupt is not set INTF1 Bit. If the external pin at this time 1 Interrupt Enable INT1EN Bit "1" And the Global interrupt flag is set, it will produce an external pin 1 Interrupted. When you do this the interrupt service routine INTF1 Will be automatically cleared or INTF1 Write bit "1" Also clears the bit.
0	INTF0	External pin 0 Interrupt flag. When the edge-triggered external pin 0 Interrupted, INTF0 It is set. When the low level triggered external pins 0 When the interrupt is not set INTF0 Bit. If the external pin at this time 0 Interrupt Enable INT0EN Bit "1" And the Global interrupt flag is set, it will produce an external pin 0 Interrupted. When you do this the interrupt service routine INTF0 Will be automatically cleared or INTF0 Write bit "1" Also clears the bit.

Arithmetic accelerator (uDSC)

- 16 Bit memory model (LD / ST)
- 32 Bit accumulator (DX)
- Single cycle 16 Bit multiplier (MUL)
- 32 Bit arithmetic logic unit (ALU)
- 16 Bit saturation operation (SD)
- 8 cycle 32/16 Divider
- Single-cycle multiply-add / multiply-subtract operation (MAC / MSC)

Outline

Digital arithmetic accelerator (uDSC) As LGT8XM An arithmetic coprocessor kernel module, with LGT8XM Kernel 16 Place LD / ST Model to achieve a 16 Bit digital signal processing unit. Most of the control process to meet Class A digital signal.

uDSC Internal functions and features:

1.16 Bit operand registers DX / DY

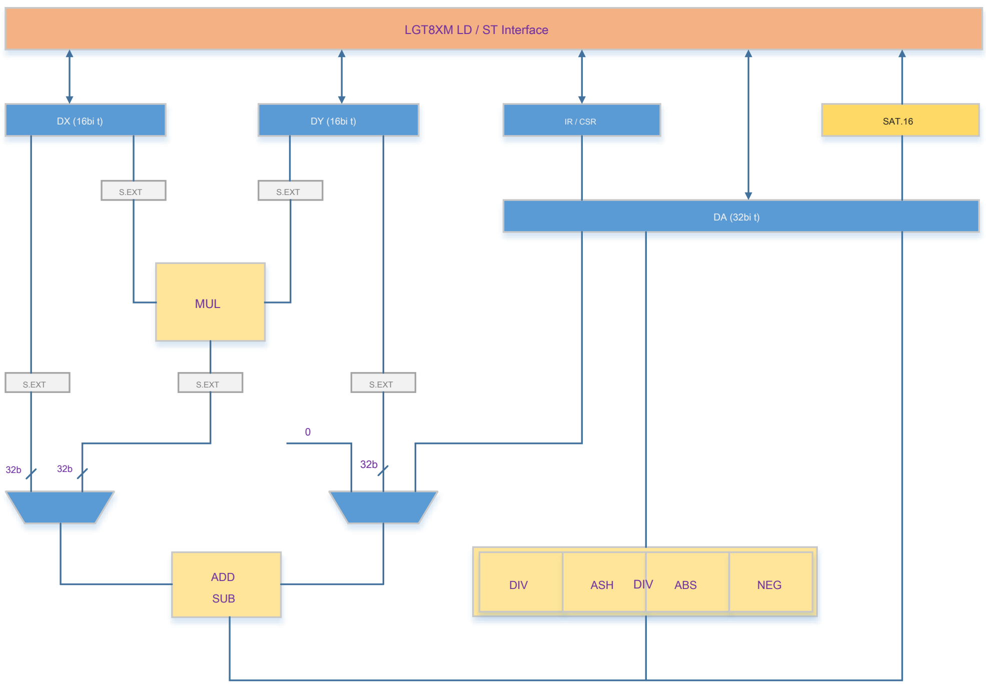
2.32 Bit accumulator register DA

3. Single cycle 17 Bit multiplier (can be achieved 16 Bit / unsigned multiplication)

4.32 Place ALU (can be realised 16/32 Bit addition, subtraction and shift operations)

5.16 Bit saturation operation (For the calculation result is stored into RAM space)

6. 32/16 Divider, 8 The complete operation cycles



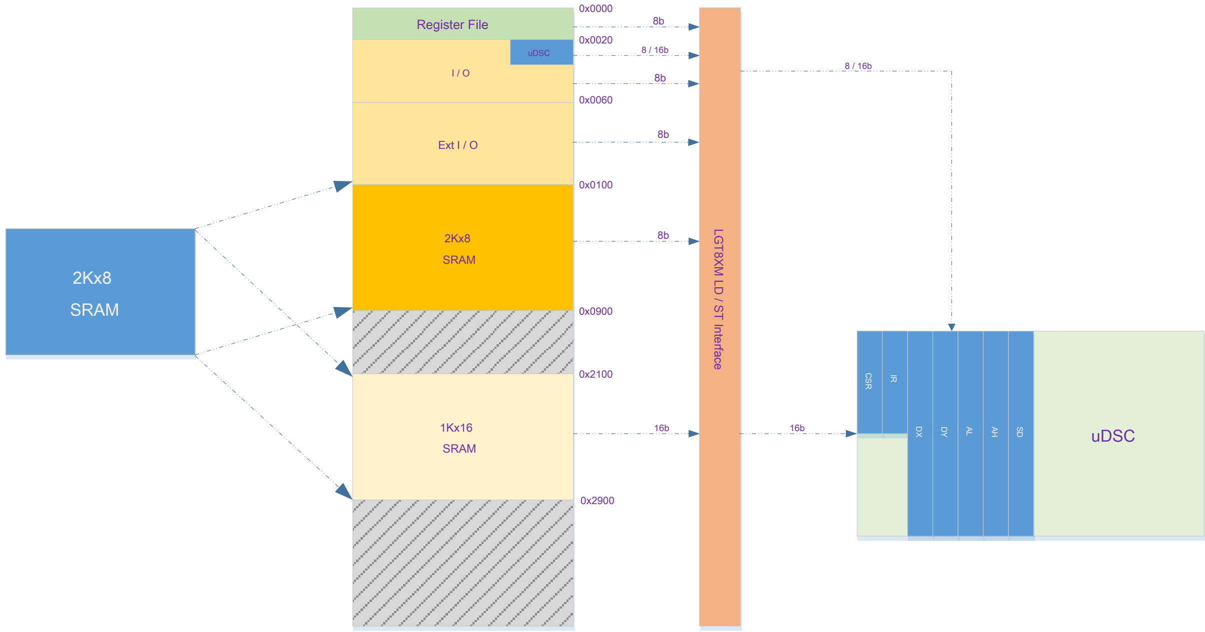
uDSC Structure chart

16 Place LD / ST Operating mode

To improve uDSC Efficiency of operation of a large number of data processing, LGT8XM Kernel implementation of a dedicated 16 Place LD / ST Memory channel may be used LDD / STD Efficient instruction in uDSC versus SRAM And a general register file for between 16 Bit data exchange.

In order not to disrupt the normal LD / ST Instruction, LGT8XM The kernel SRAM Space to remap 0x2100 ~ 0x28FF . use LD / ST Instruction from 0x2100 ~ 0x28FF Space Access SRAM When the kernel automatically open 16 Place LD / ST Function, open SRAM versus uDSC Between the direct access channel.

The figure below shows LGT8XM Kernel address space distribution of data:



As shown in FIG, LGT8XM The kernel can use LD / ST Instructions in uDSC of DX / DY / DA Register with SRAM Between direct 16 Access data stored bit access. Simultaneously uDSC Internal registers to be mapped I / O Space access uDSC Register divided 8/16 Two modes.

uDSC In addition to the internal operation DX / DY / DA External register, further comprising the additional 2 More 8 Bit register: uDSC Control Status Register CSR And an operation instruction register IR . CSR / IR Only through I / O Space Access bytes; Access DX / DY / AL / AH When 16 Bit mode. can use IN / OUT as well as LD / ST / LDD / STD / LDS / STD And other commands access.

uDSC Related control and status registers are mapped into data IO Space, directly IN / OU Instruction addressing can be done in one instruction cycle 8/16 Bits of data access.

CSR For control uDSC Working mode and record the current uDSC State flag to perform operations. IR control uDSC Computing specific implementation. uDSC Support of the majority of operations will be completed in a single cycle, the division needs to run 7 A waiting period, you can also CSR Register flag bit determines whether the current division operation is completed.

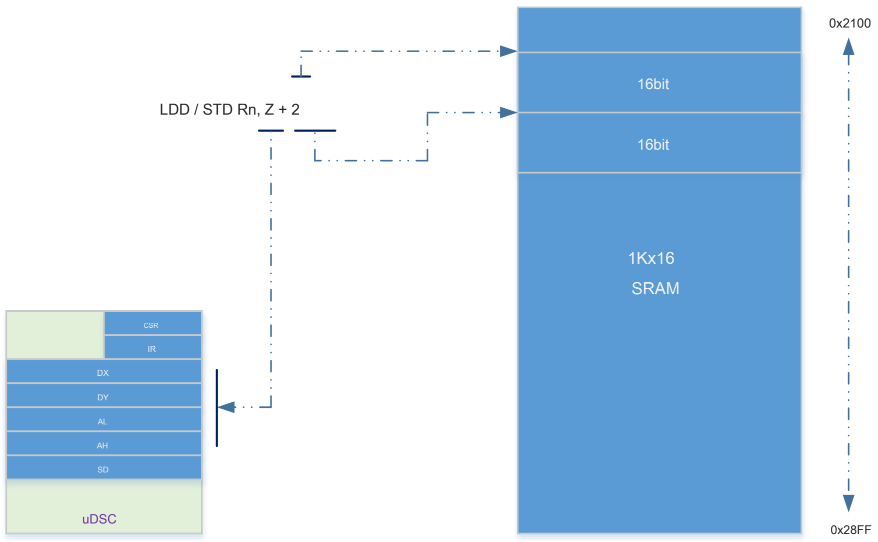
standard LD / ST Use instructions LGT8XM The internal general purpose registers as LD / ST Data use X / Y / Z As the destination address. When the destination address falls 16 Place SRAM When mapping space, this time LD / ST Meaning instruction operands vary, wherein X / Y / Z Still according to the destination address as the meaning, purpose working registers addressable uDSC Mapping mode will have two approaches. uDSC The mapping mode of action only in the 0x2100 ~ 0x28FF Address access visit. By mapping mode CSR The first register 6 Bit (MM) Settings.

16 Place LD / ST Mode, the instruction "LDD Rn, Z + q" It is represented by the [Z] Address 16 Bit data is loaded into uDSC Data register, then Z Adding an offset value "Q" . Here Rn Meaning mapping mode CSR [MM] The relationship is as follows:

LDD Rn, Z / Y + q			
CSR [MM]	[Z + q]	Opcode	Operations
0	0x2100 ~ 0x28FF	LDD R0, Z + q	DX = [Z]; Z = Z + q; R0 kept unchanged
		LDD R1, Z + q	DY = [Z]; Z = Z + q; R1 kept unchanged
		LDD R2, Z + q	AL = [Z]; Z = Z + q; R2 kept unchanged
		LDD R3, Z + q	AH = [Z]; Z = Z + q; R3 kept unchanged
1	0x2100 ~ 0x28FF	LDD Rn, Z + q	{Rn} address for DX / DY / AL / AH in I / O region [DX / DY / AL / AY] = [Z]; Z = Z + q Rn keep unchanged
STD Rn, Z / Y + q			
0	0x2100 ~ 0x28FF	STD Z + q, R0	[Z] = DX; Z = Z + q; R0 kept unchanged
		STD Z + q, R1	[Z] = DY; Z = Z + q; R1 kept unchanged
		STD Z + q, R2	[Z] = AL; Z = Z + q; R2 kept unchanged
		STD Z + q, R3	[Z] = AH; Z = Z + q; R3 kept unchanged
		STD Z + q, R4	[Z] = SD; Z = Z + q; R4 kept unchanged
1	0x2100 ~ 0x28FF	STD Z + q, Rn	{Rn} address for DX / DY / AL / AH / SD in I / O region [Z] = [DX / DY / AL / AH / SD] addressed by {Rn} Rn keep unchanged

LGT8XM Instruction set LD / ST, LDS / STS Have access to 0x2100 ~ 0x28FF Area, but LDD / STD of Y / Z + q Addressing more effective. LDD / STD Addressing based on a base address, we can Y / Z Set as RAM The base address of the data, by using LDD / STD Instructions Y / Z + q Addressing mode, access data and instructions can be executed in a single cycle, and the address pointer is automatically moved to the next target address.

LGT8XM Kernel Standard LDD / STD Instructions Y / Z + q Offset addressing mode, instruction execution [Y / Z + q] As a 8 After the address bits of data, execute complete Y / Z The value does not increase. When LDD / STD Addressing 0x2100 ~ 0x28FF When the address range, LDD / STD The command behavior changed: the instruction is executed, use [Y / Z] As a 16 Addressing address bit data after the execution, Y / Z The value increase "Q" Specified offset. This feature can improve our efficiency continuously addressed by the "Q = 2" You can achieve a continuous 16 Addressing data bits.



Variable address 16 The mapping between the address bit pattern

LGT8XM for 8 Bit processor, Data access in bytes. LGT8F328P Internal 2K Bytes of data space. This space is mapped to 0x0100 ~ 0x08FF the address of. C / C ++ The compiler automatically assigned to variables 0x0100 ~ 0x08FF

between. If we C / C ++ A defined 16 It requires the use of an array of bits uDSC Calculates, on the need to map the address of the variable to 16 Place LD / ST Address area access (0x2100 ~ 0x28FF). The method is very simple, just to address the increase in variable 0x2000 It can be offset.

uDSC Operation instruction defines

Software uDSC of IR Register specifies the operation to be achieved. uDSC All arithmetic operations are DX / DY / DA

Conducted between. Users can use 16 Place LD / ST Channels DX / DY / DA as well as SRAM Fast exchange data directly.

classification	IR [7: 0]								Functional Description
ADD / SUB	0	0	S_1	0	0	1	0	1	DA = DX + DY
	0	0	S_1	0	0	0	0	1	DA = DX - DY
	0	0	0	1	1	1	0	1	DA = DY
	0	0	S_1	1	1	0	0	1	DA = -DY
	0	0	S_1	1	0	1	1	1	DA = DA + DY
	0	0	S_1	1	0	0	1	1	DA = DA - DY
MAC / MSC	0	1	$S1_2$	$S0_2$	0	1	0	0	DA = DX * DY
	0	1	$S1_2$	$S0_2$	0	0	0	0	DA = -DX * DY
	0	1	$S1_2$	$S0_2$	1	1	0	0	DA = (DX * DY) >> 1
	0	1	$S1_2$	$S0_2$	1	0	0	0	DA = (-DX * DY) >> 1
	0	1	$S1_2$	$S0_2$	0	1	1	S	DA = DA + DX * DY
	0	1	$S1_2$	$S0_2$	1	1	1	S	DA = (DA + DX * DY) >> 1
	0	1	$S1_2$	$S0_2$	0	0	1	S	DA = DA - DX * DY
	0	1	$S1_2$	$S0_2$	1	0	1	S	DA = (DA - DX * DY) >> 1
MISC	1	0	0	0	0	0	0	0	DA = 0

	1	0	0	0	0	1	0	S	DA = NEG (DA)
	1	0	0	0	1	0	0	S	DA = DX ^ 2
	1	0	0	0	1	0	1	S	DA = DY ^ 2
	1	0	1	0	0	0	0	S	DA = ABS (DA)
	1	0	1	1	0	0	0	0	DA = DA / DY
	1	0	1	1	0	0	0	1	DA = DA / DY, DY = DA% DY
SHIFT	1	1	0	0	N3	N2	N1	N0	DA = DA << N
	1	1	S	1	N3	N2	N1	N0	DA = DA >> N

Description:

1. S Operation, it represents a signed arithmetic operation or an unsigned
2. S1 Show DX Whether as signed, S2 Show DY Whether it is a signed number
3. N3 ... 0 Is a four-digit shift can be achieved up to 15 Bit shift operation
4. - Represents the value of this bit is not insignificant, can be set 0 or 1 , Recommended setting 0

Register Definition

name	IO address	Functional Description
DCSR	0x20 (0x00)	uDSC Control Status Register
DSIR	0x21 (0x01)	Arithmetic instruction register
DSSD	0x22 (0x02)	accumulator DSA of 16 Bit saturation operation result
DSDX	0x10 (0x30)	Operand DSDX, 16 Bit read and write access
DSDY	0x11 (0x31)	Operand DSDY, 16 Bit read and write access
DSAL	0x38 (0x58)	32 Bit accumulator DSA [15: 0], 16 Bit read and write access
DSAH	0x39 (0x59)	32 Bit accumulator DSA [31:16], 16 Bit read and write access

DSCR - Control Status Register

***DSCR* - uDSC Control Status Register**								
address: 0x20 (0x00)						Defaults: 0010_xxxx		
Bit	7	6	5	4	3	2	1	0
Name	DSUEN	MM	D1	D0	-	N	Z	C
R / W	R / W	R / W	R / W	R / W	-	R / W	R / W	R / W

Bit	Name	description
7	DSUEN	uDSC Enable control module; 1 = Enable, 0 = Disable
6	MM	uDSC Register map mode; refer to the detailed definition 16 Introduction bit mode of operation. 0 = Fast access mode, 1 = IO Mapping mode
5	D1	Division operation completion flag, 1 = Operation completed
4	D0	In addition to division 0 Flag
3	-	Unimplemented
2	N	Operation result is negative flag
1	Z	Flag value to zero
0	C	32 Adder carry / borrow flag

DSIR - Arithmetic instruction register

DSIR - uDSC Arithmetic instruction register								
address: 0x21 (0x01)						Defaults: 0000_0000		
Bit	7	6	5	4	3	2	1	0
Name	DSIR [7: 0]							
R / W	R / W							
Bit	Name description							
7: 0	IR	uDSC Operation instruction. See " Operation instruction defines " Section describes						

DSDX - Operand register DSDX

DSDX - uDSC Operand register DX		
address: 0x30 (0x10)		Defaults: 0000_0000
Bit	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Name	
	DSDX [15: 0]	
R / W	R / W	
Bit	Name description	
15: 0	DSDX	16 Bit operand registers DSDX

DSDY - Operand register DSDY

DSDY - uDSC Operand register DY		
address: 0x31 (0x11)		Defaults: 0000_0000
Bit	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Name	
	DSDY [15: 0]	
R / W	R / W	
Bit	Name description	
15: 0	DSDY	16 Bit operand registers DSDY

DSAL - 32 Bit accumulator DA Low 16 Place

DSAL - uDSC Operand register DSA Low 16 Place		
address: 0x58 (0x38)		Defaults: 0000_0000
Bit	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Name	
	DSA [15: 0]	
R / W	R / W	
Bit	Name description	
15: 0	DSAL	32 Bit accumulator DSA Low 16 Place

DSAH - 32 Bit accumulator DA height of 16 Place

***DSAH* - uDSC Operand register DSA height of 16 Place**	
address: 0x59 (0x39)	Defaults: 0000_0000
Bit	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Name
	DSA [31:16]
R / W	R / W
Bit	Name description
15: 0	DSAH 32 Bit accumulator DSA height of 16 Place

DSSD - DA Saturated arithmetic register

***DSSD* --16 Place DA Saturation calculation result**	
address: 0x22 (0x02)	Defaults: 0000_0000
Bit	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 Name
	DSSD [15: 0]
R / W	R / W
Bit	Name description
15: 0	DSSD 32 Bit accumulator DSA of 16 Bit saturation operation result

uDSC Applications

Examples 1. The basic configuration and operation

Here is a simple subroutine (AVRGCC) To achieve a 16 Bit multiplication operation, returns 32 Bit results:

unsigned long **dsu_xmuluu (** unsigned short dy, unsigned short dx);

For the following C Assembly function implementation code:

```
# include       "Udsc_def.inc"                  ; Opcode definitions
                . Global      dsu_xmuluu        ; Declare for called from C / C ++ code

dsu_xmuluu:
                out           DSDX, r24         ; Load DX
                out           DSDY, r22         ; Load DY
                ldi           r20, XMULUU       ; Load opcode
                out           DSIR, r20         ; Do multiply
                in            r22, DSAL         ; {R23, r22} = AL
                in            r24, DSAH         ; {R25, r24} = AH
                ret
```

Universal programmable ports (GPIO)

Outline

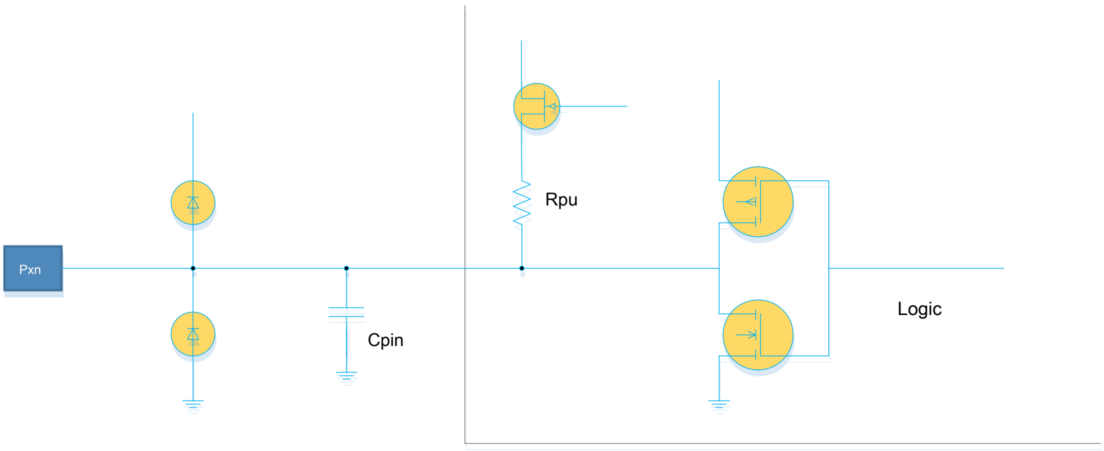
Based on all LGT8XM Core family realized MCU Have I / O Port Reading - change - write function. This means that one can use the port status SBI with CBI Command changes alone, without affecting any other I / O . Similarly, a port or changing the direction of the pull-up resistor to control it can be so.

LGT8FX8P the most part of I / O It has a symmetrical drive characteristics, and capable of absorbing a large current drive. I / O Having two drive capability, the user can control each I / O Drive capability. I / O Drive capability can directly drive some of the led .

LGT8FX8P the most part of I / O You can drive up 30mA The current can be directly used to drive the segment code led . all I / O of VCC with GND It has its own direct ESD Protection diodes, designed to withstand up to at least

5000V of ESD pulse.

I / O An equivalent circuit diagram:



All of the following description chapter unified register mode, lowercase "X" The port number of letters the name, lowercase "N" It represents the bit number of ports. However, when using port register, you must use the exact name of the register in the program. such as PORTB3 It represents PORTB The third, here is unity with PORTxn Representation. I / O Detailed definitions related registers, please reference register description.

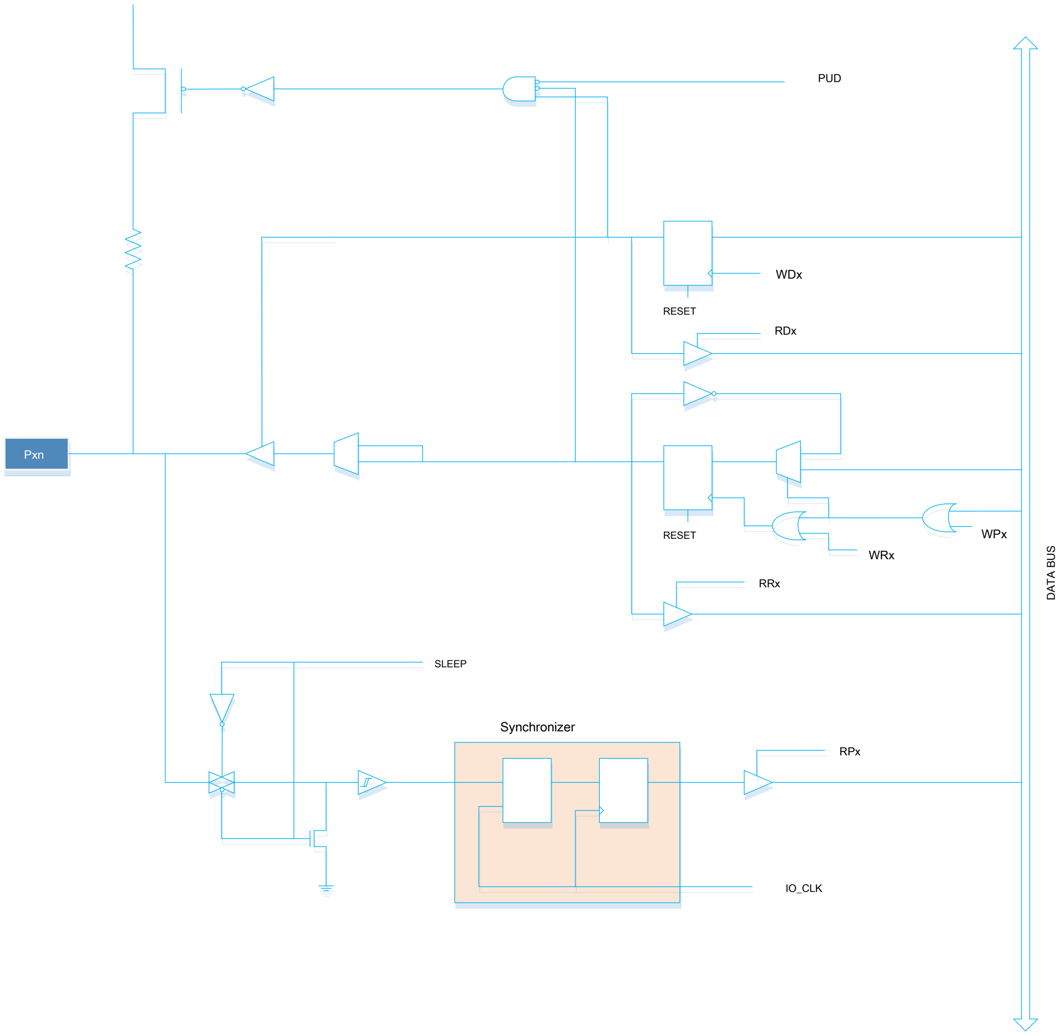
Each port is assigned three I / O Register space, they are: port data output register (PORTx) , The port direction register (DDRx) Port data input register (PINx) . Data input port registers are read only. Data output register read port direction register may be rewritten. MCUCR Register PUD Bits, is used to control all I / O The pull-up resistor, when PUD Bit 1 When would prohibit so I / O The pull-up resistor.

most I / O In addition to general-purpose input / output function, as will be multiplexed with other peripheral functions. Specific alternate functions please refer to the section on port function reuse.

Note that enabling the alternate function of some ports does not affect them as a digital port I / O use. And some multiplexing function may need to I / O Register control port input / output direction. Specific settings will be described in the documentation for each multiplexing module.

General purpose input / output port

As a general I / O When the port is bidirectional drive I / O Port, internal programmable pull. The figure below shows common I / O Equivalent circuit diagram of the port:



PUD: PULLUP DISABLE

SLEEP: SLEEP CONTROL

IO_CLK: I / O CLOCK

WDx: WRITE DDRx

RDx: READ DDRx

WRx: WRITE PORTx

RRx: READ PORTx REGISTER

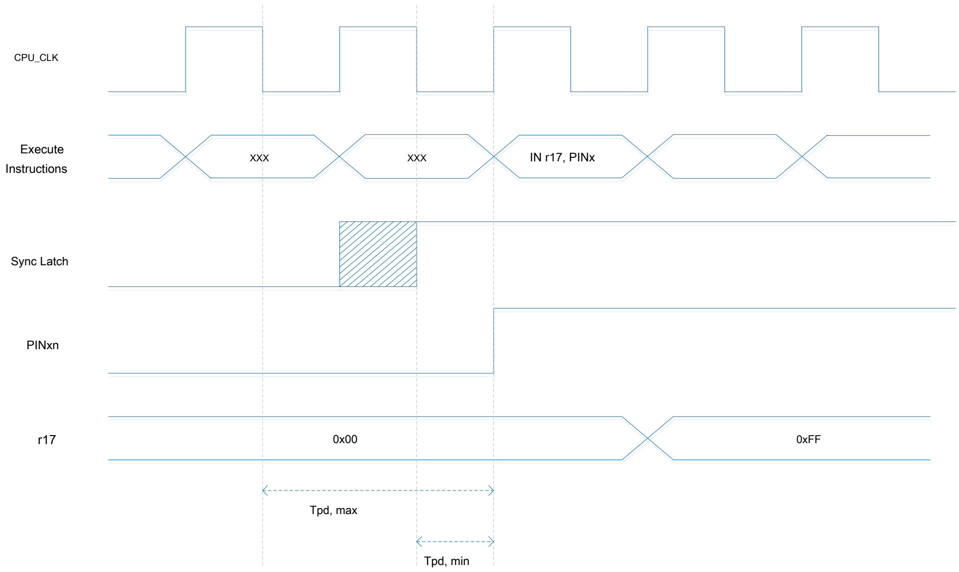
RPx: READ PORTx PIN

WPx: WRITE PINx REGISTER

Using the configuration port

Each port consists of three control register bits: DDxn , PORTxn with PINxn . among them DDxn Used by DDRx Register access, PORTxn able to pass PORTx Register access, PINxn able to pass PINx Register access.

DDRxn Register bit is used to set the input port / output direction. in case DDxn Set as 1 , Pxn It is configured as a port to an output port. in case DDxn Set as 0 , Pxn It is configured as an input port.



in case PORTxn Bits are written 1 While this port is configured as input port, the port of the pull-up resistor valid. If you want to ban port pull-up resistor, PORTxn It must be written as 0 Or this port is configured as an output port.

Reset initialization state of the port as an input, the pull-up resistor invalid.

PORTxn Set as 1 While this port is configured as an output port, the external port will be driven high. in case PORTxn Set as 0 , The port will be driven low.

Input / Output

when I / O Tristate state ([DDxn, PORTxn]) = 0b00) And output high ([DDxn, PORTxn] = 0b11) When switching between, there will be pulled low or intermediate output port status. Typically, a pull-up resistor can be accepted, because in a high-impedance environment, driven high and the difference between the pull is not important. If this is not the case, you can MCUCR Register PUD Close the pull-bit port.

Similarly, when the switching between the pull low energy input and output, the same problem occurs. The user must tri-state ([DDxn, PORTxn] = 0b00) Or high output ([DDxn, PORTxn] = 0b11) As an intermediate state.

Port drive configuration table:

DDxn	PORTxn	PUD	Port Status	Pull-Function
0	0	X	Entry	Prohibit tri-state (High-Z)
0	1	0	Entry	Enable + Internal pull mode input
0	1	1	Entry	Prohibit tri-state (High-Z)
1	0	X	Export	Prohibition low output (fan)
1	1	X	Export	Ban high output (fan-out)

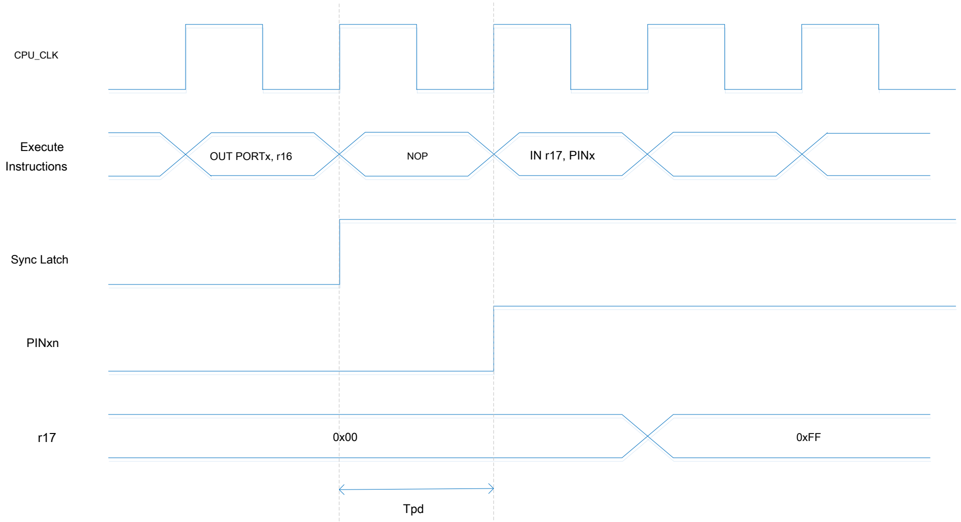
Read port value

Whether the port direction bit DDxn How to set, to pass through PINxn Register bits read current status of the port. To avoid direct read port to produce metastable, PINxn It is through a port register bit synchronizer results. The synchronizer of a latch and a register composed, so PINxn There is a small delay between the value of the current port. This delay is due to the result of the presence of the synchronizer, the delay time of up to 1 Periodic half.

We assume that the system cycle begins with the first falling edge of the system clock, the data latched in the latch clock is low, the clock is high linear data through the latch as shown in the above figure shaded. When the clock is low, data is latched in the port

Memory, and the next rising edge of the clock to register PINxn register. The image above Tpd, max as well as Tpd, min The maximum and minimum delay data ports, is divided into 1.5 Cycle and 0.5 cycle.

If you want to read the port value software settings, it is necessary I / O Write and read byte support a dummy operation instruction (NOP) . The timing is shown below:



The following code shows how to set port B Pin 0/1 High, 2/3 Low, defined Pin 4-7 And enable input pin 6 , 7 The pull-up resistor. Value is then read back pin general purpose working register, as previously described, the output and input pins directly inserted a NOP instruction.

Assembly code

```
; Define Pull-ups and set outputs high; Define
directions for port pins
LDI r16, (1 << PB7) | (1 << PB6) | (1 << PB1) | 1 << PB0)
LDI r17, (1 << DDB3) | (1 << DDB2) | (1 << DDB1) | (1 << DDB0)
OUT PORTB, r16
OUT DDRB, r17
; Insert nop for synchronization
NOP
; Read port pins
IN r16, PINB
```

C Language code

```
unsigned char I;
/ * Define pull-ups and set outputs high * / / * Define
directions for port pins * /
PORTB = (1 << PB7) | (1 << PB6) | (1 << PB1) | (1 << PB0); DDRB = (1 << DDB3) |
(1 << DDB2) | (1 << DDB1) | (1 << DDB0);
/ * Insert nop for synchronization * /
__no_operation ();
/ * Read port pins * /
I = PINB;
```

And sleep control input enable

From I / O The equivalent circuit diagram, we can see, the digital inputs can be SLEEP Under the control signal is clamped to the ground level. SLEEP Signal from the MCU Sleep controllers and various dormant mode control. This ensures that after entering hibernation, the system will not enter the port float caused by leakage.

Ports SLEEP Control of external interrupt function will be replaced. If an external interrupt request is invalid, SLEEP Control can still play a role. SLEEP Control functions may also be substituted by other second function, please refer to the following describes the specific port on the second function.

Fast Flip port status

State is set to output port IO ,able to pass PORTn Port status register changes. If the need to flip the current state output port, generally need to read the current status of the port PINx And then negated written back PORTn Register complete flip. LGT8FX8P Provide another more efficient way reversing port state, directly to the PINx Register Write

1 It can achieve the specified port status flip. For example, we write PINB [3] for 1 Can achieve PB3 The port status flip. For applications required to generate the output clock, this embodiment is very practical.

Digital / analog multiplexing port

LGT8FX8P Port number modulo function portion hybrid multiplexing port. In addition to internal DAC Output PD4 In addition, other mixing both as analog input ports. When used as an analog port, the software needs to be set to the input mode the port, and turn off the internal pull necessary to avoid influence on the analog revenue. DIDR0 ~ 2 Register for closing the mixing function port digital input channel, in order to avoid unnecessary power loss caused by the analog input to a digital circuit. DIDRx It does not close the digital output port.

High current push-pull drive port

LGT8FX8P Support for multiple 6 High-current push-pull drive ports, support up to 80mA The push-pull driver. Considering the chip VCC The maximum over current capacity constraints, is not recommended to open simultaneously 6 High-current drive. Especially for only one set of power supply ports QFP32 Package, it is recommended not to enable and drive 4 More high-current loads.

Common ports to drive 12mA Software need HDR Register large current driving open port. Port includes a large current drive capability as follows:

HDR port	QFP48	QFP32	HDR	Function Description
PD5	PD5	PD5	HDR [0]	N / A
PD6	PD6	PD6	HDR [1]	N / A
PF1	PF1	PD1 PF1	HDR [2]	QFP32 Package PD1 Internal equivalent QFP48 of PD1 versus PF1 in parallel
PF2	PF2	PD2 PF2	HDR [3]	QFP32 Package PD2 Internal equivalent QFP48 of PD2 versus PF2 in parallel
PF4	PF4	PE4 PF4	HDR [4]	QFP32 Package PE4 Internal equivalent QFP48 of PF4 versus PE4 in parallel
PF5	PF5	PE5 PF5	HDR [5]	QFP32 Package PE5 Internal equivalent QFP48 of PF5 versus PE5 in parallel

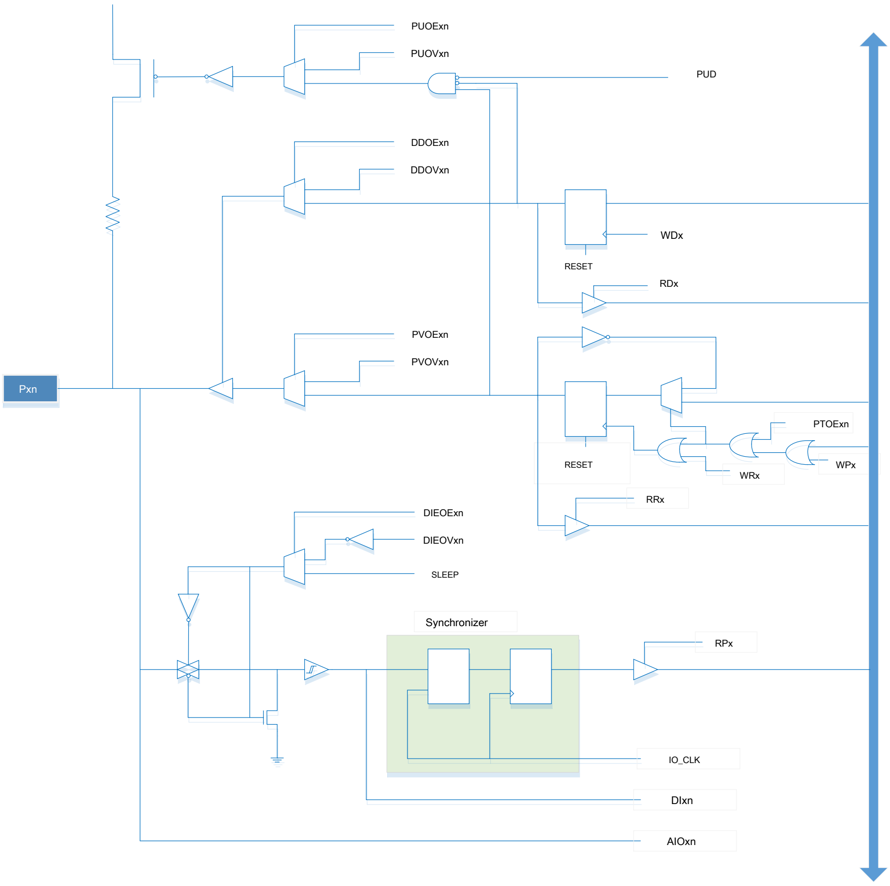
Processing idle port

If some of the port is not in use, it is recommended to drive them to a fixed level. In any case, the floating pin will bring more power and cause the system to become unstable under strong interference.

A fixed level to a port easiest way is to open a pull-up resistor port. Note that the pull-up resistor in the power-on reset is prohibited. Way pull-up resistor will also bring the excess leakage. It is recommended to use a pull-up or pull-down resistor external connection. Or directly to the port connected to the power supply it is not recommended, because if the pin is configured as an output, there may result in a very large current, resulting in a devastating impact on the chip through the port.

Port multiplexing function

Most ports have alternate functions, the following illustrates an equivalent circuit of the port of the multiplexing function control port. These alternate functions does not necessarily exist and so the port pin.



PUOExn:	Pxn PULL-UP OVERRIDE ENABLE	PUD:	PULLUP DISABLE
PUOVxn:	Pxn PULL-UP OVERRIDE VALUE	WDx:	WRITE DDRx
DDOExn:	Pxn DATA DIRECTION OVERRRIDE ENABLE	RDx:	READ DDRx
DDOVxn:	Pxn DATA DIRECTION OVERRIDE VALUE	RRx:	READ PORTx REGISTER
PVOExn:	Pxn PORT VALUE OVERRIDE ENABLE	WRx:	WRITE PORTx
PVOVxn:	Pxn PORT VALUE OVERRIDE VALUE	RPx:	READ PORTx PIN
DIEOExn:	Pxn INPUT-ENABLE OVERRIDE ENABLE	WPx:	WRITE PINx
DIEOVxn:	Pxn INPUT-ENABLE OVERRIDE VALUE	IO_CLK:	I / O CLOCK
SLEEP:	SLEEP CONTROL	DIxn:	INPUT PIN n ON PORTx
PTOExn:	Pxn PORT TOGGLE OVERRIDE ENABLE	AIOxn:	ANALOG I / O PIN n ON PORTx

General Description multiplexing function control signals:

signal	Full name	Functional Description
PUOE	The multiplexing of the enable pull	This bit is 1 , Enabled by the pull PVOV Control; If this bit is 0 Pull-up enabled by DDxn, PORTxn as well as PUD Joint control
PUOV	Pull multiplexing value	in case PUOE for 1 This bit is 1 Enable pin pull-up resistor, otherwise it will prohibit a pullup
DDOE	Port Direction enable multiplexing	Second place is 1 , By the output enable pin DDOE Control, or by the DDxn control
DDOV	Multiplexing port direction value	in case DDOE for 1 , Sub-bit 1 Will enable output enable pin, otherwise closed pin output
PVOE	Data multiplexing port enable	If the second bit is 1 And an output enable pin, pin input value by PVOV Control, or by PORTxn control
PVOV	Multiplexing port data value	reference PVOE Functional Description
PTOE	Flip enable multiplexing port	Second place is 1 , PORTxn Bit flips
DIEOE	Digital Input Enable enable reuse	If the second bit is 1 , Can make a digital input port DIEOV control System; otherwise there will be MCU Running state control
DIEOV	Digital Input Enable multiplexing value	in case DIEOE for 1 , Digital input port by the second position control, and MCU Run regardless of the state
DI	Digital input	This is the digital input signal is input to replace the function of the module. From I / O Wait for the next circuit diagram can be seen, this value after the Schmitt trigger, but I / O Input before the synchronizer. This signal is connected to the peripheral modules, the peripheral modules will be synchronized as required
AIO	Analog Input	Analog input / output signal, this signal directly I / O of PAD Is connected, it may be used as a bidirectional analog signal. This signal is directly related to the internal ADC Port, a comparator connected to the analog module etc.

The following section will be a brief description of each pin multiplexing functions and related control signals.

port B Alternate Function

Pin	Multiplexing Function Description
PB7	XTALI / TOSC2 (External main crystal pins XI) PCINT7 (Pin Change Interrupt 7)
PB6	XTALO / TOSC1 (External main crystal pins XO) PCINT6 (Pin Change Interrupt 6)
PB5	SCK (SPI Bus master clock input) PCINT5 (Pin Change Interrupt 5)
PB4	MISO (SPI Bus master input / output) PCINT4 (Pin Change Interrupt 4)

PB3	MOSI (SPI Bus master output / input) OC2A (Timer / Counter 2 Compare Match Output A) PCINT3 (Pin Change Interrupt 3)
PB2	SSN (SPI Bus Slave Select Input) OC1B (Timer / Counter 1 Compare Match Output B) PCINT2 (Pin Change Interrupt 2)
PB1	OC1A (Timer / Counter 1 Compare Match Output A) PCINT1 (Pin Change Interrupt 1)
PB0	ICP1 (Timer / Counter 1 Capture input) CLKO (System clock output) PCINT0 (Pin Change Interrupt 0)

XTALI / TOSC2 / PCINT7 - port B Pin 7

XTALI: External crystal pins XI . When the clock signal is used as the crystal, this pin can not be used as I / O use.

TOSC2: Timer external crystal pins 2 . When the internal RC Is configured as master chip clock and asynchronous timer function is enabled (ASSR Configuration register), this pin as an external oscillator pins timer. when ASSR Register AS2 set as 1 , EXCLK Is set to 0 , Will enable the timer / counter 2 Using an external asynchronous crystal clock function, PB7 The internal I / O Disconnected from the port, becoming the internal oscillator amplifier inverting output pin. In this mode, an external crystal is connected to the pin.

PCINT7: Pin Change Interrupt 7 . PB7 External interrupt sources. in case PB7 Crystal pins are used, DDB7, PORTB7 with PINB7 The value will not make any sense.

XTALO / TOSC1 / PCINT6- port B Pin 6

XTALO: External crystal pins XO .

TOSC1: Timer external crystal pins 1 . When the internal RC Is configured as master chip clock and asynchronous timer function is enabled (ASSR Configuration register), this pin as an external oscillator pins timer. when ASSR Register AS2 set as 1 , EXCLK Is set to 0 , Will enable the timer / counter 2 Using an external asynchronous crystal clock function, PB6 The internal I / O Port port pin as an input internal oscillator amplifier. In this mode, an external crystal is connected to the pin.

PCINT6: Pin Change Interrupt 6 . PB6 External interrupt sources. in case PB6 Crystal pins are used, DDB6, PORTB6 with PINB6 The value will not make any sense.

SCK / PCINT5- port B Pin 5

SCK: SPI The controller master clock output from the clock input device. when SPI The controller is configured as a device, this pin is configured as an input from the pin, from DDB5 control. when SPI The controller is configured as a master, in this direction by the pin DDB5 control. When this pin is SPI Forced to enter, can still PORTB5 Pull-up resistor control bits.

PCINT5: Pin change interrupt. PB5 External interrupt sources.

MISO / PCINT4- port B Pin 4

MISO: SPI Master control device data input, data output from the device. when SPI Configured as a master, this pin will be forced to enter, not subject to DDB4 control. when SPI As a slave device, the data side pin

To the DDB4 control. When this pin is SPI The controller is forced to enter, it can still pull-up resistor

PROTB4 control.

PCINT4: Pin change interrupt. PB4 External interrupt sources.

MOSI / OC2A / PCINT3- port B Pin 3

MOSI: SPI Master device data output controller, from data input device. when SPI Is configured as a slave, this pin will be forced to enter, not subject to DDB3 control. when SPI The controller is configured as a master, this pin by the method of DDB3 control. When this pin is SPI Forced to control the input, you can still pass PORTB3 Control its pull-up resistor.

OC2A: Timer / Counter 2 of A Group match output. PB3 As timer / counter 2 Compare match outside. At this point must DDB3 The output pin is set. Simultaneously, OC2A Also timer 2 of PWM Mode output pin.

PCINT3: Pin change interrupt. PB3 External interrupt sources.

SSN / OC1B / PCINT2- port B Pin 2

SSN: SPI Sheet from the selected input device. when SPI The controller is configured as a slave, this pin will be forced to enter, it is not subject to DDB2 control. As a slave device, SPI Controller SSN It is driven low to be effective. when SPI Configured as a master controller, by the direction of this pin DDB2 control. When this pin is SPI The controller is forced to enter, can still PORTB2 Control the pull-up resistor.

OC1B: Timer / Counter 1 of B Group match output. PB2 As timer / counter 1 Compare match outside. At this point must DDB2 The output pin is set. Simultaneously, OC1B Also timer 1 of PWM Mode output pin.

PCINT2: Pin change interrupt. PB2 External interrupt sources.

OC1A / PCINT1- port B Pin 1

OC1A: Timer / Counter 1 of A Group match output. PB1 As timer / counter 1 Compare match outside. At this point must DDB1 The output pin is set. Simultaneously, OC1A Also timer 1 of PWM Mode output pin.

PCINT1: Pin change interrupt. PB1 External interrupt sources.

ICP1 / CLKO / PCINT0- port B Pin 0

ICP1: Timer / Counter 1 The capture input pin

CLKO: The system clock output work, when CLKPR Register CLKOE Bit 1 This pin will be forced to output, from DDB0 control. Output frequency of the current system clock frequency.

PCINT0: Pin change interrupt. PB0 External interrupt sources.

port C Alternate Function

Pin	Multiplexing Function Description
PC7	ADC8 (ADC Input channel 8) APN2 (DAP Inverting input 2) PCINT15 (Pin Change input 15)
PC6	RESETN (External reset input) PCINT14 (Pin Change input 14)
PC5	ADC5 (ADC Input channel 5) SCL (TWI Clock line) PCINT13 (Pin Change input 13)
PC4	ADC4 (ADC Input channel 4) SDA (TWI Data line) PCINT12 (Pin Change input 12)
PC3	ADC3 (ADC Input channel 3) PCINT11 (Pin Change input 11)
PC2	ADC2 (ADC Input channel 2) PCINT10 (Pin Change input 10)
PC1	ADC1 (ADC Input channel 1) PCINT9 (Pin Change input 9)
PC0	ADC0 (ADC Input channel 0) PCINT8 (Pin Change input 8)

ADC8 / APN2 / PCINT15- port C Pin 6

ADC8: ADC External input channels 8

APN2: Reverse input port of the differential amplifier 2

PCINT15: Pin change interrupt. Close this pin after the external reset input function, PC7 It can be used as an external interrupt source.

RESETN / PCINT14- port C Pin 6

RESETN: An external reset pin. After the power-on reset, this pin defaults to an external reset function. able to pass IOCR Close register external reset function. After closing the external reset function, this pin as a general I / O use. But note that, in the power-on reset and other processes, this pin defaults to a reset input, so if you need to use this common pin I / O Function, can not affect the external circuit of the chip and the power reset process, it proposed that this pin is configured as an output function I / O And adding a suitable external pull-up resistor.

PCINT14: Pin change interrupt. Close this pin after the external reset input function, PC6 It can be used as an external interrupt source.

SCL / ADC5 / PCINT13- port C Pin 5

SCL: TWI Interface clock signal. TWCR Register TWEN position 1 After enabling TWI interface, PC5 will be TWI Control, become TWI Clock signal interface.

ADC5: ADC Input channel 5 . DIDR Close register number of multiplexed analog I / O The digital function to avoid the digital unit

Partial influence on the analog circuit. For details, see ADC The relevant sections.

PCINT13: Pin Change Interrupt 13

SDA / ADC4 / PCINT12- port C Pin 4

SDA: TWI Interface data signal. TWCR Register TWEN position 1 After enabling TWI interface, PC4 will be

TWI Control, become TWI Data signal interface.

ADC4: ADC Input channel 4 . DIDR Close register number of multiplexed analog I / O The digital functions, to avoid interference with the digital part of the analog circuit. For details, see ADC The relevant sections.

PCINT12: Pin Change Interrupt 12

ADC3 / APN1 / PCINT11- port C Pin 3

ADC3: ADC Input channel 3 . DIDR Close register number of multiplexed analog I / O The digital functions, to avoid interference with the digital part of the analog circuit. For details, see ADC The relevant sections.

APN1: Inverting input of the differential amplifier 1

PCINT11: Pin Change Interrupt 11

ADC2 / APN0 / PCINT10- port C Pin 2

ADC2: ADC Input channel 2 . DIDR Close register number of multiplexed analog I / O The digital functions, to avoid interference with the digital part of the analog circuit. For details, see ADC The relevant sections.

APN0: Inverting input of the differential amplifier 0

PCINT10: Pin Change Interrupt 10

ADC1 / APP1 / PCINT9- port C Pin 1

ADC1: ADC Input channel 1 . DIDR Close register number of multiplexed analog I / O The digital functions, to avoid interference with the digital part of the analog circuit. For details, see ADC The relevant sections.

APP1: The positive input of the differential amplifier 1

PCINT9: Pin Change Interrupt 9

ADC0 / APP0 / PCINT8- port C Pin 0

ADC0: ADC Input channel 0 . DIDR Close register number of multiplexed analog I / O The digital functions, to avoid interference with the digital part of the analog circuit. For details, see ADC The relevant sections.

APP0 : Differential amplifier positive input 0

PCINT8: Pin Change Interrupt 8

port D Alternate Function

Pin	Multiplexing Function Description
PD7	ACXN (Analog comparator 0/1 Common negative input) PCINT23 (Pin Change Interrupt twenty three)
PD6	AC0P (QFP32: Analog comparator 0 Positive input) OC0A (Timer / Counter 0 Compare Match Output A) OC3A (QFP32: Timer / Counter 3 Compare Match Output A) PCINT22 (Pin Change Interrupt twenty two)
PD5	T1 (Timer / Counter 1 External count clock input) OC0B (Timer / Counter 0 Compare Match Output B) PCINT21 (Pin Change Interrupt twenty one)
PD4	XCK (USART External Clock Input / Output) DAO (internal 8bit DAC Analog Output) T0 (Timer / Counter 0 External count clock input) PCINT20 (Pin Change Interrupt 20)
PD3	INT1 (External interrupt input 1) OC2B (Timer / Counter 2 Compare Match Output B) PCINT19 (Pin Change Interrupt 19)
PD2	INT0 (External interrupt input 0) AC0O (Comparators 0 Output) OC3B (QFP32: Timer / Counter 3 Compare Match Output B) PCINT18 (Pin Change Interrupt 18)
PD1	TXD (USART Data output) OC3A (QFP32: Timer / Counter 3 Compare Match Output A) PCINT17 (Pin Change Interrupt 17)
PD0	RXD (USART data input) PCINT16 (Pin Change Interrupt 16)

ACXN / OC2B / PCINT23- port D Pin 7

ACXN: Analog comparator 0/1 Public negative input

OC2B: Timer / Counter 2 of B Group match output. PD7 As timer / counter 2 Compare match outside. At this point must DDD7 The output pin is set. Simultaneously, OC2B Also timer 2 of PWM Mode output pin;

PCINT23: Pin Change Interrupt twenty three

AC0P / OC0A / PCINT22- port D Pin 6

AC0P: Analog comparator 0 Positive input.

OC0A: Timer / Counter 0 of A Group match output. PD6 As timer / counter 0 Compare match outside. At this point must DDD6 The output pin is set. Simultaneously, OC0A Also timer 0 of PWM Mode output pin

PCINT22: Pin Change Interrupt twenty two

T1 / OC0B / PCINT21- port D Pin 5

T1: Timer / Counter 1 External count clock input

OC0B: Timer / Counter 0 of B Group match output. PD5 As timer / counter 0 Compare match outside. At this point must DDD5 The output pin is set. Simultaneously, OC0B Also timer 0 of PWM Mode output pin

PCINT21: Pin Change Interrupt twenty one

XCK / T0 / DAO / PCINT20- port D Pin 4

XCK: Synchronous mode USART The external clock signal

T0: Timer / Counter 0 External count clock input

DAO: internal 8 Place DAC Analog Output

PCINT20: Pin Change Interrupt 20

INT1 / OC2B / PCINT19- port D Pin 3

INT1: External interrupt input 1

OC2B: Timer / Counter 2 of B Group match output. PD3 As timer / counter 2 Compare match outside. At this point must DDD3 The output pin is set. Simultaneously, OC2B Also timer 2 of PWM Mode output pin

PCINT19: Pin Change Interrupt 19

INT0 / OC3B / AC0O / PCINT18- port D Pin 2

INT0: External interrupt input 0

OC3B: Timing counter 3 Compare Match Output B . only at QFP32 When the package, PD2 versus QFP48 / PF2 Merge into one IO ,therefore PF2 Up OC3B It will also feature PD2 Output

AC0O: Analog comparator 0 Direct comparison output. by AC0FR Register control

PCINT18: Pin Change Interrupt 18

TXD / OC3A / PCINT17- port D Pin 1

TXD: transfer data(USART Data output). USART After the transmitter is enabled, PD1 It is forced to output, from DDD1 control

OC3A: Timing counter 3 Compare Match Output A . only at QFP32 When the package, PD1 versus QFP48 / PF1 Merge into one IO ,therefore PF1 Up OC3A It will also feature PD1 Output

PCINT17: Pin Change Interrupt 17

RXD / PCINT16- port D Pin 0

RXD: transfer data(USART data input). USART The receiver is enabled, PD0 They will be forced to enter, without DDD0 control. When the pin is USART Forced to enter, via the pull-up resistors PORTD0 Level control

PCINT16: Pin Change Interrupt 16

port E Alternate Function

Pin	Multiplexing Function Description
PE7	ADC11 (ADC Input channel 11) PCINT31 (Pin Change Interrupt 31)
PE6	AVREF (QFP32: ADC External reference voltage) ADC10 (ADC Input channel 10) PCINT30 (Pin Change Interrupt 30)
PE5	CLKO (System clock output) AC1O (Analog comparator 1 Output) PCINT29 (Pin Change Interrupt 29)
PE4	OC0A (Timer / Counter 0 Compare output configuration A) PCINT28 (Pin Change Interrupt 28)
PE3	ADC7 (ADC Input channel 7) AC1N (Analog comparator 1 Negative input) PCINT27 (Pin Change Interrupt 27)
PE2	SWD (SWD Debugger data line) PCINT26 (Pin Change Interrupt 26)
PE1	ADC6 (ADC Input channel 6) ACXP (Analog than the machine 0/1 Common positive input terminal) PCINT25 (Pin Change Interrupt 25)
PE0	SWC (SWD Debug clock input) APN4 (Inverting input of the differential amplifier 4) PCINT24 (Pin Change Interrupt twenty four)

ADC11 / PCINT31- port E Pin 7

ADC11: ADC External input channels 11

PCINT31: Pin Change Interrupt 30

AVREF / ADC10 / PCINT30- port E Pin 6

AVREF: ADC External reference power supply input, when used as an analog function, the corresponding figures I / O It is provided as an input, and close the pull-up resistor, in order to avoid interference to the digital circuit analog circuit

ADC10: ADC Analog input channels 10

PCINT30: Pin Change Interrupt 30

CLKO / AC1O / PCINT29- port E Pin 5

CLKO: This feature PB0 of CLKO The same function. can be used as PB0 / CLKO Alternate pin

AC1O: Analog comparator 1 Export

PCINT29: Pin Change Interrupt 29

OC0A / PCINT28- port E Pin 4

OC0A: Timer / Counter 0 of A Group match output. PE4 As timer / counter 0 Compare match outside. At this point must DDE4 The output pin is set. Simultaneously, OC0A Also timer 0 of PWM Mode output pin.

PCINT28: Pin Change Interrupt 28

ADC7 / AC1N / PCINT27- port E Pin 3

ADC7: ADC Input channel 7 . DIDR Close register number of multiplexed analog I / O The digital functions, to avoid interference with the digital part of the analog circuit. For details, see ADC Related Sections

AC1N: Analog comparator 1 Negative input

PCINT27: Pin Change Interrupt 27

SWD / PCINT26- port E Pin 2

SWD: SWD Commissioning data lines. PE2 The default is SWD Features. Users can be MCUSR register SWDD position 1 shut down SWD Debugger function. SWD After being closed, the debugging features will not be used.

PCINT26: Pin Change Interrupt 26

ADC6 / ACXP / PCINT25- port E Pin 1

ADC6: ADC Input channel 6 . DIDR Close register number of multiplexed analog I / O The digital functions, to avoid interference with the digital part of the analog circuit. For details, see ADC Related Sections

ACXP: Analog comparator 0/1 Public input positive terminal

PCINT25: Pin Change Interrupt 25

SWC / APN4 / PCINT24- port E Pin 0

SWC: SWD The debugger clock line. PE0 The default is SWC Features. Users can be MCUSR register SWDD position 1 shut down SWD Debugger function. SWD After being closed, the debugging features will not be used

APN4: Inverting input of the differential amplifier 4

PCINT24: Pin Change Interrupt twenty four

port F Alternate Function

Pin	Multiplexing Function Description
PF7	OC2B (Timer / Counter 2 Compare Match Output B) PCINT39 (Pin Change Interrupt 39)
PF6	T3 (Timer / Counter 3 External clock input) OC2A (Timer / Counter 2 Compare Match Output A) PCINT38 (Pin Change Interrupt 38)
PF5	OC1A (Timer / Counter 1 Compare Match Output A) PCINT37 (Pin Change Interrupt 37)
PF4	OC1B (Timer / Counter 1 Compare output configuration B) ICP3 (Timer / Counter 3 External capture input) PCINT36 (Pin Change Interrupt 36)
PF3	OC0B (Timer / Counter 0 Compare output configuration B) PCINT35 (Pin Change Interrupt 35)
PF2	OC3B (Timer / Counter 3 Compare Match Output B) PCINT34 (Pin Change Interrupt 34)
PF1	OC3A (Timer / Counter 3 Compare Match Output A) PCINT33 (Pin Change Interrupt 33)
PF0	ADC9 (ADC External input channels 9) APN3 (Inverting input of the differential amplifier 3) PCINT32 (Pin Change Interrupt 32)

OC2B / PCINT39 - port F Pin 7

OC2B: Timer / Counter 2 Compare Match Output B . Output selection by PMX1 Register control

PCINT39: Pin Change Interrupt 39

OC2A / T3 / PCINT38 - port F Pin 6

OC2A: Timer / Counter 2 Compare Match Output A . Output selection by PMX1 Register control

T3: Timer / Counter 3 External clock input

PCINT38: Pin Change Interrupt 38

0C1A / PCINT37 - port F Pin 5

OC1A: Timer / Counter 1 Compare Match Output A . Output selection by PMX0 Register control

PCINT37: Pin Change Interrupt 37

ICP3 / OC1B / PCINT36 - port F Pin 4

OC1B: Timer / Counter 1 of B Group match output. Output selection by PMX0 Register control

ICP3: Timer / Counter 3 External capture input

PCINT36: Pin Change Interrupt 36

OC3C / OC0B / PCINT35- port F Pin 3

OC0B: Timer / Counter 0 of B Group match output. Output selection by PMX0 Register control

OC3C: Timer / Counter 3 of C Group match output

PCINT35: Pin Change Interrupt 35

OC3B / PCINT34- port F Pin 2

OC3B: Timer / Counter 3 of B Group match output

PCINT34: Pin Change Interrupt 34

OC3A / PCINT33- port F Pin 1

OC3A: Timer / Counter 3 of B Group match output. Output selection by PMX1 Register control

PCINT33: Pin Change Interrupt 33

ADC9 / APN3 / PCINT32- port F Pin 0

ADC9: ADC External input channel mode 9

APN3: Inverting input of the differential amplifier 3

PCINT32: Pin Change Interrupt 32

Register Definition

port B Output Data Register - PORTB

PORTB - port B Output data register								
PORTB: 0x05 (0x25)				Defaults: 0x00				
Bits	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	PORTB	B Port output register group						

port B Direction Register - DDRB

DDRB - port B Direction Register								
DDRB: 0x04 (0x24)				Defaults: 0x00				
DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	DDB	port B Group direction control bit; 1 = Output, 0 = Entry						

port B Input Data Register - PINB

PINB - port B Input data register								
PINB: 0x03 (0x23)				Defaults: 0x00				
PINB	PINB7 PINB6 PINB5 PINB4 PINB3 PINB2 PINB1 PINB0							
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	PINB	B Port status register group. read PINB Direct access to the current state of the port; write PINBn Place 1 The flip PORTBn The output state						

port C Output Data Register - PORTC

PORTC - port C Output data register								
PORTC: 0x08 (0x28)				Defaults: 0x00				
PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	PORTC	C Port output register group						

port C Direction Register - DDRC

DDRC - port C Direction Register								
DDRC: 0x07 (0x27)				Defaults: 0x00				
DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	DDC	C Group port direction control bit; 1 = Output, 0 = Entry						

port C Input Data Register - PINC

PINC - port C Input data register								
PINB: 0x06 (0x26)				Defaults: 0x00				
PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	PINC	C Port status register group; read PINC Get the current status of the write port PINC Will flip the current output port						

port D Output Data Register - PORTD

PORTD - port D Output data register								
PORTD: 0x0B (0x2B)				Defaults: 0x00				
Bits	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								

[7: 0]	PORTD	D Port output register group

port D Direction Register - DDRD

DDRD - port D Direction Register								
DDRD: 0x0A (0x2A)				Defaults: 0x00				
DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	DDD	D Output port direction control register group						

port D Input Data Register - PIND

PIND - port D Input data register								
PIND: 0x09 (0x29)				Defaults: 0x00				
PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	PIND	D Group port status register read PIND Get the current port-level state to write PINDn for 1, Overturn PORTDn State of the corresponding bit						

port E Output Data Register - PORTE

PORTE - port E Output data register								
PORTE: 0x0E (0x2E)				Defaults: 0x00				
Bits	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	PORTE	E Port output register group						

port E Direction Register - DDRE

DDRE - port E Direction Register								
DDRE: 0x0D (0x2D)				Defaults: 0x00				
DDRE	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	DDE	E Port Direction control register group						

port E Input Data Register - PINE

PINE - port E Input data register								
PINE: 0x0C (0x2C)				Defaults: 0x00				
PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0

R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	PINE	E Group port status register read PINE Get the current port-level state to write PINEn for 1 Flip PORTEn Bit status						

port F Output register - PORTF

PINF - port F Input data register								
PORTF: 0x14 (0x34)				Defaults: 0x00				
Bits	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	PORTF	F Port group input port status register mode, the corresponding bit write 1 The open port of the internal pull-up output mode, corresponding to the write bit 1 The driven high						

port F Direction Control Register - DDRF

DDRF - port F Direction Control Register								
DDRF: 0x13 (0x33)				Defaults: 0x00				
Bits	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	DDRF	F Port Direction control register group						

port F Status Register - PINF

PINF - port F Status Register								
PINF: 0x12 (0x32)				Defaults: 0x00				
Bits	PINF7	PINF6	PINF5	PINF4	PINF3	PINF2	PINF1	PINF0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								
[7: 0]	PINF	F Group port status register read PINF Get port F The current level of the state PINFn write 1 Flip PORTFn State of the corresponding bit						

Drive control register Port - HDR

HDR0 - Port drive control register								
HDR: 0xE0				Defaults: 0x00				
Bit	-	-	HDR5	HDR4	HDR3	HDR2	HDR1	HDR0
R / W	-	-	R / W	R / W	R / W	R / W	R / W	R / W
Bit Definitions								

[7: 6]	-	Are reserved
5	HDR5	PF5 Output driver control; 1 = 80mA drive, 0 = 12mA drive
4	HDR4	PF4 Output driver control; 1 = 80mA drive, 0 = 12mA drive
3	HDR3	PF2 Output driver control; 1 = 80mA drive, 0 = 12mA drive
2	HDR2	PF1 Output driver control; 1 = 80mA drive, 0 = 12mA drive
1	HDR1	PD6 Output driver control; 1 = 80mA drive, 0 = 12mA drive
0	HDR0	PD5 Output driver control; 1 = 80mA drive, 0 = 12mA drive

Port multiplexing control register 0- PMX0

PMX0 - Port multiplexing control register 0								
PMX0: 0xEE				Defaults: 0x00				
Bit	WCE	C1BF4	C1AF5 C0BF3		C0AC0	SSB1	TXD6	RXD5
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit Definitions		
7	WCE	PMX0 / 1 Update enable control; update PMX0 / 1 Before register, you need to write WCE Bit 1 , After the 6 Complete cycles of the systems PMX0 / 1 Updates.
6	C1BF4	OC1B Auxiliary output control 1 = OC1B Output to PF4 0 = OC1B Output to PB2
5	C1AF5	OC1A Auxiliary output control 1 = OC1A Output to PF5 0 = OC1A Output to PB1
4	C0BF3	OC0B Auxiliary output control 1 = OC0B Output to PF3 0 = OC0B Output to PD5
3	C0AC0	OC0A Auxiliary output control 0C0A Output from the C0AC0 Bits and TCCR0B Register C0AS Jointly control: {C0AC0, C0AS} = 00 = OC0A Output to PD6 01 = 0C0A Output to PE4 10 = 0C0A Output to PC0 11 = OC0A While the output to PE4 with PC0
2	SSB1	SPSS Auxiliary output control 1 = SPSS Output to PB1 0 = SPSS Output to PB2
1	TXD6	Serial ports TXD Auxiliary output control 1 = TXD Output to PD6 , 0 = TXD Output to PD1
0	RXD5	Serial ports RXD Auxiliary Input Control 1 = RXD Input from PD5 , 0 = RXD Input from PD0

Port multiplexing control register 1- PMX1

PMX1 - Port multiplexing control register 1								
PMX1: 0xED				Defaults: 0x00				
Bit	-	-	-	-	-	C3AC	C2BF7	C2AF6
R / W	-	-	-	-	- R / W		R / W	R / W
Bit Definitions								
[7: 3]	-	Are reserved						
2	C3AC	OC3A Auxiliary output control 1 = OC3A Output to QFP48 / ACOP 0 = OC3A Output to PF1						
1	C2BF7	OC2B Auxiliary output control 1 = OC2B Output to PF7 0 = OC2B Output to PD3						
0	C2AF6	OC2A Auxiliary output control 1 = OC2A Output to PF6 0 = OC2A Output to PB3						
Instructions for use								
PMX0 / 1 Shared register update the protection control bits PMX0 [7], Update PMX1 When, please refer to PMX0 Register on PMX0 [7] The control instructions.								

Port multiplexing control register 2 - PMX2

PMX2 - Port multiplexing control register 2								
PMX2: 0xF0				Defaults: 0x00				
Bit	WCE	STSC1	STSC0	-	-	XIEN	E6EN	C6EN
R / W	R / W	R / W	R / W	-	- R / W		R / W	R / W
Bit Definitions								
[7]	WCE	PMX2 Update enable control; update PMX2 Before register, you need to write WCE Bit 1 , After the 6 Complete cycles of the systems PMX2 Updates.						
[6]	STSC1	Fast Crystal IO Start-up circuit is controlled by PMCR After enabling high-speed oscillator, STSC1 Automatically enabled. When the system clock is switched to the external high speed oscillator, STSC1 Automatic clear. Software can also be stable in the crystal clear manual STSC1, Closed oscillator start-up circuit, save power.						
[5]	STSC0	Low-speed oscillator IO Start-up circuit is controlled by PMCR After low speed oscillator is enabled, STSC0 Automatically enabled. When the system clock is switched to the external low speed oscillator, STSC0 Automatic clear. Software can also be stable in the crystal clear manual STSC0, Closed oscillator start-up circuit, save power.						
[4: 3]	-	Are reserved						
[2]	XIEN	Enable external clock input, you need to enable an external crystal						
[1]	E6EN Enable PE6 Universal IO Function; default PE6 for AVREF Features							
[0]	C6EN Enable PC6 Universal IO Function; default PC6 External reset input							

Pin Change Interrupt

- 40 A pin change interrupt source
- 5 Interrupt entry

Overview

Pin Change interrupted by PBn , PCn , PDn, PEn with PFn Pin trigger. As long as pin change interrupt is enabled, even if these pins are configured as outputs can also trigger an interrupt. This software can be used to generate an interrupt.

Any enabled PBn Flip pin triggers an interrupt pin level PCI0 , Enabled PCn Flip the trigger pin PCI1 , Enabled PDn Flip the trigger pin PCI2 , Enabled PEn Flip the trigger pin PCI3 . Each pin change interrupt enable respectively, by PCMSK0 ~ 4 Control register. All pin change interrupts are asynchronous detection, wake-up source can be used under certain sleep mode.

Register Definition

Pin Change Interrupt Register List

register	address	Defaults	description
PCICR	0x68	0x00	Pin Change Interrupt Control Register
PCIFR	0x3B	0x00	Pin change interrupt flag register
PCMSK0	0x6B	0x00	Pin change interrupt mask register 0
PCMSK1	0x6C	0x00	Pin change interrupt mask register 1
PCMSK2	0x6D	0x00	Pin change interrupt mask register 2
PCMSK3	0x73	0x00	Pin change interrupt mask register 3
PCMSK4	0x74	0x00	Pin change interrupt mask register 4

PCICR - Pin Change Interrupt Control Register

PCICR - Pin Change Interrupt Control Register								
address: 0x68					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	PCIE4	PCIE3	PCIE2	PCIE1	PCIE0
R / W	-	-	-	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 5	-	Reservations.
4	PCIE4	Pin change interrupt enable control bit 4 . When set PCIE4 Bit "1" And when the global interrupt enable pin change interrupt 4 It is enabled. Any enabled PFn Pin level change will have PCI4 Interrupted. PFn Pin interrupts can be independently by the PCMSK4 Control register. When set PCIE3 Bit "0" When, pin change interrupt 3 Prohibited.
3	PCIE3	Pin change interrupt enable control bit 3 . When set PCIE3 Bit "1" And when the global interrupt enable pin change interrupt 3 It is enabled.

		Any enabled PEn Pin level change will have PCI3 Interrupted. PEn Pin interrupts can be independently by the PCMSK3 Control register. When set PCIE3 Bit "0" When, pin change interrupt 3 Prohibited.
2	PCIE2	Pin change interrupt enable control bit 2 . When set PCIE2 Bit "1" And when the global interrupt enable pin change interrupt 2 It is enabled. Any enabled PDn Pin level change will have PCI2 Interrupted. PDn Pin interrupts can be independently by the PCMSK2 Control register. When set PCIE2 Bit "0" When, pin change interrupt 2 Prohibited.
1	PCIE1	Pin change interrupt enable control bit 1 . When set PCIE1 Bit "1" And when the global interrupt enable pin change interrupt 1 It is enabled. Any enabled PCn Pin level change will have PCI1 Interrupted. PCn Pin interrupts can be independently by the PCMSK1 Control register. When set PCIE1 Bit "0" When, pin change interrupt 1 Prohibited.
0	PCIE0	Pin change interrupt enable control bit 0 . When set PCIE0 Bit "1" And when the global interrupt enable pin change interrupt 0 It is enabled. Any enabled PBn Pin level change will have PCI0 Interrupted. PBn Pin interrupts can be independently by the PCMSK0 Control register. When set PCIE0 Bit "0" When, pin change interrupt 0 Prohibited.

PCIFR - Pin change interrupt flag register

PCIFR **- Pin change interrupt flag register**								
address: 0x3B					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	PCIF4	PCIF3	PCIF2	PCIF1	PCIF0
R / W	-	-	-	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 5	-	Reservations.
4	PCIF4	Pin change interrupt flag 4 . Any enabled PFn Pin level change will be set PCIF4 . when PCIE4 And Global are set when an interrupt, MCU It will jump to PCI4 Interrupt entry address. PFn Pin interrupts can be independently by the PCMSK4 Control register. Or to execute the interrupt service routine PCIF4 Write bit "1" Will be cleared PCIF4 Bit.
3	PCIF3	Pin change interrupt flag 3 . Any enabled PEn Pin level change will be set PCIF3 . when PCIE3 And Global are set when an interrupt, MCU It will jump to PCI3 Interrupt entry address. PEn Pin interrupts can be independently by the PCMSK3 Control register. Or to execute the interrupt service routine PCIF3 Write bit "1" Will be cleared PCIF3 Bit.
2	PCIF2	Pin change interrupt flag 2 . Any enabled PDn Pin level change will be set PCIF2 . when PCIE2 And Global are set when an interrupt, MCU It will jump to PCI2 Interrupt entry address. PDn Pin interrupts can be independently by the PCMSK2 Control register. Or to execute the interrupt service routine PCIF2 Write bit "1" Will be cleared PCIF2 Bit.
1	PCIF1	Pin change interrupt flag 1 .

		Any enabled PCn Pin level change will be set PCIF1 . when PCIE1 And Global are set when an interrupt, MCU It will jump to PCI1 Interrupt entry address. PCn Pin interrupts can be independently by the PCMSK1 Control register. Or to execute the interrupt service routine PCIF1 Write bit "1" Will be cleared PCIF1 Bit.
0	PCIF0	Pin change interrupt flag 0 . Any enabled PBn Pin level change will be set PCIF0 . when PCIE0 And Global are set when an interrupt, MCU It will jump to PCI0 Interrupt entry address. PBn Pin interrupts can be independently by the PCMSK0 Control register. Or to execute the interrupt service routine PCIF0 Write bit "1" Will be cleared PCIF0 Bit.

PCMSK0 - Pin change interrupt mask register 0

PCMSK0 **- Pin change mask register 0**								
address: 0x6B					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	PCINT7	Pin change enable mask 7 . When set PCINT7 Bit "1" Time, PB7 Pin change interrupt is enabled. PB7 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT7 Bit "0" Time, PB7 Pin change interrupts are disabled.
6	PCINT6	Pin change enable mask 6 . When set PCINT6 Bit "1" Time, PB6 Pin change interrupt is enabled. PB6 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT6 Bit "0" Time, PB6 Pin change interrupts are disabled.
5	PCINT5	Pin change enable mask 5 . When set PCINT5 Bit "1" Time, PB5 Pin change interrupt is enabled. PB5 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT5 Bit "0" Time, PB5 Pin change interrupts are disabled.
4	PCINT4	Pin change enable mask 4 . When set PCINT4 Bit "1" Time, PB4 Pin change interrupt is enabled. PB4 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT4 Bit "0" Time, PB4 Pin change interrupts are disabled.
3	PCINT3	Pin change enable mask 3 . When set PCINT3 Bit "1" Time, PB3 Pin change interrupt is enabled. PB3 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT3 Bit "0" Time, PB3 Pin change interrupts are disabled.
2	PCINT2	Pin change enable mask 2 . When set PCINT2 Bit "1" Time, PB2 Pin change interrupt is enabled. PB2 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT2 Bit "0" Time, PB2 Pin change interrupts are disabled.
1	PCINT1	Pin change enable mask 1 . When set PCINT1 Bit "1" Time, PB1 Pin change interrupt is enabled. PB1 Pin

		Changes in the level set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT1 Bit "0" Time, PB1 Pin change interrupts are disabled.
0	PCINT0	Pin change enable mask 0 . When set PCINT0 Bit "1" Time, PB0 Pin change interrupt is enabled. PB0 Level change on the pin will be set PCIF0 If the PCIE0 And a global interrupt bit set, will have PCI0 Interrupted. When set PCINT0 Bit "0" Time, PB0 Pin change interrupts are disabled.

PCMSK1 - Pin change interrupt mask register 1

***PCMSK1* - Pin change mask register 1**								
address: 0x6C					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	PCINT15	Pin change enable mask 15 . When set PCINT15 Bit "1" Time, PC7 Pin change interrupt is enabled. PC7 Level change on the pin will be set PCIF1 If the PCIE1 And a global interrupt bit set, will have PCI1 Interrupted. When set PCINT15 Bit "0" Time, PC7 Pin change interrupts are disabled.
6	PCINT14	Pin change enable mask 14 . When set PCINT14 Bit "1" Time, PC6 Pin change interrupt is enabled. PC6 Level change on the pin will be set PCIF1 If the PCIE1 And a global interrupt bit set, will have PCI1 Interrupted. When set PCINT14 Bit "0" Time, PC6 Pin change interrupts are disabled.
5	PCINT13	Pin change enable mask 13 . When set PCINT13 Bit "1" Time, PC5 Pin change interrupt is enabled. PC5 Level change on the pin will be set PCIF1 If the PCIE1 And a global interrupt bit set, will have PCI1 Interrupted. When set PCINT13 Bit "0" Time, PC5 Pin change interrupts are disabled.
4	PCINT12	Pin change enable mask 12 . When set PCINT12 Bit "1" Time, PC4 Pin change interrupt is enabled. PC4 Level change on the pin will be set PCIF1 If the PCIE1 And a global interrupt bit set, will have PCI1 Interrupted. When set PCINT12 Bit "0" Time, PC4 Pin change interrupts are disabled.
3	PCINT11	Pin change enable mask 11 . When set PCINT11 Bit "1" Time, PC3 Pin change interrupt is enabled. PC3 Level change on the pin will be set PCIF1 If the PCIE1 And a global interrupt bit set, will have PCI1 Interrupted. When set PCINT11 Bit "0" Time, PC3 Pin change interrupts are disabled.
2	PCINT10	Pin change enable mask 2 . When set PCINT10 Bit "1" Time, PC2 Pin change interrupt is enabled. PC2 Level change on the pin will be set PCIF1 If the PCIE1 And a global interrupt bit set, will have PCI1 Interrupted. When set PCINT10 Bit "0" Time, PC2 Pin change interrupt disabled

		stop.
1	PCINT9 Pin	change enable mask 1 . When set PCINT9 Bit "1" Time, PC1 Pin change interrupt is enabled. PC1 Level change on the pin will be set PCIF1 If the PCIE1 And a global interrupt bit set, will have PCI1 Interrupted. When set PCINT9 Bit "0" Time, PC1 Pin change interrupts are disabled.
0	PCINT8 Pin	change enable mask 0 . When set PCINT8 Bit "1" Time, PC0 Pin change interrupt is enabled. PC0 Level change on the pin will be set PCIF1 If the PCIE1 And a global interrupt bit set, will have PCI1 Interrupted. When set PCINT8 Bit "0" Time, PC0 Pin change interrupts are disabled.

PCMSK2 - Pin change interrupt mask register 2

PCMSK2 **- Pin change mask register 2**								
address: 0x6D					Defaults: 0x00			
Bits	7	6	5	4	3	2	1	0
	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name description
7	PCINT23 Pin change enable mask twenty three . When set PCINT23 Bit "1" Time, PD7 Pin change interrupt is enabled. PD7 Level change on the pin will be set PCIF2 If the PCIE2 And a global interrupt bit set, will have PCI2 Interrupted. When set PCINT23 Bit "0" Time, PD7 Pin change interrupts are disabled.
6	PCINT22 Pin change enable mask 6 . When set PCINT22 Bit "1" Time, PD6 Pin change interrupt is enabled. PD6 Level change on the pin will be set PCIF2 If the PCIE2 And a global interrupt bit set, will have PCI2 Interrupted. When set PCINT22 Bit "0" Time, PD6 Pin change interrupts are disabled.
5	PCINT21 Pin change enable mask twenty one . When set PCINT21 Bit "1" Time, PD5 Pin change interrupt is enabled. PD5 Level change on the pin will be set PCIF2 If the PCIE2 And a global interrupt bit set, will have PCI2 Interrupted. When set PCINT21 Bit "0" Time, PD5 Pin change interrupts are disabled.
4	PCINT20 Pin change enable mask 20 . When set PCINT20 Bit "1" Time, PD4 Pin change interrupt is enabled. PD4 Level change on the pin will be set PCIF2 If the PCIE2 And a global interrupt bit set, will have PCI2 Interrupted. When set PCINT20 Bit "0" Time, PD4 Pin change interrupts are disabled.
3	PCINT19 Pin change enable mask 19 . When set PCINT19 Bit "1" Time, PD3 Pin change interrupt is enabled. PD3 Level change on the pin will be set PCIF2 If the PCIE2 And a global interrupt bit set, will have PCI2 Interrupted. When set PCINT19 Bit "0" Time, PD3 Pin change interrupts are disabled.
2	PCINT18 Pin change enable mask 18 .

		When set PCINT18 Bit "1" Time, PD2 Pin change interrupt is enabled. PD2 Level change on the pin will be set PCIF2 If the PCIE2 And a global interrupt bit set, will have PCI2 Interrupted. When set PCINT18 Bit "0" Time, PD2 Pin change interrupts are disabled.
1	PCINT17 Pin change enable mask 17 .	When set PCINT17 Bit "1" Time, PD1 Pin change interrupt is enabled. PD1 Level change on the pin will be set PCIF2 If the PCIE2 And a global interrupt bit set, will have PCI2 Interrupted. When set PCINT17 Bit "0" Time, PD1 Pin change interrupts are disabled.
0	PCINT16 Pin change enable mask 16 .	When set PCINT16 Bit "1" Time, PD0 Pin change interrupt is enabled. PD0 Level change on the pin will be set PCIF2 If the PCIE2 And a global interrupt bit set, will have PCI2 Interrupted. When set PCINT16 Bit "0" Time, PD0 Pin change interrupts are disabled.

PCMSK3 - Pin change interrupt mask register 3

PCMSK3 **- Pin change mask register 3**								
address: 0x73					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	PCINT31	PCINT30	PCINT29	PCINT28	PCINT27	PCINT26	PCINT25	PCINT24
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name description
7	PCINT31 Pin change enable mask 31 . When set PCINT31 Bit "1" Time, PE7 Pin change interrupt is enabled. PE7 Level change on the pin will be set PCIF3 If the PCIE3 And a global interrupt bit set, will have PCI3 Interrupted. When set PCINT31 Bit "0" Time, PE7 Pin change interrupts are disabled.
6	PCINT30 Pin change enable mask 30 . When set PCINT30 Bit "1" Time, PE6 Pin change interrupt is enabled. PE6 Level change on the pin will be set PCIF3 If the PCIE3 And a global interrupt bit set, will have PCI3 Interrupted. When set PCINT30 Bit "0" Time, PE6 Pin change interrupts are disabled.
5	PCINT29 Pin change enable mask 39 . When set PCINT29 Bit "1" Time, PE5 Pin change interrupt is enabled. PE5 Level change on the pin will be set PCIF3 If the PCIE3 And a global interrupt bit set, will have PCI3 Interrupted. When set PCINT29 Bit "0" Time, PE5 Pin change interrupts are disabled.
4	PCINT28 Pin change enable mask 28 . When set PCINT28 Bit "1" Time, PE4 Pin change interrupt is enabled. PE4 Level change on the pin will be set PCIF3 If the PCIE3 And a global interrupt bit set, will have PCI3 Interrupted. When set PCINT28 Bit "0" Time, PE4 Pin change interrupts are disabled.
3	PCINT27 Pin change enable mask 27 .

		When set PCINT27 Bit "1" Time, PE3 Pin change interrupt is enabled. PE3 Level change on the pin will be set PCIF3 If the PCIE3 And a global interrupt bit set, will have PCI3 Interrupted. When set PCINT27 Bit "0" Time, PE3 Pin change interrupts are disabled.
2	PCINT26	Pin change enable mask 26 . When set PCINT26 Bit "1" Time, PE2 Pin change interrupt is enabled. PE2 Level change on the pin will be set PCIF3 If the PCIE3 And a global interrupt bit set, will have PCI3 Interrupted. When set PCINT26 Bit "0" Time, PE2 Pin change interrupts are disabled.
1	PCINT25	Pin change enable mask 25 . When set PCINT25 Bit "1" Time, PE1 Pin change interrupt is enabled. PE1 Level change on the pin will be set PCIF3 If the PCIE3 And a global interrupt bit set, will have PCI3 Interrupted. When set PCINT25 Bit "0" Time, PE1 Pin change interrupts are disabled.
0	PCINT24	Pin change enable mask twenty four . When set PCINT24 Bit "1" Time, PE0 Pin change interrupt is enabled. PE0 Level change on the pin will be set PCIF3 If the PCIE3 And a global interrupt bit set, will have PCI3 Interrupted. When set PCINT24 Bit "0" Time, PE0 Pin change interrupts are disabled.

PCMSK4 - Pin change interrupt mask register 4

PCMSK4 **- Pin change mask register 4**								
address: 0x74					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	PCINT39	PCINT38	PCINT37	PCINT36	PCINT35	PCINT34	PCINT33	PCINT32
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	PCINT39	Pin change enable mask 39 . When set PCINT39 Bit "1" Time, PF7 Pin change interrupt is enabled. PF7 Level change on the pin will be set PCIF4 If the PCIE4 And a global interrupt bit set, will have PCI4 Interrupted. When set PCINT39 Bit "0" Time, PF7 Pin change interrupts are disabled.
6	PCINT38	Pin change enable mask 38 . When set PCINT38 Bit "1" Time, PF6 Pin change interrupt is enabled. PF6 Level change on the pin will be set PCIF4 If the PCIE4 And a global interrupt bit set, will have PCI4 Interrupted. When set PCINT38 Bit "0" Time, PF6 Pin change interrupts are disabled.
5	PCINT37	Pin change enable mask 37 . When set PCINT37 Bit "1" Time, PF5 Pin change interrupt is enabled. PF5 Level change on the pin will be set PCIF4 If the PCIE4 And a global interrupt bit set, will have PCI4 Interrupted. When set PCINT37 Bit "0" Time, PF5 Pin change interrupts are disabled.
4	PCINT36	Pin change enable mask 36 .

		When set PCINT36 Bit "1" Time, PF4 Pin change interrupt is enabled. PF4 Level change on the pin will be set PCIF4 If the PCIE4 And a global interrupt bit set, will have PCI4 Interrupted. When set PCINT36 Bit "0" Time, PF4 Pin change interrupts are disabled.
3	PCINT35	Pin change enable mask 35 . When set PCINT35 Bit "1" Time, PF3 Pin change interrupt is enabled. PF3 Level change on the pin will be set PCIF4 If the PCIE4 And a global interrupt bit set, will have PCI4 Interrupted. When set PCINT35 Bit "0" Time, PF3 Pin change interrupts are disabled.
2	PCINT34	Pin change enable mask 34 . When set PCINT34 Bit "1" Time, PF2 Pin change interrupt is enabled. PF2 Level change on the pin will be set PCIF4 If the PCIE4 And a global interrupt bit set, will have PCI4 Interrupted. When set PCINT34 Bit "0" Time, PF2 Pin change interrupts are disabled.
1	PCINT33	Pin change enable mask 33 . When set PCINT33 Bit "1" Time, PF1 Pin change interrupt is enabled. PF1 Level change on the pin will be set PCIF4 If the PCIE4 And a global interrupt bit set, will have PCI4 Interrupted. When set PCINT33 Bit "0" Time, PF1 Pin change interrupts are disabled.
0	PCINT32	Pin change enable mask 32 . When set PCINT31 Bit "1" Time, PF0 Pin change interrupt is enabled. PF0 Level change on the pin will be set PCIF4 If the PCIE4 And a global interrupt bit set, will have PCI4 Interrupted. When set PCINT32 Bit "0" Time, PF0 Pin change interrupts are disabled.

Timer / Counter 0 (TMR0)

- 8 Bit counter
- Two independent comparing unit
- The counter is automatically cleared when compare match occurs and automatically loads
- No disturb pulse phase correction PWM Export
- Frequency generator
- External event counter
- 10 Bit clock prescaler
- Overflow and Compare Match Interrupt
- With dead-time control
- 6 Selectable trigger source automatically shut down PWM Export
- Generating a high-resolution high-speed (high-speed clock mode 500KHz @ 7Bit) PWM

Outline

TC0 Is a common 8 Bit timer counter module support PWM Output waveform can be generated accurately. TC0 contain 1 Count clock generation unit, 1 More 8 Bit counter, and a waveform generation mode control unit 2 Output comparison unit. Simultaneously, TC0 With TC1 Common 10 Bit prescaler, can be used independently 10 Bit prescaler. The system clock prescaler clkio Or high-speed clock rcm2x (internal 32M RC Clock oscillator output rc32m of 2 Frequency) for frequency-dividing the count clock Clkt0 . Waveform generating mode generates the control unit controls the operation mode of the counter and comparing the output waveform. Depending on the mode of operation, a counter for counting each clock Clkt0 Cleared, incremented or decremented. Clkt0 It may be generated by an internal clock or an external clock source. When the count value of the counter TCNT0 It reached its maximum value (equal to the maximum value 0xFF Or output compare register OCR0A ,defined as TOP , The maximum value of the definition MAX When to distinguish), the counter is cleared or decremented. When the count value of the counter TCNT0 Reaches a minimum value (equal to

0x00 ,defined as BOTTOM), The counter will be incremented by one operation. When the count value of the counter TCNT0 Arrivals OCR0A / OCR0B When, also referred to compare match, set or cleared by the output signal of the comparison OC0A / OC0B To produce PWM Waveform. When the enable insertion of dead time, the dead time is set (DTR0 Count clock number corresponding to the register) will be inserted into the generated PWM Waveform. Software by clearing COM0A / COM0B Bit close to zero
OC0A / OC0B The waveform output, or set the respective trigger source, when a triggering event occurs automatically cleared by hardware
COM0A / COM0B Bit to close OC0A / OC0B The waveform output.

Count clock can be internal or external clock source to generate, select, and divided by the selected frequency clock source located TCCR0B Register CS0 Control bits, see the detailed description TC0 with TC1 Prescaler section.

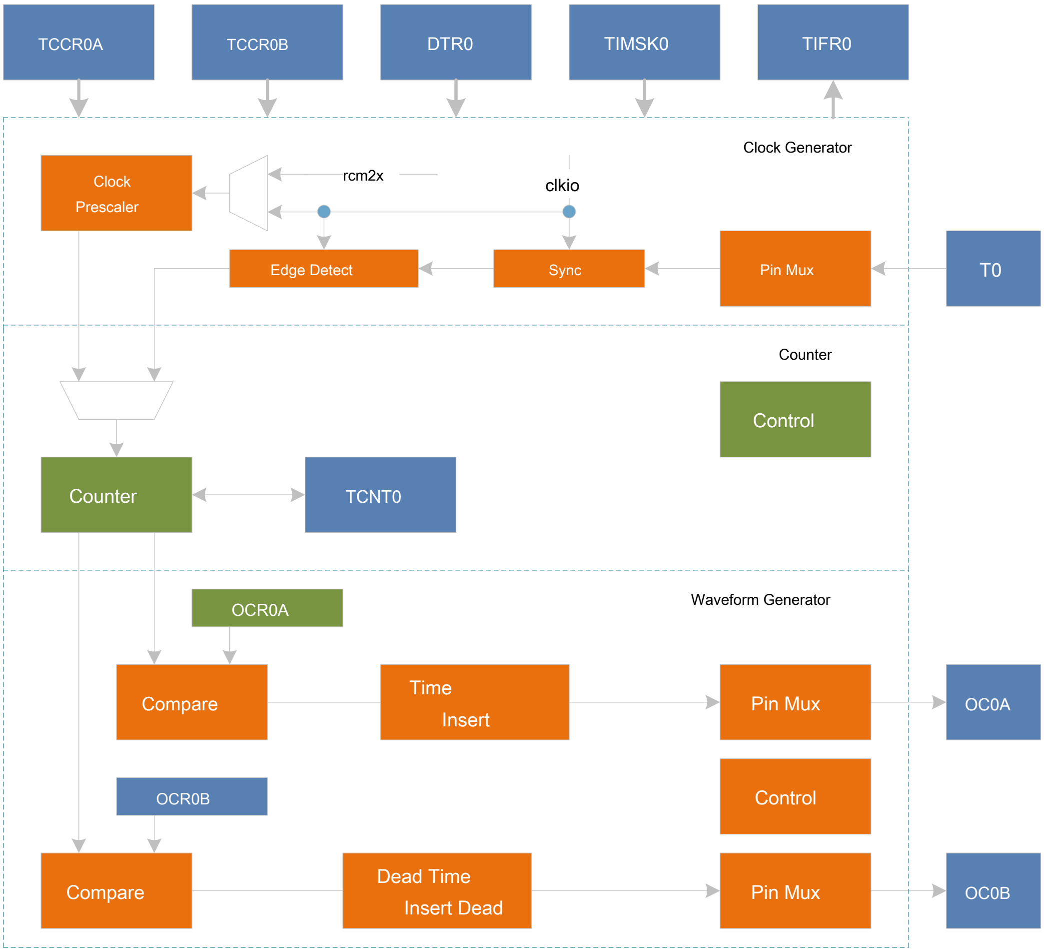
Length counter is 8 Bit, supporting bi-directional counter. I.e., Waveform generating mode by the operation mode counter is located TCCR0A with TCCR0B Register WGM0 Bit to control. Depending on the mode of operation, a counter for counting each clock Clkt0 Cleared, incremented or decremented. When an overflow occurs count Located TIFR0 Counter register overflow flag TOV0 Bit is set. When the interrupt is enabled may produce TC0 Counter overflow interrupt.

Count value output of the comparison unit TCNT0 And output compare register OCR0A with OCR0B The value, when TCNT0 equal OCR0A or OCR0B When referred to as Comparative match occurs, it is located TIFR0 Output compare flag register OCF0A or OCF0B Bit is set. When the interrupt is enabled may produce TC0 Output Compare match interrupt. It should be noted that, in the PWM Under work mode, OCR0A with OCR0B Register is double buffered. In the normal mode and

CTC Mode, double buffering function failure. When the count reaches maximum or minimum value of the buffer register is updated simultaneously comparing register OCR0A with OCR0B Go. See section describes the operating modes.

Waveform generator and comparator generates a mode control output waveform control pattern matching and Comparative counter overflow signal to generate an output waveform comparison OC0A with OC0B . DETAILED generation mode and the operation mode register, see section below. We should compare the output signal waveform OC0A with OC0B Corresponding to the output pin, the data direction register must be set to the output pin.

The figure below shows TC0 The internal structure of FIG. TC0 contain 1 Count clock generation unit, 1 More 8 Bit counter, 2 And output the comparison unit 2 Waveform generation control unit.



TC0 Structure chart

Operating mode

Timing counter 0 There are four different operating modes, including normal mode (Normal), Cleared on compare match (CTC) Mode, fast pulse width modulation (FPWM) Mode and a phase correction pulse width modulation (PCPWM) Mode, the mode control bits generated by the waveform WGM0 [2: 0] To choose. The following four modes will be described specifically. Since there are two separate output of the comparison unit, respectively "A" with "B" Represented by lowercase "X" To represent the two channel outputs the comparison unit.

Normal mode

Normal mode timer counter is the simplest mode of operation, this time waveform generation mode control bit WGM0 [2: 0] = 0 Count maximum value TOP for MAX (0xFF). In this mode, a counting mode for each clock count plus an increment, when the counter reaches TOP After the spill back BOTTOM Re-start accumulating. The count value TCNT0 The same count clock becomes zero set timer counter's overflow flag TOV0 . In this mode TOV0 The first sign is like 9 Count bit, but will only be set is not cleared. Overflow interrupt service routine will automatically clear TOV0 Logos, software can use it to improve the resolution of the timer counter. Normal mode is not to be considered a special case, a new count value can be written at any time. Set up OC0x Pin data direction register as an output a comparison signal to obtain an output OC0x Waveform. when COM0x = 1

When, flips compare match OC0x Signal, in this case the frequency waveform may be calculated using the following formula:

$$f_{oc0xnormal} = f_{sys} / (2 * N * 256)$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024).

Output Compare unit can be used to generate interrupts, but does not recommend the use of interrupts in the normal mode, it will take up too much CPU time.

CTC mode

Set up WGM0 [2: 0] = 2 When the timer counter 0 enter CTC Max mode, counting TOP for OCR0A . In this mode, a counting mode for each clock count plus an increment, when the value of the counter TCNT0 equal TOP When the counter is cleared. OCR0A It defines the maximum count, i.e., the resolution of the counter. This mode allows the user to easily control the frequency of the compare match output also simplifies the operation of the external event count. When the counter reaches a maximum count, an output compare match flag OCF0 Is set, an interrupt will be generated when the corresponding interrupt enable bit is set. Can be updated in the interrupt service routine OCR0A I.e., the maximum count register. In this mode

OCR0A Do not use double buffering, the counter prescaler to work under no or very low prescaler will be updated as close to the maximum value of the minimum time to be careful. If you write OCR0A The value is less than the time TCNT0 When the value of the counter will miss the compare match. Before a match occurs the next comparison, the first counter had counted to TOP And then from BOTTOM
To start counting OCR0A value. And normal mode, as the count value back BOTTOM The count clock in the set TOV0 Mark. Set up OC0x Pin data direction register as an output a comparison signal to obtain an output OC0x Waveform. when COM0x = 1
When, flips compare match OC0x Signal, in this case the frequency waveform may be calculated using the following formula:

$$f_{oc0xctc} = f_{sys} / (2 * N * (1 + OCR0x))$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024). As can be seen from the formula, when set OCR0A for 0x0 And when no prescaler, allowing for maximum frequency $f_{sys} / 2$ The output waveform.

fast PWM mode

Set up WGM0 [2: 0] = 3 or 7 When the timer counter 0 Enter the fast PWM Mode, can be used to generate high frequency
PWM Waveform, the counter maximum value TOP Respectively MAX (0xFF)or OCR0x . fast PWM Patterns and other PWM Except that it is a one-way mode operation. Counter from the minimum 0x00 To accumulate TOP Then came back BOTTOM Re-count. When the count value TCNT0 Arrivals OCR0x or BOTTOM , The output signal of the comparison OC0x It will be set or cleared, depending on the comparison output mode COM0x Setting, as detailed register description. Since the one-way operation, fast PWM Operating frequency of the phase correction mode is employed bi-directionally operable PWM Double mode. It makes the fast frequency PWM Mode is suitable for power regulation, rectification and DAC application. High-frequency signal can be reduced external components (capacitors, inductors) in size, thereby reducing system cost.

When the count value reaches the maximum value, the timer counter overflow flag TOV0 It will be set, and updates the value of the compare buffer

The comparison value. If enabled, the interrupt service routine can be updated relatively buffer OCR0x register. Set up OC0x Pin data direction register as an output a comparison signal to obtain an output OC0x Waveform. Frequency of the waveform following formula can be calculated:

$$f_{oc0xfpwm} = f_{sys} / (N * (1 + TOP))$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024). when TCNT0 with OCR0x Compare match, the waveform generator to set (clear) OC0x Signal, when TCNT0 When cleared, the waveform generator will be cleared (set) OC0x Signal in order to produce PWM wave. thus OCR0x The extremes will produce special PWM Waveform. when OCR0x Set as 0x00 , The output of PWM For each (1 + TOP) There is a clock count of a narrow spike. when OCR0x When set to the maximum value, the output waveform for sustained high or low.

Phase correction PWM mode

When set WGM0 [2: 0] = 1 or 5 When the timer counter 0 Enter phase correction PWM Max mode, counting TOP Respectively MAX (0xFF)or OCR0A . Bidirectional counter operation by BOTTOM Increments to TOP And then descending to BOTTOM , Then repeat this operation. Count reaches TOP with BOTTOM Have to change direction when the count value TOP or BOTTOM On average only stay a count clock. In the process increments or decrements the count value TCNT0 versus OCR0x Match, the comparison signal output OC0x It will be set or cleared, depending on the comparison output mode COM0x setting. Compared with the one-way operation, bidirectional operation obtainable maximum operation frequency, but its excellent symmetry is more suitable for motor control. Phase correction PWM Mode, when the count reaches BOTTOM When set TOV0 Flag when the count reaches TOP When the buffer is updated to compare the value of the comparison value. If enabled, the interrupt service routine can be updated relatively buffer OCR0x register. Set up OC0x Pin data direction register as an output a comparison signal to obtain an output OC0x Waveform. Frequency of the waveform following formula can be calculated:

$$f_{oc0xpcpwm} = f_{sys} / (N * TOP * 2)$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024). In up-counting process, when TCNT0 versus OCR0x Match, the waveform generator will be cleared (set) OC0x signal. In the process of counting down, when TCNT0 versus OCR0x When the match is set to the waveform generator (clear) OC0x signal. thus OCR0x The extremes will produce a special PWM wave. when OCR0x When set to the maximum or minimum value, OC0x Output signal will remain low or high.

In order to ensure that the output PWM Wave symmetry of both sides of the minimum value, a compare match does not occur, there will be two cases flipping OC0x signal. The first case is when OCR0x Value by the maximum value 0xFF When changes to other data. when OCR0x The maximum value, the count value reaches the maximum, OC0x The same output result of the comparison in the previous match count in descending, i.e. holding OC0x constant. At this value will be updated relatively new OCR0x The value of the (non 0xFF), OC0x Value will remain set until the comparison match occurs ascending counting flip. at this time OC0x Signal to the minimum value as the center is not symmetrical, requiring the TCNT0 Flip reaches the maximum value OC0x Signal, namely when the comparator inverting no match occurs OC0x A first of the signal. The second case is when TCNT0 From the ratio OCR0x Counting high value, and thus will miss the compare match, thereby causing an asymmetric situation generated. Also you need to flip OC0x Signal to achieve symmetry of both sides of the minimum.

PWM Automatically shutdown and restart of output

When set TCCR0A Register DOC0x Bit is high, PWM When auto-off feature is enabled, the trigger condition is met, the hardware clears the corresponding output COM0x Bits, PWM output signal OC0x And its output pin is disconnected, the switching to a common IO Output achieved PWM Automatically shut down the output. At this time, the state of the output pin by a general IO To control the output.

PWM Off automatically after the output is enabled, which also need to set the trigger conditions from TCCR0C Register DSX0n Bits to select trigger source. Triggered by an analog comparator interrupt, external interrupt, the interrupt pin change and the timer overflow interrupt, please refer to the specific circumstances TCCR0C Register description. Or when a certain trigger source is selected as the trigger condition, in which the interrupt flag is set at the same time, the hardware will be cleared COM0x Bit to close PWM Output.

In the event of a triggering event closed PWM After the output, the timer module is no corresponding interrupt flag, the software needs to know the trigger and the trigger event by source interrupt flag read.

when PWM When the output is automatically switched off and the need to restart output again, the software only needs to be reset COM0x Position to switch OC0x Signal is output to the corresponding pin. It should be noted, occurs automatically shut down after the timer did not stop working,
OC0x State of the signal has also been updated. After the software or compare match timer overflows, then set COM0x Bit output OC0x Signal, so you can get a clear PWM Output state.

Dead-time control

Set up DTEN0 Bit "1" When inserting the dead time function is enabled, OC0A with OC0B The output waveform will B Deadtime comparator output channel waveform based on the generated set of insertion, the length of time of DTR0 Register count clock number corresponding to the time value. As shown below, OC0A with OC0B Deadtime insertion are based channel B Comparing the output waveform as a reference. when COM0A with COM0B The same "2" or "3" Time, OC0A The polarity of the waveform OC0B The waveform of the same polarity, when COM0A with COM0B Respectively "2" or "3" Time, OC0A The waveform OC0B Opposite polarity waveform.

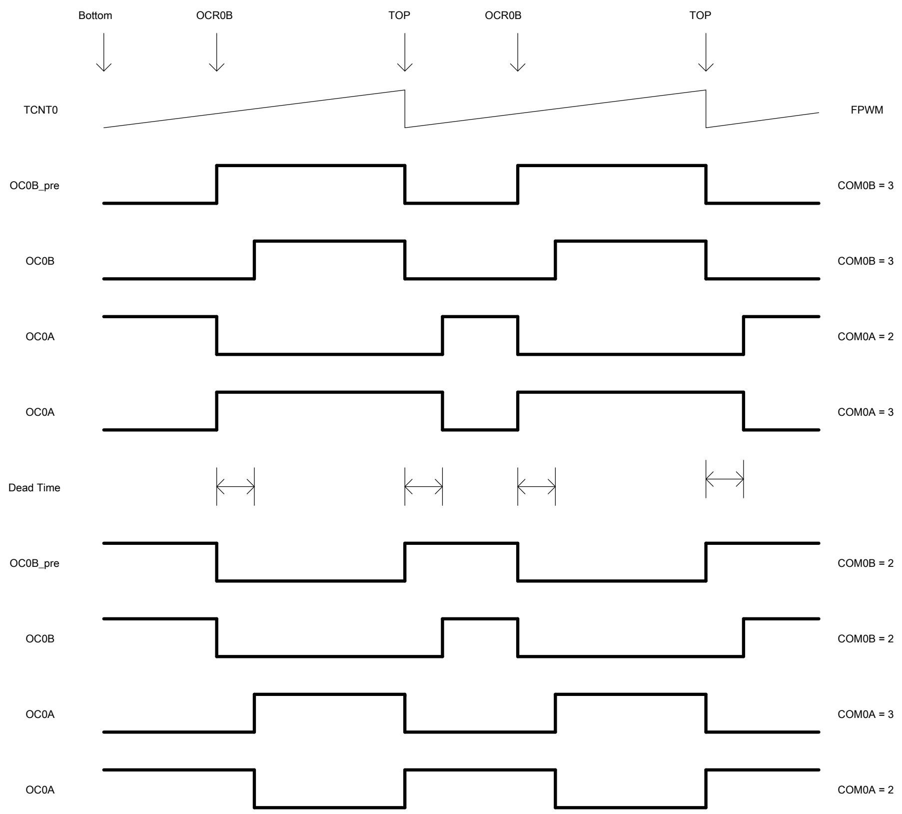


Figure 1 FPWM Mode TC0 Dead-time control

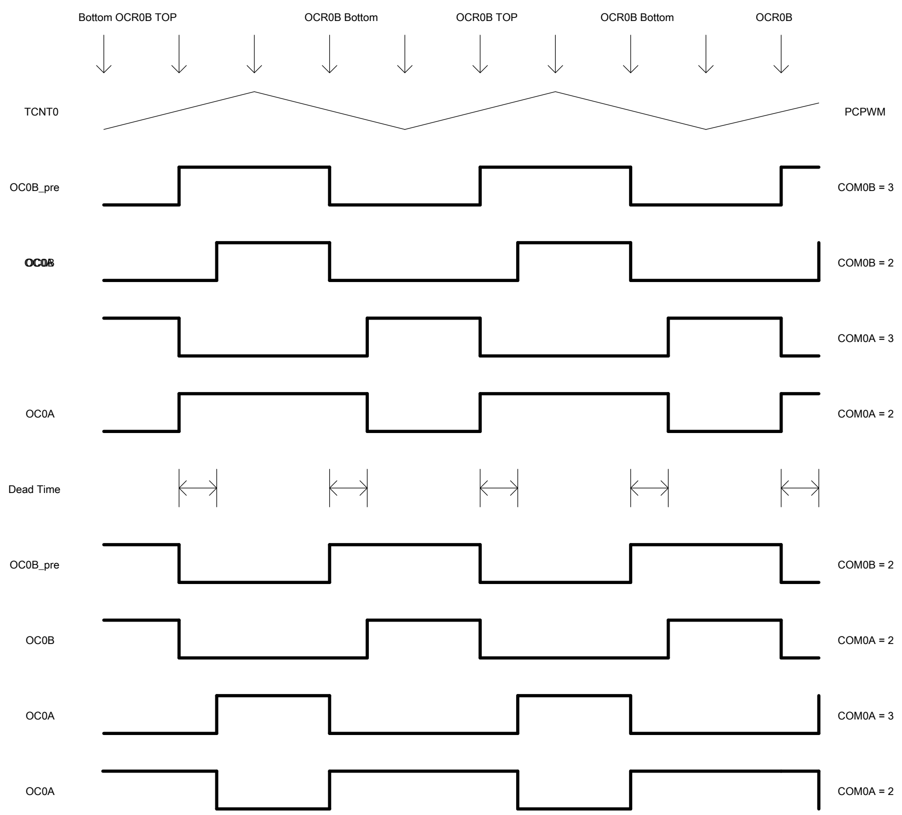


Figure 2 PCPWM Mode TC0 Dead-time control

Set up DTEN0 Bit "0" When inserting the dead time function is disabled, OC0A with OC0B The waveform of the output waveform generated by each comparator output.

High-speed clock mode

The high-speed clock mode using a higher frequency clock count as the clock source for generating higher speed and higher resolution PWM Waveform. This is achieved by the internal clock frequency 32M RC Oscillator output clock rc32m get on 2 Frequency doubling to produce a. Thus, before entering the high-frequency mode, the need to enable the internal 32M RC Oscillator frequency function, i.e. set TCKCSR Register F2XEN Position, and wait for a certain time until the output frequency of the clock signal stable. May then be set TCKCSR of TC2XS0 Timer counter bit to enter the high-speed clock mode.

In this mode, the system clocks are asynchronous with the high-speed clock, and some register (see TC0 Register list) working in the high-speed clock domain, and therefore, such a configuration register and reading is asynchronous, note operation.

No special requirements of high speed clock domain registers in read and write non-continuous, and continuous read and write operations, wait for a system clock, according to the following steps:

1) Write register A ;

2) Waiting for a system clock (NOP Clock register operating system or under);

3) Read or write register A or B .

4) Waiting for a system clock (NOP Registers in the clock or operating system).

When the high-speed clock domain register read operation, in addition to TCNT0 The registers are directly readable outside, when the counter is still counting, TCNT0 The value changes with a high speed clock, pause counter (provided CS0 Zero) then read TCNT0 Value.

Register Definition

TC0 Register List

register	address	Defaults	description
TCCR0A *	0x44	0x00	TC0 Control register A
TCCR0B *	0x45	0x00	TC0 Control register B
TCNT0 *	0x46	0x00	TC0 Count value register
OCR0A *	0x47	0x00	TC0 Output Compare Register A
OCR0B *	0x48	0x00	TC0 Output Compare Register B
DSX0 *	0x49	0x00	TC0 Trigger source control register
DTR0 *	0x4F	0x00	TC0 Dead time register
TIMSK0	0x6E	0x00	Timing counter 0 Interrupt mask register
TIFR0	0x35	0x00	Timing counter 0 Interrupt Flag Register
TCKCSR	0xEC	0x00	TC Clock control and status register

[Note] with "*" The register operation at high speed clock and a system clock domains, not with "*" The working register only at the system clock domain.

TC0 Control register A- TCCR0A

TCCR0A **-** TC0 Control register A								
address: 0x44						Defaults: 0x00		
Bit	7	6	5	4	3	2	1	0
	COM0A1	COM0A0	COM0B1	COM0B0	DOC0B	DOC0A	WGM01	WGM00
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	COM0A1	TC0 Compare match A High-output mode control. COM0A1 with COM0A0 Together comprise comparison output mode control COM0A [1: 0] To control OC0A The output waveform. in case COM0A of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC0A Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM0A The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
6	COM0A0	TC0 Compare match A Low output mode control. COM0A0 with COM0A1 Together comprise comparison output mode control COM0A [1: 0] To control OC0A The output waveform. in case COM0A of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC0A Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM0A The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
5	COM0B1	TC0 Compare match B High-output mode control. COM0B1 with COM0B0 Together comprise comparison output mode control COM0B [1: 0] To control OC0B The output waveform. in case COM0B of 1 Position or 2 Bits are set,

		Compare output waveform occupies OC0B Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM0B The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
4	COM0B0	TC0 Compare match B Low output mode control. COM0B0 with COM0B1 Together comprise comparison output mode control COM0B [1: 0] To control OC0B The output waveform. in case COM0B of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC0B Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM0B The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
3	DOC0B	TC0 Close control of the high output of the comparator is enabled. when DOC0B Bit "1" It is triggered off the output comparison signal source OC0B It is enabled. When a trigger event occurs, the hardware is automatically cleared COM0B Position, close OC0B The waveform output. By setting software COMB May re-open PWM Output. when DOC0B Bit "0" It is triggered off the output comparison signal source OC0B Prohibited.
2	DOC0A	TC0 Close control of the low output of the comparator is enabled. When set DOC0A Bit "1" It is triggered off the output comparison signal source OC0A It is enabled. When a trigger event occurs, the hardware automatically shut down OC0A The waveform output. When set DOC0A Bit "0" It is triggered off the output comparison signal source OC0A Prohibited. When a trigger event occurs, will not close OC0A The waveform output.
1	WGM01	TC0 Waveform generation mode control bits. WGM01 with WGM00 , WGM02 Together form waveform generation mode control WGM0 [2: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
0	WGM00	TC0 Waveform generation mode control low. WGM00 with WGM01 , WGM02 Together form waveform generation mode control WGM0 [2: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.

TC0 Control register B- TCCR0B

TCCR0B **-** TC0 Control register B								
address: 0x45					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	FOC0A	FOC0B	OC0AS	DTEN0	WGM02	CS02	CS01	CS00
R / W	W	W	W / R	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	FOC0A	TC0 Force Output Compare A Control bit. In non PWM Mode, the force output by comparing bits FOC0A write "1" The way to compare match. Forcing compare match will not set OCF0A Flag or reload or clear the timer, but the output pin OC0A Will be in accordance with COM0A It sets the appropriate update, just compare match had really happened. Read FOC0A The return value is always zero.
6	FOC0B	TC0 Force Output Compare B Control bit.

		In non PWM Mode, the force output by comparing bits FOC0B write "1" The way to compare match. Forcing compare match will not set OCF0B Flag or reload or clear the timer, but the output pin OC0B Will be in accordance with COM0B It sets the appropriate update, just compare match had really happened. Read FOC0B The return value is always zero.
5	OC0AS	OC0A Output port selection control bits. When set OC0AS Bit "0" Time, OC0A The waveform from the pin PD6 Output; when set OC0AS Bit "1" Time, OC0A The waveform from the pin PE4 Output (QFP32 Package valid).
4	DTEN0	TC0 Dead time enable control bit. When set DTEN0 Bit "1" When, enabling dead-time insertion. OC0A with OC0B They are in B Insertion of dead time waveform of the comparison output is generated based on the channel, inserted by the dead time interval DTR0 Register corresponding to the count time determined. OC0A The polarity of the output waveform COM0 with COM0B The correspondence between the decision, see OC0A After insertion of dead time waveform table shown polarity. When set DTEN0 Bit "0" Is prohibited dead-time insertion, OC0A with OC0B Comparing each of the generated output waveforms.
3	WGM02	TC0 Waveform generation mode control high. WGM02 with WGM00 , WGM01 Together form waveform generation mode control WGM0 [2: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
2	CS02	TC0 Clock control high. For selecting a timing counter 0 The clock source.
1	CS01	TC0 Clock selection control bits. For selecting a timing counter 0 The clock source.
0	CS00	TC0 Clock control low. For selecting a timing counter 0 The clock source.

CS0 [2: 0]	description
0	No clock source, stops counting
1	clk_{sys}
2	clk_{sys} / 8 From prescaler
3	clk_{sys} / 64 From prescaler
4	clk_{sys} / 256 From prescaler
5	clk_{sys} / 1024 From prescaler
6	External Clock T0 Pin, falling edge
7	External Clock T0 Pin on the rising edge

The following table non PWM Mode (ie, normal mode and CTC Mode), the comparison output of the comparator mode control output waveform.

COM0x [1: 0]	description
0	OC0x Disconnect, GM IO Port operations
1	Flip compare match OC0x signal
2	Clear compare match OC0x signal
3	When set compare match OC0x signal

The following table fast PWM Mode mode control comparator output waveform of the output comparator.

COM0x [1: 0]	description
0	OC0x Disconnect, GM IO Port operations
1	Retention
2	Clear compare match OC0x Signal is set to match the maximum value OC0x signal
3	When set compare match OC0x Signal is cleared when the maximum matching OC0x signal

The following table shows the comparison output of the phase correction mode the mode control output of the comparator waveform.

COM0x [1: 0]	description
0	OC0x Disconnect, GM IO Port operations
1	Retention
2	Cleared when the match count comparator ascending OC0x Down signal, compare match count descending When set OC0x signal
3	Ascending count comparator match the set OC0x Down signal, compare match count descending When cleared OC0x signal

The following table is a waveform generation mode control.

WGM0 [2: 0]	Operating mode	TOP Value	update OCR0X Time	set TOV0 time
0	Normal	0xFF	immediately	MAX
1	PCPWM	0xFF	TOP	BOTTOM
2	CTC	OCR0A	immediately	MAX
3	FPWM	0xFF	TOP	MAX
4	Retention	-	-	-
5	PCPWM	OCR0A	TOP	BOTTOM
6	Retention	-	-	-
7	FPWM	OCR0A	TOP	TOP

The following table is a dead time enabled OC0A Polarity control signal output waveform.

Dead time enabled mode OC0A Polarity control signal output waveform

DTEN0	COM0A [1: 0]	COM0B [1: 0]	description
0	-	-	OC0A Signal polarity by the OC0A Compare output mode control
1	0	-	OC0A Disconnect, GM IO Port operations
1	1	-	Retention
1	2	2	OC0A Signals OC0B Signals with the same polarity
		3	OC0A Signals OC0B Opposite signal polarity
1	3	2	OC0A Signals OC0B Opposite signal polarity
		3	OC0A Signals OC0B Signals with the same polarity

【note】:

OC0B The polarity of the signal output from the waveform OC0B Compare output control mode, so that the same can not dead time mode.

TC0 Control register C - TCCR0C

TCCR0C - ***TC0 Control register C***								
address: 0x49					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	DSX07	DSX06	DSX05	DSX04	-	-	DSX01	DSX00
R / W	R / W	R / W	R / W	R / W	-	-	R / W	R / W

Bit	Name	description
7	DSX07	TC0 Select the trigger source control enables the first 7 Bit. When set DSX07 Bit "1" Time, TC1 As the output of the comparator is off the overflow signal waveform OC0A / OC0B The trigger source is enabled. when DOC0A / DOC0B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC0A / OC0B The waveform output. When set DSX07 Bit "0" Time, TC1 As the output of the comparator is off the overflow signal waveform OC0A / OC0B The trigger source is prohibited.
6	DSX06	TC0 Select the trigger source control enables the first 6 Bit. When set DSX06 Bit "1" Time, TC2 As the output of the comparator is off the overflow signal waveform OC0A / OC0B The trigger source is enabled. when DOC0A / DOC0B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC0A / OC0B The waveform output. When set DSX06 Bit "0" Time, TC2 As the output of the comparator is off the overflow signal waveform OC0A / OC0B The trigger source is prohibited.
5	DSX05	TC0 Select the trigger source control enables the first 5 Bit. When set DSX05 Bit "1" When, pin change 0 As a comparison output signal waveform is off OC0A / OC0B The trigger source is enabled. when DOC0A / DOC0B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC0A / OC0B The waveform output. When set DSX05 Bit "0" When, pin change 0 As a comparison output signal waveform is off OC0A / OC0B The trigger source is prohibited.
4	DSX04	TC0 Select the trigger source control enables the first 4 Bit. When set DSX04 Bit "1" When the external interrupt 0 As a comparison output signal waveform is off OC0A / OC0B The trigger source is enabled. when DOC0A / DOC0B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC0A / OC0B The waveform output. When set DSX04 Bit "0" When the external interrupt 0 As a comparison output signal waveform is off OC0A / OC0B The trigger source is prohibited.
3: 2	-	Are reserved
1	DSX01	TC0 Select the trigger source control enables the first 1 Bit. When set DSX01 Bit "1" When, analog comparator 1 As a comparison output signal waveform is off OC0A / OC0B The trigger source is enabled. when DOC0A / DOC0B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC0A / OC0B The waveform output.

		When set DSX01 Bit "0" When, analog comparator 1 As a comparison output signal waveform is off OC0A / OC0B The trigger source is prohibited.
0	DSX00	TC0 Select the trigger source control enables the first 0 Bit. When set DSX00 Bit "1" When, analog comparator 0 As a comparison output signal waveform is off OC0A / OC0B The trigger source is enabled. when DOC0A / DOC0B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC0A / OC0B The waveform output. When set DSX00 Bit "0" When, analog comparator 0 As a comparison output signal waveform is off OC0A / OC0B The trigger source is prohibited.

The following table shows the selection control trigger source waveform output.

shut down OC0A / OC0B Trigger source waveform output from the selection control

DOC0x	DSX0n = 1	Trigger source	description
0	-	-	DOC0x Bit "0" , Trigger source waveform output off function is disabled
1	0	Analog comparator 0	ACIF0 The rising edge will be closed OC0x Waveform output
1	1	Analog comparator 1	ACIF1 The rising edge will be closed OC0x Waveform output
1	4	External Interrupt 0	INTF0 The rising edge will be closed OC0x Waveform output
1	5	Pin Change 0	PCIF0 The rising edge will be closed OC0x Waveform output
1	6	TC2 overflow	TOV2 The rising edge will be closed OC0x Waveform output
1	7	TC1 overflow	TOV1 The rising edge will be closed OC0x Waveform output

note:

1) DSX0n = 1 Show DSX0 The first register n Bit 1 When each register bit may be set simultaneously.

TC0 Count value register - TCNT0

TCNT0 -*TC0 Count value register*								
address: 0x46					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	TCNT07	TCNT06	TCNT05	TCNT04	TCNT03	TCNT02	TCNT01	TCNT00
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	TCNT0	TC0 Count value register. by TCNT0 Directly to the counter register 8 Read and write access to the counter value. CPU Correct TCNT0 Write to register on the next timer clock cycle to prevent the occurrence of compare match, even if the timer has stopped. This allows initialization TCNT0 And the value of the register OCR0 The value of the agreement without causing disruption. If you write TCNT0 The value is equal to or bypassed OCR0 Value, compare match will be lost, resulting in incorrect waveform generation. When the timer stops counting the clock source is not selected, but CPU Still access TCNT0 . CPU Write counter is cleared or a higher priority than addition and subtraction operations.

TC0 Output Compare Register A- OCR0A

OCR0A - *TC0 Output Compare Register A*								
address: 0x47					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR0A7	OCR0A6	OCR0A5	OCR0A4	OCR0A3	OCR0A2	OCR0A1	OCR0A0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	OCR0A	TC0 Output compare register. OCR0A It contains a 8 Bit data, with the counter value continuously TCNT0 Compare. Compare match can be used to generate an output compare interrupt, or to the OC0A Waveform generation pins. When PWM When mode, OCR0A Using double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR0A Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR0A When the buffer register, double buffering is disabled CPU Access is OCR0A itself.

TC0 Output Compare Register B- OCR0B

OCR0B - TC0 Output Compare Register B								
address: 0x48					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OCR0B7	OCR0B6	OCR0B5	OCR0B4	OCR0B3	OCR0B2	OCR0B1	OCR0B0 R / WR / W
		R / W	R / W	R / W	R / W	R / W	R / W	R / W
Initial	0	0	0	0	0	0	0	0

Bit	Name	description
7: 0	OCR0B	TC0 Output Compare B register. OCR0B It contains a 8 Bit data, with the counter value continuously TCNT0 Compare. Compare match can be used to generate an output compare interrupt, or to the OC0B Waveform generation pins. When PWM When mode, OCR0B Using double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR0B Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR0B When the buffer register, double buffering is disabled CPU Access is OCR0B itself.

TC0 Interrupt Mask Register - TIMSK0

TIMSK0 - TC0 Interrupt mask register								
address: 0x6E					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	OCIE0B	OCIE0A	TOIE0
R / W	-	-	-	-	-	R / W	R / W	R / W

Bit	Name	description
7: 3		Reservations.
2	OCIE0B	TC0 Output Compare B Match interrupt enable bit. when OCIE0B Bit "1" And Global Interrupt Set, TC0 Output Compare B Match interrupt is enabled. When a compare match occurs, i.e., TIFR0 in OCF0B When the bit is set, an interrupt is generated. when OCIE0B Bit "0" Time, TC0 Output Compare B Match interrupts are disabled.
1	OCIE0A	TC0 Output Compare A Match interrupt enable bit. when OCIE0A Bit "1" And Global Interrupt Set, TC0 Output Compare A Match interrupt is enabled. When a compare match occurs, i.e., TIFR0 in OCF0A When the bit is set, an interrupt is generated. when OCIE0A Bit "0" Time, TC0 Output Compare A Match interrupts are disabled.
0	TOIE0	TC0 Overflow interrupt enable bit. when TOIE0 Bit "1" And Global Interrupt Set, TC0 Overflow interrupt is enabled. when TC0 Overflow occurs, that is, TIFR middle TOV0 When the bit is set, an interrupt is generated. when TOIE0 Bit "0" Time, TC0 Overflow interrupts are disabled.

TC0 Interrupt Flag Register - TIFR0

TIFR0 - TC0 Interrupt Flag Register								
address: 0x35					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OC0A	OC0B	-	-	-	OCF0B	OCF0A	TOV0
R / W	R / O	R / O	-	-	-	R / W	R / W	R / W

Bit	Name	description
7	OC0A	Compare output waveform signal OC0A . Compare output waveform signal OC0A Software read but not write. Software can not enable OC0A Signal to its respective IO Before the pin, can first reading OC0A The polarity of the value of the bit to be acquired waveform signal output from the comparator, and by configuring COM0A Bit and set FOC0A Bits to change its polarity, enabling to avoid OC0A Signal to its respective IO Unwanted disturb pulse produced after the pin.
6	OC0B	Compare output waveform signal OC0B . Compare output waveform signal OC0B Software read but not write. Software can not enable OC0B Signal to its respective IO Before the pin, can first reading OC0B Bit

		Value to be output to a polarity comparator waveform signal, and configure COM0B Bit and set FOC0B Bits to change its polarity, enabling to avoid OC0B Signal to its respective IO Unwanted disturb pulse produced after the pin.
5: 3		Retention
2	OCF0B	TC0 Output Compare B Matching flag. when TCNT0 equal OCR0B , The comparison unit signals a match, the comparison flag is set and OCF0B . If the output of the comparator at this time B Interrupt Enable OCIE0B for "1" And the Global interrupt flag is set, it will produce output compare B Interrupted. When you do this the interrupt service routine OCF0B Will be automatically cleared or OCF0B Write bit "1" Also clears the bit.
1	OCF0A	TC0 Output Compare A Matching flag. when TCNT0 equal OCR0A , The comparison unit signals a match, the comparison flag is set and OCF0A . If the output of the comparator at this time A Interrupt Enable OCIE0A for "1" And the Global interrupt flag is set, it will produce output compare A Interrupted. When you do this the interrupt service routine OCF0A Will be automatically cleared or OCF0A Write bit "1" Also clears the bit.
0	TOV0	TC0 Overflow flag. When the counter overflows, the overflow flag is set TOV0 . If this time overflow interrupt enable TOIE0 for "1" And the Global interrupt flag is set, it will generate an overflow interrupt. When you do this the interrupt service routine TOV0 Will be automatically cleared or TOV0 Write bit "1" Also clears the bit.

DTR0 - TC0 Dead time control register

DTR0 **- TC0 Dead time control register**								
address: 0x4F					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	DTR07	DTR06	DTR05	DTR04	DTR03	DTR02	DTR01	DTR00
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
[7: 4]	DTR0H	TC0 Dead time register high. when TCCR0B Register DTEN0 Bit "1" Time, OC0A with OC0B Composition complementary outputs, the insertion of dead time control is enabled, OC0B The upper channel dead time inserted by the DTR0H It determines the length of time for DTR0H Clock count corresponding to the time.
[3: 0]	DTR0L	TC0 Dead time register lower. when TCCR0B Register DTEN0 Bit "1" Time, OC0A with OC0B Composition complementary outputs, the insertion of dead time control is enabled, OC0A The upper channel dead time inserted by the DTR0L It determines the length of time for DTR0H Clock count corresponding to the time.

TCKCSR - TC Clock control and status registers

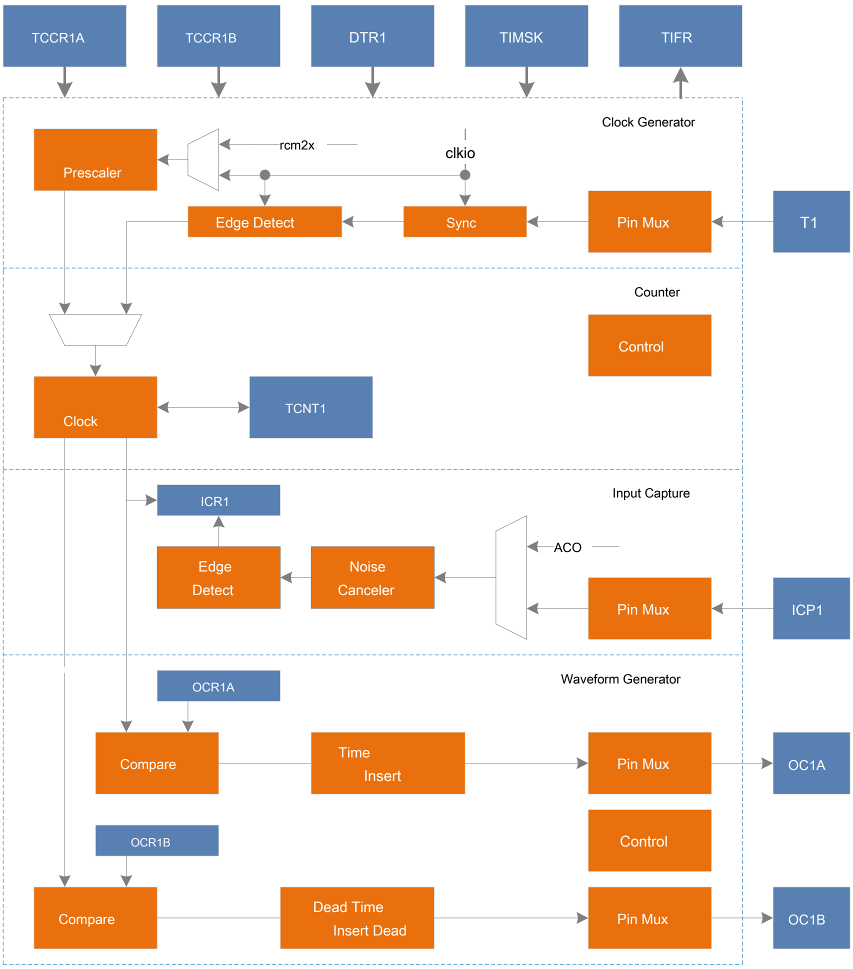
TCKSCR - TC Clock control and status registers								
address: 0xEC					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	F2XEN	TC2XF1	TC2XF0	-	AFCKS	TC2XS1	TC2XS0
R / W	-	R / W	R	R	- R / W		R / W	R / W

Bit	Name	description
7	-	Retention
6	F2XEN	RC 32M Output enable control bit multiplier. When set F2XEN Bit "1" Time, 32M RC Output frequency of the oscillator is enabled, the output 64M The high-speed clock. When set F2XEN Bit "1" Time, 32M RC Frequency output of the oscillator is disabled, can not output 64M The high-speed clock.
5	TC2XF1	TC High-speed clock mode flag 1 . See the timing counter 1 Register description.
4	TC2XF0	TC High-speed clock mode flag 0 . When read TC2XF0 Bit "1" , It indicates that the timer counter 0 Work on the high-speed clock mode, as "0" , It indicates that the timer counter 0 Work on the system clock mode.
3: 2	-	Reservations.
1	TC2XS1	TC High speed clock mode selection control bits 1 . See the timing counter 1 Register description.
0	TC2XS0	TC High speed clock mode selection control bits 0 . When set TC2XS0 Bit "1" When selecting the timer counter 0 Work on the high-speed clock mode. When set TC2XS0 Bit "0" When selecting the timer counter 0 Work on the system clock mode.

Timer / Counter 1 (TMR1)

- truly 16 Digital design, allowing 16 Bit PWM
- 2 Separate outputs the comparison unit
- Double buffered output compare register
- 1 Input capture unit
- Input Capture Noise Suppressor
- The counter is automatically cleared when compare match and automatically load
- No disturb pulse phase correction PWM
- Variable PWM cycle
- Frequency generator
- External event counter
- 4 Independent interrupt sources
- Support dead time control PWM
- 6 Selectable trigger source automatically shut down PWM Export
- Generating a high-resolution high-speed (high-speed clock mode @ 7BIT 500KHZ) the PWM

Outline



TC1 Structure chart

TC1 Is a common 16 Bit timer counter module support PWM Output waveform can be generated accurately. TC1 contain 1 More 16 Bit counter, waveform generation mode control unit, 2 Separate outputs and the comparison unit 1 Input capture unit. Simultaneously, TC1 With TC0 Common 10 Bit prescaler, can be used independently 10 Bit prescaler. The system clock prescaler clkio Or high-speed clock rcm2x (internal 32M RC Clock oscillator output rc32m of 2 Frequency) for frequency-dividing the count clock Clkt1 . Waveform generating mode generates the control unit controls the operation mode of the counter and comparing the output waveform. Depending on the mode of operation, a counter for counting each clock Clkt1 Cleared, incremented or decremented. Clkt1 It may be generated by an internal clock or an external clock source. When the count value of the counter TCNT1 It reached its maximum value (equal to the maximum value 0xFFFF Or a fixed value or output compare register OCR1A Or the input capture register ICR1 ,defined as TOP , The maximum value of the definition MAX When to distinguish), the counter is cleared or decremented. When the count value of the counter TCNT1

Reaches a minimum value (equal to 0x0000 ,defined as BOTTOM), The counter will be incremented by one operation. When the count value of the counter TCNT1 Arrivals OCR1A or OCR1B When, also referred to compare match, set or cleared by the output signal of the comparison OC1A or OC1B To produce PWM Waveform. When the enable insertion of dead time, the dead time is set (DTR1 Count clock number corresponding to the register) will be inserted into the generated PWM Waveform. When the input capture function is turned on, i.e. the counter is activated to start or stop counting, ICR1 Register records the captured count values trigger period signal. Software by clearing COM1A / COM1B Bit close to zero OC1A / OC1B The waveform output, or set the respective trigger source, when a triggering event occurs automatically cleared by hardware COM1A / COM1B Bit to close OC1A / OC1B The waveform output.

Count clock can be internal or external clock source to generate, select, and divided by the selected frequency clock source located TCCR1B Register CS1 Control bits, see the detailed description TC0 with TC1 Prescaler section.

Length counter is 16 Bit, supporting bi-directional counter. I.e., Waveform generating mode by the operation mode counter is located TCCR1A with TCCR1B Register WGM1 Bit to control. Depending on the mode of operation, a counter for counting each clock Clkt1 Cleared, incremented or decremented. When an overflow occurs count Located TIFR1 Counter register overflow flag TOV1 Bit is set. When the interrupt is enabled may produce TC1 Counter overflow interrupt.

Count value output of the comparison unit TCNT1 And output compare register OCR1A with OCR1B The value, when TCNT1 equal OCR1A or OCR1B When referred to as Comparative match occurs, it is located TIFR1 Output compare flag register OCF1A or OCF1B Bit is set. When the interrupt is enabled may produce TC1 Output Compare match interrupt. It should be noted that, in the PWM Under work mode, OCR1A with OCR1B Register is double buffered. In the normal mode and CTC Mode, double buffering function failure. When the count reaches maximum or minimum value of the buffer register is updated simultaneously comparing register OCR1A with OCR1B Go. See section describes the operating modes.

Waveform generator and comparator generates a mode control output waveform control pattern matching and Comparative counter overflow signal to generate an output waveform comparison OC1A with OC1B . DETAILED generation mode and the operation mode register, see section below. We should compare the output signal waveform OC1A with OC1B Corresponding to the output pin, the data direction register must be set to the output pin.

Operating mode

Timing counter 1 There are six different modes, including normal mode (Normal), Cleared on compare match (CTC) Mode, fast pulse width modulation (FPWM) Mode, a phase correction pulse width modulation (PCPWM) Mode, a phase correction pulse width modulation frequency (PFCPWM) Mode, and input capture (ICP)mode. Mode control bit is generated by the waveform WGM1 [3: 0] To choose. This is described in detail below six modes. Since there are two separate output of the comparison unit, respectively "A" with "B" Represented by lowercase "X" To represent the two channel outputs the comparison unit.

Normal mode

Normal mode timer counter is the simplest mode of operation, this time waveform generation mode control bit WGM1 [3: 0] = 0 Count maximum value TOP for MAX (0xFFFF). In this mode, a counting mode for each clock count plus an increment, when the counter reaches TOP After the spill back BOTTOM Re-start accumulating. The count value TCNT1 The same count clock becomes zero set timer counter's overflow flag TOV1 . In this mode TOV1 The first sign is like 17 Count bit, but will only be set is not cleared. Overflow interrupt service routine will automatically clear TOV1 Logos, software can use it to improve the resolution of the timer counter. Normal mode is not to be considered a special case, a new count value can be written at any time.

Set up OC1x Pin data direction register as an output a comparison signal to obtain an output OC1x Waveform. when COM1x = 1

When, flips compare match OC1x Signal, in this case the frequency waveform may be calculated using the following formula:

$$f_{oc1xnormal} = f_{sys} / (2 * N * 65536)$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024).

Output Compare unit can be used to generate interrupts, but does not recommend the use of interrupts in the normal mode, it will take up too much CPU time.

CTC mode

Set up WGM1 [3: 0] = 4 or 12 When the timer counter 1 enter CTC mode. when WGM1 [3] = 0 The count maximum TOP for OCR1A , when WGM1 [3] = 1 The count maximum TOP for ICR1 . Below WGM1 [3: 0] = 4 As an example to describe CTC Mode In this mode, a counting mode for each clock count plus an increment, when the value of the counter TCNT1

equal TOP When the counter is cleared. This mode allows the user to easily control the frequency of the compare match output also simplifies the operation of the external event count.

When the counter reaches TOP Output Compare match flag OCF1 Is set, an interrupt will be generated when the corresponding interrupt enable bit is set. Can be updated in the interrupt service routine OCR1A register. In this mode OCR1A Do not use double buffering, the counter prescaler to work under no or very low prescaler will be updated as close to the maximum value of the minimum time to be careful. If you write OCR1A The value is less than the time TCNT1 When the value of the counter will miss the compare match. Before a match occurs the next comparison, the first counter had counted to MAX And then from BOTTOM To start counting OCR1A . And normal mode, as the count value back 0x0 The count clock in the set TOV1 Mark.

Set up OC1x Pin data direction register as an output a comparison signal to obtain an output OC1x Waveform. Frequency waveform may be calculated using the following formula:

$$f_{oc1xctc} = f_{sys} / (2 * N * (1 + OCR1A))$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024). As can be seen from the formula, when set OCR1A for 0x0 And when no prescaler, allowing for maximum frequency $f_{sys} / 2$ The output waveform.

when WGM1 [3: 0] = 12 When the WGM1 [3: 0] = 4 Similarly, just and OCR1A Related replaced ICR1 It can be.

fast PWM mode

Set up WGM1 [3: 0] = 5 , 6 , 7 , 14 or 15 When the timer counter 1 Enter the fast PWM Mode, the maximum count TOP Respectively 0xFF , 0x1FF , 0x3FF , ICR1 or OCR1A , It can be used to generate high frequency PWM Waveform. fast

PWM Patterns and other PWM Except that it is a one-way mode operation. From the counter BOTTOM To accumulate TOP Then came back BOTTOM Re-count. When the count value TCNT1 Arrivals TOP or BOTTOM , The output signal of the comparison OC1x It will be set or cleared, depending on the comparison output mode COM1 Setting, as detailed register description. Since the one-way operation, fast PWM Operating frequency of the phase correction mode is employed bi-directionally operable PWM Double mode. It makes the fast frequency

PWM Mode is suitable for power regulation, rectification and DAC application. High-frequency signal can be reduced external components (capacitors, inductors) in size, thereby reducing system cost.

When the count value reaches TOP When the timer counter overflow flag TOV1 It will be set, and the updated buffer value comparison value to the comparator. If enabled, can be updated in the interrupt service routine OCR1A register.

Set up OC1x Pin data direction register as an output a comparison signal to obtain an output OC1x Waveform. Frequency of the waveform following formula can be calculated:

$f_{oc1xfpwm} = f_{sys} / (N * (1 + TOP))$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024).

when TCNT1 with OCR1x Compare match, the waveform generator to set (clear) OC1x Signal, when TCNT1 When cleared, the waveform generator will be cleared (set) OC1x Signal in order to produce PWM wave. thus OCR1x The extremes will produce special PWM Waveform. when OCR1x Set as 0x00 , The output of PWM For each (1 + TOP) There is a clock count of a narrow spike. when OCR1x Set as TOP Waveform, the output is continuously high or low. If you use OCR1A As a TOP And set COM1A = 1 , The comparator output signal OC1A It will have a duty cycle of 50% of PWM

wave.

Phase correction PWM mode

When set WGM0 [3: 0] = 1 , 2 , 3 , 10 or 11 When the timer counter 1 Enter phase correction PWM Max mode, counting TOP Respectively 0xFF , 0x1FF , 0x3FF , ICR1 or OCR1A . Bidirectional counter operation by BOTTOM

Increments to TOP And then descending to BOTTOM , Then repeat this operation. Count reaches TOP with BOTTOM Have to change direction when the count value TOP or BOTTOM On average only stay a count clock. In the process increments or decrements the count value

TCNT1 versus OCR1x Match, the comparison signal output OC1x It will be set or cleared, depending on the comparison output mode COM1 setting. Compared with the one-way operation, bidirectional operation obtainable maximum operation frequency, but its excellent symmetry is more suitable for motor control.

Phase correction PWM Mode, when the count reaches BOTTOM When set TOV1 Flag when the count reaches TOP When the buffer is updated to compare the value of the comparison value. If enabled, the interrupt service routine can be updated relatively buffer OCR1x Register.

Set up OC1x Pin data direction register as an output a comparison signal to obtain an output OC1x Waveform. Frequency of the waveform following formula can be calculated:

$f_{oc1xcpcpwm} = f_{sys} / (N * TOP * 2)$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024).

In up-counting process, when TCNT1 versus OCR1x Match, the waveform generator will be cleared (set) OC1x signal. in

Down counting process, when TCNT1 versus OCR1x When the match is set to the waveform generator (clear) OC1x signal. thus

OCR1x The extremes will produce a special PWM wave. when OCR1x Set as TOP or BOTTOM Time, OC1x Output signal will remain low or high. If you use OCR1A As a TOP And set COM1A = 1 , The comparator output signal OC1A It will have a duty cycle of 50% of PWM wave.

In order to ensure that the output PWM Wave BOTTOM Symmetry on both sides, a compare match does not occur, there will be two cases flipping OC1x signal. The first case is when OCR1x The value of the TOP When changes to other data. when OCR1x for

TOP , The count value reaches TOP Time, OC1x The same output result of the comparison in the previous match count in descending, i.e. holding OC1x constant. At this value will be updated relatively new OCR1x The value of the (non TOP), OC1x Value will remain set until the comparison match occurs ascending counting flip. at this time OC1x Signal to the minimum value as the center is not symmetrical, requiring the TCNT1 Flip reaches the maximum value OC1x Signal, namely when the comparator inverting no match occurs OC1x A first of the signal. The second case is when TCNT1 From the ratio OCR1x Counting high value, and thus will miss the compare match, thereby causing an asymmetric situation generated. Also you need to flip OC1x Signal to achieve symmetry of both sides of the minimum.

Phase frequency correction PWM mode

When set WGM0 [3: 0] = 8 or 9 When the timer counter 1 Into the phase frequency correction PWM Max mode, counting TOP Respectively ICR1 or OCR1A . Bidirectional counter operation by BOTTOM Increments to TOP And then descending to BOTTOM , Then repeat this operation. Count reaches TOP with BOTTOM Have to change direction when the count value TOP or

BOTTOM On average only stay a count clock. In the process increments or decrements the count value TCNT1 versus OCR1x Match, the comparison signal output OC1x It will be set or cleared, depending on the comparison output mode COM1 setting. Compared with the one-way operation, bidirectional operation obtainable maximum operation frequency, but its excellent symmetry is more suitable for motor control.

Phase frequency correction PWM Mode, when the count reaches BOTTOM When set TOV1 Flag, and comparing the value of the buffer to update the comparison value, the comparison value is updated frequency correction phase PWM And a phase correction mode PWM The biggest difference mode. If enabled, the interrupt service routine can be updated relatively buffer OCR1x Register. when CPU change TOP That value ORC1A or ICR1 When the value, you must ensure that the new TOP Value is not less than the already in use TOP Value, or compare match will not happen again.

Set up OC1x Pin data direction register as an output a comparison signal to obtain an output OC1x Waveform. Frequency of the waveform following formula can be calculated:

$$f_{oc1xcpfcpwm} = f_{sys} / (N * TOP * 2)$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024).

In up-counting process, when TCNT1 versus OCR1x Match, the waveform generator will be cleared (set) OC1x signal. In the process of counting down, when TCNT1 versus OCR1x When the match is set to the waveform generator (clear) OC1x signal. thus

OCR1x The extremes will produce a special PWM wave. when OCR1x Set as TOP or BOTTOM Time, OC1x Output signal will remain low or high. If you use OCR1A As a TOP And set COM1A = 1 , The comparator output signal OC1A It will have a duty cycle of 50% of PWM wave.

because OCR1x Register in BOTTOM Time updates, so TOP Value count ascending and descending on both sides are the same length, it generates the correct frequency and phase are symmetrical waveform.

When using a fixed TOP Value, is preferably used ICR1 Register as a TOP Value, that is set WGM1 [3: 0] = 8 ,at this time OCR1A

Only register used to generate PWM Output. If you want to generate a frequency change PWM Wave, must change TOP value, OCR1A Double buffering characteristics would be more suitable for this application.

Input Capture Mode

Input capture to capture external events and give them a time stamp indicating the time the event occurs, may be performed in front of the counting mode, but used to remove ICR1 As the count value TOP Waveform value generation patterns.

External trigger event occurs by pin ICP1 Input may be realized by an analog comparator unit. When the pin ICP1 Logic level on the output is changed, or the analog comparator ACO Level is changed, and this change in level is input to the capture unit captures input capture is triggered, then 16 Bit count value TCNT1 Data is copied into the input capture register ICR1 While input capture flag ICF1 Set, if ICIE1 Bit "1" , Input Capture Flag generates an Input Capture interrupt.

By setting the Analog Comparator Control and Status Register ACSR The analog comparator input capture control bit ACIC To select the input capture trigger source ICP1 or ACO . It should be noted that the change may cause a trigger source input capture, and therefore must be changed after the trigger source ICF1 To conduct a clearing operation to avoid erroneous results.

Capture Input selection control signal after an optional noise suppressor edge detector, based on the input capture ICES1 Configuration, see whether or not the detected edge trigger condition is met. Noise suppressor is a simple digital filtering, the input signal 4 Samples only when 4 When samples are equal the output value will be the edge detector. By the noise suppressor TCCR1B Register ICNC1 Bit control their enabled or disabled.

When using the input capture function, when ICF1 After being set, should be read as early as possible ICR1 Value of the register, because the next time capture after the event ICR1 The value will be updated. Recommended enable input capture interrupt at any input capture mode, the change count is not recommended during operation TOP value.

Input captured timestamp other features may be used to calculate the frequency and the duty ratio signal, as a trigger event and create a log. Measuring the duty cycle required external signal each time after the capture trigger edge is changed, so read ICR1 After the value of the edge-triggered signal to be changed as soon as possible.

PWM Automatically shutdown and restart of output

When set TCCR1C Register DOC1x Bit is high, PWM When auto-off feature is enabled, the trigger condition is met, the hardware clears the corresponding output COM1x Bits, PWM output signal OC1x And its output pin is disconnected, the switching to a common IO Output achieved PWM Automatically shut down the output. At this time, the state of the output pin by a general IO To control the output.

PWM Off automatically after the output is enabled, which also need to set the trigger conditions from TCCR1D Register DSX1n Bits to select trigger source. Triggered by an analog comparator interrupt, external interrupt, the interrupt pin change and the timer overflow interrupt, please refer to the specific circumstances TCCR1D Register description. Or when a certain trigger source is selected as the trigger condition, in which the interrupt flag is set at the same time, the hardware will be cleared COM1x Bit to close PWM Output.

In the event of a triggering event closed PWM After the output, the timer module is no corresponding interrupt flag, the software needs to know the trigger and the trigger event by source interrupt flag read.

when PWM When the output is automatically switched off and the need to restart output again, the software only needs to be reset COM1x Position to switch

OC1x Signal is output to the corresponding pin. It should be noted, occurs automatically shut down after the timer did not stop working,

OC1x State of the signal has also been updated. After the software or compare match timer overflows, then set COM1x Bit output OC1x Signal, so you can get a clear PWM Output state.

Dead-time control

Set up DTEN1 Bit "1" When inserting the dead time function is enabled, OC1A with OC1B The output waveform will B Deadtime comparator output channel waveform based on the generated set of insertion, the length of time of DTR1 Register count clock number corresponding to the time value. As shown below, OC1A with OC1B Deadtime insertion are based channel B Comparing the output waveform as a reference. when COM1A with COM1B The same "2" or "3" Time, OC1A The polarity of the waveform OC1B The waveform of the same polarity, when COM1A with COM1B Respectively "2" or "3" Time, OC1A The waveform OC1B Opposite polarity waveform.

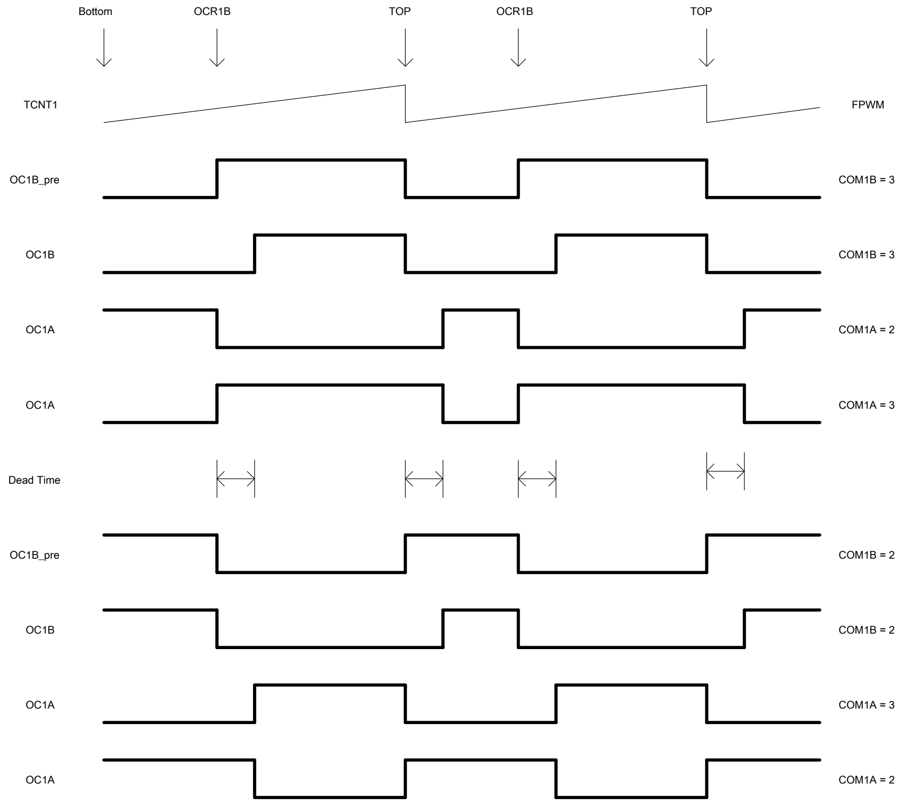


Figure 3 FPWM Mode TC1 Dead-time control

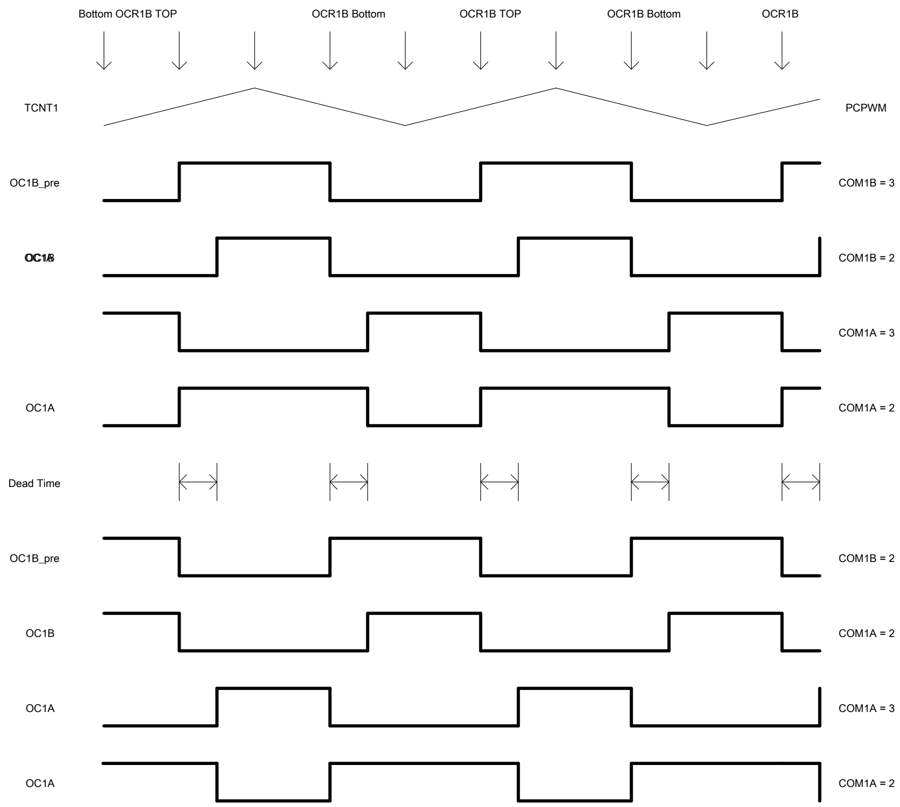


Figure 4 PCPWM Mode TC1 Dead-time control

Set up DTEN1 Bit "0" When inserting the dead time function is disabled, OC1A with OC1B The waveform of the output waveform generated by each comparator output.

High-speed counting mode

The high-speed clock mode using a higher frequency clock count as the clock source for generating higher speed and higher resolution PWM Waveform. This is achieved by the internal clock frequency 32M RC Oscillator output clock rc32m get on 2 Frequency doubling to produce a. Thus, before entering the high-frequency mode, the need to enable the internal 32M RC Oscillator frequency function, i.e. set TCKCSR Register F2XEN Position, and wait for a certain time until the output frequency of the clock signal stable. May then be set TCKCSR of TC2XS1 Timer counter bit to enter the high-speed clock mode.

In this mode, the system clocks are asynchronous with the high-speed clock, and some register (see TC1 Register list) working in the high-speed clock domain, and therefore, such a configuration register and reading is asynchronous, note operation.

No special requirements of high speed clock domain registers in read and write non-continuous, and continuous read and write operations, wait for a system clock, according to the following steps:

5) Write register A ;

6) Waiting for a system clock (NOP Clock register operating system or under);

7) Read or write register A or B .

8) Waiting for a system clock (NOP Registers in the clock or operating system).

When the high-speed clock domain register read operation, a width 8 Bit registers are directly readable, and to read 16 Bit value of the register (OCR1A , OCR1B, ICR1, TCNT1), The low value of the first register is read, the system waits for a clock

After then read the value of the high register, the reading TCNT1 When the value of the counter when the counting is still in progress, TCNT1 The value changes with a high speed clock, pause counter (provided CS1 Zero) then read TCNT1 Value.

Read OCR1A , OCR1B with ICR1 When, according to the following steps:

1) Read OCR1AL / OCR1BL / ICR1L ;

2) Waiting for a system clock (NOP);

3) Read OCR1AH / OCR1BH / ICR1H .

Read TCNT1 When, according to the following steps:

1) Set CS1 Zero;

2) Waiting for a system clock (NOP);

3) Read TCNT1L Value;

4) Waiting for a system clock (NOP); Reading TCNT1H Value.

Register Definition

TC1 Register List

register	address	Defaults	description
TCCR1A *	0x80	0x00	TC1 Control register A
TCCR1B *	0x81	0x00	TC1 Control register B
TCCR1C *	0x82	0x00	TC1 Control register C
DSX1	0x83	0x00	TC1 Trigger source control register
TCNT1L *	0x84	0x00	TC1 Low byte count value register
TCNT1H *	0x85	0x00	TC1 High byte count value register
ICR1L *	0x86	0x00	TC1 Input Capture Register Low Byte
ICR1H *	0x87	0x00	TC1 Input Capture MSB
OCR1AL *	0x88	0x00	TC1 Output Compare Register A Low byte
OCR1AH *	0x89	0x00	TC1 Output Compare Register A High Byte
OCR1BL *	0x8A	0x00	TC1 Output Compare Register B Low byte
OCR1BH *	0x8B	0x00	TC1 Output Compare Register B High Byte
DTR1 *	0x8C	0x00	TC1 Dead time control register
TIMSK1	0x6F	0x00	Timer counter interrupt mask register
TIFR1	0x36	0x00	Timer counter Interrupt Flag Register
TCKCSR1	0xEC	0x00	TC1 Clock Control Status Register

【note】

band "*" The register operation at high speed clock and a system clock domains, not with "*" The working register only at the system clock domain.

TCCR1A -TC1 Control register A

TCCR1A - TC1 Control register A								
address: 0x80					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	COM1A1	COM1A0	COM1B1	COM1B0	-	-	WGM11	WGM10
R / W	R / W	R / W	R / W	R / W	-	-	R / W	R / W

Bit	Name	description
7	COM1A1	Compare Match Output A Mode control high. COM1A1 with COM1A0 composition COM1A [1: 0] To control the output waveform of comparator OC1A . in case COM1A of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC1A Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM1A The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
6	COM1A0	Compare Match Output A Mode control low. COM1A1 with COM1A0 composition COM1A [1: 0] To control the output waveform of comparator OC1A . in case COM1A of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC1A Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM1A The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
5	COM1B1	Compare Match Output B Mode control high. COM1B1 with COM1B0 composition COM1B [1: 0] To control the output waveform of comparator OC1B . in case COM1B of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC1B Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM1B The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
4	COM1B0	Compare Match Output B Mode control low. COM1B1 with COM1B0 composition COM1B [1: 0] To control the output waveform of comparator OC1B . in case COM1B of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC1B Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM1B The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
3: 2	-	Remain unchanged
1	WGM11	Waveform generation mode control times lower. WGM11 with WGM13, WGM12, WGM10 Together form waveform generation mode control WGM1 [3: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
0	WGM10	Waveform generation mode control lowest bit. WGM10 with WGM13, WGM12, WGM11 Together form waveform generation mode control WGM1 [3: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.

The following table non PWM Mode (ie, normal mode and CTC Mode), the comparison output of the comparator mode control output waveform.

COM1x [1: 0]	description
0	OC1x Disconnect, GM IO Port operations
1	Flip compare match OC1x signal
2	Clear compare match OC1x signal
3	When set compare match OC1x signal

The following table fast PWM Mode mode control comparator output waveform of the output comparator.

COM1x [1: 0]	description
0	OC1x Disconnect, GM IO Port operations
1	WGM1 for 15 When: Flip compare match OC1A signal, OC1B disconnect WGM1 When other values: OC1x Disconnect, GM IO Port operations
2	Clear compare match OC1x Signal is set to match the maximum value OC1x signal
3	When set compare match OC1x Signal is cleared when the maximum matching OC1x signal

The following table shows the comparison output of the phase correction mode the mode control output of the comparator waveform.

COM1x [1: 0]	description
0	OC1x Disconnect, GM IO Port operations
1	WGM1 for 9 or 11 When: Flip compare match OC1A signal, OC1B disconnect WGM1 When other values: OC1x Disconnect, GM IO Port operations
2	Match clears the count comparator ascending OC1x Signal, the match count comparator arranged in descending order bits OC1x signal
3	Comparison of the configuration bit match count ascending OC1x Down signal, in descending count comparator match clears OC1x signal

TCCR1B -TC1 Control register B

TCCR1B - TC1 Control register B								
address: 0x81					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	ICNC1	ICES1	-	WGM13 WGM12 CS12			CS11	CS10
R / W	R / W	R / W	- R / W		R / W	R / WR / WR / W		

Bit	Name	description
7	ICNC1	Input Capture noise suppressor enable control bit. When set ICNC1 Bit "1" When the enable input capture noise suppressor, when external pin ICP1 The input is filtered continuously 4 Sampling values of the input signal is valid when equal, the function input capture is delayed 4 Clock cycles. When set ICNC1 Bit "0" When prohibit input capture noise suppressor, this time external pin ICP1 Direct and effective input.
6	ICES1	Input Capture Edge Select control bits. When set ICES1 Bit "1" When the rising edge of selection level input capture trigger; provided when ICES1 Bit "0" When selecting the level of the falling edge of the input capture trigger. When a capture is triggered, the counter value is copied into ICR1 Register, while the set input capture flag ICF1 . If the interrupt is enabled, the input capture interrupt.
5	-	Reservations.

4	WGM13	Waveform generation mode control high. WGM13 with WGM12, WGM11, WGM10 Together form waveform generation mode control WGM1 [3: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
3	WGM12	Second uppermost waveform generation mode control. WGM12 with WGM13, WGM11, WGM10 Together form waveform generation mode control WGM1 [3: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
2	CS12	Clock control high. For selecting a timing counter 1 The clock source.
1	CS11	Clock selection control bits. For selecting a timing counter 1 The clock source.
0	CS10	Clock control low. For selecting a timing counter 1 The clock source.

CS1 [2: 0]	description
0	No clock source, stops counting
1	clk_{sys}
2	clk_{sys} / 8 From prescaler
3	clk_{sys} / 64 From prescaler
4	clk_{sys} / 256 From prescaler
5	clk_{sys} / 1024 From prescaler
6	External Clock T1 Pin, falling edge
7	External Clock T1 Pin on the rising edge

The following table is a waveform generation mode control.

WGM1 [3: 0]	Operating mode	TOP value	Update OCR0 Time	set TOV0 time
0	Normal	0xFFFF	immediately	MAX
1	8 Place PCPWM	0x00FF	TOP	BOTTOM
2	9 Place PCPWM	0x01FF	TOP	BOTTOM
3	10 Place PCPWM	0x03FF	TOP	BOTTOM
4	CTC	OCR1A	immediately	MAX
5	8 Place FPWM	0x00FF	BOTTOM	TOP
6	9 Place FPWM	0x01FF	BOTTOM	TOP
7	10 Place FPWM	0x03FF	BOTTOM	TOP
8	PFCPWM	ICR1	BOTTOM	BOTTOM
9	PFCPWM	OCR1A	BOTTOM	BOTTOM
10	PCPWM	ICR1	TOP	BOTTOM
11	PCPWM	OCR1A	TOP	BOTTOM
12	CTC	ICR1	immediately	MAX
13	Retention	-	-	-
14	FPWM	ICR1	TOP	TOP
15	FPWM	OCR1A	TOP	TOP

TCCR1C -TC1 Control register C

TCCR1C - TC1 Control register C								
address: 0x82					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	FOC1A	FOC1B	DOC1B	DOC1A	DTEN1	-	-	-
R / W	W	W	R / W	R / W	R / W	-	-	-

Bit	Name	description
7	FOC1A	Force Output Compare A . In non PWM Mode, the force output by comparing bits FOC1A write "1" The way to compare match. Forcing compare match will not set OCF1A Flag or reload or clear the timer, but the output pin OC1A Will be in accordance with COM1A It sets the appropriate update, just compare match had really happened. Work on PWM When mode, write TCCR1A Cleared when you want to register. Read FOC1A The return value is always zero.
6	FOC1B	Force Output Compare B . In non PWM Mode, the force output by comparing bits FOC1B write "1" The way to compare match. Forcing compare match will not set OCF1B Flag or reload or clear the timer, but the output pin OC1B Will be in accordance with COM1B It sets the appropriate update, just compare match had really happened. Work on PWM When mode, write TCCR1A Cleared when you want to register. Read FOC1B The return value is always zero.
5	DOC1B	TC1 Close control of the high output of the comparator is enabled. When set DOC1B Bit "1" It is triggered off the output comparison signal source OC1B It is enabled. When a trigger event occurs, the hardware is automatically cleared COM1B Position, close OC1B The waveform output. Software by setting COM1B Re-open PWM Output. When set DOC1B Bit "0" It is triggered off the output comparison signal source OC1B Prohibited.
4	DOC1A	TC1 Close control of the low output of the comparator is enabled. When set DOC1A Bit "1" It is triggered off the output comparison signal source OC1A It is enabled. When a trigger event occurs, the hardware is automatically cleared COM1A Position, close OC1A The waveform output. Software by setting COM1A Re-open PWM Output. When set DOC1A Bit "0" It is triggered off the output comparison signal source OC1A Prohibited.
3	DTEN1	TC1 Dead time enable control bit. When set DTEN1 Bit "1" When, enabling dead-time insertion. OC1A with OC1B They are in B Insertion of dead time waveform of the comparison output is generated based on the channel, inserted by the dead time interval DTR1 Register corresponding to the count time determined. OC1A The polarity of the output waveform COM1A with COM1B The correspondence between the decision, see OC1A After insertion of dead time waveform table shown polarity. When set DTEN1 Bit "0" Is prohibited dead-time insertion, OC1A with OC1B Comparing each of the generated output waveforms.
2: 0	-	Retention

The following table is a dead time enabled OC1A Polarity control signal output waveform.

Dead time enabled mode OC1A Polarity control signal output waveform

DTEN1	COM1A [1: 0]	COM1B [1: 0]	description
0	-	-	OC1A Signal polarity by the OC1A Compare output mode control
1	0	-	OC1A Disconnect, GM IO Port operations
1	1	-	Retention
1	2	2	OC1A Signals OC1B Signals with the same polarity
		3	OC1A Signals OC1B Opposite signal polarity
1	3	2	OC1A Signals OC1B Opposite signal polarity
		3	OC1A Signals OC1B Signals with the same polarity

【note】:

OC1B The polarity of the signal output from the waveform OC1B Compare output control mode, so that the same can not dead time mode.

TCCR1D -TC1 Control register D

TCCR1D - TC Control register D								
address: 0x83					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	DSX17	DSX16	DSX15	DSX14	-	-	DSX11	DSX10
R / W	R / W	R / W	R / W	R / W	-	-	R / W	R / W

Bit	Name	description
7	DSX17	TC1 Select the trigger source control enables the first 7 Bit. When set DSX17 Bit "1" Time, TC0 As the output of the comparator is off the overflow signal waveform OC1A / OC1B The trigger source is enabled. when DOC1A / DOC1B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC1A / OC1B The waveform output. When set DSX17 Bit "0" Time, TC0 As the output of the comparator is off the overflow signal waveform OC1A / OC1B The trigger source is prohibited.
6	DSX16	TC1 Select the trigger source control enables the first 6 Bit. When set DSX16 Bit "1" Time, TC2 As the output of the comparator is off the overflow signal waveform OC1A / OC1B The trigger source is enabled. when DOC1A / DOC1B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC1A / OC1B The waveform output. When set DSX16 Bit "0" Time, TC2 As the output of the comparator is off the overflow signal waveform OC1A / OC1B The trigger source is prohibited.
5	DSX15	TC1 Select the trigger source control enables the first 5 Bit. When set DSX15 Bit "1" When, pin change 1 As a comparison output signal waveform is off OC1A / OC1B The trigger source is enabled. when DOC1A / DOC1B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC1A / OC1B The waveform output. When set DSX15 Bit "0" When, pin change 1 As a comparison output signal waveform is off OC1A / OC1B The trigger source is prohibited.
4	DSX14	TC1 Select the trigger source control enables the first 4 Bit. When set DSX14 Bit "1" When the external interrupt 1 As a comparison output signal waveform is off OC1A / OC1B The trigger source is enabled. when DOC1A / DOC1B Bit

		"1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC1A / OC1B The waveform output. When set DSX14 Bit "0" When the external interrupt 1 As a comparison output signal waveform is off OC1A / OC1B The trigger source is prohibited.
3: 2	-	Retention
1	DSX11	TC1 Select the trigger source control enables the first 1 Bit. When set DSX11 Bit "1" When, analog comparator 1 As a comparison output signal waveform is off OC1A / OC1B The trigger source is enabled. when DOC1A / DOC1B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC1A / OC1B The waveform output. When set DSX11 Bit "0" When, analog comparator 1 As a comparison output signal waveform is off OC1A / OC1B The trigger source is prohibited.
0	DSX10	TC1 Select the trigger source control enables the first 0 Bit. When set DSX10 Bit "1" When, analog comparator 0 As a comparison output signal waveform is off OC1A / OC1B The trigger source is enabled. when DOC1A / DOC1B Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC1A / OC1B The waveform output. When set DSX10 Bit "0" When, analog comparator 0 As a comparison output signal waveform is off OC1A / OC1B The trigger source is prohibited.

The following table shows the selection control trigger source waveform output.

shut down OC1A / OC1B Trigger source waveform output from the selection control

DOC1x	DSX1n = 1	Trigger source	description
0	-	-	DOC1x Bit "0" , Trigger source waveform output off function is disabled
1	0	Analog comparator 0	ACIF0 The rising edge will be closed OC1x Waveform output
1	1	Analog comparator 1	ACIF1 The rising edge will be closed OC1x Waveform output
1	4	External Interrupt 1	INTF1 The rising edge will be closed OC1x Waveform output
1	5	Pin Change 1	PCIF1 The rising edge will be closed OC1x Waveform output
1	6	TC2 overflow	TOV2 The rising edge will be closed OC1x Waveform output
1	7	TC0 overflow	TOV0 The rising edge will be closed OC1x Waveform output

【note】:

DSX1n = 1 Show DSX1 The first register n Bit 1 When each register bit may be set simultaneously.

TCNT1L -TC1 Low byte count value register

TCNT1L - TC1 Low byte count value register								
address: 0x84					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	TCNT1L7	TCNT1L6	TCNT1L5	TCNT1L4	TCNT1L3	TCNT1L2	TCNT1L1	TCNT1L0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name description							
7: 0	TCNT1 TC1 Low byte count value.							

		TCNT1H with TCNT1L Incorporated into the composition together TCNT1 ,by TCNT1 Directly to the counter register 16 Count value read and write access. Read and write 16 Bit register requires two operations. write 16 Place TCNT1 When, you should write TCNT1H . read 16 Place TCNT1 When, it should read TCNT1L . CPU Correct TCNT1 Write to register on the next timer clock cycle to prevent the occurrence of compare match, even if the timer has stopped. This allows initialization TCNT1 And the value of the register OCR1x The value of the agreement without causing disruption. If you write TCNT1 The value is equal to or bypassed OCR1x Value, compare match will be lost, resulting in incorrect waveform generation. When the timer stops counting the clock source is not selected, but CPU Still access TCNT1 . CPU Write counter is cleared or a higher priority than addition and subtraction operations.

TCNT1H -TC1 High byte count value register

***TCNT1H* - TC1 High byte count value register**								
address: 0x85					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	TCNT1H7	TCNT1H6	TCNT1H5	TCNT1H4	TCNT1H3	TCNT1H2	TCNT1H1	TCNT1H0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	TCNT1H	TC1 The count value of the high byte. TCNT1H with TCNT1L Incorporated into the composition together TCNT1 ,by TCNT1 Directly to the counter register 16 Count value read and write access. Read and write 16 Bit register requires two operations. write 16 Place TCNT1 When, you should write TCNT1H . read 16 Place TCNT1 When, it should read TCNT1L . CPU Correct TCNT1 Write to register on the next timer clock cycle to prevent the occurrence of compare match, even if the timer has stopped. This allows initialization TCNT1 And the value of the register OCR1x The value of the agreement without causing disruption. If you write TCNT1 The value is equal to or bypassed OCR1x Value, compare match will be lost, resulting in incorrect waveform generation. When the timer stops counting the clock source is not selected, but CPU Still access TCNT1 . CPU Write counter is cleared or a higher priority than addition and subtraction operations.

ICR1L -TC1 Input Capture Register Low Byte

***ICR1L* - TC1 Input Capture Register Low Byte**								
address: 0x86					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	ICR1L7 ICR1L6 ICR1L5 ICR1L4 ICR1L3 ICR1L2 ICR1L1 ICR1L0 R / WR / W							
		R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	ICR1L	TC1 Input capture the low byte value. ICR1H with ICR1L Incorporated into the composition together 16 Bit ICR1 . Read and write 16 Bit register requires two operations. write 16 Place ICR1 When, you should write ICR1H . read 16 Place

		ICR1 When, it should read ICR1L . When the input capture is triggered, the count value TCNT1 Will be updated to copy ICR1 Register. ICR1 Count register is also used to define the TOP value.

ICR1H -TC1 Input Capture MSB

***ICR1H* - TC1 Input Capture MSB**								
address: 0x87					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	ICR1H7	ICR1H6	ICR1H5	ICR1H4	ICR1H3	ICR1H2	ICR1H1	ICR1H0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name description							
7: 0	ICR1H	TC1 Input capture high byte values. ICR1H with ICR1L Incorporated into the composition together 16 Bit ICR1 . Read and write 16 Bit register requires two operations. write 16 Place ICR1 When, you should write ICR1H . read 16 Place ICR1 When, it should read ICR1L . When the input capture is triggered, the count value TCNT1 Will be updated to copy ICR1 Register. ICR1 Count register is also used to define the TOP value.						

OCR1AL -TC1 Output Compare Register A Low byte

***OCR1AL* - TC1 Output Compare Register A Low byte**								
address: 0x88					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR1AL7	OCR1AL6	OCR1AL5	OCR1AL4	OCR1AL3	OCR1AL2	OCR1AL1	OCR1AL0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name description							
7: 0	OCR1AL	Output Compare Register A The low byte. OCR1AL with OCR1AH Incorporated into the composition together 16 Bit OCR1A . Read and write 16 Bit register requires two operations. write 16 Place OCR1A When, you should write OCR1AH . read 16 Place OCR1A When, it should read OCR1AL . OCR1A Continuously with the counter value TCNT1 Compare. Compare match can be used to generate an output compare interrupt, or to the OC1A Waveform generation pins. When PWM When mode, OCR1A Using double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR1A Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR1A When the buffer register, double buffering is disabled CPU Access is OCR1A itself.						

OCR1AH -TC1 Output Compare Register A High Byte

OCR1AH **-** TC1 Output Compare Register A High Byte								
address: 0x89					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR1AH7	OCR1AH6	OCR1AH5	OCR1AH4	OCR1AH3	OCR1AH2	OCR1AH1	OCR1AH0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name description							
7: 0	OCR1AH	Output Compare Register A The high byte. OCR1AL with OCR1AH Incorporated into the composition together 16 Bit OCR1A . Read and write 16 Bit register requires two operations. write 16 Place OCR1A When, you should write OCR1AH . read 16 Place OCR1A When, it should read OCR1AL . OCR1A Continuously with the counter value TCNT1 Compare. Compare match can be used to generate an output compare interrupt, or to the OC1A Waveform generation pins. When PWM When mode, OCR1A Using double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR1A Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR1A When the buffer register, double buffering is disabled CPU Access is OCR1A itself.						

OCR1BL -TC1 Output Compare Register B Low byte

OCR1BL **-** TC1 Output Compare Register B Low byte								
address: 0x8A					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR1BL7	OCR1BL6	OCR1BL5	OCR1BL4	OCR1BL3	OCR1BL2	OCR1BL1	OCR1BL0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name description							
7: 0	OCR1BL	Output Compare Register B The low byte. OCR1BL with OCR1BH Incorporated into the composition together 16 Bit OCR1B . Read and write 16 Bit register requires two operations. write 16 Place OCR1B When, you should write OCR1BH . read 16 Place OCR1B When, it should read OCR1BL . OCR1B Continuously with the counter value TCNT1 Compare. Compare match can be used to generate an output compare interrupt, or to the OC1B Waveform generation pins. When PWM When mode, OCR1B Using double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR1B Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR1B When the buffer register, double buffering is disabled CPU Access is OCR1B itself.						

OCR1BH -TC1 Output Compare Register B High Byte

OCR1BH - TC1 Output Compare Register B High Byte								
address: 0x8B					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR1BH7	OCR1BH6	OCR1BH5	OCR1BH4	OCR1BH3	OCR1BH2	OCR1BH1	OCR1BH0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	OCR1BH	Output Compare Register B The high byte. OCR1BL with OCR1BH Incorporated into the composition together 16 Bit OCR1B . Read and write 16 Bit register requires two operations. write 16 Place OCR1B When, you should write OCR1BH . read 16 Place OCR1B When, it should read OCR1BL . OCR1B Continuously with the counter value TCNT1 Compare. Compare match can be used to generate an output compare interrupt, or to the OC1B Waveform generation pins. When PWM When mode, OCR1B Using double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR1B Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR1B When the buffer register, double buffering is disabled CPU Access is OCR1B itself.

TIMSK1 - TC1 Interrupt mask register

TIMSK1 - TC1 Interrupt mask register								
address: 0x6F					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	-	-	TICIE1	-	-	OCIE1A	OCIE1B	TOIE1
R / W	-	-	R / W	-	-	R / W	R / W	R / W

Bit	Name	description
7: 6	-	Reservations.
5	TICIE1	TC1 Input Capture interrupt enable control bit. when ICIE1 Bit "1" When, and Global Interrupt set, TC1 Input Capture interrupt is enabled. When the input capture trigger, that is, TIFR1 of ICF1 Flag is set, an interrupt occurs. when ICIE1 Bit "0" Time, TC1 Input capture interrupts are disabled.
4: 3	-	Reservations.
2	OCIE1B	TC1 Output Compare B Match interrupt enable bit. when OCIE1B Bit "1" And Global Interrupt Set, TC1 Output Compare B Match interrupt is enabled. When a compare match occurs, i.e., TIFR in OCF1B When the bit is set, an interrupt is generated. when OCIE1B Bit "0" Time, TC1 Output Compare B Match interrupts are disabled.
1	OCIE1A	TC1 Output Compare A Match interrupt enable bit. when OCIE1A Bit "1" And Global Interrupt Set, TC1 Output Compare A Matching

		Interrupt is enabled. When a compare match occurs, i.e., TIFR in OCF1A When the bit is set, an interrupt is generated. when OCIE1A Bit "0" Time, TC1 Output Compare A Match interrupts are disabled.
0	TOIE1	TC1 Overflow interrupt enable bit. when TOIE1 Bit "1" And Global Interrupt Set, TC1 Overflow interrupt is enabled. when TC1 Overflow occurs, that is, TIFR middle TOV1 When the bit is set, an interrupt is generated. when TOIE1 Bit "0" Time, TC1 Overflow interrupts are disabled.

TIFR1 - TC1 Interrupt Flag Register

TIFR1 - TC1 Interrupt Flag Register								
address: 0x36					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	-	-	ICF1	-	-	OCF1B	OCF1A	TOV1
R / W	-	- R / W		-	- R / W		R / W	R / W

Bit	Name	description
7: 6	-	Reservations.
5	ICF1	Input capture flag. When the input capture event occurs, ICF1 Flag is set. when ICR1 It is counted as TOP Value, and the count value reaches TOP Value, ICF1 Flag is set. If the ICIE1 for "1" And the Global interrupt flag is set, it will generate an interrupt input capture. When you do this the interrupt service routine ICF1 Will be automatically cleared or ICF1 Write bit "1" Also clears the bit.
4: 3	-	Reservations.
2	OCF1B	Output Compare B Matching flag. when TCNT1 equal OCR1B , The comparison unit signals a match, the comparison flag is set and OCF1B . If then the output compare interrupt enable OCIE1B for "1" And the Global interrupt flag is set, it will generate an output compare interrupt. When you do this the interrupt service routine OCF1B Will be automatically cleared or OCF1B Write bit "1" Also clears the bit.
1	OCF1A	Output Compare A Matching flag. when TCNT1 equal OCR1A , The comparison unit signals a match, the comparison flag is set and OCF1A . If then the output compare interrupt enable OCIE1A for "1" And the Global interrupt flag is set, it will generate an output compare interrupt. When you do this the interrupt service routine OCF1A Will be automatically cleared or OCF1A Write bit "1" Also clears the bit.
0	TOV1	Overflow flag. When the counter overflows, the overflow flag is set TOV1 . If this time overflow interrupt enable TOIE1 for "1" And the Global interrupt flag is set, it will generate an overflow interrupt. When you do this the interrupt service routine TOV1 Will be automatically cleared or TOV1 Write bit "1" Also clears the bit.

DTR1L -TC1 Dead Time Register Low Byte

DTR1 - TC1 Dead time register								
address: 0x8C					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0

	DTR1L							
R / WR / W		R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name description							
7: 0	DTR1L	High byte dead time register. when DTEN1 Bit is high, OC1A with OC1B Complementary output, OC1A The output from the dead time inserted DTR1L Count clock determined.						

DTR1H -TC1 High byte dead time register

DTR1H **-** TC1 High byte dead time register								
address: 0x8D					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	DTR1H							
R / WR / W		R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name description							
7: 0	DTR1H	High byte dead time register. when DTEN1 Bit is high, OC1A with OC1B Complementary output, OC1B The output from the dead time inserted DTR1H Count clock determined.						

TCKCSR -TC Clock Control Status Register

TCKCSR **-** TC Clock Control Status Register								
address: 0xEC					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	-	F2XEN	TC2XF1	TC2XF0	-	AFCKS	TC2XS1	TC2XS0
R / W	-	R / W	R / O	R / O	-	R / W	R / W	R / W
Bit	Name description							
7	-	Retention						
6	F2XEN	RC 32M Multiplier output enable control bit when set F2XEN Bit "1" Time, 32M RC Output frequency of the oscillator is enabled, the output 64M When the high-speed clock provided F2XEN Bit "1" Time, 32M RC Frequency output of the oscillator is disabled, can not output 64M The high-speed clock						
5	TC2XF1	TC High-speed clock mode flag 1 When read TC2XF1 Bit "1" , It indicates that the timer counter 1 Work on the high-speed clock mode, as "0" , It indicates that the timer counter 1 Work on the system clock mode						
4	TC2XF0 TC High-speed clock mode flag 0 , The reference timing counter 0 Register Description							
3: 2	-	Retention						
1	TC2XS1	TC High speed clock mode selection control bits 1 When set TC2XS1 Bit "1" When selecting the timer counter 1 Clock Mode When operating in the high-speed setting TC2XS1 Bit "0" When selecting the timer counter 1 Work on the system clock mode						
0	TC2XS0 TC High speed clock mode selection control bits 0 , The reference timing counter 0 Register Description							

TMR0 / 1/3 Prescaler

- 3 More 10 Bit prescaler
- Multiplexing mode TC0 , TC1 with TC3 Multiplexing prescaler CPS310
- Stand-alone mode TC0 Alone with prescaler CPS310 , TC1 Alone with prescaler CPS1 , TC3 Alone with prescaler CPS3
- Support software reset

Outline

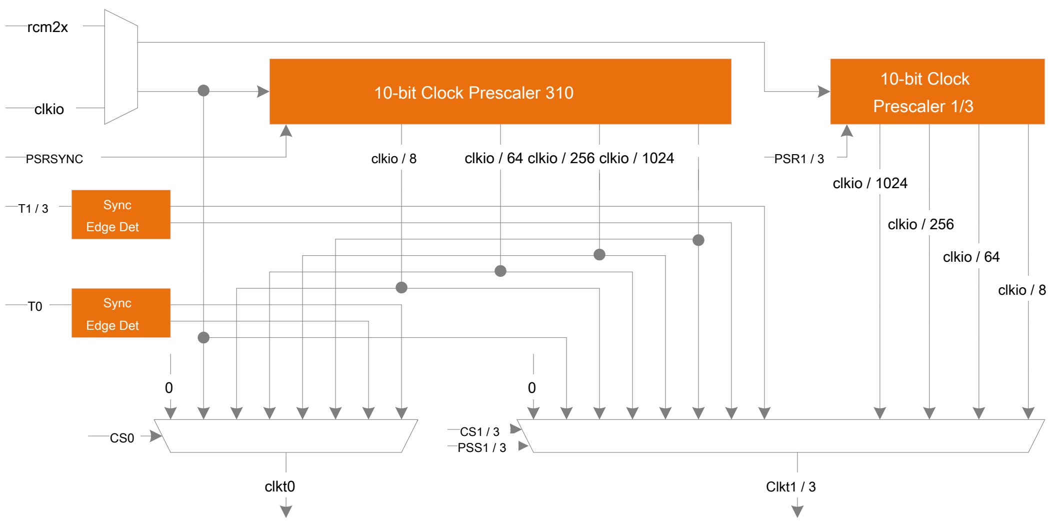
Multiplexing mode (PSS1 = 0 And PSS3 = 0), TC0 , TC1 with TC3 A share 10 Bit prescaler CPS310 But they have a different set of frequency division.

Alone mode (PSS1 = 1 And PSS3 = 0), TC1 Use a separate 10 Bit prescaler CPS1 , TC0 with TC3 A share 10 Bit prescaler CPS310 But they have a different set of frequency division.

Alone mode (PSS1 = 0 And PSS3 = 1), TC3 Use a separate 10 Bit prescaler CPS3 , TC0 with TC1 A share 10 Bit prescaler CPS310 But they have a different set of frequency division.

Stand-alone mode (PSS1 = 1 And PSS3 = 1), TC0 Use a separate 10 Bit prescaler CPS310 , TC1 Use a separate 10 Bit prescaler CPS1 , TC3 Independently prescaler CPS3 .

The following description uses in TC0 , TC1 with TC3 ,among them n representative 0 , 1 or 3 .



TC0 / TC1 / TC3 Prescaler Structure chart

Internal clock source

When set CSn [2: 0] = 1 When the timer 3 Only by the system clock clkio Driver, timer counter 0 or 1 Directly by the system clock clkio Or high-speed clock rcm2x (internal 32M RC Oscillator output clock 2 Octave) drive. Prescaler can output 4 Different clock frequencies, respectively, clkio / 8 , clkio / 64 , clkio / 256 with clkio / 1024 .

Divider reset

Multiplexed mode

When set PSS1 Bit "0" And PSS3 Bit "0" Time, TC0 , TC1 with TC3 Share a prescaler CPS310 .

The prescaler is free running, its operation is independent of the TC The clock selection logic, and which consists of TC0 , TC1 with TC3 shared. Since not affect the control of the clock selection, impact on application status will be divided clock prescaler. When the output is enabled and the timer prescaler selected as the count clock source (6> CSn [2: 0]> 1 Time), the impact it will have. From the timer is enabled to the first count may take 1 To N + 1 System clock, wherein N To prescale factor (8 ,
64 , 256 or 1024).

To synchronize the timer and reset program is run by the prescaler is possible. It must be noted, however, whether the other is using the timer prescaler prescaler reset will affect all timers connected to it.

Alone mode

When set PSS1 Bit "1" Time, TC1 Independently prescaler CPS1 , Reset by prescaler PSR1 Bit to control. Respective reset function separately, without affecting other prescaler.

When set PSS3 Bit "1" Time, TC3 Independently prescaler CPS3 , Reset by prescaler PSR3 Bit to control. Respective reset function separately, without affecting other prescaler.

When set PSS1 Bit "1" And PSS3 Bit "1" Time, TC0 Independently prescaler CPS310 , Reset by prescaler PSRSYNC Bit to control, TC1 Independently prescaler CPS1 , TC3 Independently prescaler CPS3 Respective reset function separately, without affecting other prescaler.

External clock source

by T0 / T1 / T3 External clock source pin can be used as the count clock source. T0 / T1 / T3 After the signal pin and the synchronization logic edge detector as counter clock source. Each rising edge (CSn [2: 0] = 7) Or falling edge (CSn [2: 0] = 6) Will produce a count pulse. External clock source will not be sent to the prescaler.

Since the pin is synchronized with the presence of the edge detecting circuit, T0 / T1 / T3 Changes in the level needs to be delayed 2.5 To 3.5 System clock to the counter update.

Enabling and disabling of the clock input must be T0 / T1 / T3 Stable for at least the need for a system clock cycle, otherwise it is likely to have generated error count clock pulses.

In order to ensure correct sampling clock pulse width must be greater than the external system clock cycle, the duty ratio of 50% When the external clock frequency must be less than half the system clock frequency. Due to differences in the clock oscillator frequency and duty cycle of the system itself caused the error, recommendations of the external clock frequency is not greater than the maximum f_{sys} / 2.5 .

Register Definition

GTCCR - General timer counter control register

GTCCR - General timer counter control register								
address: 0x43					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	TSM	-	-	-	-	-	PSRASY	PSRSYNC
R / W	R / W	-	-	-	-	- W		W

Bit	Name	description
7	TSM	Synchronous timing counter mode control bits. When set TSM Bit "1" When the timer counter is a synchronous mode. In synchronous mode, writing PSRASY Bit and PSRSYNC Bit value will remain, so that the corresponding prescaler has been reset. This ensures the appropriate timing counter and configured to abort the same value. When set TSM Bit "0" Time, PSRASY Bit and PSRSYNC Bit value will be cleared by hardware, and the timer counter and began to work.
6: 2	-	Reservations.
1	PSRASY	See Timer TC2 Register description.
0	PSRSYNC	Prescaler CPS310 Reset control bits. When set PSRSYNC Bit "1" When, prescaler CPS310 It will be reset. when TSM When the bit is not set, then the reset will clear the hardware PSRSYNC Bit. When set PSRSYNC Bit "0" When the setting is invalid. Multiplexing mode, TC0 / TC1 / TC3 Shared prescaler reset will affect the three timers. Stand-alone mode, the reset will only affect TC0 . Read this value will always be a "0" .

PSSR - Prescaler selection register

PSSR - Prescaler selection register								
address: 0xE2					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	PSS1	PSS3	-	-	-	-	PSR3	PSR1
R / W	R / W	R / W	-	-	-	- R / W		R / W

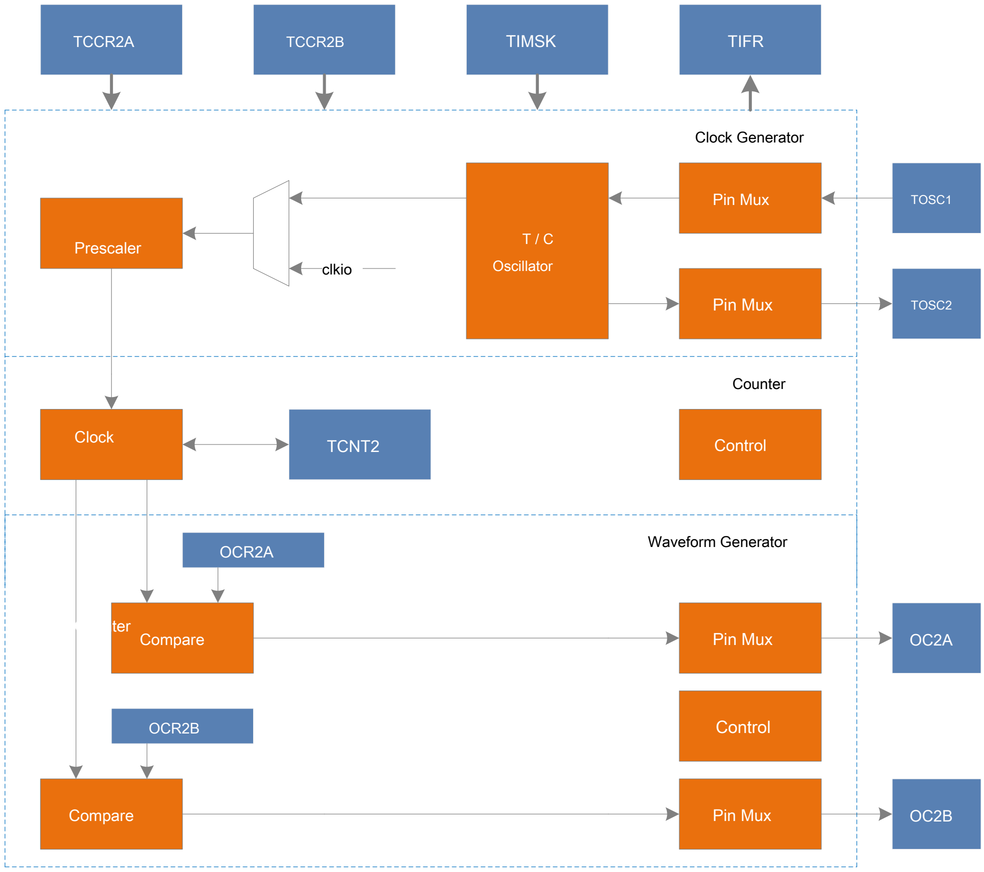
Bit	Name	description
7	PSS1	Prescaler select bit. When set PSS1 Bit "1" Time, TC1 Prescaler is used alone CPS1 . When set PSS1 Bit "0" When, for the prescaler multiplexed mode. TC0 with TC1 Shared prescaler CPS310 . Prescaler CPS1 Invalid, it will have to be reset. If the PSS3 Bit at the same time "0" , TC3 with TC0 , TC1 Shared prescaler CPS310 . Prescaler CPS1 with CPS3 They are invalid and will always be reset.
6	PSS3	Prescaler select bit. When set PSS3 Bit "1" Time, TC3 Prescaler is used alone CPS3 .

		When set PSS3 Bit "0" When, for the prescaler multiplexed mode. TC0 with TC3 Shared prescaler CPS310 . Prescaler CPS3 Invalid, it will have to be reset. If the PSS1 Bit at the same time "0" , TC1 with TC0 , TC3 Shared prescaler CPS310 . Prescaler CPS1 with CPS3 They are invalid and will always be reset.
5: 2	-	Reservations.
1	PSR3	Prescaler CPS3 Reset control bits. PSR3 Bit only TC3 Active alone mode. When set PSR3 Bit "1" When, prescaler CPS3 It will be reset. After hardware reset will clear PSR3 Bit. When set PSR3 Bit "0" When the setting is invalid. Read this value will always be a "0" .
0	PSR1	Prescaler CPS1 Reset control bits. PSR1 Bit only TC1 Active alone mode. When set PSR1 Bit "1" When, prescaler CPS1 It will be reset. After hardware reset will clear PSR1 Bit. When set PSR1 Bit "0" When the setting is invalid. Read this value will always be a "0" .

Timer / Counter 2 (TMR2)

- 8 Bit counter
- Two independent comparing unit
- The counter is automatically cleared when compare match occurs and automatically loads
- No disturb pulse phase correction PWM Export
- Frequency generator
- External event counter
- 10 Bit clock prescaler
- Overflow and Compare Match Interrupt
- Allows the use of external 32.768KHz of RTC Crystal count

Outline



TC2 Structure chart

TC2 Is a common 8 Bit timer counter module support PWM Output waveform can be generated accurately. TC2 contain 1 More 8 Bit counter, and a waveform generation mode control unit 2 Output comparison unit. Waveform generating mode generates the control unit controls the operation mode of the counter and comparing the output waveform. Depending on the mode of operation, a counter for counting each clock Clkt2 Cleared, incremented or decremented. Clkt2 It may be generated by an internal clock or an external clock source. When using an external 32.768KHz When the count of the crystal, TC2 Can be used RTC counter. When the count value of the counter TCNT2

It reached its maximum value (equal to the maximum value 0xFF Or output compare register OCR2A ,defined as TOP , The maximum value of the definition MAX When to distinguish), the counter is cleared or decremented. When the count value of the counter TCNT2 Reaches a minimum value (equal to 0x00 ,defined as BOTTOM), The counter will be incremented by one operation. When the count value of the counter TCNT2 Arrivals
OCR2A / OCR2B When, also referred to compare match, set or cleared by the output signal of the comparison OC2A / OCR2B To produce PWM Waveform.

Operating mode

Timing counter 2 There are four different operating modes, including normal mode (Normal), Cleared on compare match (CTC) Mode, fast pulse width modulation (FPWM) Mode and a phase correction pulse width modulation (PCPWM) Mode, the mode control bits generated by the waveform WGM2 [2: 0] To choose. The following four modes will be described specifically. Since there are two separate output of the comparison unit, respectively "A" with "B" Represented by lowercase "X" To represent the two channel outputs the comparison unit.

Normal mode

Normal mode timer counter is the simplest mode of operation, this time waveform generation mode control bit WGM2 [2: 0] = 0 Count maximum value TOP for MAX (0xFF). In this mode, a counting mode for each clock count plus an increment, when the counter reaches TOP After the spill back BOTTOM Re-start accumulating. The count value TCNT2 The same count clock becomes zero set timer counter's overflow flag TOV2 . In this mode TOV2 The first sign is like 9 Count bit, but will only be set is not cleared. Overflow interrupt service routine will automatically clear TOV2 Logos, software can use it to improve the resolution of the timer counter. Normal mode is not to be considered a special case, a new count value can be written at any time. Set up OC2x Pin data direction register as an output a comparison signal to obtain an output OC2x Waveform. when COM2x = 1

When, flips compare match OC2x Signal, in this case the frequency waveform may be calculated using the following formula:

$f_{oc2xnormal} = f_{sys} / (2 * N * 256)$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024).

Output Compare unit can be used to generate interrupts, but does not recommend the use of interrupts in the normal mode, it will take up too much CPU time.

CTC mode

Set up WGM2 [2: 0] = 2 When the timer counter 2 enter CTC Max mode, counting TOP for OCR2A . In this mode, a counting mode for each clock count plus an increment, when the value of the counter TCNT2 equal TOP When the counter is cleared. OCR2A It defines the maximum count, i.e., the resolution of the counter. This mode allows the user to easily control the frequency of the compare match output also simplifies the operation of the external event count. When the counter reaches a maximum count, an output compare match flag OCF2 Is set, an interrupt will be generated when the corresponding interrupt enable bit is set. Can be updated in the interrupt service routine OCR2A I.e., the maximum count register. In this mode

OCR2A Do not use double buffering, the counter prescaler to work under no or very low prescaler will be updated as close to the maximum value of the minimum time to be careful. If you write OCR2A The value is less than the time TCNT2 When the value of the counter will miss the compare match. Before a match occurs the next comparison, the first counter had counted to TOP And then from BOTTOM
To start counting OCR2A value. And normal mode, as the count value back BOTTOM The count clock in the set TOV2 Mark. Set up OC2x Pin data direction register as an output a comparison signal to obtain an output OC2x Waveform. when COM2x = 1
When, flips compare match OC2x Signal, in this case the frequency waveform may be calculated using the following formula:

$f_{oc2xctc} = f_{sys} / (2 * N * (1 + OCR2A))$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024). As can be seen from the formula, when set OCR2x for 0x0 And when no prescaler, allowing for maximum frequency f_{sys} / 2 The output waveform.

fast PWM mode

Set up WGM2 [2: 0] = 3 or 7 When the timer counter 2 Enter the fast PWM Mode, can be used to generate high frequency PWM Waveform, the counter maximum value TOP Respectively MAX (0xFF)or OCR2A . fast PWM Patterns and other PWM Except that it is a one-way mode operation. Counter from the minimum 0x00 To accumulate TOP Then came back BOTTOM Re-count. When the count value TCNT2 Arrivals OCR2x or BOTTOM , The output signal of the comparison OC2x It will be set or cleared, depending on the comparison output mode COM2x Setting, as detailed register description. Since the one-way operation, fast PWM Operating frequency of the phase correction mode is employed bi-directionally operable PWM Double mode. It makes the fast frequency PWM Mode is suitable for power regulation, rectification and DAC application. High-frequency signal can be reduced external components (capacitors, inductors) in size, thereby reducing system cost.

When the count value reaches the maximum value, the timer counter overflow flag TOV2 It will be set, and the updated buffer value comparison value to the comparator. If enabled, the interrupt service routine can be updated relatively buffer OCR2x register. Set up OC2x Pin data direction register as an output a comparison signal to obtain an output OC2x Waveform. Frequency of the waveform following formula can be calculated:

$$f_{oc2xfpwm} = f_{sys} / (N * (1 + TOP))$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024). when TCNT2 with OCR2x Compare match, the waveform generator to set (clear) OC2x Signal, when TCNT2 When cleared, the waveform generator will be cleared (set) OC2x Signal in order to produce PWM wave. thus OCR2x The extremes will produce special PWM Waveform. when OCR2x Set as 0x00 , The output of PWM For each (1 + TOP) There is a clock count of a narrow spike. when OCR2x When set to the maximum value, the output waveform for sustained high or low.

Phase correction PWM mode

When set WGM2 [2: 0] = 1 or 5 When the timer counter 2 Enter phase correction PWM Max mode, counting TOP Respectively MAX (0xFF)or OCR2A . Bidirectional counter operation by BOTTOM Increments to TOP And then descending to BOTTOM , Then repeat this operation. Count reaches TOP with BOTTOM Have to change direction when the count value TOP or BOTTOM On average only stay a count clock. In the process increments or decrements the count value TCNT2 versus OCR2x Match, the comparison signal output OC2x It will be set or cleared, depending on the comparison output mode COM2x setting. Compared with the one-way operation, bidirectional operation obtainable maximum operation frequency, but its excellent symmetry is more suitable for motor control. Phase correction PWM Mode, when the count reaches BOTTOM When set TOV2 Flag when the count reaches TOP When the buffer is updated to compare the value of the comparison value. If enabled, the interrupt service routine can be updated relatively buffer OCR2x register. Set up OC2x Pin data direction register as an output a comparison signal to obtain an output OC2x Waveform. Frequency of the waveform following formula can be calculated:

$$f_{oc2xpcpwm} = f_{sys} / (N * TOP * 2)$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024). In up-counting process, when TCNT2 versus OCR2x Match, the waveform generator will be cleared (set) OC2x signal. In the process of counting down, when TCNT2 versus OCR2x When the match is set to the waveform generator (clear) OC2x signal. thus OCR2x The extremes will produce a special PWM wave. when OCR2x When set to the maximum or minimum value, OC2x Output signal will remain low or high.

In order to ensure that the output PWM Wave symmetry of both sides of the minimum value, a compare match does not occur, there will be two cases flipping OC2x signal. The first case is when OCR2x Value by the maximum value 0xFF When changes to other data. when OCR2x The maximum value, the count value reaches the maximum, OC2x The same output result of the comparison in the previous match count in descending, i.e. holding OC2x constant. At this value will be updated relatively new OCR2x The value of the (non 0xFF), OC2x The value will remain until

Matching comparison to overturn when ascending count. at this time OC2x Signal to the minimum value as the center is not symmetrical, requiring the TCNT2 Flip reaches the maximum value OC2x Signal, namely when the comparator inverting no match occurs OC2x A first of the signal. The second case is when TCNT2 From the ratio OCR2x Counting high value, and thus will miss the compare match, thereby causing an asymmetric situation generated. Also you need to flip OC2x Signal to achieve symmetry of both sides of the minimum.

TC2 The asynchronous mode of operation

When located ASSR Register AS2 Bit "1" Time, TC2 Work in asynchronous mode, the clock source outside the oscillator from the counter timer counter. In asynchronous mode TC2 Operating considerations must be taken.

- Switch between synchronous and asynchronous mode may cause TCNT2 , OCR2A , OCR2B , TCCR2A with TCCR2B Corrupted data. Safe operation steps are as follows:

  1. Clear OCIE2A , TOIE2 with OCIE2B Close register bit TC2 Break;
  2. Position AS2 Bit selects the appropriate clock source;
  3. Correct TCNT2 , OCR2A , TCCR2A , OCR2B with TCCR2B Register write new data;
  4. When switched to the asynchronous mode, wait TCN2UB , OCR2AUB , TCR2AUB , OCR2BUB with TCR2BUB Place Clear;
  5. Clear TC2 Interrupt flag;
  6. Enable interrupts to be used.

- Oscillator is best to use 32.768KHz Watch crystal. The system clock frequency must be higher than the crystal frequency 4 More times.
- CPU write TCNT2 , OCR2A , TCCR2A , OCR2B with TCCR2B When the hardware if the data first into the register, two TOSC1 After the rising edge of the latch clock to the corresponding register. Can not be performed before the new data is written in the data latch operation from the register to the destination register. Each register has its own independent temporary register, write TCNT2 And does not interfere with write OCR2 . Asynchronous Status Register ASSR For checking whether the data has been written to the destination register.
- If you use TC2 As a MCU Sleep mode wake-up condition, the update before the end of each register can not enter hibernation mode, or else MCU Might TC2 Before entering Sleep mode settings to take effect, so TC2 You can not wake up the system.

- If you use TC2 As a MCU Sleep mode wake-up condition, we must pay attention to the process of re-entering sleep mode. Interrupt logic needs one TOSC1 Reset clock cycle, if the time is less than the wake-up from re-entering a sleep TOSC1 Clock cycle, the interrupt will not occur, the device can not wake up. Recommended operating method is as follows:

  1. Suitable for each write data register;
  2. wait ASSR The corresponding Update Busy flag is cleared;
  3. Into sleep mode.

- When the asynchronous mode, TC2 The oscillator will always running, except in Power-down mode. Users must note that the settling time of this oscillator can be as long 1 Seconds, therefore, recommended that the user is enabled TC2 After waiting for at least an oscillator 1 Seconds before use TC2 The asynchronous mode of operation.
- Wake Sleep mode asynchronous mode of operation of the process: After the interrupt condition is met, the next timer clock starts wake up process. That is, before the processor can read the counter value of the counter is advanced by at least one clock. Wake-up MCU The interrupt service routine, after the start of execution SLEEP Program after the statement.
- Wake from sleep mode after reading a short time TCNT2 The value may return incorrect data. because TCNT2 By asynchronous TOSC1 Clocked, reads TCNT2 Must be done through an internal system clock synchronized register, synchronization occurs in each TOSC1 The rising edge. The system clock re-activation from the sleep mode wake-up, the read TCNT2 Numerical value before entering the sleep mode until the next TOSC1 The arrival of the rising edge will be updated. Wake from sleep mode TOSC1 Phase completely unpredictable, and wake-up time. Therefore, reading TCNT2

  Recommended sequence of values as follows:

  1. Write any value to OCR2A or TCCR2A ;

2. Wait until the corresponding Update Busy flag is cleared;

3. Read TCNT2 .

- In asynchronous mode, interrupt synchronization requires flag 3 System clock cycles plus 1 Timer cycle. in MCU Causing the counter value may be read interrupt flag is set before the counter advanced by at least one clock. Comparison with the change in the output signal of the timer clock is not synchronized to the system clock.

TC2 Prescaler

TC2 Referred to input clock prescaler clkt2s By located ASSR Register AS2 Internal system clock select bit clkio Or external TOSC1 Clock source, the system defaults to the clock clkio Connected. If the AS2 Position, TC2 By TOSC1 Asynchronous drive. when TOSC1 Pin and TOSC2 An external pin 32.768KHz The watch crystal, TC2 Can be used RTC counter. Not recommended TOSC1 Applying an external clock signal on the pin.

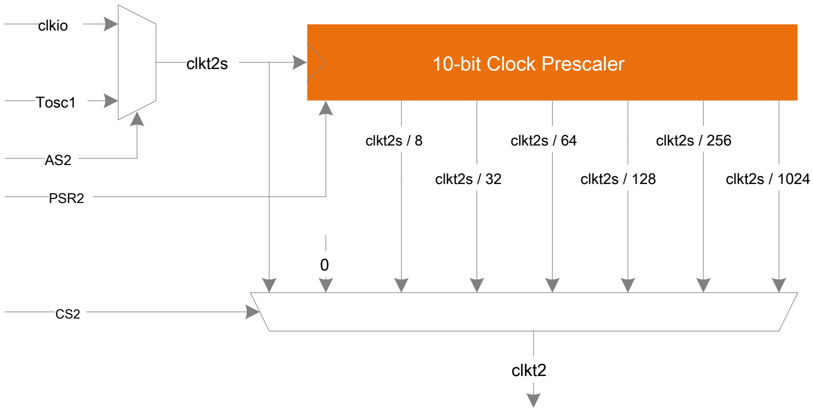


Figure 5 TC2 Prescaler structure diagram

Pictured TC2 Prescaler, as shown in FIG prescaler possible options are: clkt2s / 8, clkt2s / 32, clkt2s / 64, clkt2s / 128, clkt2s / 256, with clkt2s / 1024 . In addition you can also choose clkt2s with 0 (Stop counting). Position SFIOR Register PSR2 The reset bit prescaler, allowing the user to work from a predictable prescaler.

Register Definition

TC2 Register List

register	address	Defaults	description
TCCR2A	0xB0	0x00	TC2 Control register A
TCCR2B	0xB1	0x00	TC2 Control register B
TCNT2	0xB2	0x00	TC2 Count value register
OCR2A	0xB3	0x00	TC2 Output Compare Register A
OCR2B	0xB4	0x00	TC2 Output Compare Register B
ASSR	0xB6	0x00	TC2 Asynchronous Status Register
TIMSK2	0x70	0x00	Timer counter interrupt mask register
TIFR2	0x37	0x00	Timer counter Interrupt Flag Register

TCCR2A-TC2 Control register A

TCCR2 A **-** TC2 Control register A								
address: 0xB0						Defaults: 0x00		
Bit	7	6	5	4	3	2	1	0
	COM2A1	COM2A0	COM2B1	COM2B0	-	-	WGM21	WGM20
R / W	W	R / W	R / W	R / W	-	-	R / W	R / W

Bit	Name	description
7	COM2A1	TC2 Compare Match Output A Mode control high. COM2A1 with COM2A0 Together form the output compare mode control COM2A [1: 0] ,control OC2A The output waveform. in case COM2A of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC2A Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM2A The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
6	COM2A0	TC2 Compare Match Output A Mode control low. COM2A0 with COM2A1 Together form the output compare mode control COM2A [1: 0] ,control OC2A The output waveform. in case COM2A of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC2A Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM2A The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
5	COM2B1	TC2 Compare Match Output B Mode control high. COM2B1 with COM2B0 Together form the output compare mode control COM2B [1: 0] ,control OC2B The output waveform. in case COM2B of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC2B Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM2B The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
4	COM2B0	TC2 Compare Match Output B Mode control low. COM2B0 with COM2B1 Together form the output compare mode control COM2B [1: 0] ,control OC2B The output waveform. in case COM2B of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC2B Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM2B The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
3: 2	-	Reservations.
1	WGM21	TC2 Waveform generation mode control high. WGM20 with WGM21 , WGM22 Together form waveform generation mode control WGM2 [2: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
0	WGM20	TC2 Waveform generation mode control low. WGM21 with WGM20 , WGM22 Together form waveform generation mode control WGM2 [2: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.

TCCR2B -TC2 Control register B

TCCR2B - TC2 Control register B								
address: 0xB1					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	FOC2A	FOC2B	-	-	WGM22	CS22	CS21	CS20
R / W	W	W	-	-	R / W	R / W	R / W	R / W

Bit	Name	description
7	FOC2A	TC2 Force Output Compare A Control bit. In non PWM Mode, the force output by comparing bits FOC2A write "1" The way to compare match. Forcing compare match will not set OCF2A Flag or reload or clear the timer, but the output pin OC2A Will be in accordance with COM2A It sets the appropriate update, just compare match had really happened. Read FOC2A The return value is always zero.
6	FOC2B	TC2 Force Output Compare B Control bit. In non PWM Mode, the force output by comparing bits FOC2B write "1" The way to compare match. Forcing compare match will not set OCF2B Flag or reload or clear the timer, but the output pin OC2B Will be in accordance with COM2B It sets the appropriate update, just compare match had really happened. Read FOC2B The return value is always zero.
5: 4	-	Reservations.
3	WGM22	TC2 Waveform generation mode control high. WGM22 with WGM20 , WGM21 Together form waveform generation mode control WGM2 [2: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
2	CS22	TC2 Clock control high. For selecting a timing counter 2 The clock source.
1	CS21	TC2 Clock selection control bits. For selecting a timing counter 2 The clock source.
0	CS20	TC2 Clock control low. For selecting a timing counter 2 The clock source.

CS2 [2: 0]	description
0	No clock source, stops counting
1	clk_{t2s}
2	clk_{t2s} / 8 From prescaler
3	clk_{t2s} / 32 From prescaler
4	clk_{t2s} / 64 From prescaler
5	clk_{t2s} / 128 From prescaler
6	clk_{t2s} / 256 From prescaler
7	clk_{t2s} / 1024 From prescaler

The following table non PWM Mode (ie, normal mode and CTC Mode), the comparison output of the comparator mode control output waveform.

Table 1 non- PWM Mode OC2x Compare output mode control

COM2x [1: 0]	description
0	OC2x Disconnect, GM IO Port operations
1	Flip compare match OC2x signal
2	Clear compare match OC2x signal
3	When set compare match OC2x signal

The following table fast PWM Mode mode control comparator output waveform of the output comparator.

Table 2 fast PWM Mode OC2x Compare output mode control

COM2x [1: 0]	description
0	OC2x Disconnect, GM IO Port operations
1	Retention
2	Clear compare match OC2x Signal is set to match the maximum value OC2x signal
3	When set compare match OC2x Signal is cleared when the maximum matching OC2x signal

The following table shows the comparison output of the phase correction mode the mode control output of the comparator waveform.

Table 3 Phase correction PWM Mode OC2x Compare output mode control

COM2x [1: 0]	description
0	OC2x Disconnect, GM IO Port operations
1	Retention
2	Cleared when the match count comparator ascending OC2x Signal, the match count comparator descending Set OC2x signal
3	Ascending count comparator match the set OC2x Signal is cleared when the match count comparator DESC OC2x signal

The following table is a waveform generation mode control.

Table 4 Waveform Generation Mode Control

WGM2 [2: 0]	Operating mode	TOP Value	update OCR2x Time	set TOV2 time
0	Normal	0xFF	immediately	MAX
1	PCPWM	0xFF	TOP	BOTTOM
2	CTC	OCR2A	immediately	MAX
3	FPWM	0xFF	TOP	MAX
4	Retention	-	-	-
5	PCPWM	OCR2A	TOP	BOTTOM
6	Retention	-	-	-
7	FPWM	OCR2A	TOP	TOP

TCNT2 -TC2 Count value register

TCNT2 - TC2 Count value register								
address: 0xB2					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	TCNT27	TCNT26	TCNT25	TCNT24	TCNT23	TCNT22	TCNT21	TCNT20 R / W
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	TCNT2	TC2 Count value register. by TCNT2 Directly to the counter register 8 Read and write access to the counter value. CPU Correct TCNT2 Write to register on the next timer clock cycle to prevent the occurrence of compare match, even if the timer has stopped. This allows initialization TCNT2 And the value of the register OCR2 The value of the agreement without causing disruption. If you write TCNT2 The value is equal to or bypassed OCR2 Value, compare match will be lost, resulting in incorrect waveform generation. When the timer stops counting the clock source is not selected, but CPU Still access TCNT2 . CPU Write counter is cleared or a higher priority than addition and subtraction operations.

OCR2A - TC2 Output Compare Register A

OCR2A - TC2 Output Compare Register A								
address: 0xB3					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR2A7	OCR2A6	OCR2A5	OCR2A4	OCR2A3	OCR2A2	OCR2A1	OCR2A0 R / WR / W
		R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	OCR2A	TC2 Output Compare Register A . OCR2A It contains a 8 Bit data, with the counter value continuously TCNT2 Compare. Compare match can be used to generate an output compare interrupt, or to the OC2A Waveform generation pins. When PWM When mode, OCR2A Using double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR2A Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR2A When the buffer register, double buffering is disabled CPU Access is OCR2A itself.

OCR2B - TC2 Output Compare Register B

OCR2B - TC2 Output Compare Register B								
address: 0xB4					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR2B7	OCR2B6	OCR2B5	OCR2B4	OCR2B3	OCR2B2	OCR2B1	OCR2B0 R / W
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	OCR2B	TC2 Output Compare B register. OCR2B It contains a 8 Bit data, with the counter value continuously TCNT2 Compare. Compare match can be used to generate an output compare interrupt, or to the OC2B Waveform generation pins. When PWM When mode, OCR2B Using double buffered registers. The normal operating mode and match clear mode, double buffering function is disabled. Double buffering may be updated OCR2B Register with the maximum or minimum count up the time synchronization, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR2B When the buffer register, double buffering is disabled CPU Access is OCR2B itself.

TIMSK2 - TC2 Interrupt mask register

TIMSK2 - TC2 Interrupt mask register								
address: 0x70					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	OCIE2B	OCIE2A	TOIE2
R / W	-	-	-	-	-	R / W	R / W	R / W

Bit	Name	description
7: 3		Reservations.
2	OCIE2B	TC2 Output Compare B Match interrupt enable bit. when OCIE2B Bit "1" And Global Interrupt Set, TC2 Output Compare B Match interrupt is enabled. When a compare match occurs, i.e., TIFR2 in OCF2B When the bit is set, an interrupt is generated. when OCIE2B Bit "0" Time, TC2 Output Compare B Match interrupts are disabled.
1	OCIE2A	TC2 Output Compare A Match interrupt enable bit. when OCIE2A Bit "1" And Global Interrupt Set, TC2 Output Compare A Match interrupt is enabled. When a compare match occurs, i.e., TIFR2 in OCF2A When the bit is set, an interrupt is generated. when OCIE2A Bit "0" Time, TC2 Output Compare A Match interrupts are disabled.
0	TOIE2	TC2 Overflow interrupt enable bit. when TOIE2 Bit "1" And Global Interrupt Set, TC2 Overflow interrupt is enabled. when TC2 Overflow occurs, that is, TIFR2 middle TOV2 When the bit is set, an interrupt is generated. when TOIE2 Bit "0" Time, TC2 Overflow interrupts are disabled.

TIFR2 - TC2 Interrupt Flag Register

TIFR2 - TC2 Interrupt Flag Register								
address: 0x37					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	OCF2B	OCF2A	TOV2
R / W	-	-	-	-	-	R / W	R / W	R / W

Bit	Name	description
7: 3	-	Reservations.
2	OCF2B	TC2 Output Compare B Matching flag.

		when TCNT2 equal OCR2B , The comparison unit signals a match, the comparison flag is set and OCF2B . If the output of the comparator at this time B Interrupt Enable OCIE2B for "1" And the Global interrupt flag is set, it will produce output compare B Interrupted. When you do this the interrupt service routine OCF2B Will be automatically cleared or OCF2B Write bit "1" Also clears the bit.
1	OCF2A	TC2 Output Compare A Matching flag. when TCNT2 equal OCR2A , The comparison unit signals a match, the comparison flag is set and OCF2A . If the output of the comparator at this time A Interrupt Enable OCIE2A for "1" And the Global interrupt flag is set, it will produce output compare A Interrupted. When you do this the interrupt service routine OCF2A Will be automatically cleared or OCF2A Write bit "1" Also clears the bit.
0	TOV2	TC2 Overflow flag. When the counter overflows, the overflow flag is set TOV2 . If this time overflow interrupt enable TOIE2 for "1" And the Global interrupt flag is set, it will generate an overflow interrupt. When you do this the interrupt service routine TOV2 Will be automatically cleared or TOV2 Write bit "1" Also clears the bit.

ASSR - Asynchronous Interface Status Register

***ASSR* - TC2 Asynchronous Interface Status Register**								
address: 0xB6					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	INTCK	-	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB
R / W	R / W	-	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	INTCK	Asynchronous clock selection control bits. When set INTCK Bit 1 , The internal selection RC32K An asynchronous clock source. When set INTCK Bit 0 When selecting the external asynchronous crystal clock as the clock source.
6	-	Reservations.
5	AS2	Timer 2 Asynchronous mode selection control bits. When set AS2 Bit 1 When the timer 2 Work for asynchronous mode, clock source INTCK Bits to select. When set AS2 Bit 0 When the timer 2 Working synchronous mode, the clock source Clk_{io} . when AS2 The value changes, TCNT2 , OCR2A , OCR2B , TCCR2A with TCCR2B Value of the register may be incorrect, you need to be reconfigured.
4	TCN2UB	TCNT2 Register update flag. When the timer 2 Work in asynchronous mode, for TCNT2 When a write operation, TCN2UB Bit is set. when TCNT2 After the updated value of the hardware will be cleared TCN2UB Bit. Only when TCN2UB Bit 0 When, available for TCNT2 Updated.
3	OCR2AUB	OCR2A Register update flag. When the timer 2 Work in asynchronous mode, for OCR2A When a write operation, OCR2AUB Bit is set. when OCR2A After the updated value of the hardware will be cleared OCR2AUB Bit. Only when OCR2AUB Bit 0 When, available for OCR2A Updated.
2	OCR2BUB	OCR2B Register update flag. When the timer 2 Work in asynchronous mode, for OCR2B When a write operation, OCR2BUB Bit is set. when OCR2B After the updated value of the hardware will be cleared OCR2BUB Bit. Only when OCR2BUB Bit 0 When, available for OCR2B Updated.

1	TCR2AUB	TCCR2A Register update flag. When the timer 2 Work in asynchronous mode, for TCCR2A When a write operation, TCR2AUB Bit is set. when TCCR2A After the updated value of the hardware will be cleared TCR2AUB Bit. Only when TCR2AUB Bit 0 When, available for TCCR2A Updated.
0	TCR2BUB	TCCR2B Register update flag. When the timer 2 Work in asynchronous mode, for TCCR2B When a write operation, TCR2BUB Bit is set. when TCCR2B After the updated value of the hardware will be cleared TCR2BUB Bit. Only when TCR2BUB Bit 0 When, available for TCCR2B Updated.

Timer / Counter 3 (TMR3)

- truly 16 Digital design, allowing 16 Bit PWM
- 3 Separate outputs the comparison unit
- Double buffered output compare register
- 1 Input capture unit
- Input Capture Noise Suppressor
- The counter is automatically cleared when compare match and automatically load
- No disturb pulse phase correction PWM
- Variable PWM cycle
- Frequency generator
- External event counter
- 5 Independent interrupt sources
- With dead-time control
- 6 Selectable trigger source automatically shut down PWM Export

Outline

TC3 Is a common 16 Bit timer counter module support PWM Output waveform can be generated accurately. TC3 contain 1 More 16 Bit counter, waveform generation mode control unit, 2 Separate outputs and the comparison unit 1 Input capture unit. Waveform generating mode generates the control unit controls the operation mode of the counter and comparing the output waveform. Depending on the mode of operation, a counter for counting each clock Clkt3 Cleared, incremented or decremented. Clkt3 It may be generated by an internal clock or an external clock source. When the count value of the counter TCNT3 It reached its maximum value (equal to the maximum value 0xFFFF Or a fixed value or output compare register OCR3A Or the input capture register ICR3 ,defined as TOP , The maximum value of the definition MAX When to distinguish), the counter is cleared or decremented. When the count value of the counter TCNT3 Reaches a minimum value (equal to 0x0000 ,defined as BOTTOM), The counter will be incremented by one operation. When the count value of the counter TCNT3 Arrivals OCR3A or OCR3B or OCR3C When, also referred to compare match, set or cleared by the output signal of the comparison OC3A or OC3B or OC3C To produce PWM Waveform. When the input capture function is turned on, i.e. the counter is activated to start or stop counting, ICR3 Register records the captured count values trigger period signal.

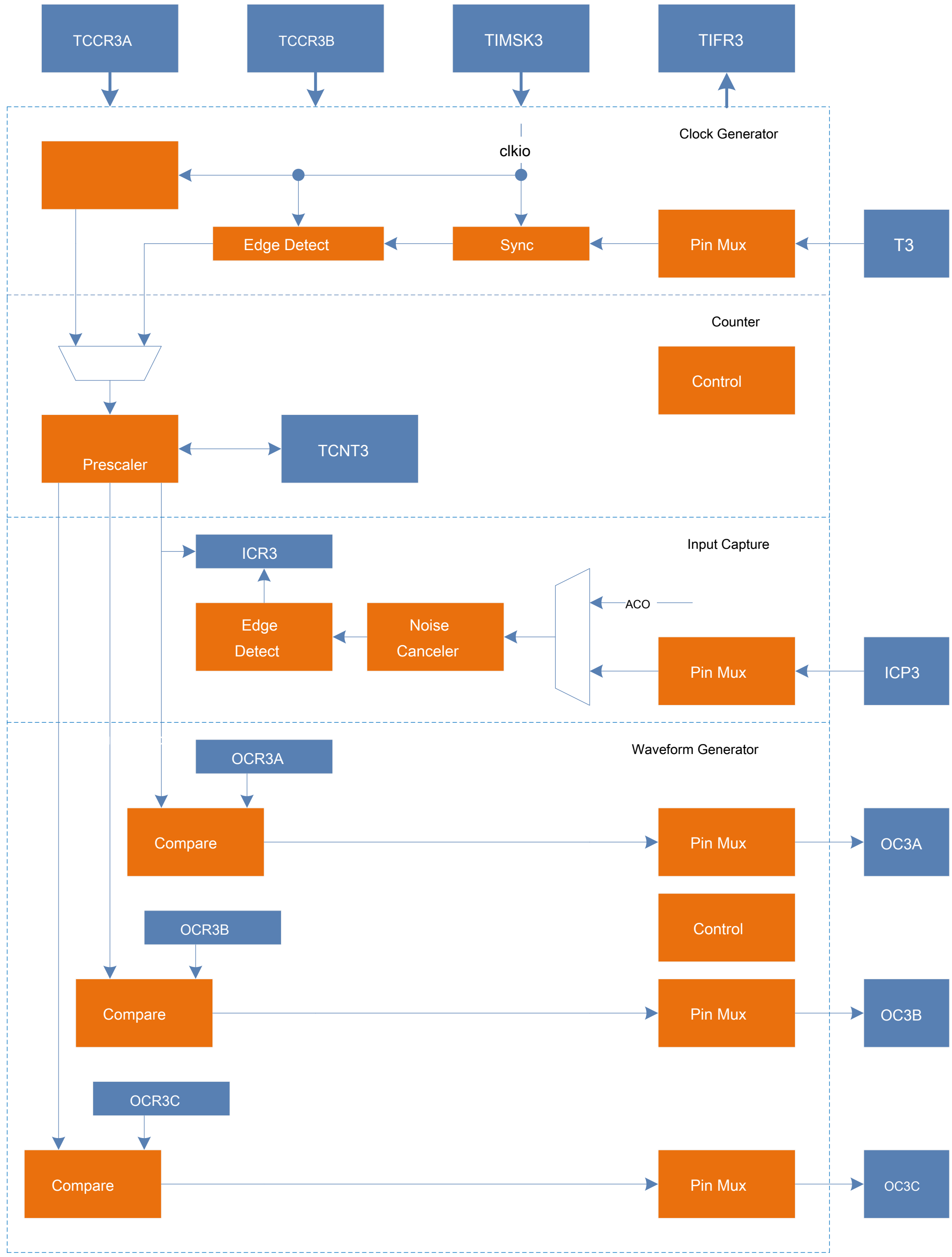


Figure 6 TC3 Structure chart

Operating mode

Timing counter 1 There are six different modes, including normal mode (Normal), Cleared on compare match (CTC) Mode, fast pulse width modulation (FPWM) Mode, a phase correction pulse width modulation (PCPWM) Mode, a phase correction pulse width modulation frequency (PFCPWM) Mode, and input capture (ICP)mode. Mode control bit is generated by the waveform

WGM3 [3: 0] To choose. This is described in detail below six modes. Since there are three separate output of the comparison unit, respectively "A" , "B" with "C" Represented by lowercase "X" To represent the two channel outputs the comparison unit.

Normal mode

Normal mode timer counter is the simplest mode of operation, this time waveform generation mode control bit WGM3 [3: 0] = 0 Count maximum value TOP for MAX (0xFFFF). In this mode, a counting mode for each clock count plus an increment, when the counter reaches TOP After the spill back BOTTOM Re-start accumulating. The count value TCNT3 The same count clock becomes zero set timer counter's overflow flag TOV3 . In this mode TOV3 The first sign is like 17 Count bit, but will only be set is not cleared. Overflow interrupt service routine will automatically clear TOV3 Logos, software can use it to improve the resolution of the timer counter. Normal mode is not to be considered a special case, a new count value can be written at any time.

Set up OC3x Pin data direction register as an output a comparison signal to obtain an output OC3x Waveform. when COM3x = 1 When, flips compare match OC3x Signal, in this case the frequency waveform may be calculated using the following formula:

$$f_{OC3xnormal} = f_{sys} / (2 * N * 65536)$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024).

Output Compare unit can be used to generate interrupts, but does not recommend the use of interrupts in the normal mode, it will take up too much CPU time.

CTC mode

Set up WGM3 [3: 0] = 4 or 12 When the timer counter 1 enter CTC mode. when WGM3 [3] = 0 The count maximum TOP for OCR3A , when WGM3 [3] = 1 The count maximum TOP for ICR3 . Below WGM3 [3: 0] = 4 As an example to describe CTC Mode In this mode, a counting mode for each clock count plus an increment, when the value of the counter TCNT3 equal TOP When the counter is cleared. This mode allows the user to easily control the frequency of the compare match output also simplifies the operation of the external event count.

When the counter reaches TOP = OCR3A Output Compare match flag OCF3A Is set, when the counter reaches TOP = ICR3 Output Compare match flag ICF3 Is set, an interrupt will be generated when the corresponding interrupt enable bit is set. Can be updated in the interrupt service routine OCR3A register. In this mode OCR3A Do not use double buffering, the counter prescaler to work under no or very low prescaler will be updated as close to the maximum value of the minimum time to be careful. If you write OCR3A The value is less than the time TCNT3 When the value of the counter will miss the compare match. Before a match occurs the next comparison, the first counter had counted to MAX And then from BOTTOM To start counting OCR3A . And normal mode, as the count value back 0x0 The count clock in the set TOV3 Mark.

Set up OC3x Pin data direction register as an output a comparison signal to obtain an output OC3x Waveform. Frequency waveform may be calculated using the following formula:

$$f_{OC3xctc} = f_{sys} / (2 * N * (1 + OCR3A))$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024). As can be seen from the formula, when set OCR3A for 0x0 And when no prescaler, allowing for maximum frequency $f_{sys} / 2$ The output waveform.

when WGM3 [3: 0] = 12 When the WGM3 [3: 0] = 4 Similarly, just and OCR3A Related replaced ICR3 It can be.

fast PWM mode

Set up WGM3 [3: 0] = 5 , 6 , 7 , 14 or 15 When the timer counter 1 Enter the fast PWM Mode, the maximum count TOP Respectively 0xFF , 0x1FF , 0x3FF , ICR3 or OCR3A , It can be used to generate high frequency PWM Waveform. fast PWM

Patterns and other PWM Except that it is a one-way mode operation. From the counter BOTTOM To accumulate TOP Then came back BOTTOM Re-count. When the count value TCNT3 Arrivals TOP or BOTTOM , The output signal of the comparison OC3x It will be set or cleared, depending on the comparison output mode COM3 Setting, as detailed register description. Since the one-way operation, fast PWM Operating frequency of the phase correction mode is employed bi-directionally operable PWM Double mode. It makes the fast frequency PWM Mode is suitable for power regulation, rectification and DAC application. High-frequency signal can be reduced external components (capacitors, inductors) in size, thereby reducing system cost.

When the count value reaches TOP When the timer counter overflow flag TOV3 It will be set, and the updated buffer value comparison value to the comparator. If enabled, can be updated in the interrupt service routine OCR3A register.

Set up OC3x Pin data direction register as an output a comparison signal to obtain an output OC3x Waveform. Frequency of the waveform following formula can be calculated:

$f_{OC3xfpwm} = f_{sys} / (N * (1 + TOP))$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024).

when TCNT3 with OCR3x Compare match, the waveform generator to set (clear) OC3x Signal, when TCNT3 When cleared, the waveform generator will be cleared (set) OC3x Signal in order to produce PWM wave. thus OCR3x The extremes will produce special PWM Waveform. when OCR3x Set as 0x00 , The output of PWM For each (1 + TOP) There is a clock count of a narrow spike. when OCR3x Set as TOP Waveform, the output is continuously high or low. If you use OCR3A As a TOP And set COM3A = 1 , The comparator output signal OC3A It will have a duty cycle of 50% of PWM wave.

Phase correction PWM mode

When set WGM3 [3: 0] = 1 , 2 , 3 , 10 or 11 When the timer counter 1 Enter phase correction PWM Max mode, counting TOP Respectively 0xFF , 0x1FF , 0x3FF , ICR3 or OCR3A . Bidirectional counter operation by BOTTOM Increments to TOP And then descending to BOTTOM , Then repeat this operation. Count reaches TOP with BOTTOM Have to change direction when the count value TOP or BOTTOM On average only stay a count clock. In the process increments or decrements the count value TCNT3 versus OCR3x Match, the comparison signal output OC3x It will be set or cleared, depending on the comparison output mode COM3 setting. Compared with the one-way operation, bidirectional operation obtainable maximum operation frequency, but its excellent symmetry is more suitable for motor control.

Phase correction PWM Mode, when the count reaches BOTTOM When set TOV3 Flag when the count reaches TOP When the buffer is updated to compare the value of the comparison value. If enabled, the interrupt service routine can be updated relatively buffer OCR3x Register.

Set up OC3x Pin data direction register as an output a comparison signal to obtain an output OC3x Waveform. Frequency of the waveform following formula can be calculated:

$f_{OC3xcpcpwm} = f_{sys} / (N * TOP * 2)$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024).

In up-counting process, when TCNT3 versus OCR3x Match, the waveform generator will be cleared (set) OC3x signal. In the process of counting down, when TCNT3 versus OCR3x When the match is set to the waveform generator (clear) OC3x signal. thus OCR3x The extremes will produce a special PWM wave. when OCR3x Set as TOP or BOTTOM Time, OC3x Signal output

Out will remain low or high. If you use OCR3A As a TOP And set COM3A = 1 , The comparator output signal

OC3A It will have a duty cycle of 50% of PWM wave.

In order to ensure that the output PWM Wave BOTTOM Symmetry on both sides, a compare match does not occur, there will be two cases flipping OC3x signal. The first case is when OCR3x The value of the TOP When changes to other data. when OCR3x

for TOP , The count value reaches TOP Time, OC3x The same output result of the comparison in the previous match count in descending, i.e. holding OC3x constant. At this value will be updated relatively new OCR3x The value of the (non TOP), OC3x Value will remain set until the comparison match occurs ascending counting flip. at this time OC3x Signal to the minimum value as the center is not symmetrical, requiring the TCNT3

Flip reaches the maximum value OC3x Signal, namely when the comparator inverting no match occurs OC3x A first of the signal. The second case is when TCNT3 From the ratio OCR3x Counting high value, and thus will miss the compare match, thereby causing an asymmetric situation generated. Also you need to flip OC3x Signal to achieve symmetry of both sides of the minimum.

Phase frequency correction PWM mode

When set WGM3 [3: 0] = 8 or 9 When the timer counter 1 Into the phase frequency correction PWM Max mode, counting

TOP Respectively ICR3 or OCR3A . Bidirectional counter operation by BOTTOM Increments to TOP And then descending to

BOTTOM , Then repeat this operation. Count reaches TOP with BOTTOM Have to change direction when the count value TOP or

BOTTOM On average only stay a count clock. In the process increments or decrements the count value TCNT3 versus OCR3x Match, the comparison signal output OC3x It will be set or cleared, depending on the comparison output mode COM3 setting. Compared with the one-way operation, bidirectional operation obtainable maximum operation frequency, but its excellent symmetry is more suitable for motor control.

Phase frequency correction PWM Mode, when the count reaches BOTTOM When set TOV3 Flag, and comparing the value of the buffer to update the comparison value, the comparison value is updated frequency correction phase PWM And a phase correction mode PWM The biggest difference mode. If enabled, the interrupt service routine can be updated relatively buffer OCR3x Register. when CPU change TOP That value OCR3A or ICR3 When the value, you must ensure that the new TOP Value is not less than the already in use TOP Value, or compare match will not happen again.

Set up OC3x Pin data direction register as an output a comparison signal to obtain an output OC3x Waveform. Frequency of the waveform following formula can be calculated:

$$f_{OC3xcpfcpwm} = f_{sys} / (N * TOP * 2)$$

among them, N It represents the prescale factor (1 , 8 , 64 , 256 or 1024).

In up-counting process, when TCNT3 versus OCR3x Match, the waveform generator will be cleared (set) OC3x signal. In the process of counting down, when TCNT3 versus OCR3x When the match is set to the waveform generator (clear) OC3x signal. thus OCR3x The extremes will produce a special PWM wave. when OCR3x Set as TOP or BOTTOM Time, OC3x Output signal will remain low or high. If you use OCR3A As a TOP And set COM3A = 1 , The comparator output signal

OC3A It will have a duty cycle of 50% of PWM wave.

because OCR3x Register in BOTTOM Time updates, so TOP Value count ascending and descending on both sides are the same length, it generates the correct frequency and phase are symmetrical waveform.

When using a fixed TOP Value, is preferably used ICR3 Register as a TOP Value, that is set WGM3 [3: 0] = 8 ,at this time

OCR3A Only register used to generate PWM Output. If you want to generate a frequency change PWM Wave, must change TOP value, OCR3A Double buffering characteristics would be more suitable for this application.

Input Capture Mode

Input capture to capture external events and give them a time stamp indicating the time the event occurs, may be performed in front of the counting mode, but used to remove ICR3 As the count value TOP Waveform value generation patterns.

External trigger event occurs by pin ICP3 Input may be realized by an analog comparator unit. When the pin ICP3 Logic level on the output is changed, or the analog comparator ACO Level is changed, and this change in level is input to the capture unit captures input capture is triggered, then 16 Bit count value TCNT3 Data is copied into the input capture register ICR3 While input capture flag ICF3 Set, if ICIE1 Bit "1" , Input Capture Flag generates an Input Capture interrupt.

By setting the Analog Comparator Control and Status Register ACSR The analog comparator input capture control bit ACIC To select the input capture trigger source ICP3 or ACO . It should be noted that the change may cause a trigger source input capture, and therefore must be changed after the trigger source ICF3 To conduct a clearing operation to avoid erroneous results.

Capture Input selection control signal after an optional noise suppressor edge detector, based on the input capture ICES1 Configuration, see whether or not the detected edge trigger condition is met. Noise suppressor is a simple digital filtering, the input signal 4 Samples only when 4 When samples are equal the output value will be the edge detector. By the noise suppressor TCCR3B Register ICNC1 Bit control their enabled or disabled.

When using the input capture function, when ICF3 After being set, should be read as early as possible ICR3 Value of the register, because the next time capture after the event ICR3 The value will be updated. Recommended enable input capture interrupt at any input capture mode, the change count is not recommended during operation TOP value.

Input captured timestamp other features may be used to calculate the frequency and the duty ratio signal, as a trigger event and create a log. Measuring the duty cycle required external signal each time after the capture trigger edge is changed, so read ICR3 After the value of the edge-triggered signal to be changed as soon as possible.

PWM Automatically shutdown and restart of output

When set TCCR3C Register DOC3x Bit is high, PWM When auto-off feature is enabled, the trigger condition is met, the hardware clears the corresponding output COM3x Bits, PWM output signal OC3x And its output pin is disconnected, the switching to a common IO Output achieved PWM Automatically shut down the output. At this time, the state of the output pin by a general IO To control the output.

PWM Off automatically after the output is enabled, which also need to set the trigger conditions from TCCR3D Register DSX3n Bits to select trigger source. Triggered by an analog comparator interrupt, external interrupt, the interrupt pin change and the timer overflow interrupt, please refer to the specific circumstances TCCR3D Register description. Or when a certain trigger source is selected as the trigger condition, in which the interrupt flag is set at the same time, the hardware will be cleared COM3x Bit to close PWM Output.

In the event of a triggering event closed PWM After the output, the timer module is no corresponding interrupt flag, the software needs to know the trigger and the trigger event by source interrupt flag read.

when PWM When the output is automatically switched off and the need to restart output again, the software only needs to be reset COM3x Position to switch OC3x Signal is output to the corresponding pin. It should be noted, occurs automatically shut down after the timer did not stop working, OC3x State of the signal has also been updated. After the software or compare match timer overflows, then set COM3x Bit output OC3x Signal, so you can get a clear PWM Output state.

Dead-time control

Set up DTEN3 Bit "1" When inserting the dead time function is enabled, OC3A with OC3B The output waveform will B Deadtime comparator output channel waveform based on the generated set of insertion, the length of time of DTR3 Register count clock number corresponding to the time value. As shown below, OC3A with OC3B Deadtime insertion are based channel B Comparing the output waveform as a reference. when COM3A with COM3B The same "2" or "3" Time, OC3A The polarity of the waveform OC3B The waveform of the same polarity, when COM3A with COM3B Respectively "2" or "3" Time, OC3A The waveform OC3B Opposite polarity waveform.

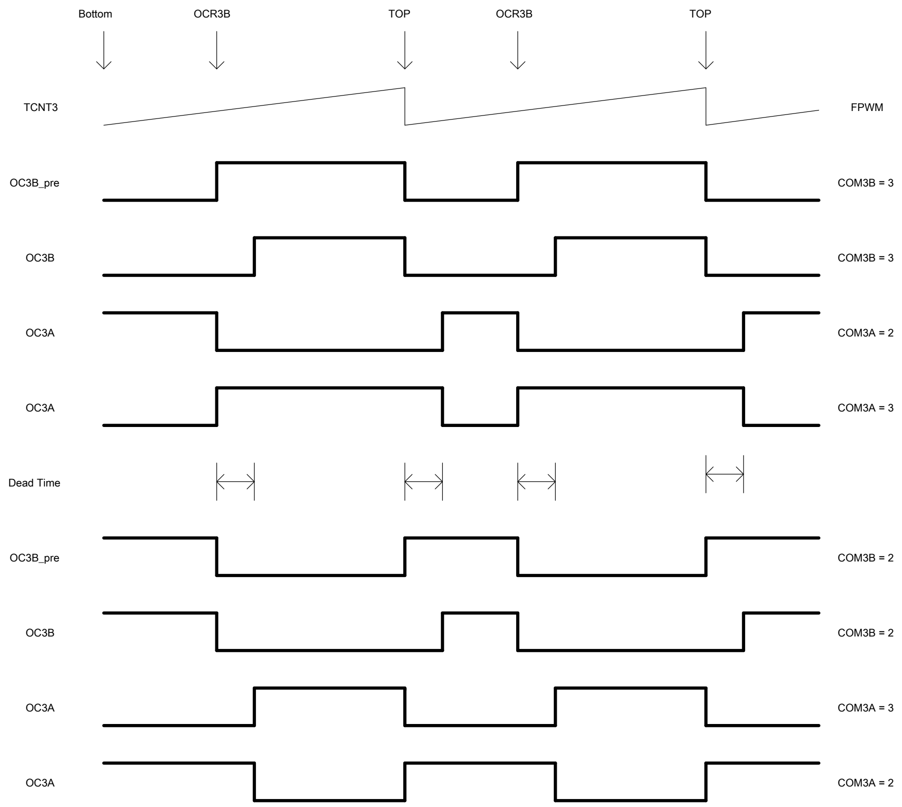


Figure 7 FPWM Mode TC3 Dead-time control

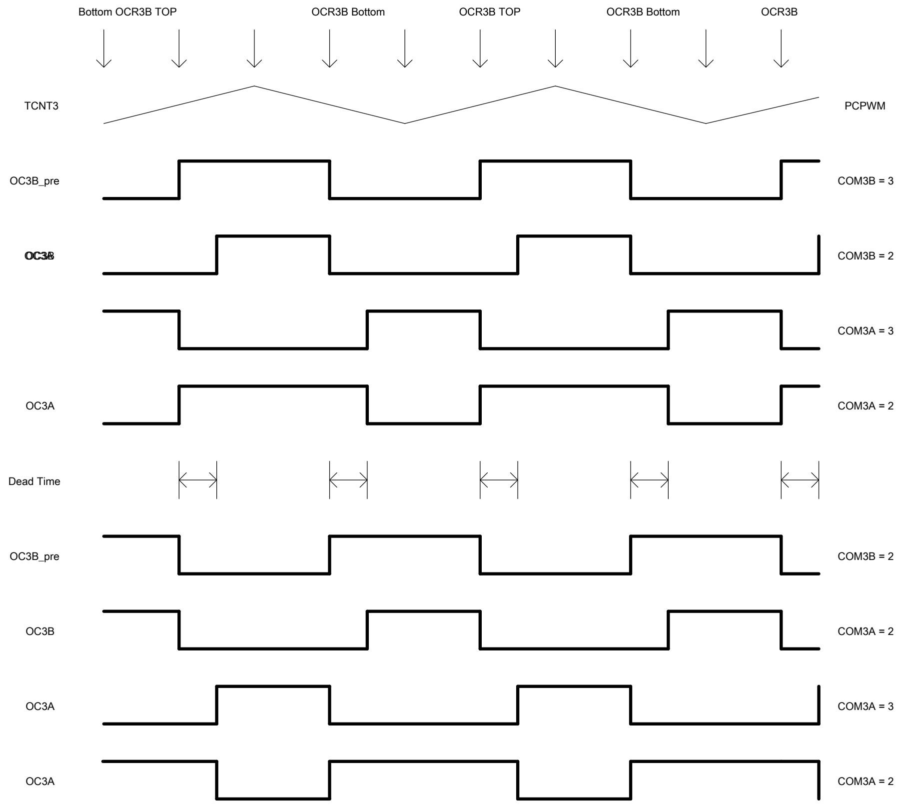


Figure 8 PCPWM Mode TC3 Dead-time control

Set up DTEN3 Bit "0" When inserting the dead time function is disabled, OC3A with OC3B The waveform of the output waveform generated by each comparator output.

Register Definition

TC3 Register List

register	address	Defaults	description
TCCR3A	0x90	0x00	TC3 Control register A
TCCR3B	0x91	0x00	TC3 Control register B
TCCR3C	0x92	0x00	TC3 Control register C
TCCR3D	0x93	0x00	TC3 Control register D
TCNT3L	0x94	0x00	TC3 Low byte count value register
TCNT3H	0x95	0x00	TC3 High byte count value register
ICR3L	0x96	0x00	TC3 Input Capture Register Low Byte
ICR3H	0x97	0x00	TC3 Input Capture MSB
OCR3AL	0x98	0x00	TC3 Output Compare Register A Low byte
OCR3AH	0x99	0x00	TC3 Output Compare Register A High Byte
OCR3BL	0x9A	0x00	TC3 Output Compare Register B Low byte
OCR3BH	0x9B	0x00	TC3 Output Compare Register B High Byte
DTR3L	0x9C	0x00	TC3 Dead Time Register Low Byte
DTR3H	0x9D	0x00	TC3 High byte dead time register
OCR3CL	0x9E	0x00	TC3 Output Compare Register C Low byte

OCR3CH	0x9F	0x00	TC3 Output Compare Register C High Byte
TIMSK3	0x71	0x00	Timer counter interrupt mask register
TIFR3	0x38	0x00	Timer counter Interrupt Flag Register

TCCR3A-TC3 Control register A

TCCR3A - TC3 Control register A								
address: 0x90					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	COM3A1	COM3A0	COM3B1	COM3B0	COM3C1	COM3C0	WGM31	WGM30
R / W	R / W	R / W	R / W	R / W	W	W	R / W	R / W

Bit	Name	description
7	COM3A1	Compare Match Output A Mode control high. COM3A1 with COM3A0 composition COM3A [1: 0] To control the output waveform of comparator OC3A . in case COM3A of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC3A Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM3A The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
6	COM3A0	Compare Match Output A Mode control low. COM3A1 with COM3A0 composition COM3A [1: 0] To control the output waveform of comparator OC3A . in case COM3A of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC3A Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM3A The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
5	COM3B1	Compare Match Output B Mode control high. COM3B1 with COM3B0 composition COM3B [1: 0] To control the output waveform of comparator OC3B . in case COM3B of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC3B Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM3B The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
4	COM3B0	Compare Match Output B Mode control low. COM3B1 with COM3B0 composition COM3B [1: 0] To control the output waveform of comparator OC3B . in case COM3B of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC3B Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM3B The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
3	COM3C1	Compare Match Output C Mode control high. COM3C1 with COM3C0 composition COM3C [1: 0] To control the output waveform of comparator OC3C . in case COM3C of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC3C Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM3C The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
2	COM3C0	Compare Match Output C Mode control low. COM3C1 with COM3C0 composition COM3C [1: 0] To control the output waveform of comparator OC3C . in case

		COM3C of 1 Position or 2 Bits are set, the output waveform of comparator occupies OC3C Pin, but the pin data direction register must be set to a high output from this waveform. In different operating modes, COM3C The control waveform output of the comparator is different, the comparison output mode control specifically see table below.
1	WGM31	Waveform generation mode control times lower. WGM31 with WGM33, WGM32, WGM30 Together form waveform generation mode control WGM3 [3: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
0	WGM30	Waveform generation mode control lowest bit. WGM30 with WGM33, WGM32, WGM31 Together form waveform generation mode control WGM3 [3: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.

The following table non PWM Mode (ie, normal mode and CTC Mode), the comparison output of the comparator mode control output waveform.

non- PWM Compare output mode control mode

COM3x [1: 0]	description
0	OC3x Disconnect, GM IO Port operations
1	Flip compare match OC3x signal
2	Clear compare match OC3x signal
3	When set compare match OC3x signal

The following table fast PWM Mode mode control comparator output waveform of the output comparator.

fast PWM Compare output mode control mode

COM3x [1: 0]	description
0	OC3x Disconnect, GM IO Port operations
1	WGM3 for 15 When: Flip compare match OC3A signal, OC3B disconnect WGM3 When other values: OC3x Disconnect, GM IO Port operations
2	Clear compare match OC3x Signal is set to match the maximum value OC3x signal
3	When set compare match OC3x Signal is cleared when the maximum matching OC3x signal

The following table shows the comparison output of the phase correction mode the mode control output of the comparator waveform.

Phase correction and frequency correction phase PWM Compare output mode control mode

COM3x [1: 0]	description
0	OC3x Disconnect, GM IO Port operations
1	WGM3 for 9 or 11 When: Flip compare match OC3A signal, OC3B disconnect WGM3 When other values: OC3x Disconnect, GM IO Port operations
2	Match clears the count comparator ascending OC3x Signal, the match count comparator arranged in descending order bits OC3x signal
3	Comparison of the configuration bit match count ascending OC3x Down signal, in descending count comparator match clears OC3x signal

TCCR3B-TC3 Control register B

TCCR3B - TC3 Control register B								
address: 0x91					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	ICNC3	ICES3	-	WGM33	WGM32	CS32	CS31	CS30
R / W	R / W	R / W	-	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	ICNC3	Input Capture noise suppressor enable control bit. When set ICNC3 Bit "1" When the enable input capture noise suppressor, when external pin ICP3 The input is filtered continuously 4 Sampling values of the input signal is valid when equal, the function input capture is delayed 4 Clock cycles. When set ICNC3 Bit "0" When prohibit input capture noise suppressor, this time external pin ICP3 Direct and effective input.
6	ICES3	Input Capture Edge Select control bits. When set ICES3 Bit "1" When the rising edge of selection level input capture trigger; provided when ICES3 Bit "0" When selecting the level of the falling edge of the input capture trigger. When a capture is triggered, the counter value is copied into ICR3 Register, while the set input capture flag ICF3 . If the interrupt is enabled, the input capture interrupt.
5	-	Reservations.
4	WGM33	Waveform generation mode control high. WGM33 with WGM32, WGM31, WGM30 Together form waveform generation mode control WGM3 [3: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
3	WGM32	Second uppermost waveform generation mode control. WGM32 with WGM33, WGM31, WGM30 Together form waveform generation mode control WGM3 [3: 0] , Control and counting of the counter waveform generation mode, see the specific waveform generation pattern table is described.
2	CS32	Clock control high. For selecting a timing counter 3 The clock source.
1	CS31	Clock selection control bits. For selecting a timing counter 3 The clock source.
0	CS30	Clock control low. For selecting a timing counter 3 The clock source.

CS3 [2: 0]	description
0	No clock source, stops counting
1	clk sys
2	clk sys / 8 From prescaler
3	clk sys / 64 From prescaler
4	clk sys / 256 From prescaler
5	clk sys / 1024 From prescaler
6	External Clock T3 Pin, falling edge
7	External Clock T3 Pin on the rising edge

The following table is a waveform generation mode control.

Table 5 Waveform Generation Mode Control

WGM3 [3: 0]	Operating mode	TOP Value	update OCR1A time	Position TOV3 time
0	Normal	0xFFFF	immediately	MAX
1	8 Place PCPWM	0x00FF	TOP	BOTTOM
2	9 Place PCPWM	0x01FF	TOP	BOTTOM
3	10 Place PCPWM	0x03FF	TOP	BOTTOM
4	CTC	OCR3A	immediately	MAX
5	8 Place FPWM	0x00FF	BOTTOM	TOP
6	9 Place FPWM	0x01FF	BOTTOM	TOP
7	10 Place FPWM	0x03FF	BOTTOM	TOP
8	PFCPWM	ICR3	BOTTOM	BOTTOM
9	PFCPWM	OCR3A	BOTTOM	BOTTOM
10	PCPWM	ICR3	TOP	BOTTOM
11	PCPWM	OCR3A	TOP	BOTTOM
12	CTC	ICR3	immediately	MAX
13	Retention	-	-	-
14	FPWM	ICR3	TOP	TOP
15	FPWM	OCR3A	TOP	TOP

TCCR3C-TC3 Control register C

TCCR3C **-** TC3 Control register C								
address: 0x92					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	FOC3A	FOC3B	DOC3B	DOC3A	DTEN3	- DOC3C		FOC3C
R / W	W	W	-	-	-	-	-	-

Bit	Name	description
7	FOC3A	Force Output Compare A . In non PWM Mode, the force output by comparing bits FOC3A write "1" The way to compare match. Forcing compare match will not set OCF3A Flag or reload or clear the timer, but the output pin OC3A Will be in accordance with COM3A It sets the appropriate update, just compare match had really happened. Work on PWM When mode, write TCCR3A Cleared when you want to register. Read FOC3A The return value is always zero.
6	FOC3B	Force Output Compare B . In non PWM Mode, the force output by comparing bits FOC3B write "1" The way to compare match. Forcing compare match will not set OCF3B Flag or reload or clear the timer, but the output pin OC3B Will be in accordance with COM3B It sets the appropriate update, just compare match had really happened. Work on PWM When mode, write TCCR3A Cleared when you want to register. Read FOC3B The return value is always zero.
5	DOC3B	Prohibit output of the comparator B Enable control bit.

		when DOC3B Bit disables the output is relatively high, hardware B Is enabled, the output after the prohibition condition is satisfied, COM3B Bit is cleared, the output pin OC3B Off the pin becomes universal IO operating. when DOC3B Bit is low, the output of the comparator is prohibited hardware B Function is disabled.
4	DOC3A	Prohibit output of the comparator A Enable control bit. when DOC3A Bit disables the output is relatively high, hardware A Is enabled, the output after the prohibition condition is satisfied, COM3A Bit is cleared, the output pin OC3A Off the pin becomes universal IO operating. when DOC3A Bit is low, the output of the comparator is prohibited hardware A Function is disabled.
3	DTEN3	Dead time enable control bit. when DTEN3 Bit is high, the dead time is enabled, OC3A with OC3B Become complementary output, and press DTR3L with DTR3H Set to insert dead time. when DTEN3 Bit is low, the dead time is disabled. OC3A with OC3B Are single output.
2	-	
1	DOC3C	Prohibit output of the comparator C Enable control bit. when DOC3C Bit disables the output is relatively high, hardware C Is enabled, the output after the prohibition condition is satisfied, COM3C Bit is cleared, the output pin OC3C Off the pin becomes universal IO operating. when DOC3C Bit is low, the output of the comparator is prohibited hardware C Function is disabled.
0	FOC3C	Force Output Compare C . In non PWM Mode, the force output by comparing bits FOC3C write "1" The way to compare match. Forcing compare match will not set OCF3C Flag or reload or clear the timer, but the output pin OC3C Will be in accordance with COM3C It sets the appropriate update, just compare match had really happened. Work on PWM When mode, write TCCR3A Cleared when you want to register. Read FOC3C The return value is always zero.

TCCR3D-TC3 Control register D

TCCR3D **-** TC3 Control register D								
address: 0x93					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	DSX37	DSX36	DSX35	DSX34	-	-	DSX31	DSX30
R / W	R / W	R / W	R / W	R / W	-	-	R / W	R / W

Bit	Name	description
7	DSX37	TC3 Select the trigger source control enables the first 7 Bit. When set DSX37 Bit "1" Time, TC0 As the output of the comparator is off the overflow signal waveform OC3x The trigger source is enabled. when DOC3x Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC3x The waveform output. When set DSX37 Bit "0" Time, TC0 As the output of the comparator is off the overflow signal waveform OC3x The trigger source is prohibited.
6	DSX36	TC3 Select the trigger source control enables the first 6 Bit. When set DSX36 Bit "1" Time, TC2 As the output of the comparator is off the overflow signal waveform OC3x The trigger source is enabled. when DOC3x Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC3x The waveform output. When set DSX36 Bit "0" Time, TC2 As the output of the comparator is off the overflow signal waveform OC3x The trigger source is prohibited.

5	DSX35	TC3 Select the trigger source control enables the first 5 Bit. When set DSX35 Bit "1" When, pin change 1 As a comparison output signal waveform is off OC3x The trigger source is enabled. when DOC3x Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC3x The waveform output. When set DSX35 Bit "0" When, pin change 1 As a comparison output signal waveform is off OC3x The trigger source is prohibited.
4	DSX34	TC3 Select the trigger source control enables the first 4 Bit. When set DSX34 Bit "1" When the external interrupt 1 As a comparison output signal waveform is off OC3x The trigger source is enabled. when DOC3x Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC3x The waveform output. When set DSX34 Bit "0" When the external interrupt 1 As a comparison output signal waveform is off OC3x The trigger source is prohibited.
3: 2	-	Reservations.
1	DSX31	TC3 Select the trigger source control enables the first 1 Bit. When set DSX31 Bit "1" When, analog comparator 1 As a comparison output signal waveform is off OC3x The trigger source is enabled. when DOC3x Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC3x The waveform output. When set DSX31 Bit "0" When, analog comparator 1 As a comparison output signal waveform is off OC3x The trigger source is prohibited.
0	DSX30	TC3 Select the trigger source control enables the first 0 Bit. When set DSX30 Bit "1" When, analog comparator 0 As a comparison output signal waveform is off OC3x The trigger source is enabled. when DOC3x Bit "1" Rising edge triggered interrupt source, the selected flag register bits will automatically shut down OC3x The waveform output. When set DSX30 Bit "0" When, analog comparator 0 As a comparison output signal waveform is off OC3x The trigger source is prohibited.

The following table shows the selection control trigger source waveform output.

shut down OC3x Trigger source waveform output from the selection control

DOC3x	DSX3n = 1	Trigger source	description
0	-	-	DOC3x Bit "0" , Trigger source waveform output off function is disabled
1	0	Analog comparator 0	ACIF0 The rising edge will be closed OC3x Waveform output
1	1	Analog comparator 1	ACIF1 The rising edge will be closed OC3x Waveform output
1	4	External Interrupt 1	INTF1 The rising edge will be closed OC3x Waveform output
1	5	Pin Change 1	PCIF1 The rising edge will be closed OC3x Waveform output
1	6	TC2 overflow	TOV2 The rising edge will be closed OC3x Waveform output
1	7	TC0 overflow	TOV0 The rising edge will be closed OC3x Waveform output

note:

2) DSX3n = 1 Show TCCR1D The first register n Bit 1 When each register bit may be set simultaneously.

TCNT3L-TC3 Low Byte Counter Register

TCNT3L - TC3 Low byte count value register								
address: 0x94					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0

Name	TCNT3L7	TCNT3L6	TCNT3L5	TCNT3L4	TCNT3L3	TCNT3L2	TCNT3L1	TCNT3L0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	TCNT3L	TC3 Low byte count value. TCNT3H with TCNT3L Incorporated into the composition together TCNT3 ,by TCNT3 Directly to the counter register 16 Place The count value read and write access. Read and write 16 Bit register requires two operations. write 16 Place TCNT3 When, you should write TCNT3H . read 16 Place TCNT3 When, it should read TCNT3L . CPU Correct TCNT3 Writes to this register on the next clock cycle to prevent a compare match timer occurs, even if the timing It has stopped. This allows initialization TCNT3 And the value of the register OCR3x The value of the agreement without causing disruption. If you write TCNT3 The value is equal to or bypassed OCR3x Value, compare match will be lost, resulting in incorrect waveform hair Health results. When the timer stops counting the clock source is not selected, but CPU Still access TCNT3 . CPU Write counter than plus or cleared High priority subtraction operation.

TCNT3H-TC3 High Byte Counter Register

***TCNT3H* - TC3 High byte count value register**								
address: 0x95					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	TCNT3H7	TCNT3H6	TCNT3H5	TCNT3H4	TCNT3H3	TCNT3H2	TCNT3H1	TCNT3H0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	TCNT3H	TC3 The count value of the high byte. TCNT3H with TCNT3L Incorporated into the composition together TCNT3 ,by TCNT3 Directly to the counter register 16 Level Meter Values for read and write access. Read and write 16 Bit register requires two operations. write 16 Place TCNT3 When, you should write TCNT3H . read 16 Place TCNT3 When, it should read TCNT3L . CPU Correct TCNT3 Writes to this register on the next clock cycle to prevent a compare match timer occurs, even if the timing It has stopped. This allows initialization TCNT3 And the value of the register OCR3x The value of the agreement without causing disruption. If you write TCNT3 The value is equal to or bypassed OCR3x Value, compare match will be lost, resulting in incorrect waveform hair Health results. When the timer stops counting the clock source is not selected, but CPU Still access TCNT3 . CPU Write counter than plus or cleared High priority subtraction operation.

ICR3L-TC3 Capture register low byte

***ICR3L* - TC3 Input Capture Register Low Byte**								
address: 0x96					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	ICR3L7	ICR3L6	ICR3L5	ICR3L4	ICR3L3	ICR3L2	ICR3L1	ICR3L0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	ICR3L	TC3 Input capture the low byte value. ICR3H with ICR3L Incorporated into the composition together 16 Bit ICR3 . Read and write 16 Bit register requires two operations. write 16 Place ICR3 When, you should write ICR3H . read 16 Place ICR3 When, it should read ICR3L .

		When the input capture is triggered, the count value TCNT3 Will be updated to copy ICR3 Register. ICR3 Also be used to register Defined count TOP value.

ICR3H-TC3 Capture register high byte

ICR3H **-** TC3 Input Capture MSB								
address: 0x97					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	ICR3H7	ICR3H6	ICR3H5	ICR3H4	ICR3H3	ICR3H2	ICR3H1	ICR3H0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	ICR3H	TC3 Input capture high byte values. ICR3H with ICR3L Incorporated into the composition together 16 Bit ICR3 . Read and write 16 Bit register requires two operations. write 16 Place ICR3 When, you should write ICR3H . read 16 Place ICR3 When, it should read ICR3L . When the input capture is triggered, the count value TCNT3 Will be updated to copy ICR3 Register. ICR3 Also be used to register Defined count TOP value.						

OCR3AL-TC3 Output Compare Register A Low byte

OCR3AL **-** TC3 Output Compare Register A Low byte								
address: 0x98					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OCR3AL7	OCR3AL6	OCR3AL5	OCR3AL4	OCR3AL3	OCR3AL2	OCR3AL1	OCR3AL0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	OCR3AL	Output Compare Register A The low byte. OCR3AL with OCR3AH Incorporated into the composition together 16 Bit OCR3A . Read and write 16 Bit register requires two operations. write 16 Place OCR3A When, you should write OCR3AH . read 16 Place OCR3A When, it should read OCR3AL . OCR3A Continuously with the counter value TCNT3 Compare. Compare match can be used to generate an output compare interrupt, or Who used to OC3A Waveform generation pins. When PWM When mode, OCR3A Using double buffered registers. The normal mode and clear mode match , The double buffering is disabled. Double buffering may be updated OCR3A Register with the maximum or minimum counting time Synchronize, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR3A When the buffer register, double buffering is disabled CPU Access is OCR3A itself.						

OCR3AH-TC3 Output Compare Register A High Byte

OCR3AH **-** TC3 Output Compare Register A High Byte								
address: 0x99					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	OCR3AH7	OCR3AH6	OCR3AH5	OCR3AH4	OCR3AH3	OCR3AH2	OCR3AH1	OCR3AH0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	OCR3AH	Output Compare Register A The high byte.						

		OCR3AL with OCR3AH Incorporated into the composition together 16 Bit OCR3A . Read and write 16 Bit register requires two operations. write 16 Place OCR3A When, you should write OCR3AH . read 16 Place OCR3A When, it should read OCR3AL . OCR3A Continuously with the counter value TCNT3 Compare. Compare match can be used to generate an output compare interrupt, or Who used to OC3A Waveform generation pins. When PWM When mode, OCR3A Using double buffered registers. The normal mode and clear mode match , The double buffering is disabled. Double buffering may be updated OCR3A Register with the maximum or minimum counting time Synchronize, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR3A When the buffer register, double buffering is disabled CPU Access is OCR3A itself.

OCR3BL-TC3 Output Compare Register B Low byte

OCR3BL **-** TC3 Output Compare Register B Low byte								
address: 0x9A					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OCR3BL7	OCR3BL6	OCR3BL5	OCR3BL4	OCR3BL3	OCR3BL2	OCR3BL1	OCR3BL0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	OCR3BL	Output Compare Register B The low byte. OCR3BL with OCR3BH Incorporated into the composition together 16 Bit OCR3B . Read and write 16 Bit register requires two operations. write 16 Place OCR3B When, you should write OCR3BH . read 16 Place OCR3B When, it should read OCR3BL . OCR3B Continuously with the counter value TCNT3 Compare. Compare match interrupt can be used to generate an output compare, Or used OC3B Waveform generation pins. When PWM When mode, OCR3B Using double buffered registers. The normal mode and the mode matching cleared Type, the double buffering is disabled. Double buffering may be updated OCR3B The count register when the maximum or minimum value Engraved synchronize, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR3B When the buffer register, double buffering is disabled CPU Access is OCR3B itself.							

OCR3BH-TC3 Output Compare Register B High Byte

OCR3BH **-** TC3 Output Compare Register B High Byte								
address: 0x9B					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OCR3BH7	OCR3BH6	OCR3BH5	OCR3BH4	OCR3BH3	OCR3BH2	OCR3BH1	OCR3BH0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	OCR3BH	Output Compare Register B The high byte. OCR3BL with OCR3BH Incorporated into the composition together 16 Bit OCR3B . Read and write 16 Bit register requires two operations. write 16 Place OCR3B When, you should write OCR3BH . read 16 Place OCR3B When, it should read OCR3BL . OCR3B Continuously with the counter value TCNT3 Compare. Compare match can be used to generate an output compare interrupt, or Who used to OC3B Waveform generation pins. When PWM When mode, OCR3B Using double buffered registers. The normal mode and the mode matching cleared Type, the double buffering is disabled. Double buffering may be updated OCR3B The count register when the maximum or minimum value Engraved synchronize, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses.							

		When using the double buffering feature CPU Access is OCR3B When the buffer register, double buffering is disabled CPU Access is OCR3B itself.

OCR3CL-TC3 Output Compare Register C Low byte

OCR3CL **-** TC3 Output Compare Register C Low byte								
address: 0x9E					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OCR3CL7	OCR3CL6	OCR3CL5	OCR3CL4	OCR3CL3	OCR3CL2	OCR3CL1	OCR3CL0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name description							
7: 0	OCR3CL	Output Compare Register C The low byte. OCR3CL with OCR3CH Incorporated into the composition together 16 Bit OCR3C . Read and write 16 Bit register requires two operations. write 16 Place OCR3C When, you should write OCR3CH . read 16 Place OCR3C When, it should read OCR3CL . OCR3C Continuously with the counter value TCNT3 Compare. Compare match can be used to generate an output compare interrupt, or Used in OC3C Waveform generation pins. When PWM When mode, OCR3C Using double buffered registers. The normal mode and clear mode match , The double buffering is disabled. Double buffering may be updated OCR3C The count register with the maximum or minimum time Step up, thereby preventing the generation of asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR3C When the buffer register, double buffering is disabled CPU Access is OCR3C itself.						

OCR3CH-TC3 Output Compare Register C High Byte

OCR3CH **-** TC3 Output Compare Register C High Byte								
address: 0x9F					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OCR3CH7	OCR3CH6	OCR3CH5	OCR3CH4	OCR3CH3	OCR3CH2	OCR3CH1	OCR3CH0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	OCR3CH	Output Compare Register C The high byte. OCR3CL with OCR3CH Incorporated into the composition together 16 Bit OCR3C . Read and write 16 Bit register requires two operations. write 16 Place OCR3C When, you should write OCR3CH . read 16 Place OCR3C When, it should read OCR3CL . OCR3C Continuously with the counter value TCNT3 Compare. Compare match can be used to generate an output compare interrupt, or Who used to OC3C Waveform generation pins. When PWM When mode, OCR3C Using double buffered registers. The normal mode and clear mode match , The double buffering is disabled. Double buffering may be updated OCR3C Register with the maximum or minimum counting time Synchronize, thereby preventing asymmetrical PWM Pulse, eliminating interference pulses. When using the double buffering feature CPU Access is OCR3C When the buffer register, double buffering is disabled CPU Access is OCR3C itself.						

DTR3L-TC3 Dead Time Register Low Byte

DTR3L **-** TC3 Dead Time Register Low Byte	
address: 0x9C	Defaults: 0x00

Bit	7	6	5	4	3	2	1	0
Name	DTR3L7	DTR3L6	DTR3L5	DTR3L4	DTR3L3	DTR3L2	DTR3L1	DTR3L0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	DTR3L	Low byte dead time register. when DTEN3 Bit is high, OC3A with OC3B Complementary output, OC3A The output from the dead time inserted DTR3L Count clock determined.						

DTR3H-TC3 High byte dead time register

DTR3H - TC3 High byte dead time register								
address: 0x9D					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	DTR3H7	DTR3H6	DTR3H5	DTR3H4	DTR3H3	DTR3H2	DTR3H1	DTR3H0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 0	DTR3H	High byte dead time register. when DTEN3 Bit is high, OC3A with OC3B Complementary output, OC3B The output from the dead time inserted DTR3H Count clock determined.						

TIMSK3-TC3 Interrupt mask register

TIMSK3 - **TC3 Interrupt mask register**								
address: 0x71					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	-	ICIE3	-	OCIE3C	OCIE3B	OCIE3A	TOIE3
R / W	-	-	R / W	-	R / W	R / W	R / W	R / W
Bit	Name	description						
7: 6	-	Reservations.						
5	ICIE3	TC3 Input Capture interrupt enable control bit. when ICIE3 Bit "1" When, and Global Interrupt set, TC3 Input Capture interrupt is enabled. When the input capture trigger, which is TIFR3 of ICF3 Flag is set, an interrupt occurs. when ICIE3 Bit "0" Time, TC3 Input capture interrupts are disabled.						
4	-	Reservations.						
3	OCIE3C	TC3 Output Compare C Match interrupt enable bit. when OCIE3C Bit "1" And Global Interrupt Set, TC3 Output Compare C Match interrupt is enabled. When compare match occurs When, that is, TIFR3 in OCF3C When the bit is set, an interrupt is generated. when OCIE3C Bit "0" Time, TC3 Output Compare C Match interrupts are disabled.						
2	OCIE3B	TC3 Output Compare B Match interrupt enable bit. when OCIE3B Bit "1" And Global Interrupt Set, TC3 Output Compare B Match interrupt is enabled. When compare match occurs When, that is, TIFR3 in OCF3B When the bit is set, an interrupt is generated. when OCIE3B Bit "0" Time, TC3 Output Compare B Match interrupts are disabled.						
1	OCIE3A	TC3 Output Compare A Match interrupt enable bit. when OCIE3A Bit "1" And Global Interrupt Set, TC3 Output Compare A Match interrupt is enabled. When compare match occurs						

		When, that is, TIFR3 in OCF3A When the bit is set, an interrupt is generated. when OCIE3A Bit "0" Time, TC3 Output Compare A Match interrupts are disabled.
0	TOIE3	TC3 Overflow interrupt enable bit. when TOIE3 Bit "1" And Global Interrupt Set, TC3 Overflow interrupt is enabled. when TC3 Overflow occurs, that is, TIFR3 in of TOV3 When the bit is set, an interrupt is generated. when TOIE3 Bit "0" Time, TC3 Overflow interrupts are disabled.

TIFR3-TC3 Interrupt Flag Register

TIFR3 - TC3 Interrupt Flag Register								
address: 0x38					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	-	ICF3	-	-	OCF3B	OCF3A	TOV3
R / W	-	-	R / W	-	-	R / W	R / W	R / W

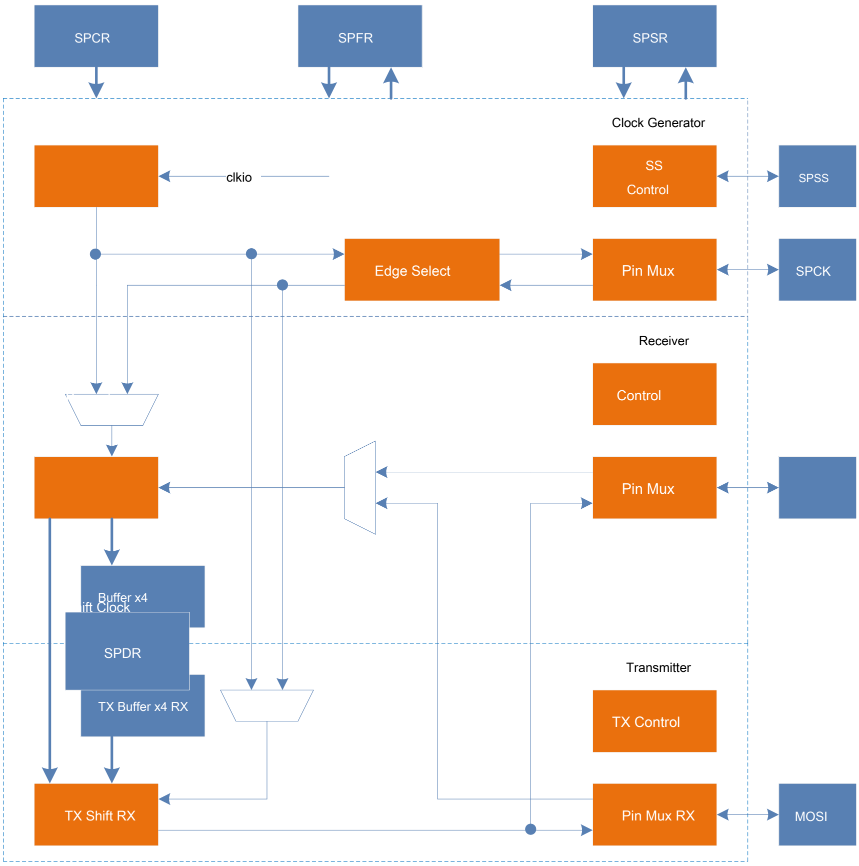
Bit	Name	description
7: 6	-	Reservations.
5	ICF3	Input capture flag. When the input capture event occurs, ICF3 Flag is set. when ICR3 It is counted as TOP Value, and the count value reaches TOP Value, ICF3 Flag is set. If the ICIE1 for "1" And the Global interrupt flag is set, it will generate an interrupt input capture. ICF3 Flag will not be cleared automatically, you need software ICF3 Write bit "1" Cleared.
4	-	Reservations.
3	OCF3C	Output Compare C Matching flag. when TCNT3 equal OCR3C , The comparison unit signals a match, the comparison flag is set and OCF3C . If then the output compare interrupt enable OCIE3C for "1" And the Global interrupt flag is set, it will generate an output compare interrupt. OCF3 Flag will not be cleared automatically, you need software OCF3C Write bit "1" This bit is cleared.
2	OCF3B	Output Compare B Matching flag. when TCNT3 equal OCR3B , The comparison unit signals a match, the comparison flag is set and OCF3B . If then the output compare interrupt enable OCIE3B for "1" And the Global interrupt flag is set, it will generate an output compare interrupt. OCF3B Flag will not be cleared automatically, you need software OCF3B Write bit "1" Cleared.
1	OCF3A	Output Compare A Matching flag. when TCNT3 equal OCR3A , The comparison unit signals a match, the comparison flag is set and OCF3A . If then the output compare interrupt enable OCIE3A for "1" And the Global interrupt flag is set, it will generate an output compare interrupt. OCF3A Flag will not be cleared automatically, you need software OCF3A Write bit "1" Cleared.
0	TOV3	Overflow flag. When the counter overflows, the overflow flag is set TOV3 . If this time overflow interrupt enable TOIE3 for "1" And the Global interrupt flag is set, it will generate an overflow interrupt. TOV3 Flag will not be cleared automatically, you need software TOV3 Write bit "1" Cleared.

Synchronous Serial Peripheral Interface (SPI)

- Full duplex, three-wire synchronous data transfer
- Master or slave operation
- The least significant bit or MSB-first transfer
- 7 Programmable Bit rate
- End of Transmit Interrupt Flag
- Write collision flag protection mechanisms
- Wake-up from idle mode
- Having a double-speed mode operation of the host
- Host mode supports two-wire input
- Input / Output are 4 A buffer register

Overview

SPI Mainly includes three parts: a clock prescaler, the clock detector, slave select the detector, the transmitter and the receiver.



SPI Structure chart

Control and status registers are shared by these three portions. Clock prescaler operating in Master mode only, the bit rate control bits to select the division ratio, thereby generating a corresponding divided clock, output to SPCK Pin on. Detector operating at a clock slave operation mode is only detected from the SPCK Clock edge on input pin, according to SPI Data transmission mode for transmitting and receiving shift register shift operations. Slave selection detector of the slave select signal SPSS Is detected, to obtain

Transmission states to control operation of the transmitter and receiver. The transmitter consists of a shift register and transmit control logic components. The receiver consists of a shift register, four reception buffers and control logic receiving the composition.

Clock Generation

Clock generation logic into the master clock and slave clock prescaler detector, respectively, in Master mode of operation and the slave operation. Clock speed prescaler control bits and control bits by the bit rate selected division factor, to produce the corresponding frequency-divided clock (Total 7 Selectable division factor, details see Register description), the output SPCK Pin provides a communication clock to provide simultaneous transmission and reception shift clock for the shift register internal. Clock Detector Clock input SPCK The edge detection, according to SPI Data transmission mode the transmitter and receiver shift operation. In order to ensure proper sampling of the clock signal, SPCK High and low levels shall be greater than the width of the clock 2 System clock cycles.

Transmission and reception

SPI Module supports simultaneous transmission and reception in the single-wire mode, the host support wire received in the wire mode only.

Single line to send and receive

SPI Host will need to communicate slave select signal SPSS Down, you can start a transfer process. Master and slave data will be ready to be transmitted, the master clock signal SPCK Generating clock pulses the data exchange of data, from the host MOSI Removed from MISO Moved, from the data from the machine MISO Removed from MOSI Moved, after exchanging data host pulled finish SPSS Signal to complete the communication.

When configured as a master, SPI Does not control module SPSS Pin, must be handled by user software. Software down SPSS Pin, the slave select, initiate transmission of communication. The software will write data to be transmitted SPDR Register is initiated clock generator, the clock generated by the hardware communication, and the 8 Bits are shifted to the slave, while the data is moved from the machine. After shifting one byte of data, stopping the clock generator, and the transfer completion flag is set SPIF . Software data can be written to once again SPDR To continue the transmission registers a byte, may be pulled SPSS It signals the end of the current transmission. Finally, the incoming data will be saved in a receive buffer.

When configured as a slave, as long as SPSS Signal remains high, SPI Module will maintain sleep and keep MISO Pin is tri-state. Then the software can be updated SPDR Contents of the register. Even at this time SPCK A clock pulse input pin, SPDR The data is not removed until SPSS Signal is pulled low. When one byte of data transfer is completed, the transfer completion flag set hardware SPIF . At this time, before reading the data into the software may continue to SPDR Write data register, the last incoming data will be saved in a receive buffer.

SPI Module in the transmit direction only four buffers in the receive direction have four buffers. When data is transmitted, when the transmission buffer is not full (i.e., transmit buffer full flag WRFULL When the bit is low), to be SPDR Register is written. When receiving the data, when the receive buffer is non-empty state (i.e., the reception buffer empty flag RDEMPT When the bit is low), can be accessed by SPDR Register read character that has been received.

Host double reception

SPI Module wire mode only effective in the master mode of operation, and in that a different wire mode MOSI with MISO They are used for the host to receive data, each SPCK Simultaneously receiving a clock pulse 2 Bits of the data (MISO On the data line before, MOSI After the data line) set by hardware after two bytes of data transmission after receiving the completion flag SPIF , Save the data in the receive buffer and the shift register. At this point the software to be read SPDR Register twice to obtain two bytes of the received data. Note that, although not to the host computer sends data from the software still needs to wire mode SPDR

Register write clock generator generates data to initiate communication clock, write once SPDR Register to receive two bytes of data.

Data Mode

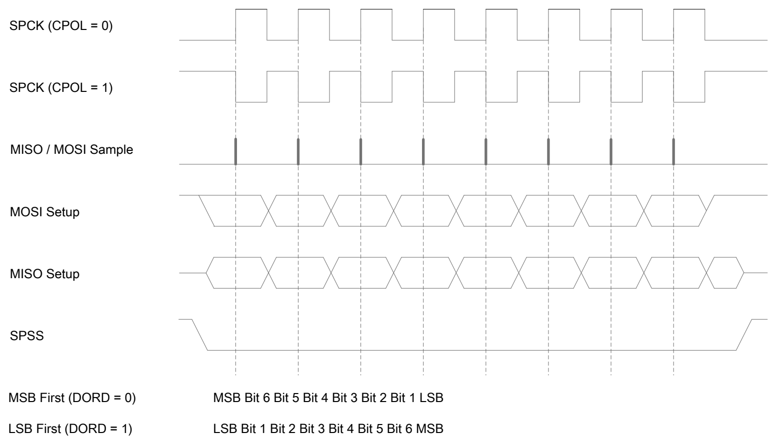
The single-wire mode, with respect to serial data, SPI Have 4 Kind SPCK Combination of phase and polarity, the CPHA with CPOL

To control, as shown in the following table.

CPHA with CPOL Selection data transmission mode

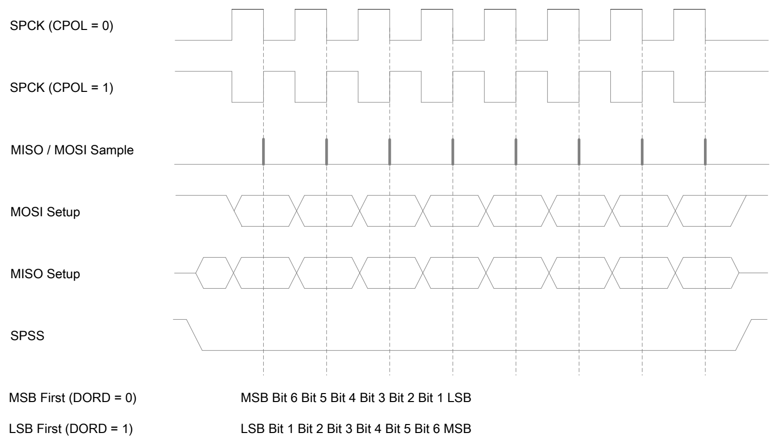
CPOL	CPHA	Starting along	Trailing Edge	SPI mode
0	0	Sampling (rising)	Setting (falling edge)	0
0	1	Setting (rising)	Sampling (falling edge)	1
1	0	Sampling (falling edge)	Setting (rising)	2
1	1	Setting (falling edge)	Sampling (rising)	3

when CPHA = 0 , The data sampling clock and disposed along as shown below:



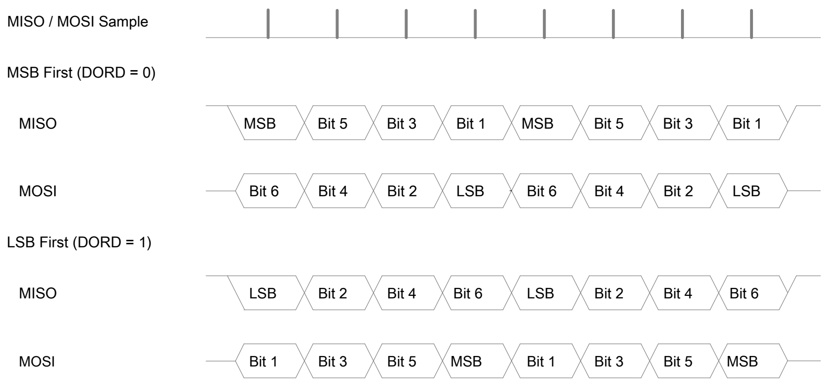
CPHA for "0" Time SPI Data transmission mode

when CPHA = 1 , The data sampling clock and disposed along as shown below:



CPHA for "1" Time SPI Data transmission mode

Wire mode, MISO with MISO Are used as the input of the host, the time still data transmission mode decision data sampling, the sampling fashion as shown below:



Host mode DUAL for "1" Time SPI Data sampling mode

SPSS Pin Function

When configured as the selection signal from the slave machine SPSS Always as an input pin. when SPSS Pin remains low, SPI The interface is activated, MISO Pin an output (software configuration corresponding port), the other pins are inputs. when SPSS

When the pin is held high, SPI Module is reset, and no longer receives data. SPSS Pin for packet / byte synchronous useful can synchronizing the bit counter and the master clock generator unit. when SPSS When pulled, SPI Slave reset immediately send and receive logic, and the shift register discards incomplete data.

When configured as host, user software can decide SPSS Pin direction. If the SPSS Configured as an output, it can be driving machine SPSS Pin. If the SPSS Configured as an input, it must be kept high to ensure the normal operation of the host. When configured as a host and SPSS An input pin, the external circuit down SPSS Pin, SPI Another module will be considered as a host to choose their own and begin to transfer data from the machine. To avoid bus contention,

SPI The module performs an operation of:

1. Located cleared SPCR Register MSTR Bits, is converted to the slave, whereby MOSI with SPCK Becomes an input;

2. Set located SPSR Register SPIF Bit, if the interrupt enabled will generate SPI Interrupted. Therefore, interrupt handling SPI Host data transfer, and there SPSS When the possibility is pulled low, the interrupt service routine should check MSTR Bit is set "1" . If they are cleared, the software shall set it to re-enable SPI Host mode.

SPI initialization

Before the first of the communication SPI Initialized. The initialization process normally includes a host operating selection from the setting data transmission mode, select the bit rate, and the direction of each pin control. Wherein the host and the direction from the pin-up operation control varies, as shown in the following table:

Direction control pin

Pin	Direction in a Host mode	Direction from the slave mode
MOSI	User-defined software	Entry
MISO	Entry	User-defined software
SPCK	User-defined software	Entry
SPSS	User-defined software	Entry

SPI Host initialization

SPI Host mode initialization process is as follows:

1. Position MSTR Bit, set the bit rate selection control bits, data transmission mode, the transmission order of data, the interrupt is enabled or not,

   And two-enabled or not;

2. Set up MOSI with SPCK Pin as an output;

3. Position SPE Bit. Host mode, when you do not want SPI Other modules are selected as the host machine from the time, can be set SPSS Pin output.

SPI Slave initialization

SPI Slave mode initialization process is as follows:

1. Clear MSTR Bit, the data transfer mode, the transmission order of data, the interrupt is enabled or not;

2. Set up MISO Pin as an output;

3. Position SPE Bit.

SPI Interrupt

When one of the following events occur or more, SPI Interrupt flag SPIF It will be set:

1. When configured as a host and SPSS An input pin, the external circuit down SPSS Pin;

2. When the transmit buffer status is full, the software continues to SPDR Register write transactions;

3. When the receive buffer full state;

4. When data is written in the transmit buffer have been sent, the transmit buffer is empty status.

when SPIF Bit is set, and SPI Interrupt enable bit SPIE When and global interrupt enable bits are high, it will produce SPI Interrupted. After entering the interrupt service routine, the hardware will SPIF Cleared. If the SPIF It is set by the above-mentioned event 1 with 2 To set in, SPIF Will be cleared; if SPIF It is set by the above-mentioned event 3 with 4 To set in, SPIF Will not be cleared, because the reception or transmission buffer status is not changed, the bit will still be set SPIF Bit, then you need to be cleared by software operations.

SPI Interrupt service routine, the software is cleared SPIF Bit sequence of operations:

1) Read SPIF Status bits, if it is low, indicating that SPIF Bit has been cleared by hardware, no software is cleared again; if it is high,

   Continue to operate it;

2) Read SPFR Register, if RDFULL Bit is high, indicating that the current status of the receive buffer is full, read SPDR Deposit

   Obtains received data, RDFULL Bit becomes low, the software can continue to read SPDR Register obtain received data until the RDEMPT Bit high;

3) Read SPFR Register, if RDFULL Bit is low, and WREMPT Bit is high, indicating that the current status of the receive buffer

   Non-full, the transmission buffer status is empty, the software can read SPDR Register obtain received data until the RDEMPT Bit high;

4) After the software acquires the received data, and then performed is cleared SPIF Bit. because SPIF Bit is read-only and can not directly SPIF

   Bit is cleared, and the need to read SPSR Register before accessing SPDR (Read or write SPDR Register) to clear the way SPIF Bit.

Register Definition

SPI Register List

register	address	Defaults	description
SPCR	0x4C	0x00	SPI Control register
SPSR	0x4D	0x00	SPI Status Register
SPDR	0x4E	0x00	SPI Data register
SDFR	0x39	0x00	SPI Buffer

SPCR - SPI Control register

SPCR - SPI Control register								
address: 0x4C					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit Name description

Bit	Name	Description
7	SPIE	SPI Interrupt enable bit. When set SPIE Bit "1" Time, SPI Interrupt is enabled. When located SPSR Register SPIF When the bit is set and the Global Interrupt Enable, generated SPI Interrupted. When set SPIE Bit "0" Time, SPI Interrupts are disabled.
6	SPE	SPI Enable. When set SPE Bit "1" Time, SPI Module is enabled. Any SPI Must be set before the operation SPE . When set SPE Bit "0" Time, SPI Module is disabled.
5	DORD	Control data order bits. When set DORD Bit "1" , The data LSB Sent first. When set DORD Bit "0" , The data MSB Sent first.
4	MSTR	Master Slave selection control bits. When set MSTR Bit "1" When the master mode is selected. When set MSTR Bit "0" When the slave mode is selected. Host mode, SPSS Pin configured as an input and is driven low, MSTR Bit will be cleared, located SPSR Register SPIF Is set, the user must reset MSTR Enter host mode.
3	CPOL	Clock polarity control bit. When set CPOL Bit "1" When the idle state SPCK High. When set CPOL Bit "0" When the idle state SPCK Low.

CPOL	Starting along	Trailing Edge
0	Rising	Falling
1	Falling	Rising

Bit	Name	Description
2	CPHA	Clock phase control bit. When set CPHA Bit "1" When, starting in the data set, an end edge sample data. When set CPHA Bit "0" When, a start edge sample data, setting data end edge.

CPHA	Starting along	Trailing Edge

		0	sampling	Set up
		1	Set up	sampling
1	SPR1 Clock rate select bit 1 . SPR1 with SPR0 Used to select SPI The clock rate of the transmission. See specific control mode SPCK And the system clock of relational tables.			
0	SPR0 Clock rate select bit 0 . SPR1 with SPR0 Used to select SPI The clock rate of the transmission. See specific control mode SPCK And the system clock of relational tables.			

SPSR - SPI Status Register

SPSR - SPI Status Register								
address: 0x4D					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	SPIF	WCOL	-	-	- DUAL		-	SPI2X
R / W	R	R	R	R	R	R / W	R	R / W
Initial	0	0	0	0	0	0	0	0

Bit	Name	description
7	SPIF	SPI Interrupt flag. After serial transfer set SPIF Under the sign, host mode, Configuring SPSS And when the input pin is pulled low, SPIF It will also be set. If at this time SPCR Register SPIE Bit and global interrupt enable bits are set, SPI An interrupt is generated. After entering the interrupt service routine SPIF Bit is automatically cleared by reading first SPSR Register visit again SPDR Register cleared SPIF Bit.
6	WCOL	Write Collision flag. In the process of writing data transmission SPDR The register set WCOL Bit. WCOL Bit by first reading SPSR Register visit again SPDR Register is cleared.
5	-	Reservations.
4	-	Reservations.
3	-	Reservations.
2	DUAL	Wire mode control bit. When set DUAL Bit "1" , Enable SPI Wire transmission mode. When set DUAL Bit "0" Is prohibited SPI Wire transmission mode. Wire transmission mode only SPI Host active mode, MISO with MOSI Are used as host data input, the data transmission wire receiving host, see chapters describe and model data.
1	-	Reservations.
0	SPI2X	SPI Speed control bits. When set SPI2X Bit "1" Time, SPI The transmission speed is doubled. When set SPI2X Bit "0" Time, SPI The transmission speed is not doubled. See specific control mode SPCK And the system clock of relational tables.

The following table SPCK And the relationship between the system clock.

SPCK And the relationship between the system clock

SPI2X	SPR1	SPR0	SPCK Frequency of
0	0	0	f_{sys} / 4
0	0	1	f_{sys} / 16
0	1	0	f_{sys} / 64
0	1	1	f_{sys} / 128
1	0	0	f_{sys} / 2
1	0	1	f_{sys} / 8
1	1	0	f_{sys} / 32
1	1	1	f_{sys} / 64

SPDR - SPI Data register

SPDR - SPI Data register								
address: 0x4E					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	SPDR7	SPDR6	SPDR5	SPDR4	SPDR3	SPDR2	SPDR1	SPDR0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit Name	description
7: 0 SPDR	SPI Transmission and reception of data. SPI Transmission data and reception data sharing SPI Data register SPDR . The data is written SPDR I.e., the transmission data shift register is written, from SPDR I.e., the read data read received data buffer.

SPFR - SPI Buffer

SPFR - SPI Buffer								
address: 0x39					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	RDFULI	RDEMPT	RDPTR1	RDPTR0	WRFULL	WREMPT	WRPTR1	WRPTR0
R / W	R	R / W	R	R	R	R / W	R	R

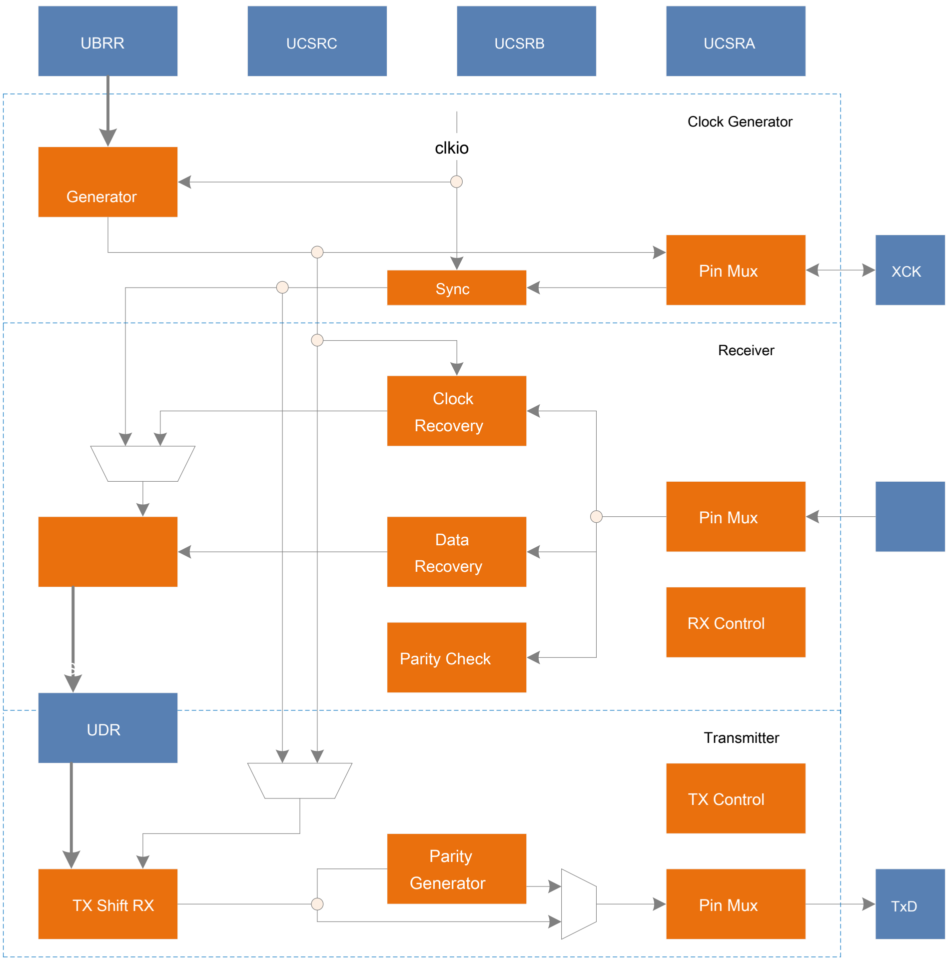
Bit	Name	description
7	RDFULL	Receive buffer full flag. When receiving the data buffer reaches four bytes, RDFULL Bit is high, indicating that the receive buffer is full, and it will set interrupt flag. If the software is not timely to go read the data in the receive buffer, the data is received again, the receive buffer overflow occurs before the data is overwritten by new data. When receiving the data buffer is less than four bytes, RDFULL Bit is low, indicating that the receive buffer is non-full, may also receive data. When at the same time RDEMPT Bit and WREMPT When the bit set operation, receive and transmit buffer address and SPI The shift register pointer are zero, RDFULL Bit is low.
6	RDEMPT	Receive Buffer Empty flag. When data is not received, RDEMPT Bit is high, indicating that the receive buffer is empty. When data is received, it will be stored in the receive buffer, RDEMPT Bit is low, indicating that the receive buffer is non-empty, then MCU You can access SPDR Register reads the reception buffer

		according to. To ensure that the received data is not lost, the software may be a non-empty state in the receive buffer i.e. RDEMPT The read bit is low down in the reception data buffer. When the pair RDEMPT Bits within an operation (write 1), The receive buffer address zero. When at the same time RDEMPT Bit and WREMPT When the bit set operation, receive and transmit buffer address and SPI The shift register pointer are zero, RDEMPT Bit high.
5	RDPTR1 Receive buffer address high.	
4	RDPTR0	Receive buffer address low. When the pair SPDR When the read register, MCU Will read the received data from the receive buffer, while the receiving buffer address will increment. When the pair RDEMPT Bits within an operation (write 1), The receive buffer address zero.
3	WRFULL	Send buffer full flag. When the data transmission buffer reaches four bytes, WRFULL Bit is high, indicating that the transmit buffer is full. When the transmit buffer is less than four bytes, WRFULL Bit is low, indicating that non-transmit buffer is full. To increase the transmission speed, the software may be a non-full state in the transmission buffer i.e. WRFULL Bit write data is low, SPI The controller will turn the data sent.
2	WREMPT	The transmit buffer empty flag. When data is written to the transmit buffer have been sent, WREMPT Bit is high, indicating that the transmit buffer is empty, and it will set the interrupt flag SPIF . When the pair SPDR After the register write operation, a transmission buffer address is accumulated, writes all the data is not the transmission buffer is transmitted, the reception buffer has at least one byte of data, WREMPT Bit is low, indicating that the transmit buffer is not empty. When the pair WREMPT Bits within an operation (write 1), The buffer address will be sent to zero. When at the same time RDEMPT Bit and WREMPT When the bit set operation, receive and transmit buffer address and SPI The shift register pointer are zero, WREMPT Bit high.
1	WRPTR1 Send buffer address high.	
0	WRPTR0	Send buffer address low. When the pair SPDR Register write operation, SPDR Data will be written in the transmission buffer and the transmission buffer address will increment. When the pair WREMPT Bits within an operation (write 1), The buffer address will be sent to zero.

USART0 - Universal Synchronous / Asynchronous Serial Transceiver

- Full-duplex operation (Separate receive and transmit serial register)
- Asynchronous or synchronous operation
- Master or slave operation
- Precision baud rate generator
- stand by 5 , 6 , 7 , 8 ,or 9 Data bits and 1 ,or 2 Stop bit
- Supported hardware parity generation and checking mechanisms
- Data overspeed detection
- Framing error detection
- Noise filtering, including false start bit detection and a digital low-pass filter
- Three separate interrupt: transmit complete interrupt, transmitting and receiving data Register Empty Interrupt End
- Multiprocessor Communication Mode
- Speed asynchronous communication mode

Overview



USART Structure chart

USART Mainly includes three parts: a clock generator, a transmitter and a receiver. Control and status registers are shared by these three portions. The clock generator and a synchronous baud rate generator operating mode from the external input clock synchronization logic components.
XCK Pin is only used for asynchronous transfer mode. Transmitting the write data buffer comprises a serial shift register, Parity Generator and Control logic for different frame formats. A write data buffer allows continuous transmission of data without delay between the data frames. The receiver having a clock and data recovery unit, for receiving asynchronous data. In addition to restoring unit, the receiver further comprising a parity, the control logic, two serial shift register and a receive buffer UDR . The receiver and the transmitter supports the same frame format, and can detect frame error, overrun data and parity errors.

Clock Generation

Clock generating logic generates the base clock for the transmitter and receiver. USART stand by 4 Clock modes: Normal asynchronous mode, double-speed asynchronous mode, the synchronous mode host, and a synchronization pattern from the machine. USCRC of UMSEL Bits select the synchronous or asynchronous mode. USCRA of U2X Position control speed asynchronous mode enabled. It is only valid in the synchronous mode XCK Pin data direction register (with IO Multiplexing) determines the source is produced (master mode) or externally generated (slave mode) from the inside.

Baud Rate Generator

Baud Rate Register UBRR And a down counter connected together as USART The programmable prescaler or baud rate generator. Descending counters work in the system clock (f_{sys}) Next, when it counts down to zero, or UBRRL When the register is written, it will automatically load UBRR Register. When the count reaches zero generating a clock, which clock baud rate generator output, the frequency of f_{sys} / (UBRR + 1) .

The following table shows the various operating modes computing the baud rate (bits / sec) and UBRR Formula values.

Operating mode	The baud rate is calculated (1)	UBRR Value calculation formula
Asynchronous Normal mode	BAUD = f_{sys} / (16 * (UBRR + 1))	UBRR = f_{sys} / (16 * BAUD) - 1
Asynchronous speed mode	BAUD = f_{sys} / (8 * (UBRR + 1))	UBRR = f_{sys} / (8 * BAUD) - 1
Synchronous Master Mode	BAUD = f_{sys} / (2 * (UBRR + 1))	UBRR = f_{sys} / (2 * BAUD) - 1

Description:

1. The baud rate is defined as the transfer rate in bit per second (bps);

2. BUAD Baud rate, f_{sys} As the system clock, UBRR Baud rate register UBRRH with UBRRL The combined value.

Speed Operation

By setting UCSRA Register U2X Bit transfer rate can be doubled, this bit is valid only in asynchronous mode, this bit is set to the synchronous operation mode, "0" .
This bit will be set to divide by half the baud rate divider, effectively doubles the transfer rate for asynchronous communication. In this case, the receiver uses only half the number of samples to the data sampling and clock recovery, and therefore more accurate baud rate setting and the system clock. The transmitter did not change.

External Clock

Synchronous drive slave modes of operation by an external clock. After synchronizing the external clock register and the edge detector was only transmitter

And the receiver uses, this process introduces a delay of two system clocks, thus the external XCK The maximum clock frequency is limited by the following equation:

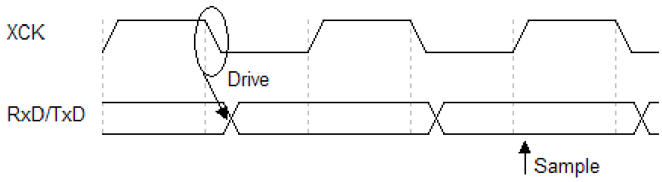
$$f_{XCK} < f_{sys} / 4$$

pay attention fsys Systematic clock stability of the decision, in order to prevent loss of data due to the frequency drift, proposed to retain a sufficient margin.

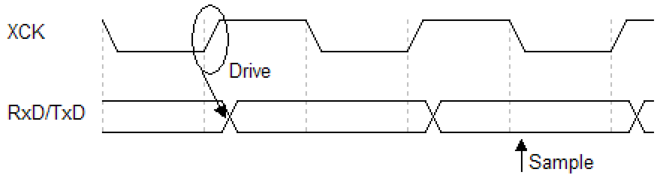
Synchronous Clock Operation

In synchronous mode, XCK A clock input pin is a clock output (master mode) (slave mode). The basic rule of the data sampling clock edge and data changes the relationship is: the data input terminal (RxD) And the clock edge data output clock edge sampling variation used is used contrary.

UCPOL = 1



UCPOL = 0



In synchronous mode XCK Timing

As shown above, when UCPOL Value "1" When, in XCK The falling edge of output data changes in XCK The rising edge of data samples; when UCPOL Value "0" When, in XCK The rising edge of output data changes in XCK The falling edge of the data sampling.

Frame format

A serial data frame synchronization bit (start and stop bits) and a parity bit for error plus a data word.

USART Accept the following 30 Data frame format combination:

- 1 Start bit
- 5 , 6 , 7 , 8 or 9 Data bits
- No parity bit, odd or even parity bit parity bit
- 1 or 2 Stop bit

Data frame begins with a start bit, followed by the least significant bit of the data word, followed by the other data bits, the highest bit data word end, most successful transmission 9 Bit data. If enabled, the parity, parity bit data word will be followed, and finally the stop bit. When a complete data frame transmission, the transmission can be immediately a new frame, or to the transmission line is idle (high) state. Below shows the possible data frame structure, the bits in square brackets are optional.

USART Frame structure of FIG.

Description:

1) IDLE Communication line (RxD or TxD No data transmission on), must be high when the line is idle

2) St Start bit, always low

3) 0-8 Data bits

4) P Parity bit, odd or even parity

5) Sp Stop bit, always a high-level data frame structure composed of UCSRB with UCSRC Register UCSZ [2: 0] , UPM [1: 0] with USBS set up. Receive and transmit using the same settings. Any changes to the settings could undermine ongoing data transmission. among them, UCSZ [2: 0] Determine the number of data bits in the frame, UPM [1: 0] And for enabling to determine the type of parity, USBS Set frame has one or two stop bits. The receiver ignores the second stop bit, and therefore only the first frame error ended a bit "0" When it is detected.

Parity bit is calculated

Parity bit is calculated for each data bit XORed. If odd parity, the exclusive-OR need negated. Relationship between the parity bit and the data bits is as follows:

$$P_{even} = d_{n-1} \oplus \dots \oplus d_3 \oplus d_2 \oplus d_1 \oplus d_0 \oplus 0 \quad P_{odd} = d_{n-1} \oplus \dots \oplus d_3 \oplus d_2 \oplus d_1 \oplus d_0 \oplus 1$$

Description:

1) P_{even} Even parity

2) P_{odd} Odd results

3) d_n The first n Data bits

USART initialization

Before the first of the communication USART Initialized. The initialization process normally comprises setting the baud rate, setting a frame structure, and can receive or transmitter according to need. For interrupt-driven USART Operation, during initialization to clear the global interrupt flag and ban USART All interrupts.

During reinitialization or a frame structure such as changing the baud rate, must ensure that no data transmission. TXC Flag may be used to detect whether or not the sender all the transmission, RXC Flag may be used to detect whether there is data in the receive buffer is not read. in case TXC Flag used for this purpose, before each transmission of data (write UDR Before register) must be cleared TXC Flag.

Transmitter

Position UCSRB Register TXEN Bit to enable USART The data is sent. After the can TxD Universal pin IO Ie function USART Functionality substituent, the transmitter's serial output. Before sending data to set the baud rate, mode of operation and frame format. If synchronous operation is applied to XCK Pin is the clock signal on clock data transmission.

send 5 To 8 The frame data

The data to be transmitted is loaded into the transmit buffer to the data transmission. CPU By writing UDR Register to load the data. When the transmit shift register can transmit a new data, the data buffer will be transferred to the shift register. When the shift register is idle (no ongoing data transmission), or the last stop bit previous frame data transmission is completed, the new data will be loaded. Once the shift register is loaded with new data, it is provided according to the established transmission

Transmission of a complete frame.

send 9 Bit data frame

If you send 9 Bit data frame, the data should first of 9 Bit write register UCSRB of TXB8 Bit, then low 8

Data written to the transmit data register bit UDR . The first 9 Communication in a multi-bit data for indicating an address frame, the synchronous communications protocol may be used for processing.

Parity bit is sent

Parity generation circuit to generate a serial data frame corresponding check bits. When the parity bit is enabled (UPM1 = 1), The transmission control logic circuit inserts the parity bits between the last and the first data word of a stop bit.

Send flag and interrupt handling

USART Transmitter has two flags: USART Data register empty flag UDRE And the transmission end flag TXC , Two flags can generate interrupts. Data register empty flag UDRE It is used to indicate whether the transmit buffer to write a new data. This bit is set when the transmit buffer is empty "1" Full time is set "0" . when UDRE Bit "1" Time, CPU Data can go register UDR Write new data, not vice versa. when UCSRB Data register empty interrupt enable register bit UDRIE for "1" When, as long as UDRE Is set (and global interrupts are enabled), will produce USART Data Register empty interrupt request. To register UDR The write operation will be cleared UDRE . When the interrupt transmission of data in the data register empty interrupt service routine must write new data to a UDR

To clear UDRE , Or disable the Data Register Empty interrupt. Otherwise, if the interrupt service routine ends, a new interrupt will occur again.

When the entire data frame is sent out of the shift register while the register and no new transmission data, the transmission end flag

TXC It will be set. when UCSRB Send the end of last interrupt enable bit TXCIE (And the Global Interrupt Enable) "1" When, as

TXC Flag is set, USART Transmit Complete Interrupt will be executed. Once in the interrupt service routine, TXC Flag, this is automatically cleared, CPU This bit can also write "1" Cleared.

Disable the transmitter

when TXEN When cleared, and all the data only after the completion of transmission the transmitter can really disabled, i.e., the transmit shift register and the transmit data buffer register are not to be transmitted. Transmitter disabled later, TxD Pin restore its versatility IO Features.

receiver

Position UCSRB Receive register enable bits (RXEN) To start USART receiver. After the can RxD Universal pin

IO Function is USART Functionality substituent's serial input port of the receiver. Before receiving the data must first set the baud rate, and the operating mode frame format. If synchronous receive mode, XCK On the clock pin is used as transfer clock.

receive 5 To 8 Bit data frame

Once the receiver detects a valid start bit, they start to receive data. Each bit that follows the start bit will be set or baud XCK Clock received until the stop bit is received the first frame data, the second stop bit will be

Receiver ignored. After each bit of the received data into the receive shift register receives the first stop bit, the receiver set positioned UCSRA Receive data register completion flag RXC Bit shift register and the complete data frame is transferred to the receive buffer, CPU By reading UDR Register may obtain received data.

receive 9 Bit data frame

If you set 9 Data frame bit data, from UDR Low reading 8 Bit register must be read before data UCSRB of RXB8 To get the first bit 9 Bit data. This rule also applies to the state flag FE , DOR as well as PE . Read UDR Location will change the state of the reception buffer, and then change likewise stored in the buffer TXB8 , FE , DOR and PE Bit.

Reception complete flag and interrupt handling

USART The receiver has a flag: Reception complete flag RXC , To indicate whether or not the data read out of the receive buffer. When the receive buffer data is not read, this bit "1" , Otherwise "0" . If the receiver is disabled, the receive buffer will be flushed, RXC It will be cleared. Position UCSRB Receive Complete Interrupt Enable bit RXCIE After long RXC Flag is set (provided that global interrupts are enabled), it will have USART Receive Complete interrupt. When interrupt-driven data reception, data reception from the end of the interrupt service routine must UDR Read data cleared RXC Logo, or as long as the interrupt handler to an end, a new interrupt will occur.

Receive error flag

USART The receiver has three error flags: Frame Error FE The data overflow DOR And parity error PE . They are located in UCSRA register. Error flag together with the frame in a receive buffer them. All error flags can generate interrupts. Framing Error FE The first bit indicates that a state in which a stop-readable frame stored in the reception buffer. Stop bits correctly (value "1")then FE Flag "0" ,otherwise FE Flag "1" . This flag is used to detect loss of synchronization, the transmission is interrupted, the protocol handling. Data overflow flag DOR Due to indicate that the receive buffer is full caused data loss. When the receiving buffer is full, the receive shift register existing data, if detected at this time a new start bit, data overrun occurs. DOR That flag is set to indicate that a read recently UDR And next read UDR Lost between one or more data frames. When the data frame is successfully transferred to the receive buffer from the shift register, DOR Flag is cleared. Parity Error Flag PE Next frame indicates that the received data had a parity error buffer upon reception. If parity is not enabled, PE Is cleared.

Parity Checker

Parity mode bits set UPM1 Will launch parity checker. Check pattern (even or odd) of UPM0 Decision. After the parity is enabled, the verifier calculates parity data input and the result of the parity bit data frame is compared. The verification result is stored in the reception buffer with the data and stop bits. CPU By reading PE Check whether the received frame bit parity error among them. If a next data read out from the receive buffer had a parity error, and parity is enabled, then UPE Is set, the receive buffer remain valid UDR To be read.

Disabling the Receiver

Compared with the transmitter, the receiver prohibits immediate. Is receiving data will be lost. Disabling the Receiver (RXEN When cleared), the receiver will not take up RxD Pin, the receive buffer will be flushed.

Receiving asynchronous data

USART A clock recovery and a data recovery unit for handling asynchronous data reception. Synchronization logic for clock recovery from

RxD Baud clock pin and the interior of the asynchronous serial data. The data recovery logic used for data acquisition, filtering and each one of the input data through a low pass filter to improve the noise performance of the receiver. Asynchronous Receiver operating range depends on the accuracy of the internal clock of the baud rate of the input frame data bits and one contains.

Asynchronous Operational Range

The working range of the receiver depends on the degree of mismatch between the received data with the internal baud rate. If the transmission is too fast or too slow in bit rate data transmission, the receiver or internally generated baud rate is not the same frequency, the receiver can not be synchronized with the start bit. In order to ensure that the receiver will not miss the start bit of the next frame of samples, the input data and the internal receiver baud rate is not much difference, the ratio between them with a margin of error will be described baud rate. The following two tables are given the maximum baud rate error range in the normal mode and the permissible speed mode.

In normal mode the maximum error range of the receiver baud

Data bits + parity length and	The maximum error range (%)	Recommended error range (%)
5	+ 6.7 / -6.8	± 3.0
6	+ 5.8 / -5.9	± 2.5
7	+ 5.1 / -5.2	± 2.0
8	+ 4.6 / -4.5	± 3.0
9	+ 4.1 / -4.2	± 1.5
10	+ 3.8 / -3.8	± 1.5

The maximum reception speed mode Baud Rate Error

Data bits + parity length and	The maximum error range (%)	Recommended error range (%)
5	+ 5.7 / -5.9	± 2.5
6	+ 4.9 / -5.1	± 2.0
7	+ 4.4 / -4.5	± 1.5
8	+ 3.9 / -4.0	± 1.5
9	+ 3.5 / -3.6	± 1.0
10	+ 3.2 / -3.3	± 1.0

As can be seen from the table, the normal mode the baud rate allows a greater range of variation. The recommendations of the baud rate error range is assumed premise receiver and transmitter equally divides the maximum total error derived. There are two possible reasons for the receiver baud rate error. First, the stability of the system clock of the receiver operating voltage and temperature. This is generally not a problem when using a crystal to generate the system clock, but when using the internal oscillator, the system clock may be biased. The second reason is not necessarily the baud rate generator by dividing the system clock to obtain exactly the desired baud rate. At this point you can adjust

UBRR Value, such low error can be accepted.

Set the baud rate and the error introduced

For standard crystal and resonator frequencies, the actual baud rate of communication in the asynchronous mode may be calculated by obtaining the baud rate, the error between it and the communication baud rate used to calculate the following formula can be used:

$$\text{Error [\%]} = (\text{Baud}_{real} / \text{Baud} - 1) * 100\%$$

among them, Baud A commonly used communication baud rate, Baud_{real} Is calculated by the formula baud rate, the baud rate into the calculation formula can be obtained with the system clock baud rate error f_{sys} And baud rate register UBRR The relationship between the values are as follows: Normal mode:

$$\text{Error [\%]} = (f_{sys} / (16 * (\text{UBRR} + 1)) / \text{Baud} - 1) * 100\%$$

Speed mode:

$$\text{Error [\%]} = (f_{sys} / (8 * (\text{UBRR} + 1)) / \text{Baud} - 1) * 100\%$$

When the clock error regardless of traffic on both sides, i.e., the system clock f_{sys} When a standard clock, baud rate error can be obtained UBRR The relationship between values. The following table shall be 16MHz Under different system clock UBRR Setting the baud rate error value.

16MHz The system clock is set at UBRR Error generated

Baud Rate (Bps)	f_{sys} = 16.000MHz			
	Normal mode (U2X = 0)		Speed mode (U2X = 1)	
	UBRR	error	UBRR	error
240048009600	416	-0.1%	832	0.0%
	207	0.2%	416	-0.1%
	1,036,851,342,516,128,3	0.2%	207	0.2%
14.4K	0	0.6%	1,381,036,834,512,516,173.	-0.8%
19.2K		0.2%	1	0.2%
28.8K		-0.8%		0.6%
38.4K		2.1%		-0.8%
57.6K		0.2%		0.2%
76.8K		0.2%		0.2%
115.2K		-3.5%		2.1%
230.4K		8.5%		-3.5%
250K		0%		0%
0.5M		0%		0%
1M		0%		0%

Multiprocessor Communication Mode

Position UCSRA Multi-processor communication mode (MPCM) Bits can USART The receiver receives the data frame filtering. Those frames no address information will be ignored and will not be stored in the receive buffer. In a multiprocessor system, the processors communicate via the same serial bus, which effectively reduces the need for CPU Number of processed data frames.

MPCM Set bit does not affect the transmitter, but a multi-processor communication system, a method of its use will vary.

If the receiver the received data frame length 5 To 8 Position, then the first stop bit is used to indicate the current frame contains data or address information. If the data received by the receiver is the frame length 9 Bits, then by the first 9 Position to determine whether data or address information. If the frame type for the flag "1" , Then this is the address of the frame is a data frame.

Multi-processor communication mode that allows a plurality of receiving data from the host processor from the processor. Determining a first decoded address addressed by a frame which is from the processor. Addressed normal receive the subsequent data from the processor, while the other processor from the data frames until the next frame address is ignored.

As for a host processor, it may be used 9 Bit data frame format, with the first and 9 It identifies the frame bit data format. In this communication mode, the processor must operate in the 9 Bit data frame format. The following steps shall be carried out in the data exchange multiprocessor communication mode:

1 . All work in a multi-processor communication mode (set from the processor MPCM);
2 . The main processor sends an address frame, all the frame received from the processors. From the processor UCSRA Register RXC Place Normal set;
3 . Each processor reads from UDR The contents of the register, decodes the address to determine whether the frame is selected. If selected, It clears UCSRA Register MPCM Bit, not selected, will remain MPCM for "1" And waits for the next address of the frame;
4 . The new address until it receives a frame addressed receiving all data frames from the processor. From the unaddressed Ignore the data frame processor;
5 . It addressed after the last received data frame from the processor, set MPCM Position, and wait for the next frame address arrival. From the second step is then repeated.

use 5 To 8 Bit data frame format is possible, but impractical because the receiver must use n with n + 1 Switching between frame formats. Since the receiver and transmitter use the same character size settings, which makes full-duplex operation becomes difficult. If you use 5 To 8 Bit data frame format, the transmitter should be provided two stop bits, wherein the first stop bit is used for the frame type.

Register Definition

UCSRA - USART Control and status registers A

UCSRA - USART Control and status registers A								
address: 0xC0					Defaults: 0x20			
Bit	7	6	5	4	3	2	1	0
Name	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPME
R / W	R	R / W	R	R	R	R	R / W	R / W

Bit	Name	description
7	RXC	Receive Complete flag. when RXC Value "1" , It indicates that there is data in the receive buffer is not read out. when RXC Value "0" , It indicates that there are no data in the receive buffer is read out. When the receiver is disabled, the receive buffer is refreshed, resulting in RXC Is cleared. When the receiving end interrupt enable bit RXCIE for "1" Time, RXC It can be used to generate a Receive Complete interrupt.
6	TXC	Send flag. When the data transmission is sent to the shift register, and the transmit buffer is empty TXC Position. When performing transmission end interrupt TXC Automatically cleared, it can also pair TXC write "1" To be cleared. When sending end interrupt enable bit TXCIE for "1" Time, TXC It can generate a Transmit Complete interrupt.

5	UDRE	Data register empty flag. when UDRE for "1" When the show USART Transmission data buffer is empty, data can be written. when UDRE for "0" When the show USART Transmit data buffer is full, you can not write data. When the Data Register Empty Interrupt Enable bit UDRIE for "1" Time, UDRE Used to generate the data register empty interrupt.
4	FE	Framing error flag. when FE for "1" , It indicates that the reception data buffer the received data framing error, i.e., the first stop bit "0" . when FE for "0" , It indicates that the reception data buffer the received data frame is not erroneous, i.e., the first stop bit "1" . FE After being set remains in effect to UDR To be read. Correct UCSRA When writing, FE This is a write "0" .
3	DOR	Data overflow flag. When the receiving buffer is full (two characters), the receive shift register data, if detected at this time a new start bit, data overflow, DOR It is set, to remain in effect UDR To be read. Correct UCSRA When writing, DOR This is a write "0" .
2	PE	Parity error flag. When parity is enabled (UPM1 for "1"), The receive buffer and the received data frame has a parity error, PE It is set, to remain in effect UDR To be read. Correct UCSRA When writing, PE This is a write "0" .
1	U2X	Speed transmit enable bit. when U2X for "1" , The transmission rate of the asynchronous communication mode is doubled. when U2X for "0" , The transmission rate of the asynchronous communication mode for the normal rate. This bit is only valid in asynchronous mode of operation, this bit to zero when using synchronous mode of operation.
0	MPCM	Multiprocessor communication mode enable bit. Set up MPCM The start bit multiprocessor communication mode. MPCM After the set, USART Those received by the receiver input frame does not contain address information will be ignored. The transmitter is not MPCM Effects of the setting.

UCSRB - USART Control and status registers B

UCSRB **- USART Control and status registers B**								
address: 0xC1					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R	R / W

Bit	Name	description
7	RXCIE	Receive Complete interrupt enable bit. After setting enabling RXC Interruption, after clearing ban RXC Interrupted. when RXCIE for "1" , The global interrupt enable, UCSRA Register RXC for "1" Can generate when USART Receive Complete interrupt.
6	TXCIE	End of Transmit Interrupt Enable bit. After setting enabling TXC Interruption, after clearing ban TXC Interrupted. when TXCIE for "1" , The global interrupt enable, UCSRA Register TXC for "1" Can generate when USART Transmit Complete interrupt.
5	UDRIE	Data Register Empty interrupt enable bit. After setting enabling UDRE Interruption, after clearing ban UDRE Interrupted. when UDRIE for "1" , The global interrupt enable, UCSRA Register UDRE for "1" Can generate when USART Data Register Empty

		Interrupted.
4	RXEN	Receive Enable bit. After starting set USART receiver. RxD Universal pin IO Function is USART Receiving group. Disabling the Receiver will flush the receive buffer, and FE , DOR and PE Flag is not valid.
3	TXEN	Transmit Enable bit. After starting set USART Transmitter. TxD Universal pin IO Function is USART Transmitting the group. TXEN When cleared, only to wait until all the data is sent to truly complete ban USART send.
2	UCSZ2	Control characters in length 2 Bit. UCSZ2 versus UCSRC Register UCSZ1: 0 Together provided number of data bits contained in the frame.
1	RXB8	Receiving data of 8 Bit. When the data frame length 9 Bits, RXB8 Is the most significant bit of received data. Read UDR Low contained 8 Before reading the first bit of data RXB8 .
0	TXB8	The first transmit data 8 Bit. When the data frame length 9 Bits, TXB8 It is the highest transmit data. Write UDR Low contained 8 Written before the first bit of data TXB8 .

UCSRC- USART Control and status registers C

UCSRC **- USART Control and status registers C**								
address: 0xC2					Defaults: 0x06			
Bit	7	6	5	4	3	2	1	0
Name	UMSEL1	UMSEL0	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description	
7: 6	UMSEL1: 0	USART Mode Select bit. UMSEL Select synchronous or asynchronous modes of operation.	
		UMSEL	mode
		0	USART Asynchronous mode of operation
		1	USART Synchronous mode of operation
		2	SPI Slave modes of operation
		3	SPI The host operating mode
5: 4	UPM1: 0	Parity mode selection bit. High UPM1 Select enable or disable parity, low UPM0 Select odd or even parity.	
		UPM1: 0	mode
		0	Parity disabled
		1	Reserved
		2	Enable Enable odd
		3	parity even parity
3	USBS	Stop Bit Selection bit. Select the number of bits of stop bits.	
		USBS	Stop Bit
		0	1

		1	2	
2: 1	UCSZ1: 0	Character data frame length selection bits. UCSZ1: 0 versus UCSRB Register UCSZ2 Combined set of data bits contained in the data frame.		
		UCSZ2: 0	Data frame length	
		0	5 Place	
		1	6 Place	
		2	7 Place	
		3	8 Place	
		4	Retention	
		5	Retention	
		6	Retention	
		7	9 Place	
0	UCPOL	Clock Polarity Select bit. in USART Synchronous mode of operation, UCPOL Sampling and synchronization clock is provided to change the input data and output data XCK The relationship between. Use asynchronous mode of operation and UCPOL Nothing to do, this bit to zero		
		UCPOL	Transmit data changes	Receiving data samples
		0	XCK The rising edge	XCK Of falling
		1	XCK Of falling	XCK The rising edge

UBRRL - USART Baud Rate Register Low Byte

UBRRL **- USART Baud Rate Register Low Byte**								
address: 0xC4					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	UBRR7	UBRR6	UBRR5	UBRR4	UBRR3	UBRR2	UBRR1	UBRR0 R / W
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	UBRR [7: 0]	USART Low byte portion of register baud rate. USART Baud rate register comprising UBRRL with UBRRH Two parts, joined together to set the baud rate.

UBRRH - USART Baud Rate Register High Byte

UBRRH **- USART Baud Rate Register High Byte**								
address: 0xC5					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	UBRR11	UBRR10	UBRR9	UBRR8
R / W	-	-	-	-	R / W	R / W	R / W	R / W

Bit	Name	description
7: 4	-	Reservations.

<table>
<tr><td rowspan="5">3: 0</td><td rowspan="5">UBRR [11: 8]</td><td colspan="2">USART High byte portion of register baud rate.
USART Baud rate register comprising UBRRL with UBRRH Two parts, joined together to set the baud rate.
UBRR = {UBRR [11: 8], UBRRL}</td></tr>
<tr><td>Operating mode</td><td>The baud rate is calculated</td></tr>
<tr><td>Asynchronous Normal mode</td><td>BAUD = f $_{sys}$ / (16 * (UBRR + 1))</td></tr>
<tr><td>Asynchronous speed mode</td><td>BAUD = f $_{sys}$ / (8 * (UBRR + 1))</td></tr>
<tr><td>Synchronous Master Mode</td><td>BAUD = f $_{sys}$ / (2 * (UBRR + 1))</td></tr>
</table>

UDR - USART Data register

UDR - USART Data register								
address: 0xC6					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	UDR7	UDR6	UDR5	UDR4	UDR3	UDR2	UDR1	UDR0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	UDR	USART Transmission and reception of data. USART Transmission data and reception data buffer shared buffer USART Data register UDR . The data is written UDR That is written to the transmit data buffer, from UDR I.e., the read data read received data buffer. in 5 To 8 Lower frame mode data, the unused 9 Bits are ignored transmitter and the receiver they are set to 0 . Only when UCSRA Register UDRE Flag "1" When the transmit buffer to write, otherwise the operation of the transmitter to be wrong. When the transmit shift register is empty, the transmitter will transmit data in the buffer is loaded into the transmit shift register, and then serially from the data TxD Pin output. A receive buffer contains two FIFO Once the receive buffer is read, FIFO It will change its state.

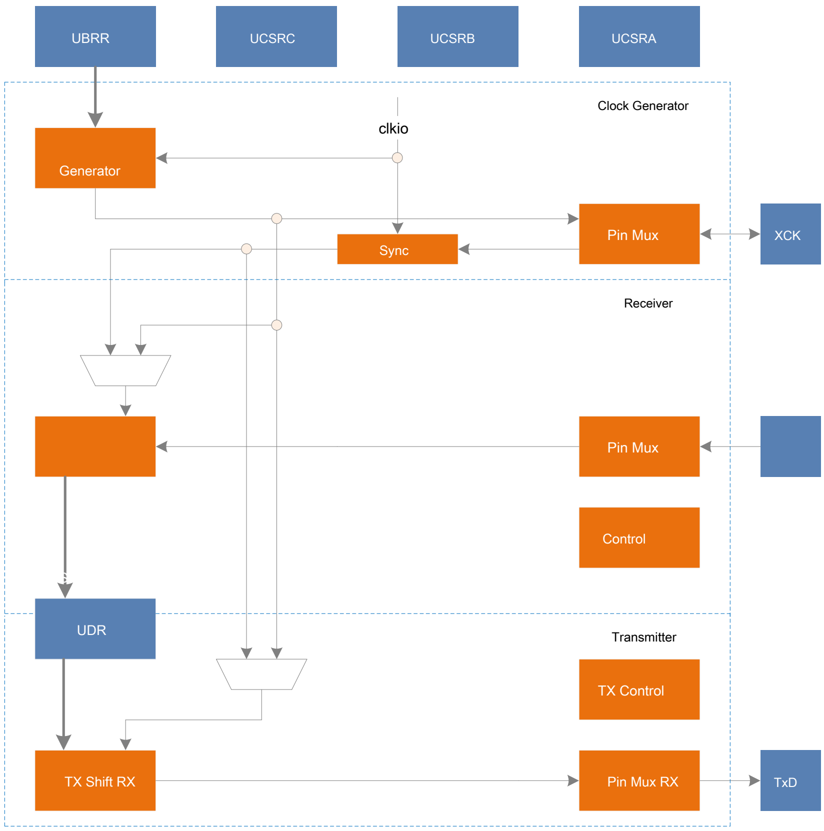
USART0 - SPI Operating mode

- Full-duplex operation, Three-wire synchronous data transfer
- Master or slave operation
- It supports all four operating modes (Mode 0 , 1 , 2 with 3)
- First, low or high transmission (transmission order data configurable)
- Queue operation (double buffer)
- High-resolution baud-rate generator

Overview

When set USCRC of UMSEL1 Bit "1" , Enable SPI Mode of operation, with USPI To represent. this SPI Three-wire module SPI Operating modes, and four-wire SPI Compared mode select line missing from the other three lines are consistent. USPI Occupancy

USART Resources, including transmit and receive shift register and a buffer, and the baud rate generator. Parity generation and checking logic, data and clock recovery logic are invalid. Address control and status registers is the same, but will function register bits with SPI Need to work patterns and change.



USART in SPI Structure chart

Clock Generation

when SPI Operating in master mode, it is necessary to provide communication with the clock, multiplexing USART The baud rate generator to generate the clock. The clock from XCK Pin output, XCK Pin data direction register (DDR_XCK) Must be set

"1" .

Clock frequency determined in the following formula:

BAUD = f_{sys} / (2 * (UBRR + 1))

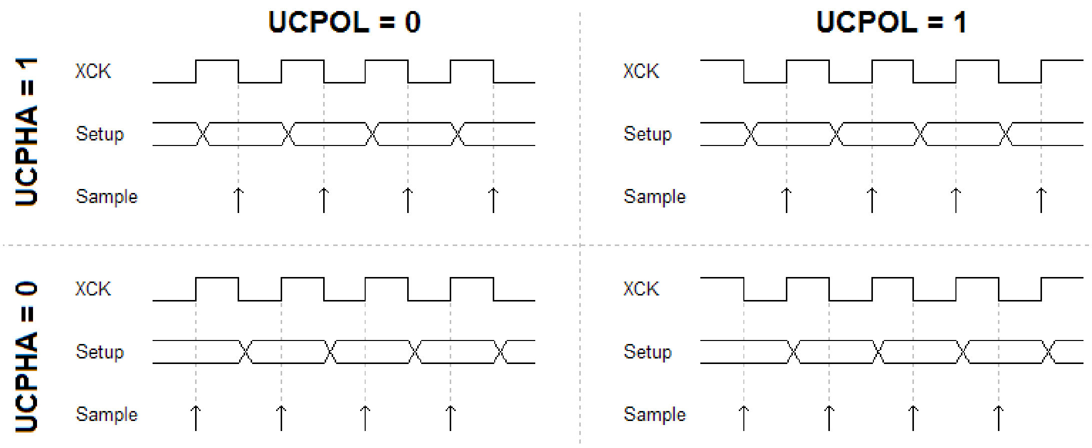
when SPI Operating in slave mode, the communication clock provided by the external host, from XCK Pin input, XCK Pin data direction register (DDR_XCK) Must be set "0" .

SPI Data mode and timing

SPI There are four kinds of combinations of polarity and clock phase, there are control bits UCPHA with UCPOL Determined, specific control and shown below in the following table:

SPI Operating mode

SPI mode	UCPOL	UCPHA	Starting along	Trailing Edge
0	0	0	The rising edge of sampling	Setting falling
1	0	1	Rising settings	Sampling falling
2	1	0	Sampling falling	Rising settings
3	1	1	Setting falling	The rising edge of sampling



SPI Work mode icon

Frame format

SPI A serial frame may start from the lowest or highest position, to the high or low end position, a total of 8 Bit data. After the end of a frame to be transmitted immediately a new frame, end of transmission to the data line pulled to the idle state.

data transmission

SPI Put UCSRB Register TXEN Bit "1" To enable the transmitter, TxD Pin is occupied by a transmitter transmits the serial output data. At this time, the receiver may not be enabled.

SPI Put UCSRB Register RXEN Bit "1" To enable the receiver, RxD Pin occupied by the receiver to receive the serial input data. At this point the transmitter must be enabled.

SPI Are used to send and receive XCK To as the transfer clock.

Before the first of the communication SPI Initialized. The initialization process normally includes setting the baud rate setting, the bit transmission order of the frame data, and if necessary, to enable the receiver or transmitter. For interrupt-driven SPI Operation, initialization

To clear the global interrupt flag and ban SPI All interrupts.

During reinitialization or a frame structure such as changing the baud rate, must ensure that no data transmission. TXC Flag may be used to detect whether or not the sender all the transmission, RXC Flag may be used to detect whether there is data in the receive buffer is not read. in case TXC Flag used for this purpose, before each transmission of data (write UDR Before register) must be cleared TXC Flag.

initialization SPI Later, to UDR Write data register to start data transfer. Since the transmitter controlling the transmission clock, data transmission and reception operation is true. When the transmit shift register is ready to transmit a new data, the transmitter will be written to the UDR Register data move buffer from the transmission in the transmit shift register and transmitted. In order to ensure synchronous transmission data input buffer and, after the transmission of each byte of data must be read once UDR register. When the data overflow occurs, the most recently received data will be lost, not the data was first received.

Send Flags and Interrupts

SPI Transmitter has two flags: SPI Data register empty flag UDRE And the transmission end flag TXC , Two flags can generate interrupts.

Data register empty flag UDRE It is used to indicate whether the transmit buffer to write a new data. This bit is set when the transmit buffer is empty "1" Full time is set "0" . when UDRE Bit "1" Time, CPU Data can go register UDR Write new data, not vice versa.

when UCSRB Data register empty interrupt enable register bit UDRIE for "1" When, as long as UDRE Is set (and global interrupts are enabled), will produce SPI Data Register empty interrupt request. To register UDR The write operation will be cleared
UDRE . When the interrupt transmission of data in the data register empty interrupt service routine must write new data to a UDR To clear UDRE , Or disable the Data Register Empty interrupt. Otherwise, if the interrupt service routine ends, a new interrupt will occur again.

When the entire data frame is sent out of the shift register while the register and no new transmission data, the transmission end flag TXC It will be set.
when UCSRB Send the end of last interrupt enable bit TXCIE (And the Global Interrupt Enable) "1" When, as TXC Flag is set, SPI Transmit Complete Interrupt will be executed. Once in the interrupt service routine, TXC Flag, this is automatically cleared, CPU This bit can also write "1" Cleared.

Disable the transmitter

when TXEN When cleared, and all the data only after the completion of transmission the transmitter can really disabled, i.e., the transmit shift register and the transmit data buffer register are not to be transmitted. Transmitter disabled later, TxD Pin restore its versatility
IO Features.

Reception complete flag and interrupt

SPI The receiver has a flag: Reception complete flag RXC , To indicate whether or not the data read out of the receive buffer. When the receive buffer data is not read, this bit "1" , Otherwise "0" . If the receiver is disabled, the receive buffer will be flushed, RXC It will be cleared. Position UCSRB Receive Complete Interrupt Enable bit RXCIE After long RXC Flag is set (provided that global interrupts are enabled), it will have SPI Receive Complete interrupt. When interrupt-driven data reception, data reception from the end of the interrupt service routine must UDR Read data cleared RXC Logo, or as long as

Interrupt handler to an end, a new interrupt will occur.

Disabling the Receiver

Compared with the transmitter, the receiver prohibits immediate. Is receiving data will be lost. Disabling the Receiver (RXEN When cleared), the receiver will not take up RxD Pin, the receive buffer will be flushed.

Register Definition

USART Register List

register address		Defaults	description
UCSRA	0xC0	0x20	USPI Control and status registers A
UCSRB	0xC1	0x00	USPI Control and status registers B
UCSRC	0xC2	0x06	USPI Control and status registers C
UBRRL	0xC4	0x0	USPI Baud Rate Register Low Byte
UBRRH	0xC5	0x0	USPI Baud Rate Register High Byte
UDR	0xC6	0x0	USPI Data register

UCSRA - USPI Control and status registers A

UCSRA - USPI Control and status registers A								
address: 0xC0					Defaults: 0x20			
Bit	7	6	5	4	3	2	1	0
Name	RXC	TXC	UDRE	-	-	-	-	-
R / W	R	R / W	R	-	-	-	-	-

Bit	Name	description
7	RXC	Receive Complete flag. when RXC Value "1" , It indicates that there is data in the receive buffer is not read out. when RXC Value "0" , It indicates that there are no data in the receive buffer is read out. When the receiver is disabled, the receive buffer is refreshed, resulting in RXC Is cleared. When the receiving end interrupt enable bit RXCIE for "1" Time, RXC It can be used to generate a Receive Complete interrupt.
6	TXC	Send flag. When the data transmission is sent to the shift register, and the transmit buffer is empty TXC Position. When performing transmission end interrupt TXC Automatically cleared, it can also pair TXC write "1" To be cleared. When sending end interrupt enable bit TXCIE for "1" Time, TXC It can generate a Transmit Complete interrupt.
5	UDRE	Data register empty flag. when UDRE for "1" When the show USPI Transmission data buffer is empty, data can be written. when UDRE for "0" When the show USPI Transmit data buffer is full, you can not write data. When the Data Register Empty Interrupt Enable bit UDRIE for "1" Time, UDRE Used to generate the data register empty interrupt.
4: 0	-	USPI Under Reserved.

UCSRB - USPI Control and status registers B

UCSRB - USPI Control and status registers B								
address: 0xC1					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	RXCIE	TXCIE	UDRIE	RXEN	TXEN	-	-	-
R / W	R / W	R / W	R / W	R / W	R / W	-	-	-

Bit	Name	description
7	RXCIE	Receive Complete interrupt enable bit. After setting enabling RXC Interruption, after clearing ban RXC Interrupted. when RXCIE for "1" , The global interrupt enable, UCSRA Register RXC for "1" Can generate when USPI Receive Complete interrupt.
6	TXCIE	End of Transmit Interrupt Enable bit. After setting enabling TXC Interruption, after clearing ban TXC Interrupted. when TXCIE for "1" , The global interrupt enable, UCSRA Register TXC for "1" Can generate when USPI Transmit Complete interrupt.
5	UDRIE	Data Register Empty interrupt enable bit. After setting enabling UDRE Interruption, after clearing ban UDRE Interrupted. when UDRIE for "1" , The global interrupt enable, UCSRA Register UDRE for "1" Can generate when USPI Data Register Empty interrupt.
4	RXEN	Receive Enable bit. After starting set USPI receiver. RxD Universal pin IO Function is USPI Receiving group. Disabling the Receiver will flush the receive buffer.
3	TXEN	Transmit Enable bit. After starting set USPI Transmitter. TxD Universal pin IO Function is USPI Transmitting the group. TXEN When cleared, only to wait until all the data is sent to truly complete ban USART send.
2: 0	-	USPI Under Reserved.

UCSRC- USART Control and status registers C

UCSRC - USART Control and status registers C								
address: 0xC2					Defaults: 0x86			
Bit	7	6	5	4	3	2	1	0
Name	UMSEL1	UMSEL0	-	-	-	DORD	UCPHA	UCPOL
R / W	R / W	R / W	-	-	-	R / W	R / W	R / W

Bit	Name	description
7: 6	UMSEL1: 0	USART Mode Select bit. UMSEL Select synchronous or asynchronous modes of operation. UMSEL / mode: 0 - USART Asynchronous mode of operation 1 - USART Synchronous mode of operation 2 - SPI Slave modes of operation 3 - SPI The host operating mode
5: 3	-	USPI Under Reserved.

<table>
<tr><td rowspan="4">2</td><td rowspan="4">DORD</td><td colspan="3">Data transfer select bit sequence.</td></tr>
<tr><td>DORD</td><td colspan="2">Order data</td></tr>
<tr><td>0</td><td colspan="2">MSB-first transfer</td></tr>
<tr><td>1</td><td colspan="2">LSB first transmission</td></tr>
<tr><td rowspan="4">1</td><td rowspan="4">UCPHA</td><td colspan="3">Clock phase selection.
UCPHA Select data sampling occurs at the start edge or the end edge.</td></tr>
<tr><td>UCPHA</td><td colspan="2">Sampling time</td></tr>
<tr><td>0</td><td colspan="2">Starting along</td></tr>
<tr><td>1</td><td colspan="2">Trailing Edge</td></tr>
<tr><td rowspan="4">0</td><td rowspan="4">UCPOL</td><td colspan="3">Clock polarity selection.
UCPOL And changing the selection data sampled on the rising edge or falling edge.</td></tr>
<tr><td>UCPOL</td><td>Change the transmission of data</td><td>Sampling the received data</td></tr>
<tr><td>0</td><td>XCK The rising edge</td><td>XCK Of falling</td></tr>
<tr><td>1</td><td>XCK Of falling</td><td>XCK The rising edge</td></tr>
</table>

UBRRL - USPI Baud Rate Register Low Byte

UBRRL - USPI Baud Rate Register Low Byte								
address: 0xC4					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	UBRR7	UBRR6	UBRR5	UBRR4	UBRR3	UBRR2	UBRR1	UBRR0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	UBRR [7: 0]	USPI Low byte portion of register baud rate. USPI Baud rate register comprising UBRRL with UBRRH Two parts, joined together to set the baud rate.

UBRRH - USPI Baud Rate Register High Byte

UBRRH - USPI Baud Rate Register High Byte								
address: 0xC5					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	UBRR11	UBRR10	UBRR9	UBRR8
R / W	-	-	-	-	R / W	R / W	R / W	R / W

Bit	Name	description
7: 4	-	USPI Under Reserved.
3: 0	UBRR [11: 8]	USPI High byte portion of register baud rate. USPI Baud rate register comprising UBRRL with UBRRH Two parts, joined together to set the baud rate. UBRR = {UBRR [11: 8], UBRRL}

		Operating mode	The baud rate is calculated
		Slave mode	The baud rate is determined by the external host
		Host mode	BAUD = f_{sys} / (2 * (UBRR + 1))

UDR - USPI Data register

UDR - USPI Data register								
address: 0xC6					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	UDR7	UDR6	UDR5	UDR4	UDR3	UDR2	UDR1	UDR0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	UDR	USPI Transmission and reception of data. USPI Transmission data and reception data buffer shared buffer USPI Data register UDR . The data is written UDR That is written to the transmit data buffer, from UDR I.e., the read data read received data buffer. in 5 To 8 Lower frame mode data, the unused 9 Bits are ignored transmitter and the receiver they are set to 0 . Only when UCSRA Register UDRE Flag "1" When the transmit buffer to write, otherwise the operation of the transmitter to be wrong. When the transmit shift register is empty, the transmitter will transmit data in the buffer is loaded into the transmit shift register, and then serially from the data TxD Pin output. A receive buffer contains two FIFO Once the receive buffer is read, FIFO It will change its state.

TWI - Two-wire serial bus (I2C)

- Simple and powerful and flexible communication interface, only 2 line
- Support master and slave operation
- Device may operate in transmission mode or reception mode
- 7 Bit address space allows 128 Slaves
- It supports multi-master arbitration
- Up 400Kbps Data transfer rate
- Fully programmable slave address and a public address
- You can wake address match in sleep mode

TWI Bus Introduction

Two-wire Serial Interface TWI Well suited for typical microcontroller applications. TWI Protocol allows a system designer using only two bidirectional transmission line can be 128 Different devices interconnected together. These two lines are clock SCL And data SDA . Only external hardware connected to the two lines of each pull-up resistors. All devices connected to the bus has its own address. TWI Agreement to solve the problem of bus arbitration.

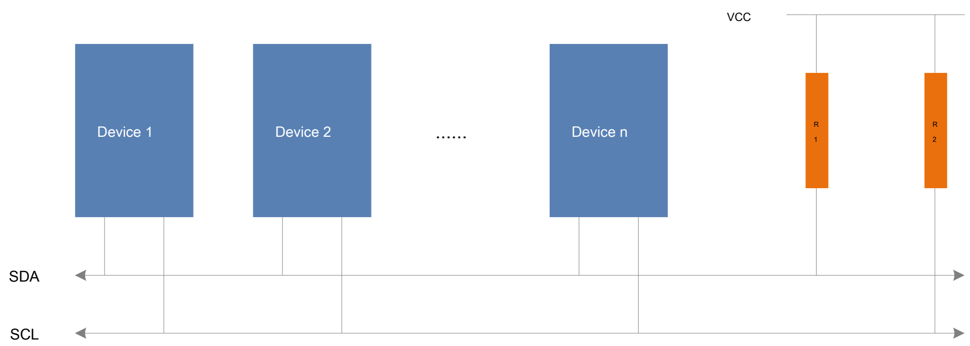
TWI the term

The following defined terms appear frequently in this section.

the term	description
Host computer	Starting and stopping the transmission equipment. Host also responsible for generating SCL clock.
Slave	Addressed by a master device
Transmitter	Device placing data on the bus
receiver	Receiving data from devices on the bus

Electrical connections

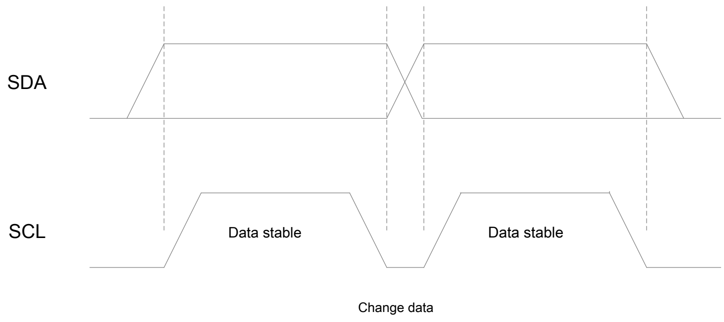
As shown below, TWI Two-wire interface through pull-up resistors connected to the positive supply. all TWI The bus driver compliant devices are open-drain or open-collector line and thus achieve the function of the interface operation. when TWI Output devices "0" Time, TWI It generates a low level bus. When all TWI When the tri-state output device, allows pull-up resistor bus voltage high. To ensure that all bus operations, all with TWI Devices connected to the bus must be powered on.



TWI The bus interconnect of FIG.

Data transmission and frame structure

TWI Every data transfer on the bus and the clock are synchronized. While the clock is high, the level of the data line must remain stable, except to start or stop generating state.

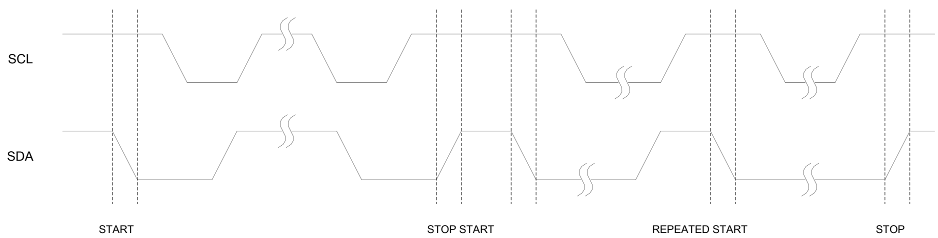


TWI Data validation map

Start and stop state

TWI The transmission is started and stopped by the host. Host issues on the bus START Send its data transfer status, issued STOP State to stop the data transmission. in START with STOP Between the state, the bus is considered busy, do not allow other hosts trying to take the control of the bus. There is a special case only allowed to occur in START with STOP Generating a new state between START State, which is called REPEATED START Status for the current host to start a new transfer, without giving up control of the bus. REPEATED START Until next STOP Previously, the bus is still considered busy. This START It is the same, so in this document, unless otherwise stated, are used START To express START

with REPEATED START . As shown below, START with STOP Conditions in SCL When the line is high, changes SDA The level of status line.



START , REPEATED START with STOP State diagram

Address Packet Format

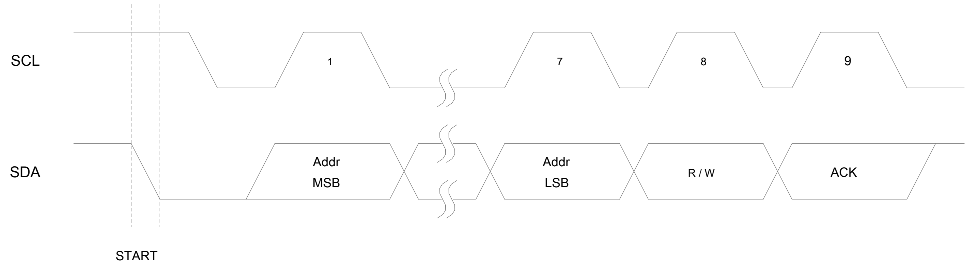
all TWI Address packet transmitted on the bus are 9 Bit data length, from the 7 Bit address, 1 Place READ / WRITE And control bits 1 Bit acknowledgment bit. when READ / WRITE Bit "1" , The read operation is performed; when READ / WRITE Bit "0" , The write operation is performed. When a slave is addressed must first 9 More SCL (ACK) By pulling cycle SDA Line to make a response. If the slave is busy or there are other reasons not respond to the host, you should ACK Keep the cycle SDA Line is high. The host can then issue STOP State or REPEATED START State resumes sent.

Address of the packet includes a slave address and a read or write control bits, respectively, SLA + R or SLA + W To represent.

Address byte MSB Bit occurs first. In addition to retaining Address "00000000" It was left for broadcast calls and all of the form "1111xxxx" Address formats need to be retained for future use, the other slave address can be freely assigned designer.

When a general call occurs, all slaves should ACK Cycle by pulling SDA Line to make a response. When the host needs to send the same information to a plurality of slaves in the system using the broadcast feature. When the call address plus WRITE After the bits are sent on the bus, all in response to the need to broadcast the call from the machine ACK Cycle down SDA line. All of the general call response from the receiving unit will be followed by a data packet. It should be noted that, coupled with a general call address READ Bit does not make sense, because if several slaves simultaneously transmit different data bus will bring conflict.

Address packet format as shown below:

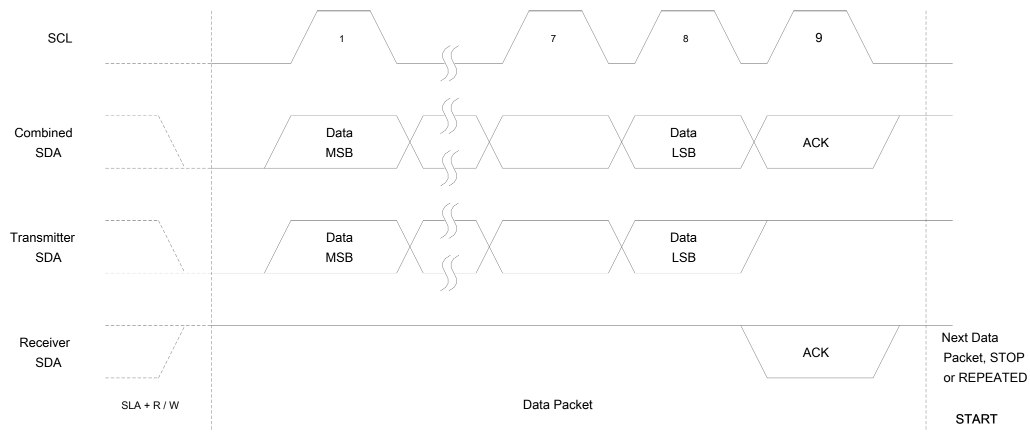


TWI Address Packet Format FIG.

Packet format

all TWI On the bus packets are transmitted 9 Bit data length, from the 1 Data bytes and 1 Bit acknowledgment bit. During data transfer, the master is responsible for generating the transmission clock SCL with START and STOP State, the transmitter transmits the data byte to be transmitted, the receiver generates a reception response. Confirmation signal ACK At the receiver is 9 More SCL (ACK) By pulling cycle SDA Lines generated. If the receiver ACK Keep the cycle SDA Line is high, the signal sent unacknowledged NACK . When the receiver has received the last byte, or for some reason can not receive any data, you should receive the last byte sent by NACK To inform the sender. Data bytes MSB Bit first.

Packet format is shown below:

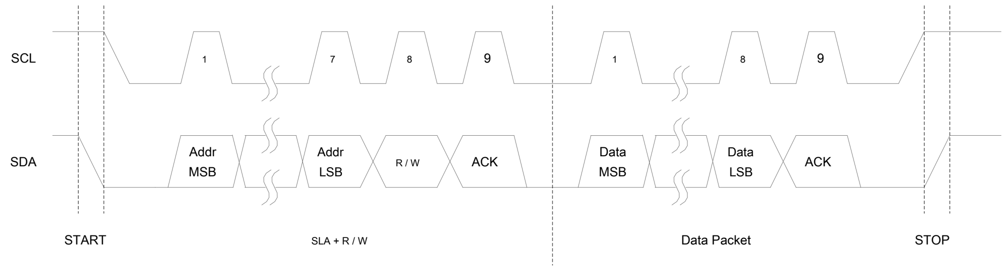


TWI Packet Format FIG.

Transmitting the combined address and data packets, a transmission consists essentially of 1 More START , 1 More SLA + R / W , 1 Or more

Packet and 1 More STOP composition. only START with STOP Empty information is illegal. can use SCL Wire line and shake hands with the main function to achieve from the machine. Slave down by SCL To extend the line SCL The ground level cycle. When the host is set much faster than the clock slave or slave requires additional time to process the data, this feature is very useful. Slave to extend SCL LOW period does not affect SCL High-level period, it is still determined by the host. It can be seen, by changing the slave SCL To reduce the duty cycle TWI The data transmission speed.

A typical data transfer is shown below. note SLA + R / W versus STOP It can be transferred between a plurality of bytes, depending on the application software to implement the protocols.



typical TWI transmission

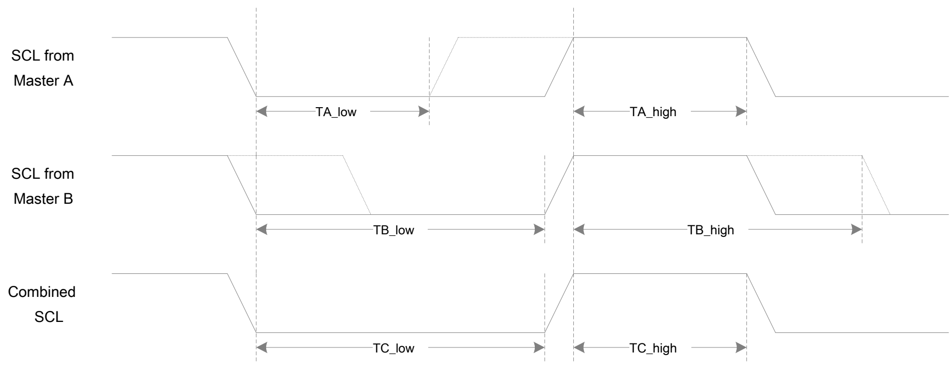
Multi-host system and arbitration and synchronization

TWI Bus protocol allows multiple hosts, and the use of special measures to ensure that even if two or more hosts can be simultaneously start the transfer process the same as normal transmission. Multi-host system there will be two questions:

1. The algorithm allows only one host, multiple hosts to complete the transfer. When other hosts find that they will lose the right to choose
   To cease their transmission. The selection process is called arbitration. When a contending master arbitration found to fail, the address should switch immediately to the host whether it is control of the bus slave mode to detect. Indeed multiple hosts simultaneously should not be detected from the machine at the start of transmission, i.e., destruction of data being transferred is not allowed on the bus.
2. Different hosts may use different SCL frequency. To ensure a consistent transfer, you must design a synchronous serial host
   Line clock program. This will facilitate the arbitration process.

Bus line and the function is to solve the above problems. All hosts are serial clock line to generate a composition with clock, high time which is equal to a master clock in all the shortest, equal to its low level in all the longest of the host clock. All masters listen SCL When combined SCL When the clock goes high or low, respectively, they can be effectively calculate respective start SCL High and low out period.

Multi-host SCL The clock synchronization mechanism as shown below:



Multi-Host SCL Clock synchronization timing chart

After the output data of all the masters continuously monitoring SDA Line to implement the arbitration. If the SDA Numerical values of the host read back output does not match, the hosts lost the arbitration. It is noted that the host outputs a high level SDA , And another master outputs a low level SDA When will lose the arbitration. The hosts lost the arbitration shall be immediately converted to the slave mode, and detects whether being addressed. The host must be lost arbitration SDA Line is set high, but a clock signal may also be generated before the end of the current data or address packet. Arbitration will continue until only one host, which may consume more bits. When the master unit from the same address, the packet will continue arbitration.

Arbitration between the two hosts

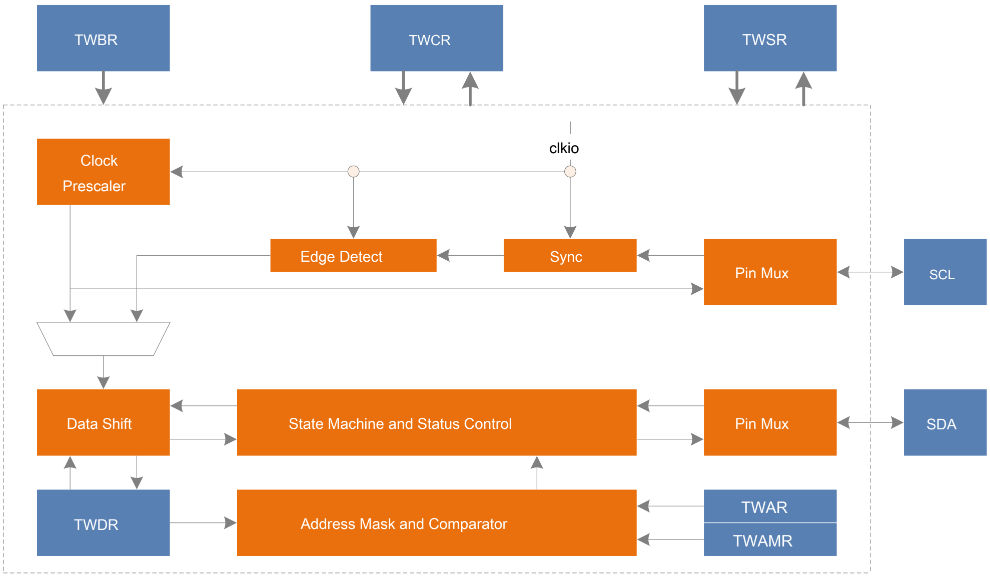
Note that arbitration is not allowed in the following situations:

- One REPEATED START Between a state and a data bit;
- One STOP Between a state and a data bit;
- One REPEATED START State and STOP Between states;

Applications must consider the above, to ensure that these illegal arbitration case does not appear. This means that in a multi-host system, all data must be transmitted by the same SLA + R / W And data packets. In other words, all of the transmission must contain the same number of data packets, otherwise the result of the arbitration can not be defined.

TWI Module Summary

TWI FIG module configuration as shown in FIG.



TWI Block Structure chart

TWI Generator module includes a bit rate, the bus interface unit, the address comparator and the control unit or the like. See in particular the following detailed description.

Bit Rate Generator Unit

Bit rate generator mode control host unit is mainly SCL Clock cycle. SCL Clock cycle by the TWI Bit Rate Register TWBR with TWI Status Register TWSR The prescaler control bits joint decision. From the operating bit rate or not affect the frequency prescaler setting, but to ensure that the slave clock working at least SCL Frequency of 16 Times. Note that the slave may be extended SCL LOW period, thereby reducing TWI The average frequency of the bus clock. SCL Clock frequency is generated has the following formula:

$f_{scl} = f_{sys} / (16 + 2 * TWBR * 4_{TWPS})$

among them, TWBR for TWI Register bit rate value, TWPS for TWI Status register pre-division control bits.

Bus Interface Unit

Bus interface unit includes a data shift register and an address TWDR , START / STOP And the controller determines the arbitration hardware.

TWDR It contains the address or data bytes to be sent, or an address or data byte has been received. In addition to containing 8 Bit TWDR The bus interface unit further includes a transmission or reception of ACK / NACK register. This one ACK / NACK Register can not be accessed applications. When data is received, it can be TWI Control register TWCR To set or cleared. When transmitting data, received ACK / NACK Value of TWI Status Register TWSR middle TWS Value to reflect.

START / STOP Controller is responsible for generation and detection START , REPEATED START with STOP status. when MCU While in some sleep modes, START / STOP The controller can still be detected START with STOP State, when the TWI Addressing on the bus master when MCU Wake-up from sleep mode.

in case TWI Host-initiated data transfer mode, arbitration detection circuit will continue to monitor the bus to determine if still has control of the bus. when TWI After the loss of control of the bus module, the control unit will perform the proper operation and generate the appropriate status code to notify MCU .

Address matching means

Address matching means for checking whether the received address byte and TWI Address register 7 Bit address match. when TWAR Register TWI Broadcast Enable bit call identification (TWGCE) Is set, the address received from the bus to the broadcast address will be compared. Upon an address match, the control unit will execute the correct action. TWI Response, or module does not respond to its address, depending on the TWCR Register is set. Even in the sleep mode, the address matching unit may compare the address, if they are addressed by a master on the bus, then MCU Wake-up from sleep mode.

control unit

The control unit is responsible for monitoring the bus and in accordance with TWCR Setting produces a corresponding response. when TWI When an event occurs it requires applications to participate on the bus, TWI Interrupt flag TWINT It will be set. In the next clock cycle, TWI Status Register TWSR It will be updated to show the status code of the event. in TWINT When set, TWSR It contains the exact status information. At other times, TWSR For a special status code indicating that there is no exact status information. once TWINT Flag is set, SCL Line has been kept low, pause on the bus TWI Transmission, so that the application process events.

Under the following circumstances, TWINT Flag will be set:

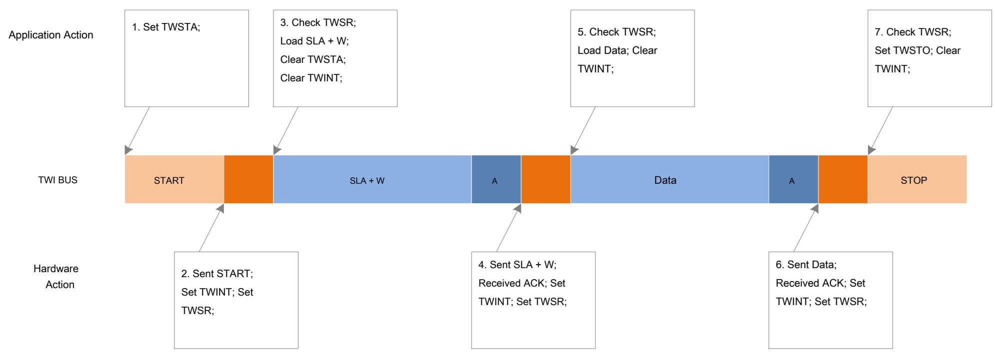
- TWI End transmission START / REPEATED START After the state
- TWI End transmission SLA + R / W Rear
- TWI After transmitting an address byte
- TWI Bus after arbitration loss
- TWI After being addressed by the master (or slave address match broadcast)
- It addressed as work from the machine, receive STOP or REPEATED START Rear
- The illegal START or STOP When the state caused by the bus error

TWI usage of

TWI The interface is byte-oriented and interrupt based. All bus event, such as a byte received or transmitted an START Signal, will have a TWI Interrupted. due to TWI Is interrupt-based, so TWI Byte transfer process, the application software can perform other operations freely. TWCR Register TWI Interrupt enable bit TWIE And global interrupt enable bit in the control together TWINT Whether generated when the flag is set TWI Interrupted. in case TWIE Bit is cleared, the application must query TWINT Way to detect flag TWI Action on the bus.

when TWINT When the flag is set, it indicates TWI Interface to complete the current operation, wait for the response from the application. under these circumstances, TWI Status Register TWSR It contains reflect the current state of the bus status code. Applications can set TWCR with TWDR Register, to decide in the next TWI Bus cycle TWI How the interfaces work.

The following figure shows the applications and TWI Examples of connection interface. In this embodiment, the host desires to transmit one byte of data to the slave. Described here is very simple, the next chapter will have a more detailed presentation.



TWI A typical transmission procedure of FIG.

Shown in FIG. TWI Transmission process is:

1. TWI The first step is to send transmission START . Go through TWCR Register writing a specific value, indicating TWI Send hardware START signal. Value is written will be explained in detail subsequently. Writing the value to be set TWINT It is very important to TWINT Write bit "1" This bit will be cleared. TWCR Register TWINT During the set TWI Not start any operation. Once the software is cleared TWINT Position, TWI Module start immediately START The transmitted signal.
2. when START State sent, TWCR of TWINT Flag will be set, TWSR The new update of the status code, Show START Signal was successfully sent.
3. Application View TWSR The value is determined START The state has been successfully sent. in case TWSR Display other values, Applications can perform some special operations, such as error handler is called. When the determination is consistent with the expected status code, the program SLA + W The value loaded into TWDR Register. TWDR It can be used simultaneously in the address register and data. Then the software to TWCR Register writing a specific value, indicating TWI Send hardware TWDR middle SLA + W Value. Value is written will be explained in detail subsequently. Writing the value to be set TWINT To clear TWINT Flag. TWCR Register TWINT During the set TWI Not start any operation. Once the software is cleared TWINT Position, TWI Module start address of the packet transmitted immediately.
4. When the address packet has been sent, TWCR of TWINT Flag will be set, TWSR Updated with the new status code table Illustrates address packet successfully transmitted. Status code will also reflect whether to respond to the slave address of the packet.
5. Application View TWSR Value, determine the address of the packet has been successfully sent, received ACK To the desired value. in case TWSR Display other values, the application can perform some special operations, such as error handler is called. When the determination is consistent with the expected status code, the program Data The value loaded into TWDR Register. Then the software to TWCR Register writing a specific value, indicating TWI Send hardware TWDR middle Data Value. Value is written will be explained in detail subsequently. Writing the value to be set TWINT To clear TWINT Flag. TWCR Register TWINT During the set TWI Not start any operation. Once the software is cleared TWINT Position, TWI Module immediately initiates the transfer of data packets.
6. When the data packet has been sent, TWCR of TWINT Flag will be set, TWSR Updated with the new status code table Illustrates packet successfully transmitted. Status code will also reflect whether the slave responds to the packet.
7. Application View TWSR Value, determines that the data packet was successfully transmitted, received ACK To the desired value. in case TWSR Display other values, the application can perform some special operations, such as error handler is called. When the agreement to determine the status code is as expected, to software TWCR Register writing a specific value, indicating TWI Send hardware STOP signal. Value is written will be explained in detail subsequently. Writing the value to be set TWINT To clear TWINT Flag. TWCR Register TWINT During the set TWI Not start any operation. Once the software is cleared TWINT Position, TWI Module start immediately STOP The transmitted signal. It should be noted that, in the STOP After the signal has been sent TWINT It will not be set.

Although this example is simple, but it contains TWI All the rules of data during transmission. Summarized as follows:

- when TWI Upon completion of an operation and expects feedback application, TWINT Flag. SCL Clock line is up

Down until the TWINT Is cleared;

- when TWINT Flag is set, the user must update all TWI The next value of the register TWI Bus cycle correlation values. E.g, TWDR Value register must be loaded next bus cycle be sent.
- After completion of updating all registers, and perform other necessary operations, the application writes TWCR register. Write TWCR Time, TWINT Bit must be set for clearing TWINT Mark. TWINT After being cleared, TWI Started by a TWCR Set operation.

Transfer mode

TWI You can work in the following 4 The main species: master transmitter (MT), Host receiver (MR), Transmitted from the machine (ST) And slave receivers (SR). Under the same application you can use a variety of modes. E.g, TWI can use MT Mode to TWI EEPROM Writing data, with MR Mode from EEPROM Read the data. If there are other hosts on the system, some may go TWI Transmitting data, will be used SR mode. This is determined by the application software which mode is used.

Below these modes will be described in detail. In the data transmission in each mode, the image will be described in conjunction with the possible status codes. These images contain the following abbreviations:

S : Start status

Rs : REPEATED START status

R : Read flag (SDA HIGH)

W : Write flag (SDA LOW)

A: Acknowledge bit (SDA LOW)

NA : No acknowledge bit (SDA HIGH)

Data : 8 Bit data byte

P : STOP status

SLA : Slave address

Picture used to represent the circle TWINT Flag is set, the digital circle shows TWSR Register status code, wherein the pre-division control bits are masked as "0" . In these places, the application must perform the appropriate actions to continue or complete TWI transmission. TWI Transmission will be suspended until TWINT Flag is cleared.

when TWINT Flag is set, TWSR The status code is used to determine the proper software operation. Each table shows details of the software operation and the subsequent serial transfer of code required for each state. Note that the form TWSR Prescaler bits are masked as "0" .

Host mode

In the master transmission mode, TWI It will send a certain number of data bytes to a slave-receiver. To enter host mode, you must send START signal. The next decision to address packet format TWI Mode is the master transmitter or receiver mode host. If you send SLA + W , Then enter the master transmitter mode. If you send SLA + R , The master receiver mode. The status code section referred to assume control bit prescaler "0" .

Go through TWCR Register write to emit following values START signal:

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
1	x	1	0	x	1	0	x

TWEN Bit must be set "1" To enable TWI interface, TWSTA Put "1" To send START signal, TWINT Put "1" Cleared

TWINT Flag. TWI State detection module bus, when the bus is idle transmitted immediately START signal. When sending the START

After the hardware is set TWINT Flag while updating TWSR The status code 0x08 .

To enter the master transmitter mode, you must send SLA + W . This can be accomplished by the following operation. First to the TWDR Write register SLA + W , Then go TWINT Write bit "1" Clear TWINT Flag to continue the transmission, that is to TWCR Transmitting register write the following values SLA + W :

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
1	x	0	0	x	1	0	x

when SLA + W Send completed and received the response signal, TWINT It has been set, at the same time TWSR The status code update. Possible status code 0x18 , 0x20 or 0x38 . In response to each state will be described in detail in the appropriate code status code table.

when SLA + W After sending successfully, you can start sending packets. This can be done to TWDR Writing register data to complete.

TWDR only at TWINT When the flag is high it can be written. Otherwise, access is ignored and the write collision flag TWWC

It will be set. Update complete TWDR After, to TWINT Write bit "1" Clear TWINT Flag to continue the transfer. That is to TWCR

Register write data transmitted following values:

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
1	x	0	0	x	1	0	x

When the end of packet and receive the response signal, TWINT It has been set, at the same time TWSR The status code update. Possible status code 0x28 or 0x30 . In response to each state will be described in detail in the appropriate code status code table.

When the data is sent successfully, you can continue to send data packets. This process is repeated until the last byte sent. The master generates STOP Signal or REPEATED START The entire signal transmission until the end.

Go through TWCR Register write to emit following values STOP signal:

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
1	x	0	1	x	1	0	x

Go through TWCR Register write to emit following values REPEATED START signal:

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
1	x	1	0	x	1	0	x

In sending REPEATED START (Status code 0x10)after that, TWI Interface can access the same slave again, or visit the new slave without sending a STOP signal. REPEATED START That may be different from the host machine, switching between the host and the host receiving the transmission mode without losing control of the bus.

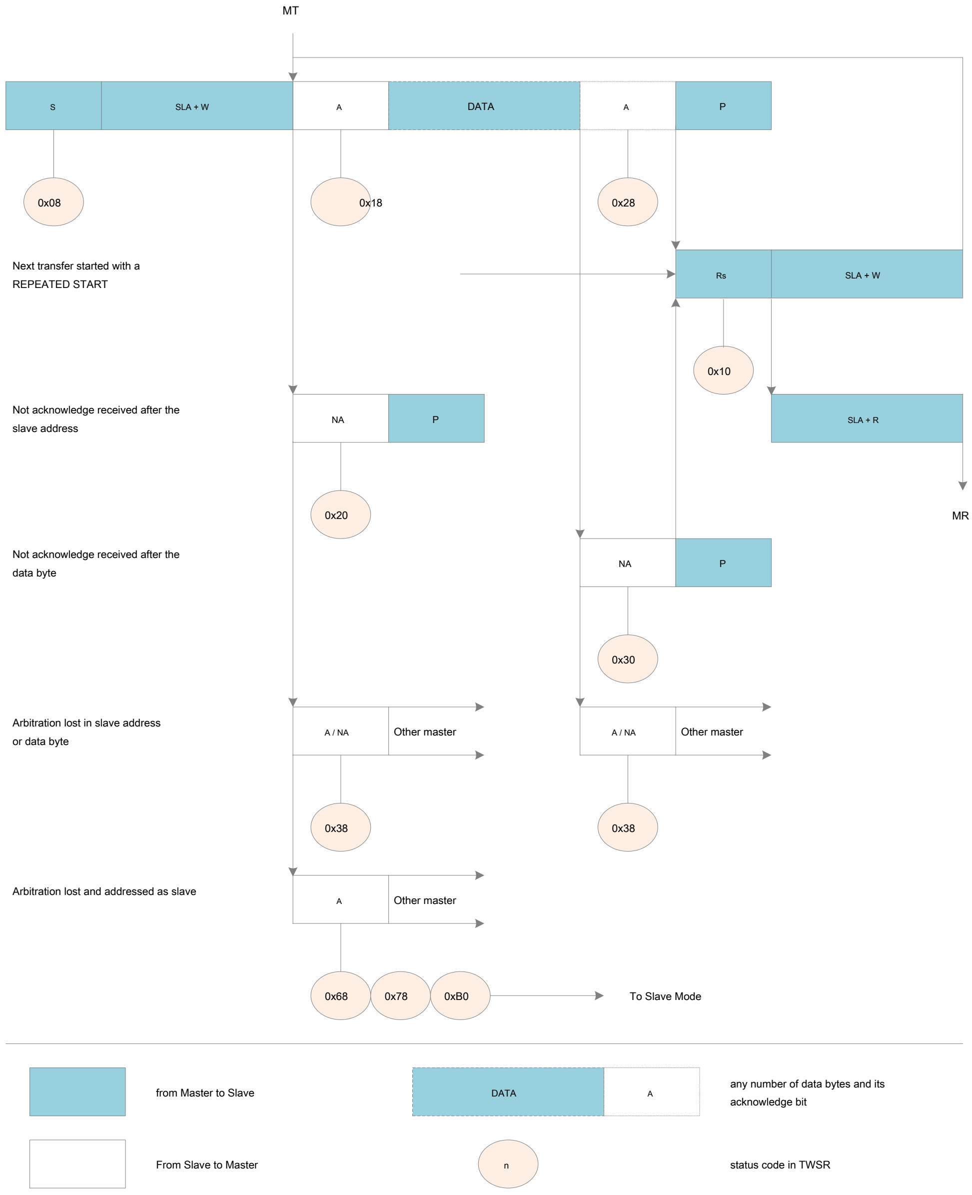
Status code in master transmission mode and a corresponding operation in the following table:

Status of the host transmission mode code table

status code	Bus and hardware status	Response application software					Hardware next move
		Read / Write TWDR	Correct TWCR Operations				
			STA	STO	TWINT	TWEA	
0x08	START Has been sent	load SLA + W	0	0	1	x	Will send SLA + W ; The reception ACK or NACK
0x10	REPEATED START sent	load SLA + W	0	0	1	x	Will send SLA + W ; The reception ACK or NACK

	give away	load SLA + R	0	0	1	x Will send SLA + R ; The reception ACK or NACK; Will switch to MR mode
0x18	SLA + W It has been sent; received ACK	Download Data	0	0	1	x Transmitting data; The reception ACK or NACK
		No action	1	0	1	x Will send REPEATED START
		No action	0	1	1	x Will send STOP ; Reset TWSTO Mark
		No action	1	1	1	x Will send STOP ; Reset TWSTO Signs; sending START
0x20	SLA + W It has been sent; received NACK	Download Data	0	0	1	x Transmitting data; The reception ACK or NACK
		No action	1	0	1	x Will send REPEATED START
		No action	0	1	1	x Will send STOP ; Reset TWSTO Mark
		No action	1	1	1	x Will send STOP ; Reset TWSTO Signs; sending START
0x28	Data bytes It has been sent; received ACK	Download Data	0	0	1	x Transmitting data; The reception ACK or NACK
		No action	1	0	1	x Will send REPEATED START
		No action	0	1	1	x Will send STOP ; Reset TWSTO Mark
		No action	1	1	1	x Will send STOP ; Reset TWSTO Signs; sending START
0x30	Data bytes It has been sent; received NACK	Download Data	0	0	1	x Transmitting data; The reception ACK or NACK
		No action	1	0	1	x Will send REPEATED START
		No action	0	1	1	x Will send STOP ; Reset TWSTO Mark
		No action	1	1	1	x Will send STOP ; Reset TWSTO Signs; sending START
0x38	SLA + W Arbitration or data failure	No action	0	0	1	x Will release the bus; The addressed slave mode does not enter
		No action	1	0	1	x Will be sent when idle START

Format and status of the host transmission mode as shown below:



Master transmission mode format and a state diagram

Master Receiver Mode

In the master reception mode, TWI You will receive an amount of data bytes from a slave transmitter. To enter host mode, you must send START signal. The next decision to address packet format TWI Mode is the master transmitter or receiver mode host. If you send SLA + W , Then enter the master transmitter mode. If you send SLA + R , The master receiver mode. The status code section referred to assume control bit prescaler "0" .

Go through TWCR Register write to emit following values START signal:

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
1	x	1	0	x	1	0	x

TWEN Bit must be set "1" To enable TWI interface, TWSTA Put "1" To send START signal, TWINT Put "1" Cleared TWINT Flag. TWI State detection module bus, when the bus is idle transmitted immediately START signal. When sending the START After the hardware is set TWINT Flag while updating TWSR The status code 0x08 .

In order to enter the host receive mode must be sent SLA + R . This can be accomplished by the following operation. First to the TWDR Write register SLA + R , Then go TWINT Write bit "1" Clear TWINT Flag to continue the transmission, that is to TWCR Transmitting register write the following values SLA + R :

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
1	x	0	0	x	1	0	x

when SLA + R Send completed and received the response signal, TWINT It has been set, at the same time TWSR The status code update. Possible status code 0x38 , 0x40 or 0x48 . In response to each state will be described in detail in the appropriate code status code table.

when SLA + R After successful transmission you can begin receiving data packets. Go through TWINT Write bit "1" Clear TWINT Flag to continue to receive. That is to TWCR Register write start receiving the following values:

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
1	x	0	0	x	1	0	x

When the received data packet and the transmission completion response signal, TWINT It has been set, at the same time TWSR The status code update. Possible status code 0x50 or 0x58 . In response to each state will be described in detail in the appropriate code status code table.

When the data is successfully received, you can continue to receive packets. This process is repeated until the last byte been received. After the host receives the last byte must be sent NACK Response signal to the slave transmitter. The master generates STOP Signal or REPEATED START The entire signal is received until the end.

Go through TWCR Register write to emit following values STOP signal:

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
1	x	0	1	x	1	0	x

Go through TWCR Register write to emit following values REPEATED START signal:

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
1	x	1	0	x	1	0	x

In sending REPEATED START (Status code 0x10)after that, TWI Interface can be accessed again the same host, or visit the new host without sending a STOP signal. REPEATED START That may be different from the host machine, switching between the host and the host receiving the transmission mode without losing control of the bus.

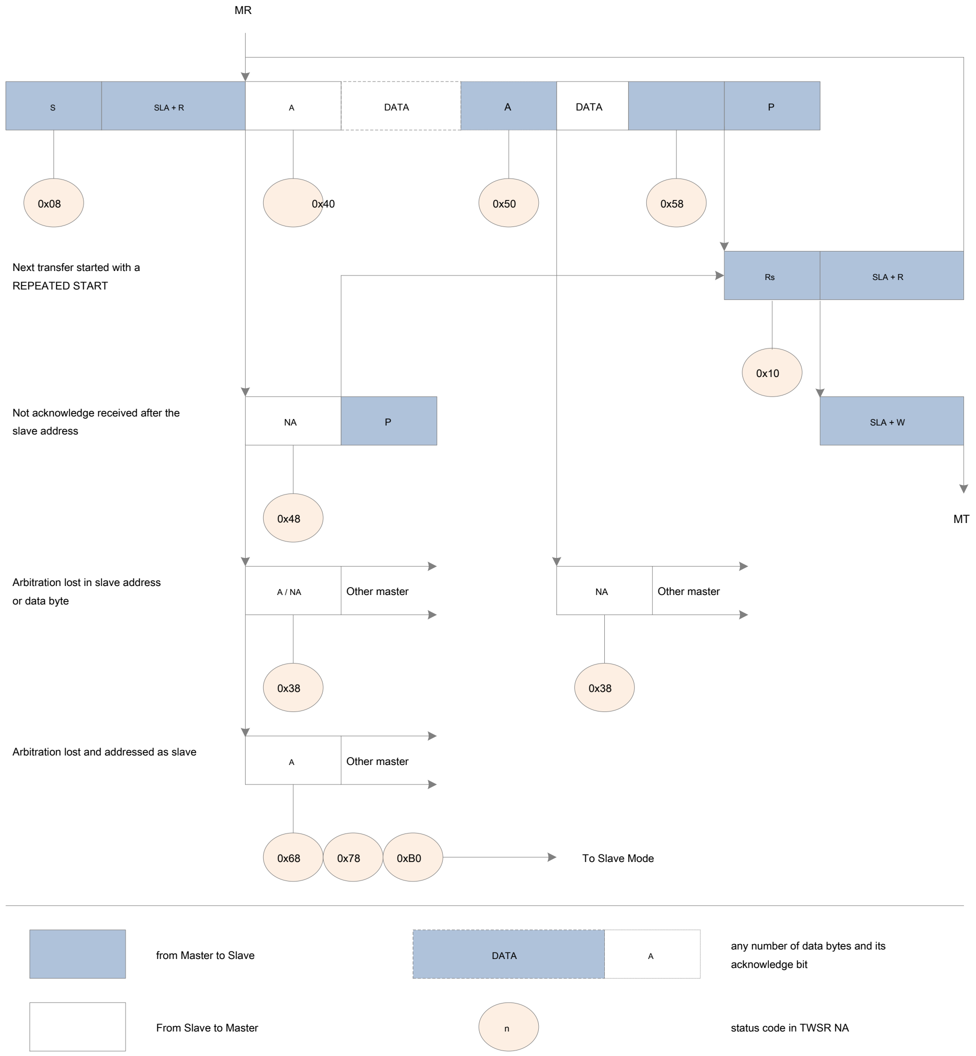
Status code in the master reception mode and a corresponding operation in the following table:

Status of the host reception mode code table

status code	Bus and hard Member state	Response application software					Hardware next move
		Read / Write	Correct TWCR Operations				
		TWDR	STA	STO	TWINT	TWEA	
0x08	START Has been sent	load SLA + R	0	0	1	x	Will send SLA + R ; The reception ACK or NACK
0x10	REPEATED START Already	load SLA + R	0	0	1	x	Will send SLA + R ; The reception ACK or NACK

	send	load SLA + W	0	0	1	x	Will send SLA + W ; The reception ACK or NACK; Will switch to MT mode
0x38	SLA + R Arbitration or data failure	No action	0	0	1	x	Will release the bus; The addressed slave mode does not enter
		No action	1	0	1	x	Will be sent when idle START
0x40	SLA + R It has been sent; received ACK	No action	0	0	1	0	The received data; Will send NACK
		No action	0	0	1	1	The received data; Will send ACK
0x48	SLA + R It has been sent; received NACK	No action	1	0	1	x	Will send REPEATED START
		No action	0	1	1	x	Will send STOP ; Reset TWSTO Mark
		No action	1	1	1	x	Will send STOP ; Reset TWSTO Signs; sending START
0x50	It received data byte; ACK Has been sent	Read data	0	0	1	0	The received data; Will send NACK
		Read data	0	0	1	1	The received data; Will send ACK
0x58	It received data byte; NACK Has been sent	Read data	1	0	1	x	Will send REPEATED START
		Read data	0	1	1	x	Will send STOP ; Reset TWSTO Mark
		Read data	1	1	1	x	Will send STOP ; Reset TWSTO Signs; sending START

Format and status of the host receiving mode as shown below:



Master receive mode and the state of the format of FIG.

Slave receive mode

In slave receive mode, may receive a certain number of data bytes from the master transmitter. The status code section referred to assume control bit prescaler "0" .

To initiate the Slave receive mode, to set TWAR with TWCR register.

TWAR Must be set as follows:

TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE
Device slave address							

TWAR height of 7 Bit is addressed by a master TWI Interface slave address will respond. If the LSB Position, TWI It responds to call address (0x00), Otherwise ignore the call address.

TWCR Must be set as follows:

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
0	1	0	0	0	1	0	x

TWEN It must be set to enable TWI interface, TWEA It must be set to cause the host address (slave address or a broadcast call) to return it to his profile ACK . TWSTA with TWSTO It must be cleared.

initialization TWAR with TWCR after that, TWI Interface waits until its slave address (or a broadcast address) to be addressed. When followed by the data direction bit slave address is "0" When (Write operations), TWI Into the slave receive mode. When the data direction bit "1" When the (read operation shown) TWI In slave transmit mode. After receiving his slave address and a write flag, TWINT Flag bit is set, the status code is also effective to update TWSR in. In response to each state will be described in detail in the appropriate code status code table. Note that, when the host mode TWI After arbitration loss can also enter slave receive mode (see Status Code 0x68 with 0x78).

If during transmission TWEA Bit is reset, TWI Will return after receiving a byte NACK (High level) to SDA on-line. This may be used to represent not receive more data from the machine. when TWEA Bit "0" Time, TWI It will not respond to its own slave address. but TWI We will continue to monitor the bus, once TWEA Is set, it can recognize and respond to the address recover. In other words, you can use TWEA Temporarily TWI Isolated from the bus interfaces.

In the sleep modes except the idle mode, TWI Clock interface can be turned off. If the slave can receive mode, the interface will continue to respond with a bus clock slave address or a broadcast address. Will then wake MCU . During the wake,
TWI Interface will remain SCL Low until TWINT Flag is cleared. when TWI After normal interface clock may receive more data.

From the state machine receiving the code pattern in the following table:

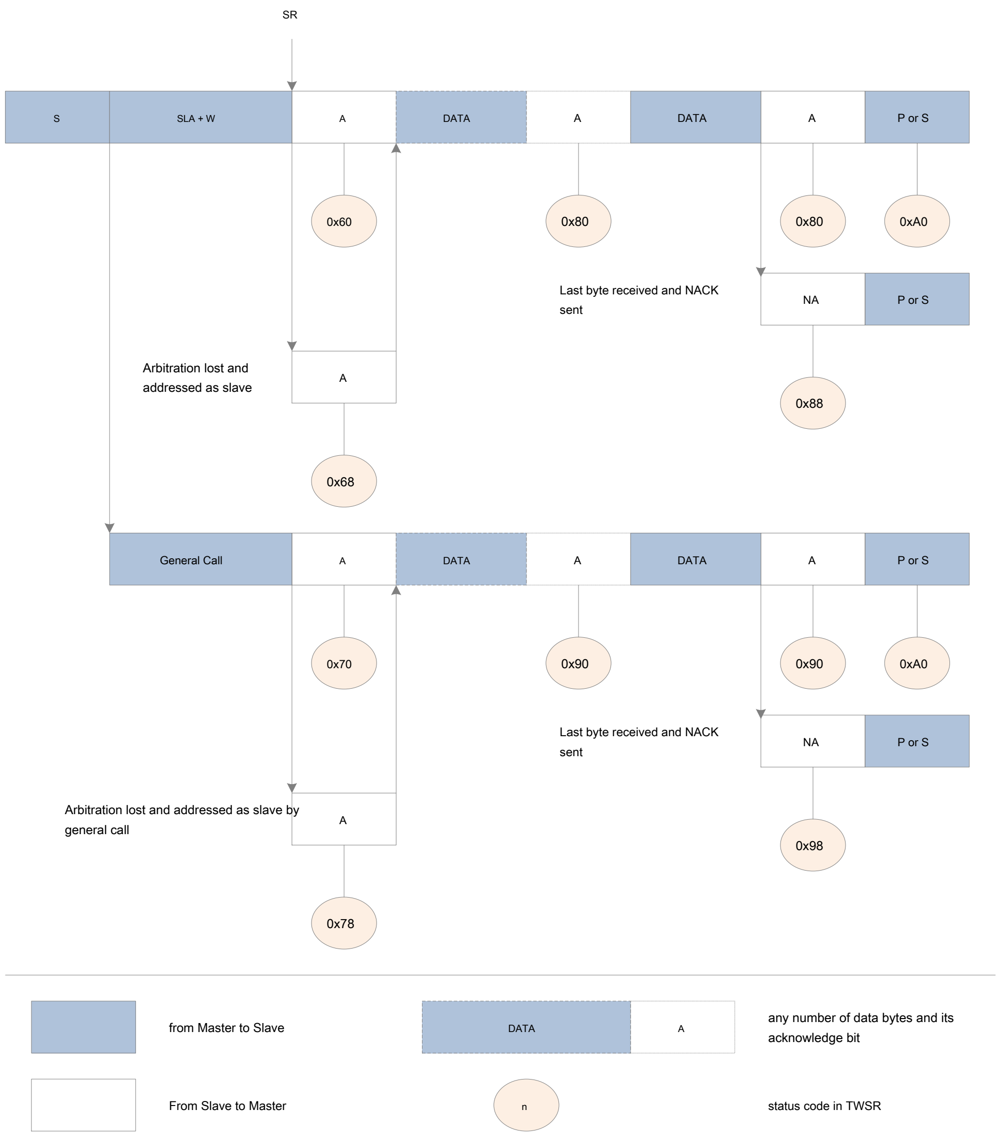
State machine receiving mode code table

status code	Bus and hardware status	Response application software					Hardware next move
		Read / Write	Correct TWCR Operations				
		TWDR	STA	STO	TWINT	TWEA	
0x60	SLA + W Received; ACK Has been sent	No action	x	0	1	0	The received data; Will send NACK
		No action	x	0	1	1	The received data; Will send ACK
0x68	send SLA + R / W Time Arbitration failure; SLA + W Received; ACK Has been sent	No action	x	0	1	0	The received data; Will send NACK
		No action	x	0	1	1	The received data; Will send ACK
0x70	Broadcast address has been received; ACK Has been sent	No action	x	0	1	0	The received data; Will send NACK
		No action	x	0	1	1	The received data; Will send ACK
0x78	send SLA + R / W Time Arbitration failure; SLA + W Received; ACK Has been sent	No action	x	0	1	0	The received data; Will send NACK
		No action	x	0	1	1	The received data; Will send ACK
0x80	Own data has been received; ACK Has been sent	Read data	x	0	1	0	The received data; Will send NACK
		Read data	x	0	1	1	The received data; Will send ACK
0x88	Own data has been received;	read 0		0	1	0	Will switch to unaddressed

	NACK Has been sent	data					Slave mode; slave will not respond to a broadcast address and
		Read data	0	0	1	1	Will switch to unaddressed Slave mode; slave address response; TWGCE = 1 The response time of broadcast
		Read data	1	0	1	0	Will switch to unaddressed Slave mode; slave will not respond to a broadcast address; transmitting the bus is free START
		Read data	1	0	1	1	Will switch to unaddressed Slave mode; slave address response; TWGCE = 1 When the response to the broadcast; transmitting the bus is free START
0x90	Broadcast data has been received; ACK Has been sent	Read data	x	0	1	0	The received data; Will send NACK
		Read data	x	0	1	1	The received data; Will send ACK
0x98	Broadcast data has been received; NACK Has been sent	Read data	0	0	1	0	Will switch to unaddressed Slave mode; slave will not respond to a broadcast address and
		Read data	0	0	1	1	Will switch to unaddressed Slave mode; slave address response; TWGCE = 1 The response time of broadcast
		Read data	1	0	1	0	Will switch to unaddressed Slave mode; slave will not respond to a broadcast address; transmitting the bus is free START
		Read 1		0	1	1	Will switch to unaddressed

		data					Slave mode; slave address response; TWGCE = 1 When the response to the broadcast; transmitting the bus is free START
0xA0	Receives from the work machine To STOP or REPEATED START	No action	0	0	1	0	Will switch to unaddressed Slave mode; slave will not respond to a broadcast address and
		No action	0	0	1	1	Will switch to unaddressed Slave mode; slave address response; TWGCE = 1 The response time of broadcast
		No action	1	0	1	0	Will switch to unaddressed Slave mode; slave will not respond to a broadcast address; transmitting the bus is free START
		No action	1	0	1	1	Will switch to unaddressed Slave mode; slave address response; TWGCE = 1 When the response to the broadcast; transmitting the bus is free START

And a state machine format from FIG reception mode is as follows:



Formats and state machine receives the pattern of FIG.

Slave transmit mode

In slave mode transmission may be sent a certain number of data bytes to the host receiver. The status code section referred to assume control bit prescaler "0" .

To initiate the Slave receive mode, to set TWAR with TWCR register.

TWAR Must be set as follows:

TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE
Device slave address							

TWAR height of 7 Bit is addressed by a master TWI Interface slave address will respond. If the LSB Position, TWI It responds to call address (0x00), Otherwise ignore the call address.

TWCR Must be set as follows:

TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
0	1	0	0	0	1	0	x

TWEN It must be set to enable TWI interface, TWEA It must be set to cause the host address (slave address or a broadcast call) to return it to his profile ACK . TWSTA with TWSTO It must be cleared.

initialization TWAR with TWCR after that, TWI Interface waits until its slave address (or a broadcast address) to be addressed. When followed by the data direction bit slave address is "0" When (Write operations), TWI Into the slave receive mode. When the data direction bit "1" When the (read operation shown) TWI In slave transmit mode. After receiving its own slave address and read flag, TWINT Flag bit is set, the status code is also effective to update TWSR in. In response to each state will be described in detail in the appropriate code status code table. Note that, when the host mode TWI After arbitration loss can enter from the transmitter mode (see Status Code 0xB0).

If during transmission TWEA Bit is reset, TWI It will switch to not addressed slave mode after sending the last byte. The receiver gives to the host the last byte of the transfer NACK or ACK Rear, TWSR Register will be updated as the status code 0xC0 or 0xC8 . If the master receiver continues to operate the transmission, the slave does not send a response, the host will receive the full
"1" Data (ie, 0xFF). When the last byte of data has been transmitted from the machine (TWEA It is cleared) and expect NACK
In response, the host wants to receive more data transmission ACK As a response, TWSR Will be updated 0xC8 .

when TWEA Bit "0" Time, TWI It will not respond to its own slave address. but TWI We will continue to monitor the bus, once TWEA
Is set, it can recognize and respond to the address recover. In other words, you can use TWEA Temporarily TWI Isolated from the bus interfaces.

In the sleep modes except the idle mode, TWI Clock interface can be turned off. If the slave can receive mode, the interface will continue to respond with a bus clock slave address or a broadcast address. Will then wake MCU . During the wake,
TWI Interface will remain SCL Low until TWINT Flag is cleared. when TWI After normal interface clock may receive more data.

From the state machine code transmission mode shown in the following table:

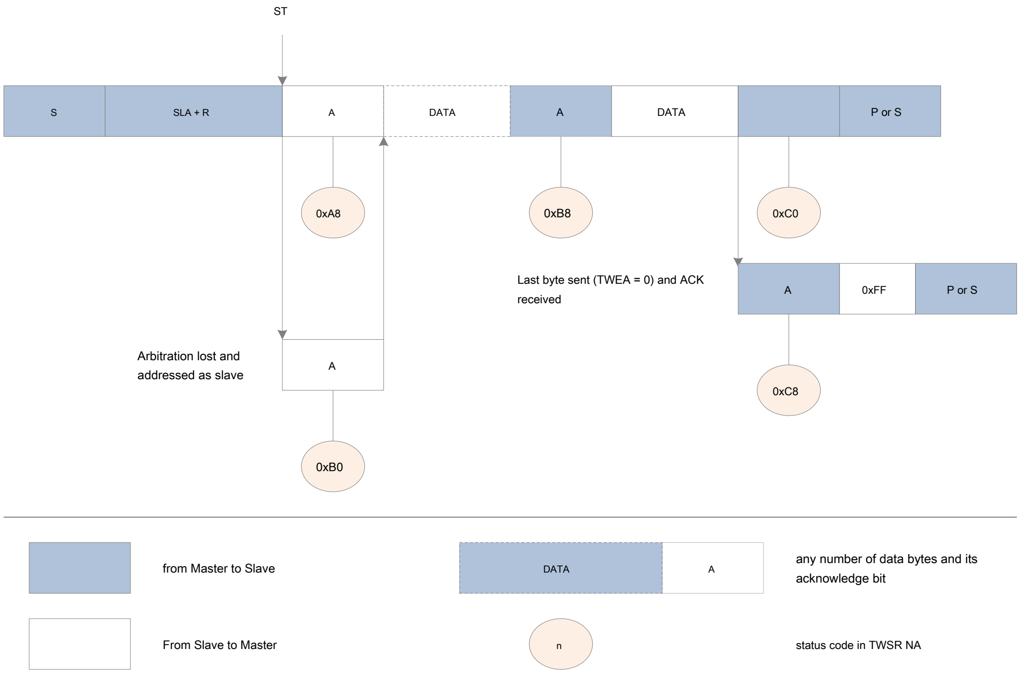
State machine transmission mode code table

status code	Bus and hard Member state	Response application software: Read / Write TWDR	Correct TWCR Operations: STA	STO	TWINT	TWEA	Hardware next move
0xA8	SLA + R Received; ACK Has been sent	Download Data	x	0	1	0	The last number will be sent According; expect to receive NACK
		Download Data	x	0	1	1	Transmitting data; The reception ACK
0xB0 send	SLA + R / W When arbitration failed; SLA + R Received; ACK Has been sent	Download Data	x	0	1	0	The last number will be sent According; expect to receive NACK
		Download Data	x	0	1	1	Transmitting data; The reception ACK

0xB8	Data Sent give away; ACK Received	Download Data x		0	1	0	The last number will be sent According; expect to receive NACK
		Download Data x		0	1	1	Transmitting data; The reception ACK
0xC0	Data Sent give away; NACK Received	No action	0	0	1	0	It will switch to not addressed Slave Mode; slave will not respond to a broadcast address and
		No action	0	0	1	1	It will switch to not addressed Slave Mode; slave address response; TWGCE = 1 The response time of broadcast
		No action	1	0	1	0	It will switch to not addressed Slave Mode; slave will not respond to a broadcast address; transmitting the bus is free START
		No action	1	0	1	1	It will switch to not addressed Slave Mode; slave address response; TWGCE = 1 When the response to the broadcast; transmitting the bus is free START
0xC8	the last one Data has been sent; ACK Received	No action	0	0	1	0	It will switch to not addressed Slave Mode; slave will not respond to a broadcast address and
		No action	0	0	1	1	It will switch to not addressed Slave Mode; slave address response; TWGCE = 1 The response time of broadcast
		No action	1	0	1	0	It will switch to not addressed Slave Mode; slave will not respond to a broadcast address; transmitting the bus is free START
		No action	1	0	1	1	It will switch to not addressed Slave mode;

							The response slave address; TWGCE = 1 When the response to the broadcast; transmitting the bus is free START

Format from the transmission mode and the state machine as shown below:



From the format and transmission mode state machine of FIG.

Other states

No two status codes corresponding TWI State is defined in the following table:

Other state code table

status code	Bus and hardware-like state	Response application software					Hardware next move
		Read / Write	Correct TWCR Operations				
		TWDR	STA	STO	TWINT	TWEA	
0xF8	No status information; TWINT = 0	No action	Does not operate TWCR				Or wait for the current operation
0x00	Unlawful START or STOP Bus errors caused	No action 0		1	1	x	Only affect the internal hardware; Will not send STOP To the bus; the bus is released and cleared TWSTO Place

status code 0xF8 Indicates that no relevant information, because TWINT Flag "0" . This state may occur TWI The interface is not participating in the current transmission or serial transmission is not yet complete.

status 0x00 It represents a serial bus error has occurred during transmission. When illegal START or STOP Error occurs when a bus appeared. For example, the address and data, address and ACK Occurs between the START or STOP . Bus error will be set

TWINT . To recover from the error, must be set TWSTO And by writing "1" To clear TWINT . This will TWI Interface enters not addressed slave mode without generating STOP And the release of SCL with SDA And cleared TWSTO Bit. Combined mode

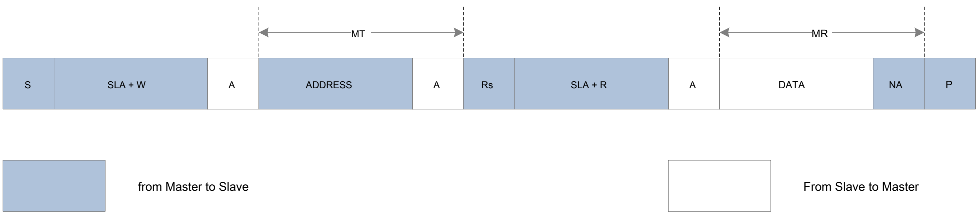
In some cases, in order to complete the desired action must be several TWI Mode combined. For example, from the serial EEPROM

Read data transmission typically comprises the steps of:

1. Transfer must be initiated;
2. You must tell EEPROM You should read position data;
3. Reading must be performed;
4. Transport must end.

Note that data can be transmitted from the master to the slave, and vice versa. It tells the host to read data from confidential position, using the master transmission mode. Next, from the data read from the machine, using the master receive mode. It will change the direction of transmission. The host must maintain control of the bus at all stages, all the steps are uninterrupted operation. If a multi-master system, at step 2 with 3 Another main change between the position of the read data, is to break this principle, the host reads the position data will be wrong. Changing the direction of data transfer between the transfer by sending and receiving data byte address REPEATED START To achieve. send REPEATED START After that, the host still has control of the bus.

The following diagram describes the transmission process:



A combination of a variety of TWI Mode to access the serial EEPROM Map

Multi-host system and arbitration

If there are multiple host connections in the same TWI On the bus, the one or more of them may be simultaneously start data transfer.

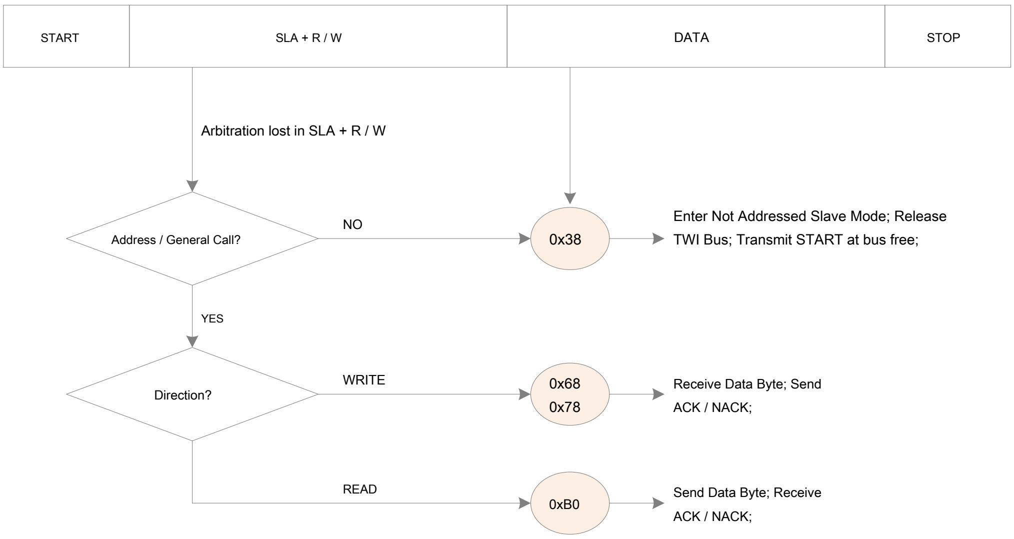
TWI Agreement to ensure that in this case, through an arbitration process, which allows a host to transmit data will not be lost. In the following two main processes attempt to send data from the machine will be described as an example of bus arbitration.

There are several different scenarios may arise during arbitration:

- Two or more hosts to communicate with a slave. In this case, either a master or slave do not know there is competition on the bus;
- Two or more masters on the same or a different data access operations from the machine direction. Arbitration takes place in this case, READ / WRITE Bits or data bits. When other hosts to SDA Send online "0" When, to SDA Send online "1" The host arbitration will fail. Failed host switches to a new transmission not addressed slave mode, or idle waiting for the bus from START Signal, which depends on the operation of the application software.
- Two or more masters are different from the machine. In this case, the arbitration will occur in SLA stage. When other hosts to SDA Send online "0" When, to SDA Send online "1" The host arbitration will fail. in SLA It failed master arbitration when the bus switches to slave mode, and checks whether it is addressed to obtain control of the bus master. If addressed, it will enter SR or ST Mode, depending on the SLA Back READ / WRITE Bit. If not look for

Site, it will switch to a new transmission not addressed slave mode, or idle waiting for the bus from START Signal, depending on the operation of the application software.

The following diagram describes a bus arbitration procedure:



Bus arbitration process map

Register Definition

TWI Register List

register	address	Defaults	description
TWBR	0x B8	0x00	TWI Bit Rate Register
TWSR	0xB9	0x00	TWI Status Register
TWAR	0xBA	0x00	TWI Address register
TWDR	0xBB	0x00	TWI Data register
TWCR	0xBC	0x00	TWI Control register
TWAMR	0xBD	0x00	TWI Address mask register

TWBR - TWI Bit Rate Register

TWBR - TWI Bit Rate Register								
address: 0xB8					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
	TWBR7	TWBR6	TWBR5	TWBR4	TWBR3	TWBR2	TWBR1	TWBR0
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	TWBR [7: 0]	TWI Bit rate select bit. TWBR It is a bit rate generator division factor. Bit rate generator is a frequency divider, for generating in the host mode SCL clock. The bit rate is calculated as follows: $f_{scl} = f_{sys} / (16 + 2 * TWBR * 4_{TWPS})$.

TWSR - TWI Status Register

TWSR - TWI Status Register								
address: 0xB9					Defaults: 0xF8			
Bit	7	6	5	4	3	2	1	0
Name	TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 3	TWS [7: 3]	TWI State flag. 5 Bit TWS reaction TWI And the logic state of the bus. Different states have different meanings values, see the specific TWI Described mode of operation. From TWSR Read values 5 Bit state value and 2 Bit prescaler control bits, the mask detection state when bit prescaler "0" . This is independent of the state detection prescaler setting.
2	-	Reservations.
1	TWPS1	TWI Prescaler high. TWPS1 with TWPS0 Together form TWPS [1: 0] , For controlling the bit rate of the prescale factor, and TWBR Together control the bit rate.
0	TWPS0	TWI Prescaler low. TWPS0 with TWPS1 Together form TWPS [1: 0] , For controlling the bit rate of the prescale factor, and TWBR Together control the bit rate.

TWPS [1: 0]	Prescale factor
0	1
1	4
2	16
3	64

TWAR - TWI Address register

TWAR - TWI Address register								
address: 0xBA					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	TWAR6	TWAR5	TWAR4	TWAR3	TWAR2	TWAR1	TWAR0	TWGCE
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 1	TWA [6: 0]	TWI Slave address bits. TWA for TWI Slave address. when TWI Works in the slave mode, the TWI This address will respond. Host mode does not require this address. However, in multi-master system, also set for other hosts to access the slave address.
0	TWGCE	TWI Broadcasting discrimination enable control bit. When set TWGCE Bit "1" , Enable TWI Bus broadcast identification. When set TWGCE Bit "0" Is prohibited TWI Bus broadcast identification. when TWGCE Set and the address frame is received 0x00 Time, TWI In response to this broadcast bus module.

TWDR - TWI Data register

TWDR - TWI Data register								
address: 0xBB						Defaults: 0xFF		
Bit	7	6	5	4	3	2	1	0
Name	TWD7	TWD6	TWD5	TWD4	TWD3	TWD2	TWD1	TWD0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 0	TWD [7: 0]	TWI Data register. TWD Is the next byte to be transmitted on the bus, or just received on the bus one byte.

TWCR - TWI Control register

TWCR - TWI Control register								
address: 0xBC						Defaults: 0x00		
Bit	7	6	5	4	3	2	1	0
Name	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
R / W	R / W	R / W	R / W	R / W	R	R / W	-	R / W

Bit	Name	description
7	TWINT	TWI Interrupt flag. when TWI Upon completion of the current job and expects application software intervention, the hardware will set TWINT Bit. If the global interrupt set and TWIE When bit, generated TWI Interruption, MCU Will perform TWI Interrupt service routine. when TWINT When the flag is set, SCL Low-level signal will be extended. TWINT Flag can only be written to this bit "1" The way is cleared. Even if the interrupt service routine, the hardware does not automatically clear the bit. Note also that clearing this bit will immediately open TWI Operation. Therefore, in the clear TWINT Before bit, to complete the first TWAR , TWAMR , TWSR with TWDR Access to the register.
6	TWEA	TWI Enable response control bit. TWEA Control response bits generated pulses. When set TWEA Bit "1" When, and meet one of the following conditions will TWI Generating a response pulse on the bus: 1) Received slave address of the device; 2) TWGCE Receives a broadcast call set; 3) Or receiving a byte of data received from the host machine in the receive mode. When set TWEA Bit "0" , The device temporarily and TWI Bus disconnected. After the device is set to resume address recognition.
5	TWSTA	TWI Initial status control bits. when CPU I want to be TWI Needs to be set when the bus master bit TWSTA Bit. Hardware detects whether the bus is available, when the bus is free, the initial state is generated on the bus. When the bus is not idle, TWI Will wait until after the Stop condition occurs, then generate the initial state to declare themselves want to be the host. After completion of sending the initial state of the software must be cleared TWSTA Bit.

4	TWSTO	TWI Stop state control bit. When in master mode, TWSTO Bit "1" Time, TWI The stop state is generated on the bus, and then automatically cleared TWSTO Bit. In the slave mode, the set TWSTO Bit can make TWI Recover from an error condition. Then the state will not stop, will only make TWI Return to a defined unaddressed slave mode, while releasing SCL with SDA A signal line to a high impedance state.
3	TWWC	TWI Write Collision flag. when TWINT Flag is low, write TWDR Register will be set TWWC Flag. when TWINT Flag is high, write TWDR Register will be cleared TWWC Flag.
2	TWEN	TWI Enable control bit. TWEN Enable bit TWI Operation and activate TWI interface. When set TWEN Bit "1" Time, TWI control IO Pin is connected to SCL with SDA Pin. When set TWEN Bit "0" Time, TWI The interface module is turned off, all of the transmission is terminated, including ongoing operations.
1	-	Reservations.
0	TWIE	TWI Interrupt enable control bit. When set TWIE Bit "1" When, and Global Interrupt set, as long as TWINT Flag is high, it activates TWI Interrupt request.

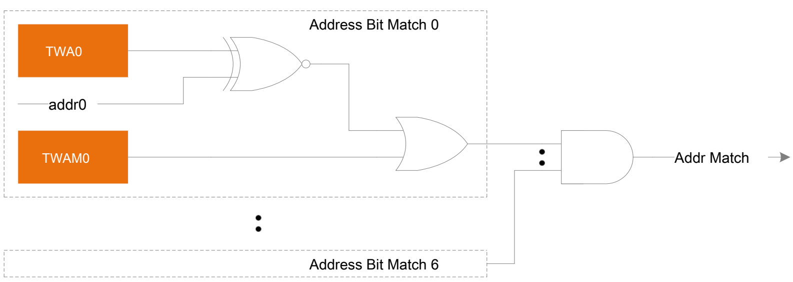
TWAMR - TWI Address mask register

TWAMR - TWI Address mask register								
address: 0xBD					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name TWAR6 TWAR5 TWAR4 TWAR3 TWAR2 TWAR1 TWAR0 TWGCE R / W								
	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7: 1	TWAM [6: 0]	TWI An address mask control bits. TWAM for 7 Place TWI Slave address mask control. TWAM Each bit is used to shield (prohibited) TWAR The corresponding address bit. When the mask bit address match logic ignores address bit received and TWA A comparison result of the corresponding bit. The following figure shows the details of the address match logic.
0	-	Reservations.

TWI Address match logic

The figure below shows TWI Address match logic diagram:



Analog comparator 0 (AC0)

- 10mV Comparison of Accuracy
- Factory offset calibration
- stand by 3 An outer sheet analog input channel
- stand by ADC Multiplexed inputs (ADMUX)
- Support internal differential amplifier input (DFFO)
- Internal support 8 Place DAC Input (DAO)
- Programmable digital filter output control

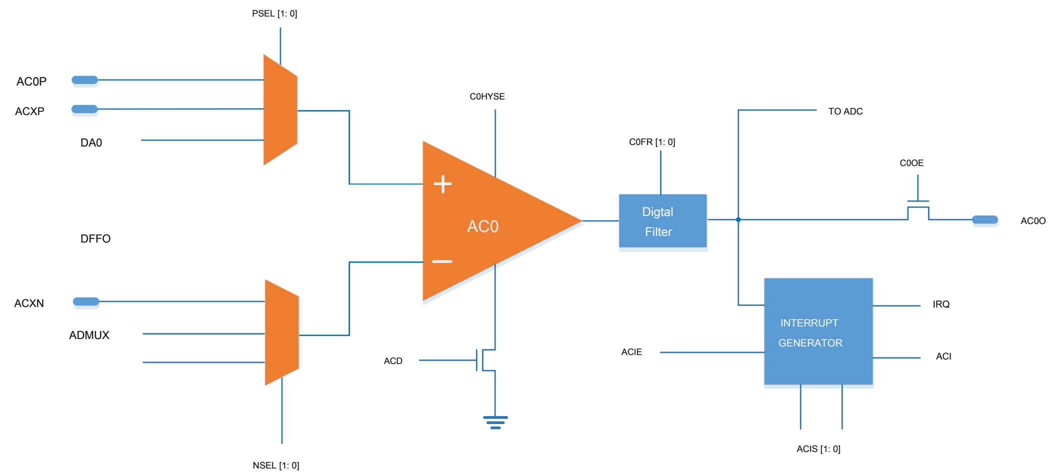
Overview

Analog comparator input terminal of the comparator comparing positive and the negative level, when a positive voltage higher than the negative terminal voltage, the analog output of the comparator ACO It is set. when ACO When the level changes, the edge of a signal can be used to trigger an interrupt. output signal ACO It may also be used to trigger the timer counter 1 Input capture and timer generated PWM Output control.

LGT8FX8P Integrated analog comparator AC0 , Includes an analog multiplexer input selector, a comparator positive and negative terminal of the input source can be selected reference source generated from the various internal or externally from the port. Analog comparator offset calibration support itself, you can ensure the consistency of the comparator work. Comparator supports an optional hardware hysteresis for improving the stability of the comparator output. While the output of the comparator integrates a hardware digital filter can be programmed, depending on the application requirements, select the appropriate filter settings to get a more stable comparison output.

The comparator output states can be read directly by a register, an interrupt request can be generated to achieve a more efficient real-time event capture function. The comparator outputs may be directly output to the outside IO port.

Operational amplifier / analog comparator 0 FIG structure as shown below.



Analog comparator 0 Functional Schematic

Analog input of the comparator

Two input terminals of analog comparator optional support multiple input sources. The positive terminal of the three-way input Optional:

1. Independent external analog input AC0P
2. Analog comparator 0/1 A common analog input ACXP
3. internal 8 Place DAC Output DAO

Input source selected by the control status register C0SR middle C0BG Bits and C0XR Register C0PS0 Joint control bits, in this section refer to the specific register description.

AC0P for AC0 Dedicated mode the positive terminal of the input channel. Note that in a different encapsulating sheet AC0P The pin is slightly different. QFP48 Package AC0P As an independent port. QFP32 This package AC0P Port and PD6 To a parallel port.

ACXP Comparator 0/1 Common positive terminal input. LGT8FX8P Two internal analog comparator, ACXP A comparator connected to both the positive terminal of the multiplexer selector, to facilitate work implement two comparators.

DAO From within 8 Place DAC Output. DAC The reference source can be input from the system power supply, the internal reference or from an external reference. DAC Please refer to the configuration DAC The relevant sections.

C0BG	C0PS0	AC0 The positive terminal of the input source
0	0	AC0P
0	1	ACXP
1	0	DAO
1	1	Closing the positive terminal of the comparator input channel

Negative input can choose from three different analog input:

1. Comparators 0/1 A common analog input ACXN
2. ADC Output multiplexer ADMUX
3. Internal differential amplifier output DFFO

The negative terminal of the comparator input by the channel selection from ADC Module ADCSRB Register CME00 / 01 Position control. When the negative terminal of the comparator input selector ADMUX When required by ADC Module ADMUX register CHMUX Select bit analog input channel, in this mode, input of the comparator can be implemented more flexibly extended.

ACXN Comparator 0/1 Common negative input, comparator facilitate 0/1 The collaborative work;

DFFO Output from the differential amplifier inside. Optional differential amplifier x1 / x8 / x16 / x32 Gain control can be achieved in small signal detection and measurement.

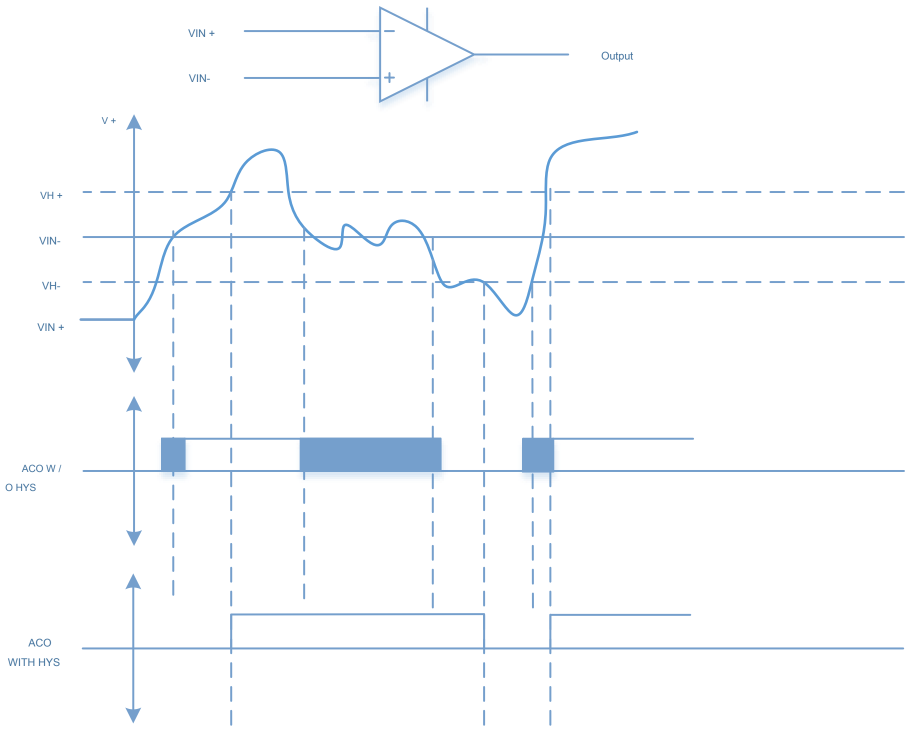
CME01	CME00	AC0 Negative input source
0	0	ACXN
0	1	ADMUX
1	0	DFFO
1	1	Close Channel negative input terminal of comparator

The comparator output filter

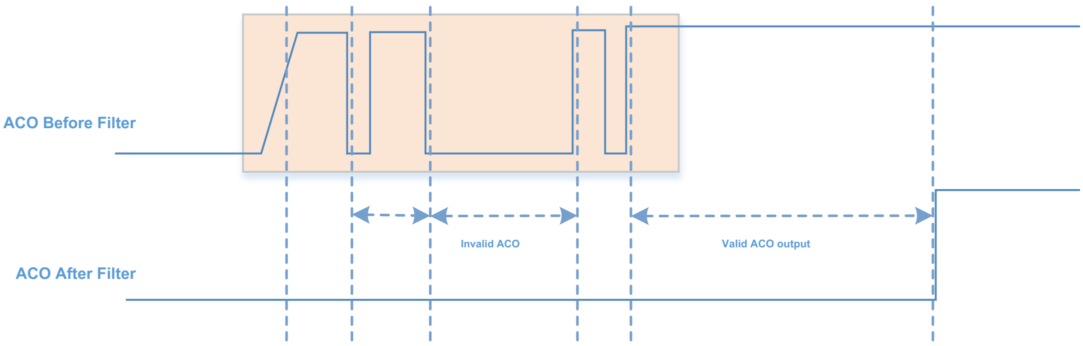
Internal support hysteresis comparator output a controllable electrically. Users can C0XR Register C0HYSE Bit enables the hysteresis circuit. Hysteresis comparator circuit may eliminate the unstable state of the state change process, reaches the output filtering function.

Recommended when using a comparator, the hysteresis circuit is opened, to obtain a stable output of the comparator. As shown below, the hysteresis comparator circuit is located between the analog output and digital output. When the input voltage of the positive terminal of the comparator V_{IN+} more than the(V_{IN-} + V_{H+}) , The comparator COUT Output is high; and when V_{IN+} Voltage is less than (V_{IN-} - V_{H-}) , The comparator output is low. A hysteresis circuit to avoid jitter when the comparator positive voltage close to the negative voltage terminal, the circuit itself is brought.

Comparator Hysteresis comparator output diagram:



Although the hysteresis circuit is effective in suppressing the ripple voltage near the threshold comparator, the actual application environment, the input signal is subject to interference of different intensity. Strong interference may cause momentary input level elevation, the range of the hysteresis circuit exceeds a threshold, it can not be effectively suppressed. LGT8FX8P The output of the comparator integrates a programmable digital filter can filter out the influence of the instantaneous interference generated by the comparator output. The digital filter according to the application needs, to select the time width appropriate filtering, only when the output of the comparator is stable for the time limit to meet the filter, the filter circuit output of the comparator is updated. So as to achieve a more stable output.



A timing comparator output filter

AC0 By digital filtering C0XR Register C0FEN as well as C0FS Control bits, refer to the specific register arrangement defined in this chapter.

The comparator output PWM control

LGT8FX8P Multi-channel support PWM Output, PWM Signals can be used with the comparator module. The output of the comparator, can be used directly off PWM Signal, in order to achieve a more flexible PWM Protection scheme.

versus PWM Related control output, please refer to the relevant part of the timer section.

Register Definition

C0SR - AC0 Control and status registers

C0SR - AC0 Control and status registers								
address: 0x50					Defaults: 0x80			
Bit	7	6	5	4	3	2	1	0
Name	C0D	C0BG	C0O	C0I	C0IE	C0IC	C0IS1	C0IS0
R / WR / W		R / W	R	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	C0D	Analog Comparator Disable bit. When set C0D Bit "1" When the analog comparator is turned off. When set C0D Bit "0" When the analog comparator is turned on.
6	C0BG	Analog comparator 0 Positive input source selection. C0BG versus C0XR Register C0PS0 Jointly set AC0 The positive terminal of the input source, { C0BG, C0PS0} = 00 = AC0P As the positive input terminal 01 = ACXP As the positive input terminal 10 = internal DAC As the positive input terminal of the output 11 = shut down AC0 The positive terminal of the input source
5	C0O	Analog output status bit comparator. The output of the analog comparator is connected directly to the sync after C0O Bit. Software can read C0O Bit value to obtain an output value of the analog comparator.
4	C0I	Analog comparator interrupt flag. When the analog comparator output event triggered by C0IS Bits defined interrupt mode, C0I Bit is set. When the interrupt enable bit C0IE for "1" And the Global Interrupt is set when an interrupt is generated. When performing analog comparator interrupt service routine, C0I Will be automatically cleared or C0I Write bit "1" Also clears the bit.
3	C0IE	Analog Comparator interrupt enable bit. When set C0IE Bit 1 And enable global interrupt, AC0 The interrupt is enabled. When set C0IE Bit 0 , AC0 Interrupts are disabled.
2	C0IC	Analog comparator input Capture Enable C0IC = 1, Timing counter 1 The input capture source output from the analog comparator. C0IC = 0, Timing counter 1 Capture source from an external input pin ICP1 .
1	C0IS1	Analog Comparator Interrupt Mode Control high.
0	C0IS0	Analog Comparator Interrupt Mode Control low. C0IS0 with C0IS1 Together form C0IS [1: 0] , Used to control analog comparator interrupt trigger.

C0IS [1: 0]	Interrupt Mode
00	ACO The transition edge
01	Reservations.
10	ACO The falling edge
11	ACO The rising edge of the trigger

ADCSRB - ADC Control and status registers B

ADCSRB **- ADC Control and status registers B**								
address: 0x7B	Defaults: 0x00							
Bit	7	6	5	4	3	2	1	0
Name	CME01	CME00	CME11	CME10	ACTS	ADTS2	ADTS1	ADTS0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	CME01	AC0 Negative input selection, CME0 = {CME01, CME00}
6	CME00	00: External ports ACXN As a AC0 Negative input 01: ADC As a multiplexed output AC0 Negative input 10: As the output of the differential amplifier AC0 Negative input 11: shut down AC0 The negative input source
5	CME11	AC1 Negative input selection, CME1 = {CME11, CME10}
4	CME10	00: External ports ACXN As a AC1 Negative input 01: External ports AC1N As a AC1 Negative input 10: ADC internal 1/5 As the partial pressure AC1 Negative input 11: Differential op amp's output as AC1 Negative input
3	ACHS	AC Trigger source channel selection 0 - AC0 Output as ADC The automatic conversion trigger 1 - AC1 Output as ADC The automatic conversion trigger
2: 0	ADTS	see ADC Register description.

C0XR - AC0 Auxiliary Control Register

C0XR **- AC0 Auxiliary Control Register**								
address: 0x51	Defaults: 0x00							
Bit	7	6	5	4	3	2	1	0
Name	-	C0OE	C0HYSE	C0PS0	C0WKE	C0FEN	C0FS1	C0FS0
R / W	-	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	-	Retention
6	C0OE	AC0 The comparator output to an external enable control port C0OE = 1, AC0 The comparator output to an external port PD2 C0OE = 0, Prohibit comparator output to an external port
5	C0HYSE	AC0 Output enable control hysteresis function. 1 = Enable output hysteresis 0 = Disable output hysteresis
4	C0PS0	AC0 The positive terminal of the input source selected low. C0PS0 versus C0BG Joint control AC0 The positive terminal of the input source, refer to C0SR Register Definition
3	COWKE	AC0 For the wake-up can be controlled. 1 = Enables the comparator output wake-up function

		0 = Close wake-up function of the comparator output
2	C0FEN	Comparator enable control digital filtering. 1 = Enable digital filter 0 = The digital filter disabled
1: 0	C0FS [1: 0]	Digital filtering width setting comparator 00 = shut down 01 = 32us 10 = 64us 11 = 96us

Analog comparator 1 (AC1)

- 10mV Comparison of Accuracy
- Factory offset calibration
- stand by 4 An outer sheet analog input channel
- Internal support 1/5 Divider input (VDO)
- Support internal differential amplifier input (DFFO)
- Internal support 8 Place DAC Input (DAO)
- Programmable control output filter

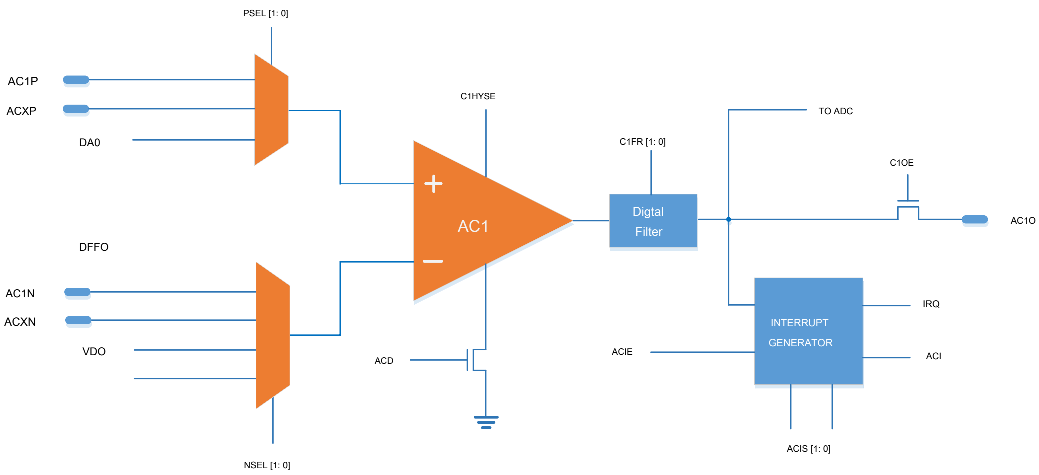
Overview

Analog comparator input terminal of the comparator comparing positive and the negative level, when a positive voltage higher than the negative terminal voltage, the analog output of the comparator ACO It is set. when ACO When the level changes, the edge of a signal can be used to trigger an interrupt. output signal ACO It may also be used to trigger the timer counter 1 Input capture and timer generated PWM Output control.

LGT8FX8P Integrated analog comparator AC1 , Includes an analog multiplexer input selector, a comparator positive and negative terminal of the input source can be selected reference source generated from the various internal or externally from the port. Analog comparator offset calibration support itself, you can ensure the consistency of the comparator work. Comparator supports an optional hardware hysteresis for improving the stability of the comparator output. While the output of the comparator integrates a hardware digital filter can be programmed, depending on the application requirements, select the appropriate filter settings to get a more stable comparison output.

The comparator output states can be read directly by a register, an interrupt request can be generated to achieve a more efficient real-time event capture function. The comparator outputs may be directly output to the outside IO port.

Analog comparator 1 FIG structure as shown below.



Analog comparator 1 Module structure diagram

Analog input of the comparator

Two input terminals of analog comparator optional support multiple input sources. The positive terminal of the three-way input Optional:

1. Independent external analog input AC1P
2. Analog comparator 0/1 A common analog input ACXP
3. internal 8 Place DAC Output DAO

Input source selected by the control status register C1SR middle C1BG Bits and C1XR Register C1PS0 Joint control bits, in this section refer to the specific register description.

AC1P for AC1 Dedicated mode the positive terminal of the input channel.

ACXP Comparator 0/1 Common positive terminal input. LGT8FX8P Two internal analog comparator, ACXP A comparator connected to both the positive terminal of the multiplexer selector, to facilitate work implement two comparators.

DAO From within 8 Place DAC Output. DAC The reference source can be input from the system power supply, the internal reference or from an external reference. DAC Please refer to the configuration DAC The relevant sections.

C1BG	C1PS0	AC1 Positive input
0	0	AC1P
0	1	ACXP
1	0	DAO
1	1	Closing the positive terminal of the comparator input channel

Negative input may be selected 4 Different types of analog inputs:

1. External analog input AC1N As a AC1 Negative input
2. Comparators 0/1 Public negative input ACXN
3. ADC internal 1/5 As the voltage divider output AC1 The negative input
4. Internal differential amplifier output DFFO As a AC1 The negative input terminal of the comparator the negative input from the channel selected by the ADC Module ADCSRB Register CME11 / 10 Position control. When the negative terminal of the comparator input selector ADC Multiple internal voltage divider output, need ADC Module ADCSRC register

VDS Demultiplexed bits select input reference voltage source.

ACXN Comparator 0/1 Common negative input, comparator facilitate 0/1 The collaborative work;

DFFO Output from the differential amplifier inside. Optional differential amplifier x1 / x8 / x16 / x32 Gain control can be achieved in small signal detection and measurement.

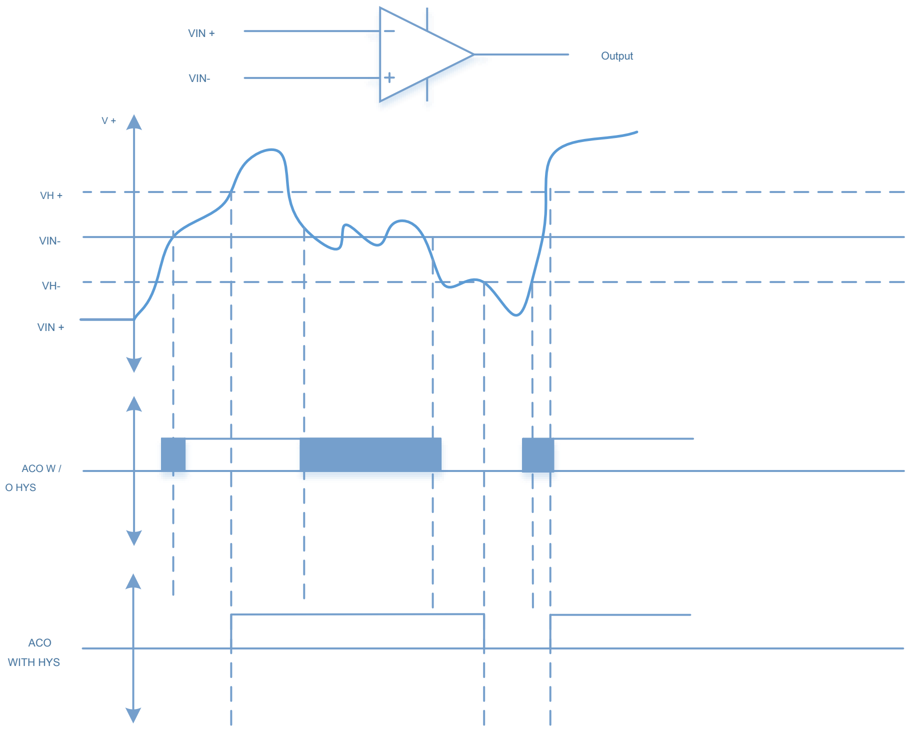
CME11	CME10	AC1 Negative input
0	0	ACXN
0	1	AC1N
1	0	VDO
1	1	DFFO

The comparator output filter

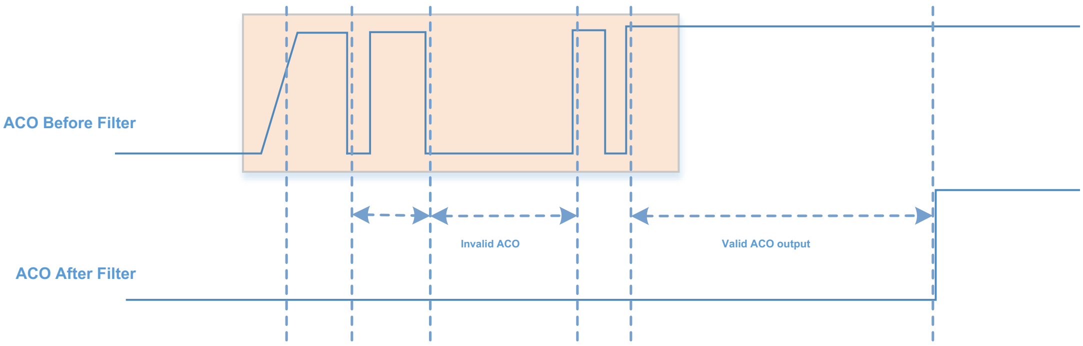
Internal support hysteresis comparator output a controllable electrically. Users can C1XR Register C1HYSE Bit enables the hysteresis circuit. Hysteresis comparator circuit may eliminate the unstable state of the state change process, reaches the output filtering function.

Recommended when using a comparator, the hysteresis circuit is opened, to obtain a stable output of the comparator. As shown below, the hysteresis comparator circuit is located between the analog output and digital output. When the input voltage of the positive terminal of the comparator V_{IN+} more than the($V_{IN-} + V_{H+}$) , The comparator COUT Output is high; and when V_{IN+} Voltage is less than ($V_{IN-} - V_{H-}$) , The comparator output is low. A hysteresis circuit to avoid jitter when the comparator positive voltage close to the negative voltage terminal, the circuit itself is brought.

Comparator Hysteresis comparator output diagram:



Although the hysteresis circuit is effective in suppressing the ripple voltage near the threshold comparator, the actual application environment, the input signal is subject to interference of different intensity. Strong interference may cause momentary input level elevation, the range of the hysteresis circuit exceeds a threshold, it can not be effectively suppressed. LGT8FX8P The output of the comparator integrates a programmable digital filter can filter out the influence of the instantaneous interference generated by the comparator output. The digital filter according to the application needs, to select the time width appropriate filtering, only when the output of the comparator is stable for the time limit to meet the filter, the filter circuit output of the comparator is updated. So as to achieve a more stable output.



A timing comparator output filter

AC1 By digital filtering C1XR Register C0FEN as well as C1FS Control bits, refer to the specific register arrangement defined in this chapter.

The comparator output PWM control

LGT8FX8P Multi-channel support PWM Output, PWM Signals can be used with the comparator module. The output of the comparator, can be used directly off PWM Signal, in order to achieve a more flexible PWM Protection scheme.

versus PWM Related control output, please refer to the relevant part of the timer section.

Register Definition

C1SR - AC1 Control and status registers

C1SR - AC1 Control and status registers								
address: 0x2F					Defaults: 0x80			
Bit	7	6	5	4	3	2	1	0
Name	C1D	C1BG	C1O	C1I	C1IE	C1IC	C1IS1	C1IS0
R / WR / W		R / W	R	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	C1D	Analog Comparator Disable bit. When set C1D Bit "1" When the analog comparator is turned off. When set C1D Bit "0" When the analog comparator is turned on.
6	C1BG	Analog comparator 1 Positive input source selection. C1BG versus C1XR Register C1PS0 Jointly set AC1 The positive terminal of the input source, { C1BG, C1PS0} = 00 = AC1P As the positive input terminal 01 = ACXP As the positive input terminal 10 = internal DAC As the positive input terminal of the output 11 = shut down AC1 The positive terminal of the input source
5	C1O	Analog output status bit comparator. The output of the analog comparator is connected directly to the sync after C1O Bit. Software can read C1O Bit value to obtain an output value of the analog comparator.
4	C1I	Analog comparator interrupt flag. When the analog comparator output event triggered by C1IS Bits defined interrupt mode, C1I Bit is set. When the interrupt enable bit C1IE for "1" And the Global Interrupt is set when an interrupt is generated. When performing analog comparator interrupt service routine, C1I Will be automatically cleared or C1I Write bit "1" Also clears the bit.
3	C1IE	Analog Comparator interrupt enable bit. When set C1IE Bit 1 And enable global interrupt, AC1 The interrupt is enabled. When set C1IE Bit 0 , AC1 Interrupts are disabled.
2	C1IC	Analog comparator input Capture Enable C1IC = 1, Timing counter 1 The input capture source output from the analog comparator. C1IC = 0, Timing counter 1 Capture source from an external input pin ICP1 .
1	C1IS1	Analog Comparator Interrupt Mode Control high.
0	C1IS0	Analog Comparator Interrupt Mode Control low. C1IS0 with C1IS1 Together form C1PS [1: 0] , Used to control analog comparator interrupt trigger.

C1IS [1: 0]	Interrupt Mode
00	AC1 The transition edge
01	Reservations.
10	AC1 The falling edge
11	AC1 The rising edge of the trigger

ADCSRB - ADC Control and status registers B

ADCSRB - ADC Control and status registers B								
address: 0x7B	Defaults: 0x00							
Bit	7	6	5	4	3	2	1	0
Name	CME01	CME00	CME11	CME10	ACTS	ADTS2	ADTS1	ADTS0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	CME01	AC0 Negative input selection, CME0 = {CME01, CME00}
6	CME00	00: External ports ACXN As a AC0 Negative input 01: ADC As a multiplexed output AC0 Negative input 10: As the output of the differential amplifier AC0 Negative input 11: shut down AC0 The negative input source
5	CME11	AC1 Negative input selection, CME1 = {CME11, CME10}
4	CME10	00: External ports ACXN As a AC1 Negative input 01: External ports AC1N As a AC1 Negative input 10: ADC internal 1/5 As the partial pressure AC1 Negative input 11: Differential op amp's output as AC1 Negative input
3	ACHS	AC Trigger source channel selection 0 - AC0 Output as ADC The automatic conversion trigger 1 - AC1 Output as ADC The automatic conversion trigger
2: 0	ADTS	see ADC Register description.

C1XR - AC1 Auxiliary Control Register

C1XR - AC1 Auxiliary Control Register								
address: 0x3A	Defaults: 0x00							
Bit	7	6	5	4	3	2	1	0
Name	-	C1OE	C1HYSE	C1PS0	C1WKE	C1FEN	C1FS1	C1FS0
R / W	-	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	-	Retention
6	C1OE	AC1 The comparator output to an external enable control port C1OE = 1, AC1 The comparator output to an external port PE5 C1OE = 0, Prohibit comparator output to an external port
5	C1HYSE	AC1 Output enable control hysteresis function. 1 = Enable output hysteresis 0 = Disable output hysteresis
4	C1PS0	AC1 The positive terminal of the input source selected low. C1PS0 versus C1BG Joint control AC1 The positive terminal of the input source, refer to C1SR Register Definition
3	C1WKE	AC1 For the wake-up can be controlled. 1 = Enables the comparator output wake-up function

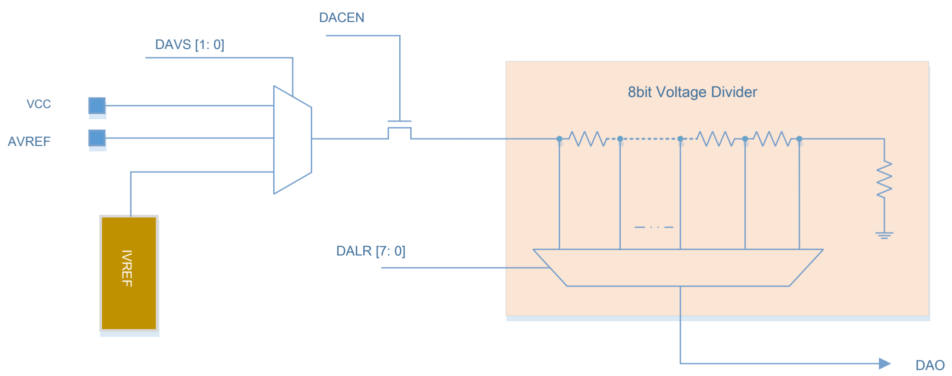
		0 = Close wake-up function of the comparator output
2	C1FEN	Comparator enable control digital filtering. 1 = Enable digital filter 0 = The digital filter disabled
1: 0	C1FS [1: 0]	Digital filtering width setting comparator 00 = shut down 01 = 32us 10 = 64us 11 = 96us

DAC (DAC)

- 8 Bit analog conversion output
- DAC Analog comparator output can be used as a reference input
- stand by DAC Output to an external port (DAO)
- Optional VCC / AVREF / IVREF Splitting power

Overview

LGT8FX8P The internal integration of a 8 Bit programmable DAC (DAC) . DAC Reference may be selected as the power input, the internal reference voltage source from the system operating power from the chip or external port AVREF Input. DAC Selected as the output of internal comparator AC0 / 1 The input source may be directly output to the external pins on the chip as an external reference. when DAC Output to external pins, not directly for driving a load, required by the voltage follower circuit, or other similar drive. DAC An internal configuration as shown below:



Register Definition

DACON - DAC Control register

DACON- DAC Control register								
address: 0xA0					0000_0000			
Bit	7	6	5	4	3	2	1	0
	-	-	-	-	DACEN	DAOE	DAVS1	DAVS0
R / W	-	-	-	-	R / W	W / R	R / W	W / R

Bit	Name description	
7: 4	-	Retention
3	DACEN	DAC Enable Control bit 1 = Enable DAC Module 0 = Disable DAC Module
2	DAOE	DAC Output enable control port to the outside 1 = Enable DAC Output to an external terminal PD4 0 = Ban DAC Output to an external port
1	DAVS1	DAC Select bit reference voltage source 10
	DAVS0	DAC Select bit reference voltage source 0 . [DVS1, DVS0] =

		00: Voltage source selection system voltage VCC 01: Voltage source is selected as an external input AVREF 10: Voltage source is selected as the internal reference voltage 11: shut down DAC Reference, also closes DAC Module

DALR - DAC Data register

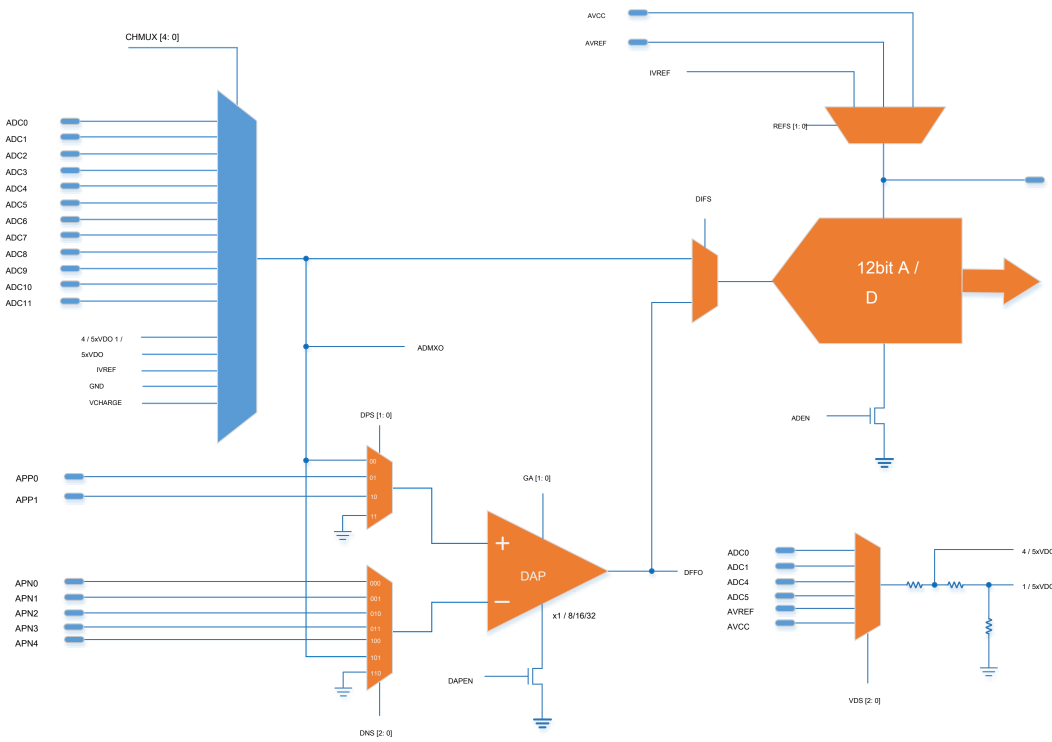
VRCON1- DAC1 Control register								
address: 0xA1					0000_0000			
Bit	7	6	5	4	3	2	1	0
	DALR [7: 0]							
R / W	W / R							

Bit	Name	description
7: 0	DALR	DAC Data register, provided DAC Mode output voltage magnitude DAC Output voltage DALR Relationship: $V_{DAO} = V_{REF} * (DALR + 1) / 256$ among them: V_{DAO} for DAC Analog voltage output V_{REF} for DAC A reference voltage source, the DACON Register DAVS Choice

12 Bit analog to digital converter (ADC)

- 12 Bit resolution, DNL for ± 1LSB , INL for ± 1.5LSB
- The highest resolution at sample rates up 500KSPS
- 12 Single-ended input channels multiplexed
- Multiple input channel programmable gain differential amplifier
- Input voltage range 0-VCC
- internal 1.024V / 2.048V / 4.096V The reference voltage
- stand by AVCC And an external reference voltage input
- Internal multiple-input 1/5 , 4/5 Dividing circuit
- Offset calibration support positive and negative directions
- Converted automatically trigger mode based on the interrupt source
- Upper support overflow / automatic channel monitor
- Conversion results support optional alignment mode
- Conversion End Interrupt Request

Outline



ADC Structure chart

ADC is a 12 Bit successive approximation ADC . ADC And a 17 Channel Analog Multiplexer is connected to the port from outside the chip can 12 Analog inputs and 5 Internal voltage supply channel for sample conversion. ADC The internal integration of a programmable gain x1 / x8 / x16 / x32 The differential operational amplifier, the amplifier may be an external input port or

ADC Output of the multiplexer. Differential op amp as a result of ADC Analog input.

ADC Internal sources include analog input from a ADC Multiple internal divider input; internal reference voltage source; internal analog ground reference and the analog output from the touch key module. Internal multiplexed input while the output voltage divider 4/5 , 1/5 Two-way

Voltage; divider input level may be selected from the external power supply system or from a port.

ADC Support for offset calibration. Offset calibration process is controlled by software. It includes a positive offset calibration, calibration of the amount of reverse two directions. Offset calibration is enabled, ADC The controller will automatically use the calibration values for both forward and reverse ADC Calibration sample results.

Offset calibration method in this section refer to the relevant section.

ADC Operations

ADC Conversion through successive approximation analog input voltage into a 12 Digital bits. The minimum value represents GND The maximum value represents the reference voltage minus 1LSB . A reference voltage source may be ADC Supply voltage AVCC External Reference AVREF Or internal 1.024V / 2.048V The reference voltage, by writing ADMUX Register REFS Bits to select.

The analog input channel by writing ADMUX Register CHMUX Bits to select. any ADC Input pins, the external reference voltage pin, and can be used as the internal reference voltage source ADC The single-ended input. By setting ADTMR Register DIFS Can be ADC Input channel to the internal switching of the differential amplifier. Related differential amplifier and a gain by input source DAPCR Register settings.

By setting ADCSRA Register ADEN Place to start ADC , ADEN When cleared ADC Not power, it is proposed to close in before entering sleep mode ADC .

ADC Conversion results 12 Bit, storage and ADC Data register ADCH and ADCL in. By default, the conversion result is right-aligned, but can be provided ADMUX Register ADLAR Bit becomes left-aligned.

If set to convert the result left-justified, and only the highest 8 Bit conversion accuracy, as long as the reading ADCH Will suffice. Otherwise first reading ADCL Then read ADCH To ensure that the contents of the data register is the result of the same conversion. Once read ADCL After the data register ADCL with ADCH Is latched read ADCH After the conversion result can then update the data register ADCL with ADCH .

ADC Conversion end interrupt can be triggered. Even if the conversion occurred at the end of reading ADCL versus ADCH Between the interrupt will trigger.

Start a conversion

to ADC Start Conversion bit ADSC Write bit "1" You can start a single conversion. In the conversion process this bit remains high until cleared by hardware after the end of the conversion. If you change the channel during the conversion process, so ADC This time the conversion will be completed before changing the channel.

ADC There are different sources of conversion trigger. Set up ADCSRA Register ADC Automatically trigger enable bit ADATE It can automatically triggered. Set up ADCSRB Register ADC Trigger select bit ADTS You can select the trigger source. When the selected trigger signal is a rising edge, ADC Prescaler reset and start the conversion. This provides a method of starting the conversion in a fixed time interval. Even after the conversion trigger signal is still present, it will not start a new conversion. If the trigger during the conversion process has produced a rising edge, the rising edge will be ignored. Even if the specific interrupt is disabled or the global interrupt enable bit "0" That interrupt flag will be set. This will trigger a conversion without generating an interrupt. But in order to trigger a new conversion at the next interrupt event occurs, the interrupt flag must be cleared.

use ADC Interrupt Flag as a trigger source, it can start the next time after the end of the conversion currently in progress ADC Conversion. after that ADC It works in continuous conversion mode, constantly sampling and ADC Data register is updated. First turn

Change is through to the ADCSRA Register ADSC Write bit "1" To start. In this mode, subsequent ADC Conversion does not depend on ADC Interrupt flag ADIF Whether set.

If enabled automatic trigger set ADCSRA Register ADSC Will start a single conversion. ADSC Flag may also be used to detect the conversion is in progress. Regardless of how the conversion is started, during the conversion process ADSC Has been "1" .

Prescaler and ADC Conversion Timing

By default, the successive approximation circuitry requires an 300KHz To 3MHz The input clock to get maximum resolution. If the conversion is less than the desired accuracy 12 Bits, then the input clock frequency may be higher than 3MHz In order to achieve a higher sampling rate.

ADC Module comprises a prescaler, which may be generated by the system clock acceptable ADC The input clock. By prescaler ADCSRA Register ADPS Bit set. Position ADCSRA Register ADEN Will enable ADC The prescaler starts counting. as long as ADEN Bit "1" The prescaler will continue counting until ADEN Is cleared.

ADCSRA Register ADSC After being set, the next single-ended conversion ADC The rising edge of the clock cycle started. A normal conversion takes 15 More ADC Clock cycle. ADC Enable(ADCSRA Register ADEN Rear-bit) need 50 More ADC Initializing analog circuits of input clock cycles before it can first be converted effectively.

in ADC The conversion process, the sample-hold after the conversion starts 1.5 More ADC Enter the clock starts, and for the first time ADC The output of the conversion takes place after the start of 14.5 More ADC The input clock. After the conversion, ADC The results are fed ADC Data register, and ADIF Flag is set. ADSC While being cleared. After the software can be set again ADSC Logo or automatic trigger, which initiates a new conversion.

And a reference voltage sampling channels

ADMUX Register MUX and REFS Single buffered through a temporary register. CPU It may be random access to a temporary register. Before starting the conversion, CPU Channel at any time and may be selected reference source is arranged. to ensure that ADC A sufficient sampling time, soon after the start of the conversion, you can not configure a selected channel and reference. In the conversion is complete (ADCSRA Register ADIF After the set), and select the reference channel sources will be updated. The conversion starts to ADSC The next set after ADC Edge of the clock input. Therefore, we recommend users set ADSC After a ADC Input clock cycles, do not operate ADMUX To select the new channel and the reference source.

With automatic trigger, time trigger events is uncertain. In order to control the impact of the new set of conversion, updated ADMUX Be careful when register. If the ADATE and ADEN Are set, the downtime can occur at any time, thereby triggering automatic start ADC Conversion. If you change during this period ADMUX Contents of the register, then the user will not be able to distinguish a conversion is old or new configuration based on the configuration. It is recommended for the following security time ADMUX Updated:

1) ADATE or ADEN Bit "0" ;

2) During the conversion process, but at least after the occurrence of a trigger event ADC Input clock period;

3) After the conversion is complete, but before the interrupt trigger source flag is cleared. If the update in either case mentioned above ADMUX Before, the new configuration will take effect the next conversion. select ADC It should be noted when the input channel, before starting the conversion to selected passages in ADSC After a set ADC After the clock cycle you can choose a new analog input channels, but the easiest way is to wait until after the end of the conversion and then change the channel.

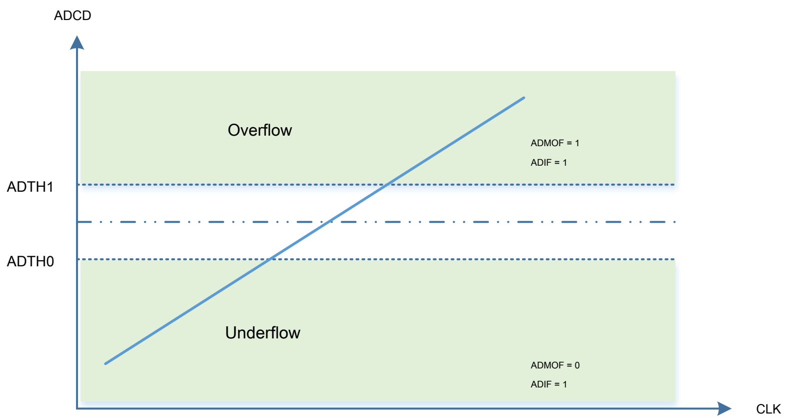
ADC A reference voltage source V_{ref} Reflects ADC The conversion range. If the single-channel level exceeds the end V_{ref} , Which is close to the maximum conversion result 0xFFF . V_{ref} It can be AVCC , External AREF Pin voltage, the internal voltage reference source.

Using the internal reference (1.024V / 2.048V / 4.096V) Precautions:

After the chip is powered on, as an internal reference calibrated by default 1.024V , If a user 1.024V The internal reference can be used directly without other operations. But if you need to use 2.048V or 4.096V Internal reference voltage, needing to update the calibration value of the internal reference. 2.048V / 4.096V The calibration value into a register after power VCAL2 / 3 (0xCE / 0xCC) In the program initialization, VCAL2 / 3 Value of the read and write VCAL (0XC8) Register complete calibration.

Automatic channel monitoring

Automatic channel monitoring mode for real-time monitoring of selected ADC Input voltage channels. Set software ADCSRC Register AMEN Channel bit enables automatic monitoring function, ADC Automatic conversion voltage of the selected channel, when given in addition to the conversion result of the overflow range, will set ADC Interrupt flag (ADIF) And at the same time stop the automatic monitoring. Software can respond to events by means of an overflow interrupt or query. ADMSC Register AMOF Bit is used to indicate the type of overflow events. ADIF Flag is automatically cleared by hardware when the service routine is reset; In query mode, by software written 1 Cleared. Only when ADIF Cleared, and by setting ADCSRC Register AMEN Bit, before re-enables automatic monitoring mode.



To overcome the single ADC Conversion result of unstable support for automatic detection of a digital filter function can be configured. Digital filtering by detecting continuous conversion results only in a continuous number of transitions have been defined in a consistent result, an overflow event is triggered only. Continuous Conversions can ADMSC Register AMFC [3: 0] Bit is set.

Automatic channel monitoring by ADCSRC Register AMEN Position control. register ADT0 For setting the underflow threshold; ADT1 For setting the overflow threshold. ADT0 / 1 for 16 Bit registers. Software Set AMEN After the bit will stop immediately ADC Current conversion operation, and a reset ADC Control state, after entering automatic conversion mode.

Before starting the automatic channel detection mode, detecting the need to set up channels and other relevant configuration. Software may at any time by clearing AMEN Register, disable automatic detection mode.

Multiple input dividing circuit (VDS)

ADC Internal dividing comprises a multiplexing module inputs. Dividing an input voltage from an external source may be selected ADC Input channels (ADC0 / 1/4/5), External reference AVREF Or an analog power supply. Dividing module while the output 4/5 as well as 1/5 Two voltages respectively to ADC internal 12 , 13 Input channels. among them 4/5 This road used for ADC Offset calibration; 1/5 In addition to the offset correction, the Similar applications used for a power supply voltage detection. Dividing circuit related functions mainly by ADCSRD Register control is realized.

ADC Offset calibration

Due to variations inherent characteristics of the circuit configuration and manufacturing process, cause ADC Internal comparator circuit generates different degrees of offset error. So the offset voltage to compensate for the high-precision generated ADC Conversion architecture is critical. LGT8FX8P Inside the chip ADC Test interfaces support offset voltage, offset measurement and can be completed in coordination with the calibration software.

Offset calibration principle:

Offset calibration mainly by changing the internal comparator input polarity, tested positive and negative directions ADC Conversion results. Since both directions offset voltage is expressed as two polarities, by converting these two subtraction result, the offset error can be obtained an intermediate. When a normal application, the conversion result can be adjusted according to this offset voltage.

Offset calibration process:

1. Configuration VDS Module, VDS Analog power input source selection (AVCC)
2. ADC Reference voltage selection analog supply (AVCC)
3. ADCSRC [SPN] = 0, ADC Read 4 / 5VDO Channel, the conversion value is recorded as PVAL
4. ADCSRC [SPN] = 1, ADC Read 4 / 5VDO Channel, the value of the recording bit conversion NVAL
5. The value (NVAL - PVAL) >> 1 Storage to OFR0 register
6. ADCSRC [SPN] = 1, ADC Read 1 / 5VDO Channel, the conversion result is recorded as NVAL
7. ADCSRC [SPN] = 0, ADC Read 1 / 5VDO Channel, recording bit conversion result PVAL
8. The value (NVAL - PVAL) >> 1 Storage to OFR1 register
9. Set up ADCSRC [OFEN] = 1 Enable offset compensation function

Special Note: Because the offset error of plus or minus direction, The above data are signed and an arithmetic operation.

Offset calibration process needs to be changed ADC Configuration, it is recommended that offset calibration is complete before configuring normal use. In order to improve calibration accuracy, it is recommended ADC Repeatedly sampling the filtered read channel conversion.

Offset calibration OFR0 / 1 After the configuration, by OFEN Bit enables automatic offset compensation. After normal after conversion, ADC Control will be based ADC Conversion result, automatically OFR0 / 1 To compensate.

ADC Dynamic Calibration

Offset calibration method described above, based on the test environment and a test input offset. When the system environment changes, ADC The imbalance will also change. Therefore, if real-time calibration can be compensated for with the working device against the environmental changes caused by differences in performance, improved ADC Measurement accuracy is very important.

There is provided a recommendation algorithm to be used, based on the principle offset calibration algorithm can be implemented to bring dynamic work environment to compensate offset errors, consistent and accurate test results.

This method does not calculate the offset voltage, it does not enable offset compensation (OFEN) . Algorithm only need SPN control ADC Conversion polarity different SPN Downsampling two measurements, two offset errors result due to the introduction of the performance of both positive and negative directions, so we can easily cancel the offset error produced by the method of the addition averaging.

We assume that when the ADC During the conversion, the offset errors introduced into the test as VOFS Therefore control SPN Conducted twice ADC Conversion, the resulting ADC Conversion result can be expressed as:

SPN = 1 Time, $V_{ADC1} = V_{REL} + V_{OFS1}$

SPN = 0 Time, $V_{ADC0} = V_{REL} - V_{OFS0}$

We will be adding the two measurements, can be eliminated V_{OFS} The actual sampling input V_{REL} Impact of. Because the matching characteristics of the circuit, V_{OFS1} with V_{OFS0} It may not be exactly the same, but the overall effect is still compensate for offset errors can be achieved.

Dynamic offset compensation algorithm process:

1. Depending on the application initialization required ADC Conversion parameters

2. Set up SPN = 1 ,start up ADC Sampling, recording ADC Sampling results VADC1
3. Set up SPN = 0 ,start up ADC Sampling, recording ADC Sampling results VADC2
4. (VADC1 + VADC2) >> 1 This is the ADC The conversion result

In practice, this algorithm can be combined with the sampling averaging algorithm, even better results can be obtained.

Register Definition

ADC Register List

register	address	Defaults	description
ADCL	0x78	0x00	ADC Low Byte Data Register
ADCH	0x79	0x00	ADC High Byte Data Register
ADCSRA	0x7A	0x00	ADC Control and status registers A
ADCSRB	0x7B	0x00	ADC Control and status registers B
ADMUX	0x7C	0x00	ADC Multiplexer control register
ADCSRC	0x7D	0x01	ADC Control and status registers C
DIDR0	0x7E	0x00	Digital Input Disable Control Register 0
DIDR1	0x7F	0x00	Digital Input Disable Control Register 0
DAPCR	0xDC	0x00	The differential amplifier control register
OFR0	0xA3	0x00	Offset compensation register 0
OFR1	0xA4	0x00	Offset compensation register 1
ADT0L	0xA5	0x00	Automatic monitoring low threshold underflow 8 Place
ADT0H	0xA6	0x00	Automatic monitoring high threshold underflow 8 Place
ADT1L	0xAA	0x00	Automatic monitoring low threshold overflow 8 Place
ADT1H	0xAB	0x00	Automatic monitoring high threshold overflow 8 Place
ADMSC	0xAC	0x01	Automatic monitoring of status and control registers
ADCSRD	0xAD	0x00	ADC Control and status registers D

ADCL - ADC Low Byte Data Register

ADCL - ADC Low Byte Data Register								
address: 0x78					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name0	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Name1	ADC3	ADC2	ADC1	ADC0	-	-	-	-
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Initial	0	0	0	0	0	0	0	0

Bit	Name	description
7: 0	ADC [7: 0] / ADC [3: 0]	ADC Data low byte register. when ADLAR Bit "0" Time, ADC Output data are aligned in the low storage register, i.e., ADCL for ADC [7: 0] ,Such as Name0 Shown; if ADLAR Bit "1" Time, ADC High output data are stored in the register are aligned, i.e., ADCL height of 4 Bit ADC [3: 0] ,low 4 Bit meaningless, as Name1 Fig.

ADCH - ADC High Byte Data Register

ADCH - ADC High Byte Data Register								
address: 0x79					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name0	-	-	-	-	ADC11	ADC10	ADC9	ADC8
Name1	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Initial	0	0	0	0	0	0	0	0

Bit	Name	description
7: 0	ADC [11: 8] / ADC [11: 4]	ADC Data low byte register. when ADLAR Bit "0" Time, ADC Output data are aligned in the low storage register, i.e., ADCH Low 4 Bit ADC [11: 8] ,high 4 Bit meaningless, as Name0 Shown; if ADLAR Bit "1" Time, ADC High output data are stored in the register are aligned, i.e., ADCH for ADC [11: 4] ,Such as Name1 Fig.

ADCSRA - ADC Control and status registers A

ADCSRA - ADC Control and status registers A								
address: 0x7A					Defaults: 0x05			
Bit	7	6	5	4	3	2	1	0
Name	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Initial	0	0	0	0	0	0	1	0

Bit	Name	description
7	ADEN	ADC Enable control bit. When set ADEN Bit "1" Time, ADC It is enabled. When set ADEN Bit "0" Time, ADC Prohibited.
6	ADSC	ADC Start the conversion. In the CPA mode, ADSC Set to start a conversion. In continuous conversion mode, ADSC Set to start the first conversion.
5	ADATE	ADC Automatically trigger enable control bit. When set ADATE Bit "1" When the automatic trigger function is enabled. The rising edge of the selected trigger signal to open a conversion. Select the trigger source from ADCSRB Register ADTS To control. When set ADATE Bit "0" When the automatic trigger function is disabled.
4	ADIF	ADC Interrupt flag. when ADC After completion of the conversion and update the data register setting ADIF . If the ADC Interrupt enable bit ADIE for "1" And Global Interrupt set, ADC An interrupt is generated. carried out ADC Interrupt cleared ADIF Bits can also be written to the bit "1" Cleared.
3	ADIE	ADC Interrupt enable control bit. When set ADIE Bit "1" And the Global Interrupt When set, ADC Interrupt is enabled. When set ADIE Bit "0" Time, ADC Interrupts are disabled.

2: 0 ADPS [2: 0] ADC Prescaler select bit.

ADPS Selection system clock generation ADC Clock prescale factor.

ADPS [2: 0]	Prescale factor
0	2
1	2
2	4
3	8
4	16
5	32 (default)
6	64
7	128

ADCSRB - ADC Control and status registers B

ADCSRB - ADC Control and status registers B								
address: 0x7B						Defaults: 0x00		
Bit	7	6	5	4	3	2	1	0
Name	ACME01	ACME00	ACME11	ACME10	ACTS	ADTS2	ADTS1	ADTS0
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W
Initial	0	0	0	0	0	0	0	0

Bit	Name	description
7	ACME01	Comparators 0 Negative input selection
6	ACME00	00 : The negative terminal of the external input select ACIN0 01 : Select the negative terminal ADC Multiplexed output 1X : Select the negative terminal of the operational amplifier 0 Output
5	ACME11	Comparators 1 Negative input selection
4	ACME10	00 : The negative terminal of the external input select ACIN2 01 : Select the negative terminal ADC Multiplexed output 1X: Select the negative terminal of the operational amplifier 1 Output
3	ACTS	AC Trigger source channel selection 0 - AC0 Output as ADC The automatic conversion trigger 1 - AC1 Output as ADC The automatic conversion trigger
2: 0	ADTS [2: 0]	ADC Automatically trigger source select bit. When set ADATE Bit "1" When triggered automatically select function is enabled by a trigger source ADTS To control. When set ADATE Bit "0" Time, ADTS The setting is invalid. The rising edge of the selected trigger signal interrupt flag open a conversion. When the flag is cleared the interrupt trigger a switch to the interrupt flag is set, the source will trigger a rising edge of the trigger signal is generated, if at this time ADEN Position, ADC It will open a conversion. When the switching to the continuous conversion mode (ADTS = 0 Time), triggering an automatic function is disabled.

ADTS [2: 0]	Trigger source
0	Continuous conversion mode
1	Comparators 0/1

		2	External Interrupt 0
		3	Timing counter 0 Compare match
		4	Timing counter 0 overflow
		5	Timing counter 1 Compare match B
		6	Timing counter 1 overflow
		7	Timing counter 1 Input capture event

ADMUX - ADC Multiplexer control register

ADMUX - ADC Multiplexer control register								
address: 0x7C				Defaults: 0x00				
Bit	7	6	5	4	3	2	1	0
Name	REFS1 REFS0 ADLAR CHMUX4 CHMUX3 CHMUX2 CHMUX1 CHMUX0 R / W							
	R / WR / WR / W			R / W	R / W	R / W	R / W	R / W
Initial	0	0	0	0	0	0	0	0

Bit	Name	description		
7: 6	REFS [1: 0]	versus ADCSRD Register REFS2 Fit for selection ADC By providing a reference voltage source REFS Reference voltage control bit, if the change in the conversion process REFS Settings, change will work only until the end of the current conversion.		
		REFS2, REFS [1: 0]	Reference voltage selection	
		0_00	AREF	
		0_01	AVCC	
		0_10	Chip 2.048V The reference voltage source	
		0_11	Chip 1.024V The reference voltage source	
		1_00	Chip 4.096V The reference voltage source	
5	ADLAR	The result is left-aligned enable control bit. When set ADLAR Bit "1" When the conversion result in ADC Align left data register. When set ADLAR Bit "0" When the conversion result in ADC Data registers are right-justified.		
4: 0	CHMUX [4: 0]	ADC Input source selection control bits.		
		CHMUX [4: 0]	Single-ended input source	description
		0_0000	PC0	External input port
		0_0001	PC1	
		0_0010	PC2	
		0_0011	PC3	
		0_0100	PC4	
		0_0101	PC5	
		0_0110	PE1	
		0_0111	PE3	
		0_1001	PC7	

		0_1010	PF0	
		0_1011	PE6	
		0_1100	PE7	
		0_1110	4 / 5VDO	Internal voltage circuit
		0_1000	1 / 5VDO	
		0_1101	IVREF	Internal Reference
		0_1111	AGND	Analog ground
		1_XXXX	DACO	internal DAC Export

ADCSRC - ADC Control Status Register C

ADCSRC - ADC Control Status Register C								
address: 0x7D				Defaults: 0x00				
Bit	7	6	5	4	3	2	1	0
Name	OFEN	- SPN		AMEN	-	SPD	DIFS	ADTM
R / W	R / W	- R / W		R / W	- R / W		R / W	R / W

Bit	Name	description
7	OFEN	1 = Enable offset compensation; 0 = Close offset compensation
6	-	Unimplemented
5	SPN	ADC Conversion polarity control input, only the offset calibration process. Normal must be cleared
4	AMEN	Enabling automatic monitoring channel; 1 : Channel Enable automatic supervising function 0 : Disable automatic channel monitoring
3	-	Unimplemented
2	SPD	0 = ADC Low conversion mode 1 = ADC High-speed conversion mode, only a low-impedance analog inputs
1	DIFS	0 = ADC Conversion from ADC Multiplexer 1 = ADC Internal conversion from the differential amplifier
0	ADTM	Test mode, from AVREF Internal reference voltage output port

DIDR0 - Digital Input Disable Control Register 0

DIDR0 - Digital Input Disable Control Register 0								
address: 0x7E					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	PE3D	PE1D	PC5D	PC4D	PC3D	PC2D	PC1D	PC0D
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
7	PE3D	1 = shut down PE3 Digital Input Function
6	PE1D	1 = shut down PE1 Digital Input Function
5	PC5D	1 = shut down PC5 Digital Input Function
4	PC4D	1 = shut down PC4 Digital Input Function

3	PC3D	1 = shut down PC3 Digital Input Function
2	PC2D	1 = shut down PC2 Digital Input Function
1	PC1D	1 = shut down PC1 Digital Input Function
0	PC0D	1 = shut down PC0 Digital Input Function

DIDR1 - Digital Input Disable Control Register 1

DIDR1 - Digital Input Disable Control Register 1								
address: 0x7F					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	PE7D	PE6D	PE0D	C0PD	PF0D	PC7D	PD7D	PD6D
R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W	R / W

Bit	Name	description
0	PD6D	1 = shut down PD6 Digital Input Function
1	PD7D	1 = shut down PD7 Digital Input Function
2	PC7D	1 = shut down PC7 Digital Input Function
3	PF0D	1 = shut down PF0 Digital Input Function
4	C0PD	1 = shut down AC0P Digital input function (LQFP48)
5	PE0D	1 = shut down PE0 Digital Input Function
6	PE6D	1 = shut down PE6 Digital Input Function
7	PE7D	1 = shut down PE7 Digital Input Function

ADCSRD - ADC Control register D

ADCSRD - ADC Control register D								
address: 0xAD					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	BGEN	REFS2	IVSEL1	IVSEL0	-	VDS2	VDS1	VDS0
R / W	R / W	R / W	R / W	R / W	- R / W		R / W	R / W

Bit	Name	description
7	BGEN	Internal Reference Global enable control, 1 = Enable
6	REFS2	versus ADMUX Register REFS For selecting a combination of ADC Conversion reference voltage Please refer to ADMUX Register REFS Definition
5: 4	IVSEL	when ADC The reference voltage selected VCC or AVREF , IVSEL For controlling the output of the internal reference Voltage: 00 = 1.024V 01 = 2.048V 1x = 4.096V
3	-	Retention
2: 0	VDS [2: 0]	Dividing the input source selection circuit 000/111 = Close dividing circuit module 001 = ADC0 010 = ADC1 011 = ADC4

		100 = ADC5 101 = External reference input (AVREF) 110 = System Power

DAPCR - Differential amplifier control register

DAPCR - Differential amplifier control register								
address: 0xDC					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	DAPEN	GA1	GA0	DNS2	DNS1	DNS0	DPS1	DPS0
R / W	W / R	W / R	W / R	W / R	W / R	R / W	R / W	R / W

Bit	Name	description
7	DAPEN	1 = Enabling differential amplifier; 0 = Close differential amplifier
6: 5	GA [1: 0]	Differential amplifier gain control 00 = x1 01 = x8 10 = x16 11 = x32
4: 2	DNS [2: 0]	Inverting input terminal of the differential amplifier input source selection 000 = ADC2 / APN0 001 = ADC3 / APN1 010 = ADC8 / APN2 011 = ADC9 / APN3 100 = PE0 / APN4 101 = ADC Multiplexer 110 = AGND 111 = Close inverting input of the differential amplifier
1: 0	DPS [1: 0]	The positive input terminal of the differential amplifier source selection 00 = ADC Multiplexer 01 = ADC0 / APP0 10 = ADC1 / APP1 11 = AGND

OFR0 - Offset compensation register 0

OFR0 - Offset compensation register 0								
address: 0xA3					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OFR0 [7: 0]							
R / W	W / R							

Bit	Name	description
7: 0	OFR0	Offset compensation register 0 ; OFR0 As signed. Stored in twos complement format

OFR1 - Offset compensation register 1

OFR1 - Offset compensation register 1								
address: 0xA4					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	OFR1 [7: 0]							
R / W	W / R							

Bit	Name	description
7: 0	OFR1	Offset compensation register 1 ; OFR1 As signed. Stored in twos complement format

ADMSC - ADC Monitoring channel status and control register

ADMSC - ADC Monitoring channel status and control register								
address: 0xAC					Defaults: 0x01			
Bit	7	6	5	4	3	2	1	0
Name	AMOF	-	-	-	AMFC3	AMFC2	AMFC1	AMFC0
R / W	-	-	-	- R / W		R / W	R / W	R / W

Bit	Name	description
7	AMOF	Automatic monitoring overflow event type flag; 1 = On overflow, 0 = Underflow
6: 4	-	Unimplemented
3: 0	AMFC	Automatic monitoring control bit Digital Filter: 0000 = Disable configuration 0001 = A conversion filterless 0010 = Two consecutive agreement 0011 = Three consecutive agreement .... 1110 = 14 Consecutive agreement 1111 = 15 Consecutive agreement

ADT0L - Automatic monitoring low threshold underflow 8 Place

ADT0L - Automatic monitoring low threshold underflow 8 Place								
address: 0xA5					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	ADT0L [7: 0]							
R / W	W / R							

Bit	Name	description
7: 0	ADT0L	Overflow Threshold Register Low automatic monitoring 8 Place

ADT0H - Automatic monitoring high threshold underflow 8 Place

ADT0H - Automatic monitoring high threshold underflow 8 Place								
address: 0xA6					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	ADT0H [7: 0]							
R / W	W / R							

Bit	Name	description
7: 0	ADT0H	Overflow Threshold Register High automatic monitoring 8 Place

ADT1L - Automatic monitoring low threshold overflow 8 Place

ADT0L - Automatic monitoring low threshold overflow 8 Place								
address: 0xAA					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	ADT1L [7: 0]							
R / W	W / R							

Bit	Name	description
7: 0	ADT1L	Automatic monitoring of low overflow threshold register 8 Place

ADT1H - Automatic monitoring high threshold overflow 8 Place

ADT1H - Automatic monitoring high threshold overflow 8 Place								
address: 0xAB					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	ADT1H [7: 0]							
R / W	W / R							

Bit	Name	description
7: 0	ADT1H	Automatic monitoring high threshold register overflow 8 Place

VCAL - Internal reference calibration register

VCAL - Internal reference calibration register								
address: 0xC8					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	VCAL [7: 0]							
R / W	W / R							

Bit	Name	description
7: 0	VCAL	Internal reference calibration register. After power-loaded by default 1.024V Calibration values. The other reference voltage calibration value written to this register, Calibration can be achieved in the relevant reference. For example, for the reference configuration 2.048V After the VCAL2 Write register change, complete 2.048V Internal calibration reference.

VCAL1 - 1.024V Reference calibration register

VCAL1 - 1.024V Internal reference calibration register								
address: 0xCD					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	VCAL1 [7: 0]							
R / W	R / O							

Bit	Name	description
7: 0	VCAL1	1.024V Internal reference calibration coefficient

VCAL2 - 2.048V Reference calibration register

VCAL2 - 2.048V Internal reference calibration register								
address: 0xCE					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	VCAL2 [7: 0]							
R / W	R / O							

Bit	Name	description
7: 0	VCAL2	2.048V Internal reference calibration coefficient

VCAL3- 4.096V Reference calibration register

VCAL1 - 4.096V Internal reference calibration register								
address: 0xCC					Defaults: 0x00			
Bit	7	6	5	4	3	2	1	0
Name	VCAL3 [7: 0]							
R / W	R / O							

Bit	Name	description
7: 0	VCAL3	4.096V Internal reference calibration coefficient

Register cheat sheet

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					Extended IO Register				
$ F6	GUID3	GUID Byte 3							
$ F5	GUID2	GUID Byte 2							
$ F4	GUID1	GUID Byte 1							
$ F3	GUID0	GUID Byte 0							
$ F2	PMCR	PMCE	CLKFS	CLKSS	WCLKS	OSCKEN	OSCMEN	RCKEN	RCMEN
$ F0	PMX2	WCE	STOSC1	STOSC0	-	-	XIEN	E6EN	C6EN
$ EE	PMX0	PMXCE	C1BF4	C1AF5	C0BF3	C0AC0	SSB1	TXD6	RXD5
$ ED	PMX1	-	-	-	-	-	C3AC	C2BF7	C2AF6
$ EC	TCKSR	-	F2XEN	TC2XF1	TC2XF0	-	AFCKS	TC2XS1	TC2XS0
$ E2	PSSR	PSS1	PSS3	-	-	-	-	PSR3	PSR1
$ E1	OCPUE	PUE7	PUE6	PUE5	PUE4	PUE3	PUE2	PUE1	PUE0
$ E0	HDR	-	-	HDR5	HDR4	HDR3	HDR2	HDR1	HDR0
$ DE	DAPTE	DAPTE	-	-	-	-	-	-	-
$ DD	DAPTR	DAPTP	DAP Trimming						
$ DC	DAPCR	DAPEN	GA1	GA0	DNS2	DNS1	DNS0	DPS1	DPS0
$ D8									
$ D7									
$ D6									
$ D5									
$ D4									
$ D2									
$ D1									
$ D0									
$ CF	LDOCR	WCE				PDEN	VSEL2	VSEL1	VSEL0
$ CE	VCAL2	Calibration value for 2.048V internal reference							
$ CD	VCAL1	Calibration value for 1.024V internal reference							
$ CC	VCAL3	Calibration value for 4.096V internal reference							
$ C8	VCAL	Internal Voltage Reference calibration register							
$ C6	UDR	USART Data Register							
$ C5	UBRRH	-	-	-	-	USART Baud Rate Register High			
$ C4	UBRRL	USART Baud Rate Register Low							
$ C2	UCSRC	UMSEL1	UMSEL0	UPM1	UPM0	USBS0	UCSZ01	UCSZ00	UCPOL0
$ C1	UCSRB	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80
$ C0	UCSRA	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0
$ BD	TWAMR	TWI Address Mask							-
$ BC	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	-	TWIE
$ BB	TWDR	TWI Data							
$ BA	TWAR	TWI Address							TWGCE

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$ B9	TWSR	TWI Status bits					-	TWPS	
$ B8	TWBR	TWI Bit Rate register							
$ B6	ASSR	INTCK	-	AS2	TCN2UB	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB
$ B4	OCR2B	Timer 2 Output Compare Register B							
$ B3	OCR2A	Timer 2 Output Compare Register A							
$ B2	TCNT2	Timer 2 Counter Register							
$ B1	TCCR2B	FOC2A	FOC2B	-	-	WGM22	CS2		
$ B0	TCCR2A	COM2A1	COM2A0	COM2B1	COM2B0	-	-	WGM21	WGM20
$ AF	DPS2R	-	-	-	-	DPS2E	LPRCE	TOS1	TOS0
$ AE	IOCWK	IOCD7	IOCD6	IOCD5	IOCD4	IOCD3	IOCD2	IOCD1	IOCD0
$ AD	ADCSRD	BGEN	REFS2	IVSEL1	IVSEL0	-	VDS2	VDS1	VDS0
$ AC	ADMSC	AMOF	-	-	-	AMFC3	AMFC2	AMFC1	AMFC0
$ AB	ADT1H	ADC Auto-monitor Overflow threshold high byte							
$ AA	ADT1L	ADC Auto-monitor Overflow threshold low byte							
$ A9	PORTE	Port Output E (for compatible with LGT8FX8D)							
$ A8	DDRE	Data Direction E (for compatible with LGT8FX8D)							
$ A7	PINE	Port Input E (for compatible with LGT8FX8D)							
$ A6	ADT0H	ADC Auto-monitor Underflow threshold high byte							
$ A5	ADT0L	ADC Auto-monitor Underflow threshold low byte							
$ A4	OFR1	ADC positive offset trimming							
$ A3	OFR0	ADC negative offset trimming							
$ A1	DALR	DAC data register							
$ A0	DACON	-	-	-	-	DACEN	DAOE	DAVS1	DAVS0
$ 9F	OCR3CH	Compare output register high byte of Timer3 C channel							
$ 9E	OCR3CL	Compare output register low byte of Timer3 C channel							
$ 9D	DTR3H	Dead-band register high byte of Timer3							
$ 9C	DTR3L	Dead-band register low byte of Timer3							
$ 9B	OCR3BH	Compare output register high byte of Timer3 B channel							
$ 9A	OCR3BL	Compare output register low byte of Timer3 B channel							
$ 99	OCR3AH	Compare output register high byte of Timer3 A channel							
$ 98	OCR3AL	Compare output register low byte of Timer3 A channel							
$ 97	ICR3H	Input capture register high byte of Timer3							
$ 96	ICR3L	Input capture register low byte of Timer3							
$ 95	TCNT3H	Counter register high byte of Timer3							
$ 94	TCNT3L	Counter register low byte of Timer3							
$ 93	TCCR3D	Control register D of Timer3							
$ 92	TCCR3C	Control register C of Timer3							
$ 91	TCCR3B	Control register B of Timer3							
$ 90	TCCR3A	Control register A of Timer3							
$ 8D	DTR1H	Dead-band register high byte of Timer1							
$ 8C	DTR1L	Dead-band register low byte of Timer1							
$ 8B	OCR1BH	Timer 1 Output Compare B High							

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$ 8A	OCR1BL	Timer 1 Output Compare B Low							
$ 89	OCR1AH	Timer 1 Output Compare A High							
$ 88	OCR1AL	Timer 1 Output Compare A Low							
$ 87	ICR1H	Timer 1 Input Capture High							
$ 86	ICR1L	Timer 1 Input Capture Low							
$ 85	TCNT1H	Timer 1 Counter High							
$ 84	TCNT1L	Timer 1 Counter Low							
$ 83	TCCR1D	DSX17	DSX16	DSX15	DAX14	-	-	DSX11	DSX10
$ 82	TCCR1C	FOC1A	FOC1B	DOC1B	DOC1A	DTEN1	-	-	-
$ 81	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS1		
$ 80	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	-	-	WGM11	WGM10
$ 7F	DIDR1	PE7D	PE6D	PE0D	C0PD	PF0D	PC7D	PD7D	PD6D
$ 7E	DIDR0	PE3D	PE1D	PC5D	PC4D	PC3D	PC2D	PC1D	PC0D
$ 7D	ADCSRC	OFEN	-	SPN	AMEN	-	SPD	DIFS	ADTM
$ 7C	ADMUX	REFS1	REFS0	ADLAR	CHMUX				
$ 7B	ADCSRB	CME01	CME00	CME11	CME10	-	ADTS		
$ 7A	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS		
$ 79	ADCH	ADC Data High							
$ 78	ADCL	ADC Data Low							
$ 76	DIDR2	-	PB5D	-	-	-	-	-	-
$ 75	IVBASE	Interrupt Vector Base Address							
$ 74	PCMSK4								
$ 73	PCMSK3	PCINT [39:32]							
$ 71	TIMSK3			ICIE3	-	OCIE3C	OCIE3B	OCIE3A	TOIE3
$ 70	TIMSK2	-	-	-	-	-	OCIE2B	OCIE2A	TOIE2
$ 6F	TIMSK1	-	-	ICIE1	-	-	OCIE1B	OCIE1A	TOIE1
$ 6E	TIMSK0	-	-	-	-	-	OCIE0B	OCIE0A	TOIE0
$ 6D	PCMSK2	PCINT [23:16]							
$ 6C	PCMSK1	PCINT [15: 8]							
$ 6B	PCMSK0	PCINT [7: 0]							
$ 69	EICRA	-	-	-	-	ISC11	ISC10	ISC01	ISC00
$ 68	PCICR	-	-	-	PCIE4	PCIE3	PCIE2	PCIE1	PCIE0
$ 67	RCKCAL	RC32K Calibration							
$ 66	RCMCAL	RC32M Calibration							
$ 65	PRR1	-	-	PRWDT	-	PRTIM3	PREFL	PRPCI	-
$ 64	PRR / 0	PRTWI	PRTIM2	PRTIM0	-	PRTIM1	PRSPI	PRUART0	PRADC
$ 62	VDTCR	WCE	SWR	-	VDTS			VDREN	VDTEN
$ 61	CLKPR	WCE	CKOE1	CKOE0	-	CLKPS			
$ 60	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0
DirectIO Register									
$ 5F	SREG	I	T	H	S	V	N	Z	C
$ 5E	SPH	Stack Point High							

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$ 5D	SPL	Stack Point Low							
$ 5C	E2PD3	E2PCTL Data register byte 3							
$ 5B	C1TR	AC1 trimming data							
$ 5A	E2PD1	E2PCTL Data register byte1							
$ 59	DSAH	DSA [31:16] access port of uDSC							
$ 58	DSAL	DSA [15: 0] access port of uDSC							
$ 57	E2PD2	E2PCTL Data register byte 2							
$ 56	ECCR	WEN	EEN	ERN	SWM	CP1	CP0	ECS1	ECS0
$ 55	MCUCR	FWKEN	FPDEN	SWR	PUD	IRLD	IFAIL	IVSEL	WCE
$ 54	MCUSR	SWDD	-	-	OCDRF	WDRF	BORF	EXTRF	PORF
$ 53	SMCR	-	-	-	-	SM			SE
$ 52	C0TR	AC0 Trimming register							
$ 51	C0XR	-	C0OE	C0HYSE	C0PS0	C0WKE	C0FEN	C0FS1	C0FS0
$ 50	C0SR	C0D	C0BG	C0O	C0I	C0IE	C0IC	C0IS	
$ 4F	DTR0	TC0 Dead-band timing control register							
$ 4E	SPDR	SPI Data register							
$ 4D	SPSR	SPIF	WCOL	-	-	-	DUAL	-	SPI2X
$ 4C	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR	
$ 4B	GPIOR2	General Purpose Register 2							
$ 4A	GPIOR1	General Purpose Register 1							
$ 49	TCCR0C	DSX07	DSX06	DSX05	DSX04	-	-	DSX01	DSX00
$ 48	OCR0B	Timer 0 Output Compare Register B							
$ 47	OCR0A	Timer 0 Output Compare Register A							
$ 46	TCNT0	Timer 0 Counter							
$ 45	TCCR0B	FOC0A	FOC0B	OC0AS	DTEN0	WGM02	CS02	CS01	CS00
$ 44	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	DOC0B	DOC0A	WGM01	WGM00
$ 43	GTCCR	TSM	-	-	-	-	-	PSRASY	PSRSYNC
$ 42	EEARH	E2PCTL Address High							
$ 41	EEARL	E2PCTL Address Low							
$ 40	E2PD0	E2PCTL Data byte 0							
$ 3F	EECR	EEPM2	EEPM2	EEPM1	EEPM0	EERIE	EEMWE	EEWE	EERE
$ 3E	GPIOR0	General Purpose Register 0							
$ 3D	EIMSK	-	-	-	-	-	-	INT1	INT0
$ 3C	EIFR	-	-	-	-	-	-	INTF1	INTF0
$ 3B	PCIFR	-	-	-	-	PCIF3	PCIF2	PCIF1	PCIF0
$ 3A	C1XR	-	C1OE	C1HYSE	C1PS0	C1WKE	C1FEN	C1FS1	C1FS0
$ 39	SPFR	RDFULL	RDEMPT	RDPTR1	RDPTR0	WRFULL	WREMPT	WRPTR1	WRPTR0
$ 38	TIFR3	-	-	ICF3	-	-	OCF3B	OCF3A	TOV3
$ 37	TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2
$ 36	TIFR1	-	-	ICF1	-	-	OCF1B	OCF1A	TOV1
$ 35	TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0
$ 34	PORTF	Port Output of Group F							

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$ 33	DDRF	Data Direction of Group F							
$ 32	PINF	Port Input of Group F							
$ 31	DSDY	DSDY access port of uDSC							
$ 30	DSDX	DSDX access port of uDSC							
$ 2F	C1SR	C1D	C1BG	C1O	C1I	C1IE	C1IC	C1IS	
$ 2E	PORTE	Port Output of Group E							
$ 2D	DDRE	Data Direction of Group E							
$ 2C	PINE	Port Input of Group E							
$ 2B	PORTD	Port Output of Group D							
$ 2A	DDRD	Data Direction of Group D							
$ 29	PIND	Port Input of Group D							
$ 28	PORTC	Port Output of Group C							
$ 27	DDRC	Data Direction of Group C							
$ 26	PINC	Port Input of Group C							
$ 25	PORTB	Port Output of Group B							
$ 24	DDRB	Data Direction of Group B							
$ 23	PINB	Port Input of Group B							
$ 22	DSSD	DSSD access port of uDSC							
$ 21	DSIR	Instruction regiter of uDSC							
$ 20	DSCR	DSUEN	MM	D1	D0	-	DSN	DSZ	DSC

Instruction Set Quick Reference

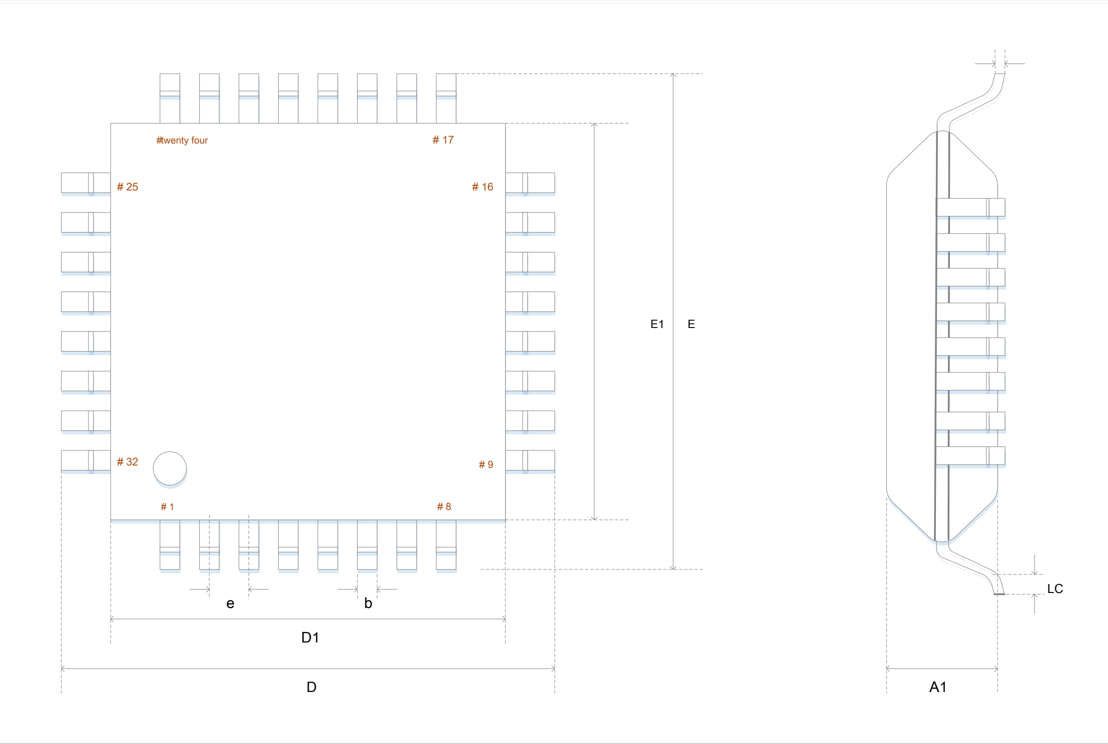
instruction	Operand	description	operating	Flag	cycle
Arithmetic and logic instructions					
ADD	R_d, R_r	Adding register	$R_d \leftarrow R_d + R_r$	Z, C, N, V, H	1
ADC	R_d, R_r	Adding the carry bit register	$R_d \leftarrow R_d + R_r + C$	Z, C, N, V, H	1
ADIW	R_{dl}, K	Now the number is added to the word	$R_{dh}:R_{dl} \leftarrow R_{dh}:R_{dl} + K$	Z, C, N, V, S	1
SUB	R_d, R_r	Add and subtract registers	$R_d \leftarrow R_d - R_r$	Z, C, N, V, H	1
SUBI	R_d, K	Constant Register Save	$R_d \leftarrow R_d - K$	Z, C, N, V, H	1
SBC	R_d, R_r	Register of addition and subtraction with borrow	$R_d \leftarrow R_d - R_r - C$	Z, C, N, V, H	1
SBCI	R_d, K	Save Register is constant with borrow	$R_d \leftarrow R_d - K - C$	Z, C, N, V, H	1
SBIW	R_{dl}, K	Subtract immediate word	$R_{dh}:R_{dl} \leftarrow R_{dh}:R_{dl} - K$	Z, C, N, V, S	1
AND	R_d, R_r	Logic and	$R_d \leftarrow R_d \& R_r$	Z, N, V	1
ANDI	R_d, K	And a constant register logic	$R_d \leftarrow R_d \& K$	Z, N, V	1
OR	R_d, R_r	Logical or	$R_d \leftarrow R_d \mid R_r$	Z, N, V	1
ORI	R_d, K	Or constant register logic	$R_d \leftarrow R_d \mid K$	Z, N, V	1
EOR	R_d, R_r	XOR register	$R_d \leftarrow R_d \oplus R_r$	Z, N, V	1
COM	R_d	Inverted	$R_d \leftarrow \$FF - R_d$	Z, C, N, V	1
NEG	R_d	2 Ban complement	$R_d \leftarrow \$00 - R_d$	Z, C, N, V, H	1
SBR	R_d, K	Setting register bit	$R_d \leftarrow R_d \vee K$	Z, N, V	1
CBR	R_d, K	Register bit clear	$R_d \leftarrow R_d \vee (\$FF - K)$	Z, N, V	1
INC	R_d	Increment	$R_d \leftarrow R_d + 1$	Z, N, V	1
DEC	R_d	Decreasing	$R_d \leftarrow R_d - 1$	Z, N, V	1
TST	R_d	Tests for 0 Or negative	$R_d \leftarrow R_d \& R_d$	Z, N, V	1
CLR	R_d	Clear register	$R_d \leftarrow R_d \oplus R_d$	Z, N, V	1
SER	R_d	Register are set to 1	$R_d \leftarrow \$FF$	None	1
MUL	R_d, R_r	Unsigned multiply	$R_1:R_0 \leftarrow R_d \times R_r$	Z, C	1
MULS	R_d, R_r	Signed multiply	$R_1:R_0 \leftarrow R_d \times R_r$	Z, C	1
MULSU	R_d, R_r	Signed unsigned multiplication	$R_1:R_0 \leftarrow R_d \times R_r$	Z, C	1
FMUL	R_d, R_r	Unsigned multiplication, shift	$R_1:R_0 \leftarrow (R_d \times R_r) \ll 1$	Z, C	1
FMULS	R_d, R_r	Signed multiply, shift	$R_1:R_0 \leftarrow (R_d \times R_r) \ll 1$	Z, C	1
FMULSU	R_d, R_r	Signed unsigned multiplication, shift	$R_1:R_0 \leftarrow (R_d \times R_r) \ll 1$	Z, C	1
Jump instructions					
RJMP	K	Relative jump	$PC \leftarrow PC + K + 1$	None	1
IJMP		Indirect jump (to Z At the address)	$PC \leftarrow Z$	None	2
JMP	K	Jump directly	$PC \leftarrow K$	None	2
RCALL	K	Relative subroutine call address	$PC \leftarrow PC + K + 1$	None	1
ICALL		Indirect subroutine call (Z At the address) $PC \leftarrow Z$		None	2
CALL	K	Direct subroutine call	$PC \leftarrow K$	None	2
RET		Subroutine returns	$PC \leftarrow Stack$	None	2
RETI		Interrupt return	$PC \leftarrow Stack$	I	2

instruction Operand		description	operating	Flag cycle	
Jump instructions (cont.)					
CPSE	R_d, R_r	That jump is equal to	If ($R_d = R_r$) PC ← PC + 2 or 3	None	1/2
CP	R_d, R_r	Compare	R_d - R_r	Z, N, V, C, H	1
CPC	R_d, R_r	Carry compare	R_d - R_r - C	Z, N, V, C, H	1
CPI	R_d, K	Compared with the immediate	R_d - K	Z, N, V, C, H	1
SBRC	R_r, b	Bit 0 Skip next instruction	If (R_r(b) = 0) PC ← PC + 2 or 3	None	1/2
SBRS	R_r, b	Bit 1 Skip next instruction	If (R_r(b) = 1) PC ← PC + 2 or 3	None	1/2
SBIC	P, b	I / O Bit 0 Skip next instruction	If (P (b) = 0) PC ← PC + 2 or 3	None	1/2
SBIS	P, b	I / O Bit 1 Skip next instruction	If (P (b) = 1) PC ← PC + 2 or 3	None	1/2
BRBS	s, k	State marked 1 That jump	If (SREG (S) = 1) PC ← PC + K + 1	None	1/2
BRBC	s, k	State marked 0 That jump	If (SREG (S) = 0) PC ← PC + K + 1	None	1/2
BREQ	k	That jump is equal to	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Range will jump	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Carry Jump	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Not Carry Jump	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Not less than jump	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Less than jump	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Negative jump	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	As a regular jump	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Signed i.e. jump is not less than	if (N ⊕ V = 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Signed less than 0 That jump	if (N ⊕ V = 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Half-carry is 1 Jump	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Half-carry is 0 Jump	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	T Set Jump	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	T Clear Jump	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Overflow jump	f (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Does not overflow jump	f (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Global Interrupt Enable jump	f (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Global Interrupt Disable Jump	f (I = 0) then PC ← PC + k + 1	None	1/2
Data Transfer Instructions					
MOV	Rd, Rr	Move data between registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Moving a data word	Rd + 1: Rd ← Rr + 1: Rr	None	1
LDI	Rd, K	Immediate loading	Rd ← K	None	1
LD	Rd, X	Indirect load	Rd ← (X)	None	1/2
LD	Rd, X +	Indirect load, the address is incremented	Rd ← (X), X ← X + 1	None	1/2
LD	Rd, -X	Address decrement, indirect load	X ← X - 1, Rd ← (X)	None	1/2
LD	Rd, Y	Indirect load	Rd ← (Y)	None	1/2
LD	Rd, Y +	Indirect load, the address is incremented	Rd ← (Y), Y ← Y + 1	None	1/2
LD	Rd, -Y	Address decrement, indirect load	Y ← Y - 1, Rd ← (Y)	None	1/2
LDD	Rd, Y + q	Indirect with offset loading	Rd ← (Y + q)	None	1/2
LD	Rd, Z	Indirect load	Rd ← (Z)	None	1/2

LD	Rd, Z +	Indirect load, the address is incremented	Rd ← (Z), Z ← Z + 1	None	1/2
LD	Rd, -Z	Address decrement, indirect load	Z ← Z - 1, Rd ← (Z)	None	1/2
LDD	Rd, Z + q Indirect with offset loading		Rd ← (Z + q)	None	1/2
LDS	Rd, k	Directly from SRAM Loaded	Rd ← (k)	None	2
ST	X, Rr	Indirect storage	(X) ← Rr	None	1
ST	X +, Rr	Indirect storage, address increment	(X) ← Rr, X ← X + 1	None	1
ST	- X, Rr	Address decrement, indirect storage	X ← X - 1, (X) ← Rr	None	1
ST	Y, Rr	Indirect storage	(Y) ← Rr	None	1
ST	Y +, Rr	Indirect storage, address increment	(Y) ← Rr, Y ← Y + 1	None	1
ST	- Y, Rr	Address decrement, indirect storage	Y ← Y - 1, (Y) ← Rr	None	1
STD	Y + q, Rr	Indirect storage tape offset	(Y + q) ← Rr	None	1
ST	Z, Rr	Indirect storage	(Z) ← Rr	None	1
ST	Z +, Rr	Indirect storage, address increment	(Z) ← Rr, Z ← Z + 1	None	1
ST	- Z, Rr	Address decrement, indirect storage	Z ← Z - 1, (Z) ← Rr	None	1
STD	Z + q, Rr	Indirect storage tape offset	(Z + q) ← Rr	None	1
STS	k, Rr	Directly to a memory SRAM in	(K) ← Rr	None	2
LPM		Spatial Data Loader	R0 ← (Z)	None	2
LPM	Rd, Z	Spatial Data Loader	Rd ← (Z)	None	2
LPM	Rd, Z +	Loader data, address increment	Rd ← (Z), Z ← Z + 1	None	2
LD	Rd, Z +	Indirect load, the address is incremented	Rd ← (Z), Z ← Z + 1	None	1
LD	Rd, -Z	Address decrement, indirect load	Z ← Z - 1, Rd ← (Z)	None	1
LDD	Rd, Z + q Indirect with offset loading		Rd ← (Z + q)	None	1
LDS	Rd, k	Directly from SRAM Loaded	Rd ← (k)	None	2
IN	Rd, P	Read Port	Rd ← P	None	1
OUT	P, Rr	Write port	P ← Rr	None	1
PUSH	Rr	Push	STACK ← Rr	None	1
POP	Rd	Pop	Rd ← STACK	None	1/2
SBI	P, b	Set up IO register	I / O (P, b) ← 1	None	1
CBI	P, b	Clear IO register	I / O (P, b) ← 0	None	1
LSL	Rd	Logical Shift Left	Rd (n + 1) ← Rd (n), Rd (0) ← 0	Z, C, N, V	1
LSR	Rd	Logical Shift Right	Rd (n) ← Rd (n + 1), Rd (7) ← 0	Z	1
ROL	Rd	Carry the left loop comprising	Rd (0) ← C, Rd (n + 1) ← Rd (n), C ← Rd (7)	Z	1
ROR	Rd	Rotate Right carry bit comprising	Rd (7) ← C, Rd (n) ← Rd (n + 1), C ← Rd (0)	Z	1
ASR	Rd	Arithmetic shift right	Rd (n) ← Rd (n + 1), n = 0: 6	Z	1
SWAP	Rd	Bit exchange	Rd (3: 0) ← Rd (7: 4), Rd (7: 4) ← Rd (3: 0) None		1
BSET	s	Status bit is set	SREG (s) ← 1	SREG (s)	1
BCLR	s	Status bit is cleared	SREG (s) ← 0	SREG (s)	1
BST	Rr, b	Storage to T Place	T ← Rr (b)	T	1
BLD	Rd, b	read out T Bit to register	Rd (b) ← T	None	1
SEC		We carry flag	C ← 1	C	1
CLC		Clear carry flag	C ← 0	C	1

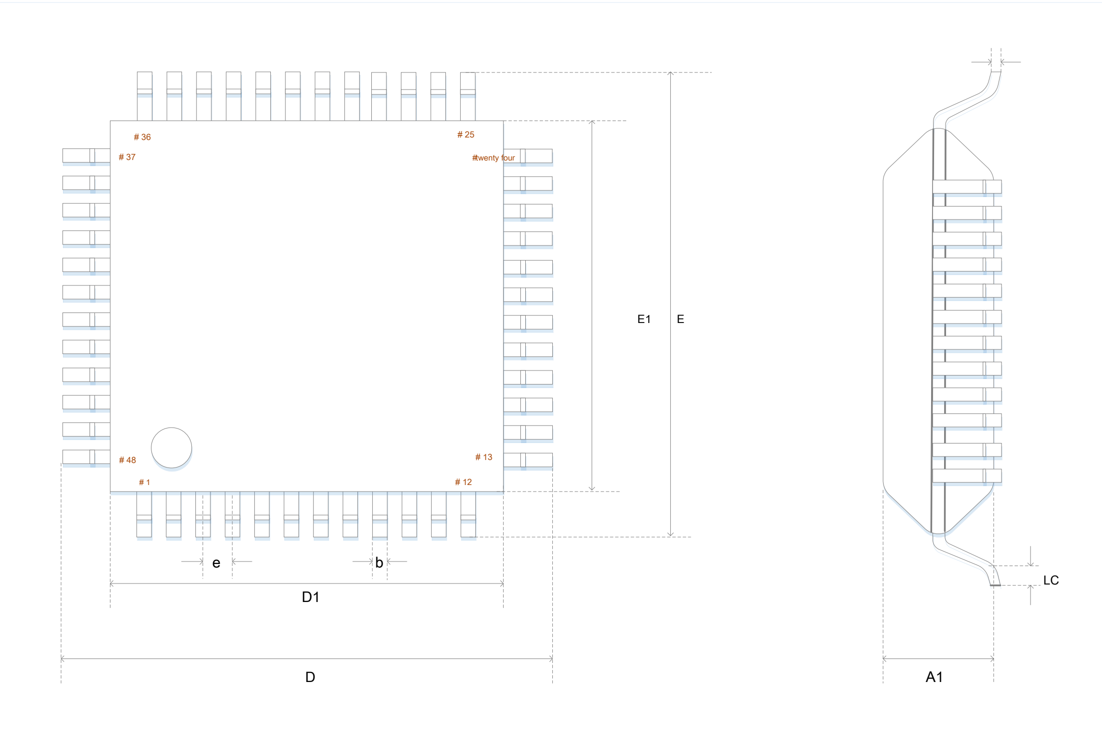
SEN		Set the negative sign	N ← 1	N	1
CLN		Clear Negative flag	N ← 0	N	1
SEZ		Set zero flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Enable global interrupt	I ← 1	I	1
CLI		Global Interrupt ban	I ← 0	I	1
SES		Set Symbol Test mark	S ← 1	S	1
CLS		Clear sign symbol test	S ← 0	S	1
SEV		Set two's complement overflow flag	V ← 1	V	1
CLV		Clear twos complement overflow flag	V ← 0	V	1
SET		Set up T Bit (SREG)	T ← 1	T	1
CLT		Remove T Bit (SREG)	T ← 0	T	1
MCU Control instruction					
NOP		Dummy instruction		None	1
SLEEP		Goes into sleep mode		None	1
WDR		Watchdog reset		None	1
BREAK		Soft Breakpoints	For debugging purposes only	None	N / A
NOP		Dummy instruction		None	1
SLEEP		Goes into sleep mode		None	1

Packaging Parameters



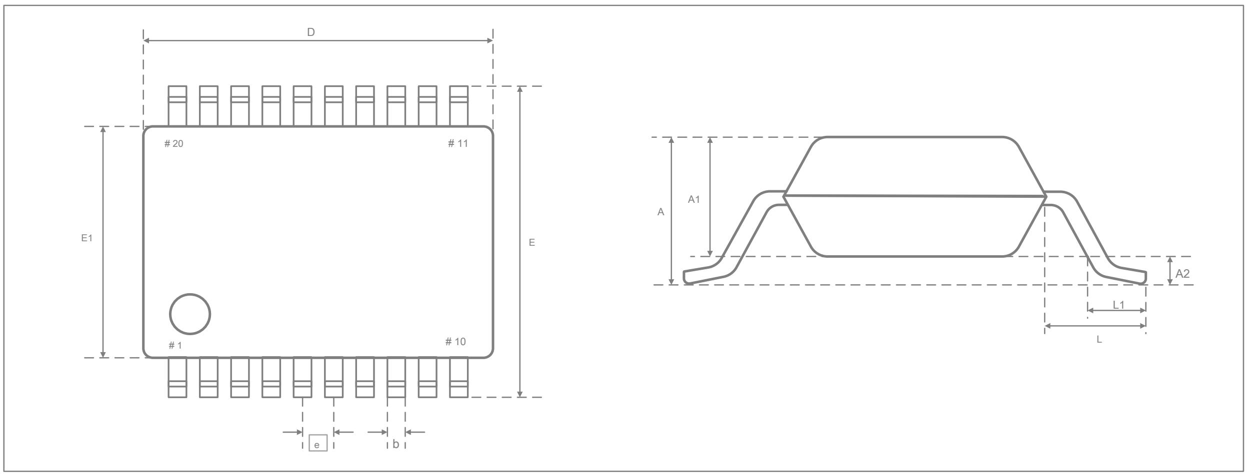
LQFP32 Universal size is defined

Character Code	Minimum	Typical values	Maximum	unit
D	8.90	9.00	9.10	mm
D1	6.90	7.00	7.10	mm
b	0.2	0.30	0.4	mm
e	0.75	0.80	0.85	mm
E	8.90	9.00	9.10	mm
E1	6.90	7.00	7.10	mm
C	-	0.10	-	mm
L	0.55	0.60	0.65	mm
A1	-	1.40	-	mm



LQFP48 Universal size is defined

Character Code	Minimum	Typical values	Maximum	unit
D	8.80	9.00	9.20	mm
D1	6.80	7.00	7.20	mm
b	0.17	0.22	0.27	mm
e	-	0.50BSC	-	mm
E	8.80	9.00	9.20	mm
E1	6.80	7.00	7.20	mm
c	0.09	-	0.2	mm
L	0.45	0.60	0.75	mm
A1	1.35	1.40	1.45	mm



SSOP20L Universal size is defined

Character Code	Minimum	Typical values	Maximum	unit
D	6.90	7.20	7.50	mm
A2	0.03	0.05	0.07	mm
b	0.22	0.30	0.38	mm
e	-	0.65	-	mm
E	7.40	7.80	8.20	mm
E1	5.00	5.30	5.60	mm
L1	0.55	-	0.95	mm
L	-	-	-	mm
A1	-	2.0	-	mm

Version History

V1.0.4 2017/11/15	correct SSOP20 PIN8 / 11 Definition
V1.0.3 2017/6/23	increase SSOP20 Package definition updates TMR3 Interrupt flag Operating instructions
V1.0.2 2017/5/15	Update TMR0 / TRM1 / TMR3 Regarding automatic PWM Shut down and restart the Notes Update SPI Section of SPI Interrupt processing instructions And update SPFR Register descriptions
V1.0.1 2017/2/13	delete I2C1 Part, this feature is not used to improve the definition section of the register
V1.0.0 2016/12/29	initial version