PROIECT CID

2023-2024

Gorgan Raluca-Sara
UNIVERSITATEA TEHNICA DIN CLUJ-NAPOCA
ELECTRONICA APLICATA, TELECOMUNICATII SI
TEHNOLOGIA INFORMATIEI

1.Rezolvarea corectă a temei de proiect pe hârtie(0.5p)

2.Circuitul combinațional (0.5p)

a) Verificarea funcționalității circuitului

3.Circuitul secvențial (0.5p)

a) Verificarea funcționalității circuitului

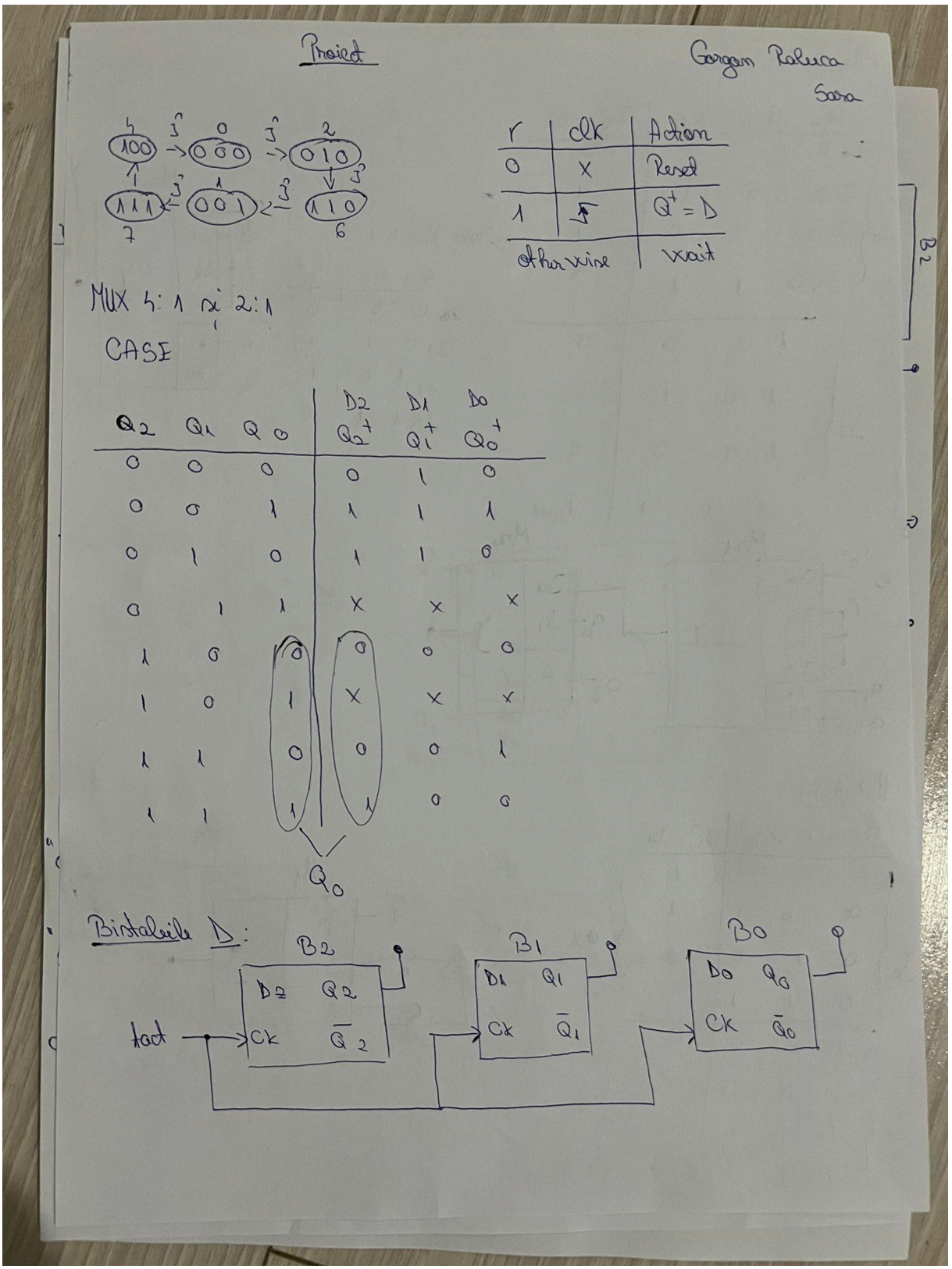
4. Implementarea finală(Arhitectura se va descrie structural)(3p)

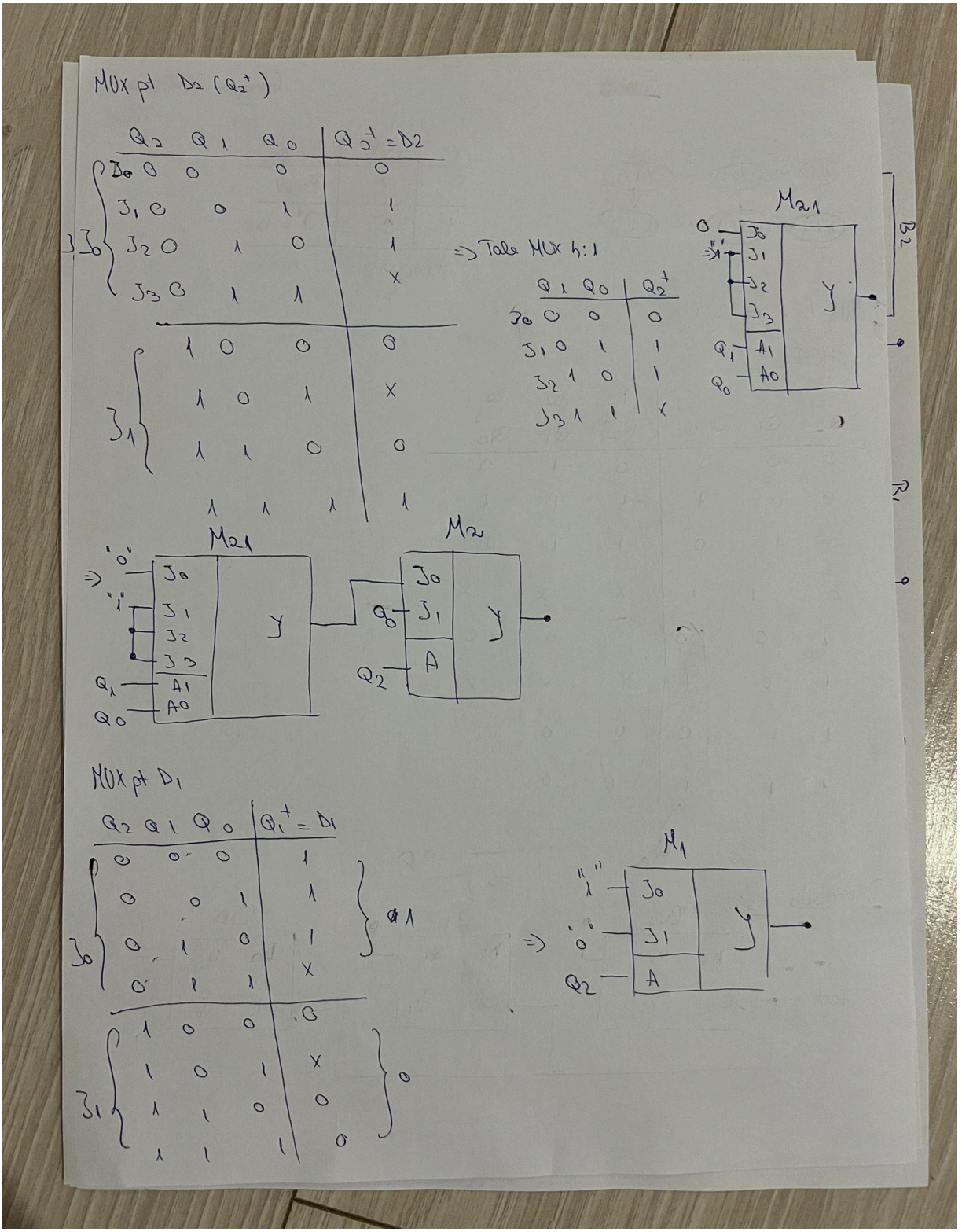
a) Verificarea funcționalității automatului

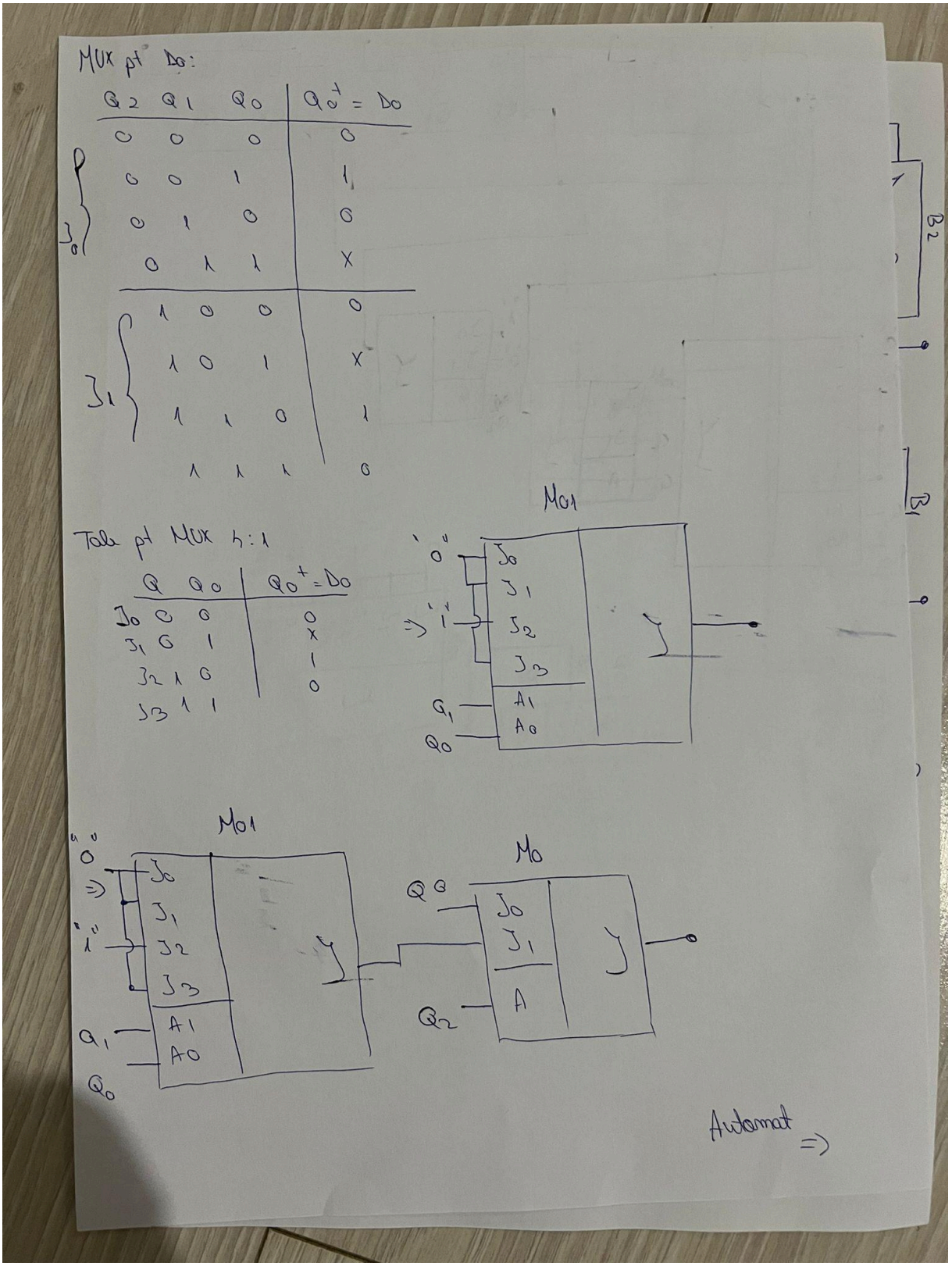
5.Aspect documentație (foi de capăt, pagini numerotate etc.)(0.5p)

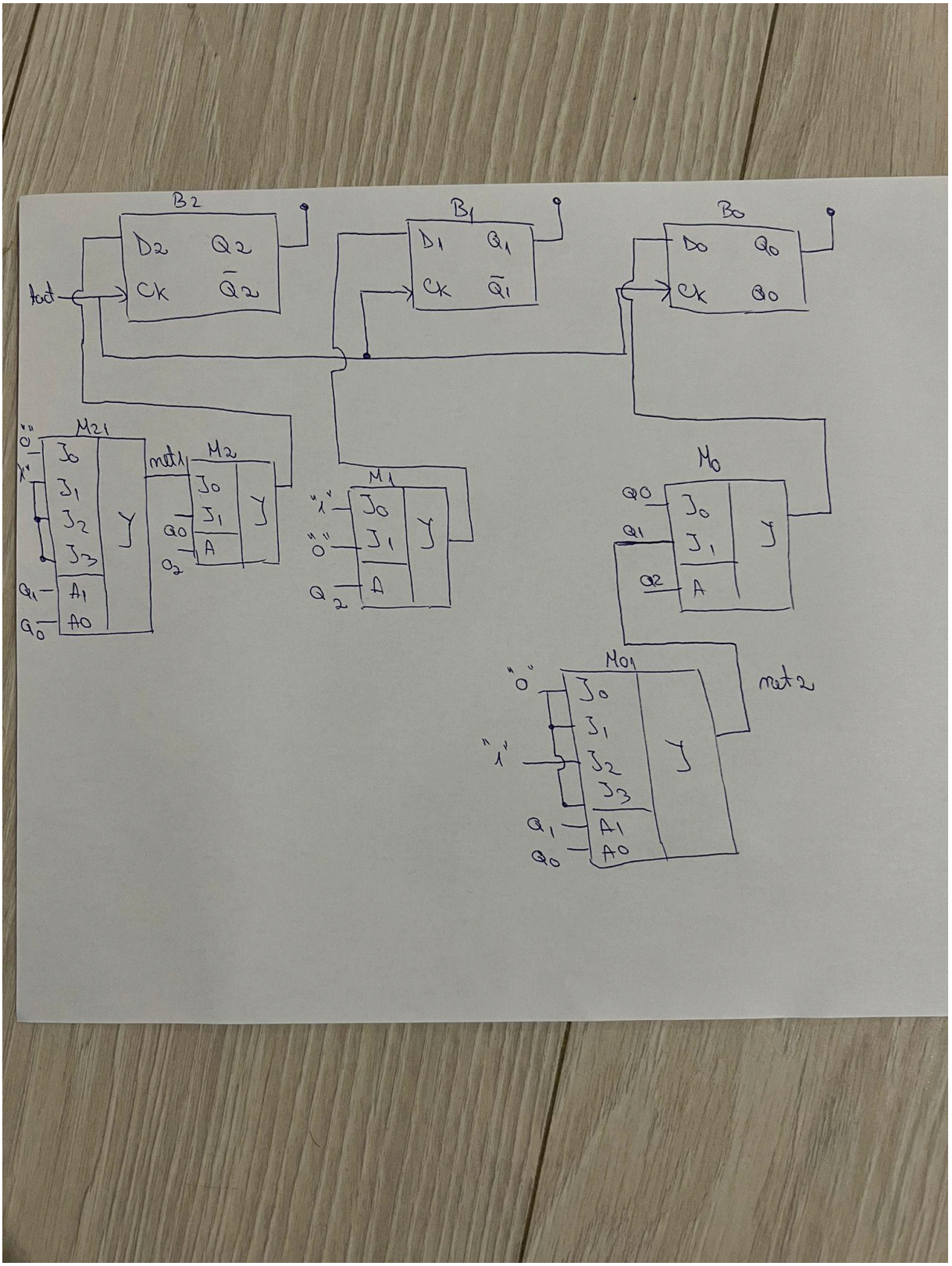
PASUL 1

Am rezolvat pe hartie circuitul:




MUX pt D2 (Q_2^+)
Q_2 Q_1 Q_0 | $Q_2^+ = D_2$
J_0 0 0 0 | 0
J_1 0 0 1 | 1
J_2 0 1 0 | 1
J_3 0 1 1 | X
1 0 0 | 0
J_1 1 0 1 | X
1 1 0 | 0
1 1 1 | 1
⇒ Tabel MUX 4:1
Q_1 Q_0 | Q_2^+
J_0 0 0 | 0
J_1 0 1 | 1
J_2 1 0 | 1
J_3 1 1 | X
M_{21}
M_2
M_1
MUX pt D_1
Q_2 Q_1 Q_0 | $Q_1^+ = D_1$
J_0 0 0 0 | 1
0 0 1 | 1
0 1 0 | 1
0 1 1 | X
ϕ_1
1 0 0 | 0
J_1 1 0 1 | X
1 1 0 | 0
1 1 1 | 0
ϕ_0
B_2
R_1


MUX pt D0:
Q2 Q1 Q0 | Q0+ = D0
J0
J1
Tabel pt MUX 4:1
Q1 Q0 | Q0+ = D0
J0 J1 J2 J3
MUX
MUX
MUX
Automat =>


B2
B1
B0
D2
Q2
CK
Q̄2
D1
Q1
Q̄1
D0
Q0
tact
M21
M2
M1
M0
M01
mot1
mot2
J0
J1
J2
J3
A1
A0
Y
A
"0"
"1"

Pasul 2:MUX4:1 + SIMULARE

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```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity m4_sim is
5  --  Port ( );
6  end m4_sim;
7
8  architecture Behavioral of m4_sim is
9  signal i0: std_logic;
10     signal i1: std_logic;
11     signal i2: std_logic;
12     signal i3: std_logic;
13     signal a1: std_logic;
14     signal a0: std_logic;
15     signal y: std_logic;
16 begin
17
18 dut: entity work.mux4
19         port map (
20             i0 => i0,
21             i1 => i1,
22             i2 => i2,
23             i3 => i3,
```

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```
23             i3 => i3,
24             a1 => a1,
25             a0 => a0,
26             y => y
27         );
28
29     stim_proc: process
30     begin
31         i0 <= '0';
32         i1 <= '0';
33         i2 <= '0';
34         i3 <= '0';
35         a1 <= '0';
36         a0 <= '0';
37         wait for 10 ns;
38
39         i0 <= '1';
40         i1 <= '0';
41         i2 <= '0';
42         i3 <= '1';
43         a1 <= '0';
44         a0 <= '1';
45         wait for 10 ns;
```

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```
        i0 <= '1';
        i1 <= '1';
        i2 <= '0';
        i3 <= '1';
        a1 <= '1';
        a0 <= '0';
        wait for 10 ns;

        i0 <= '1';
        i1 <= '1';
        i2 <= '1';
        i3 <= '1';
        a1 <= '1';
        a0 <= '1';
        wait for 10 ns;

        i0 <= '1';
        i1 <= '0';
        i2 <= '1';
        i3 <= '0';
        a1 <= '1';
        a0 <= '0';
        wait for 10 ns;

        i0 <= '1';
        i1 <= '1';
        i2 <= '0';
        i3 <= '1';
        a1 <= '0';
        a0 <= '1';
        wait for 10 ns;

        end process;

end Behavioral;
```

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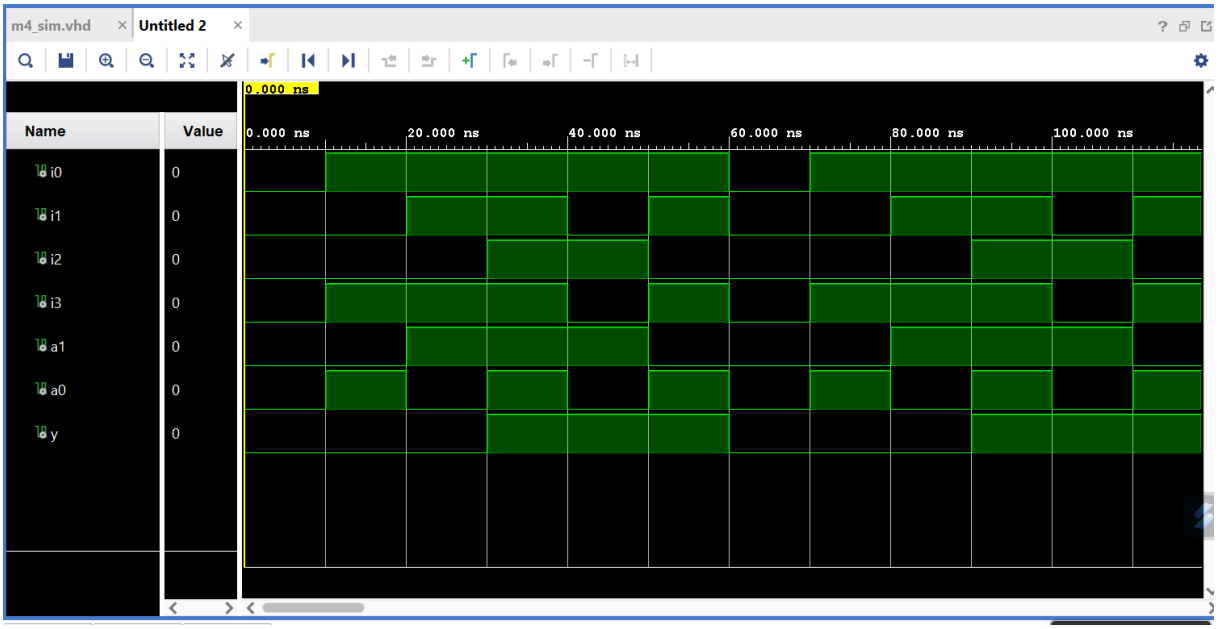
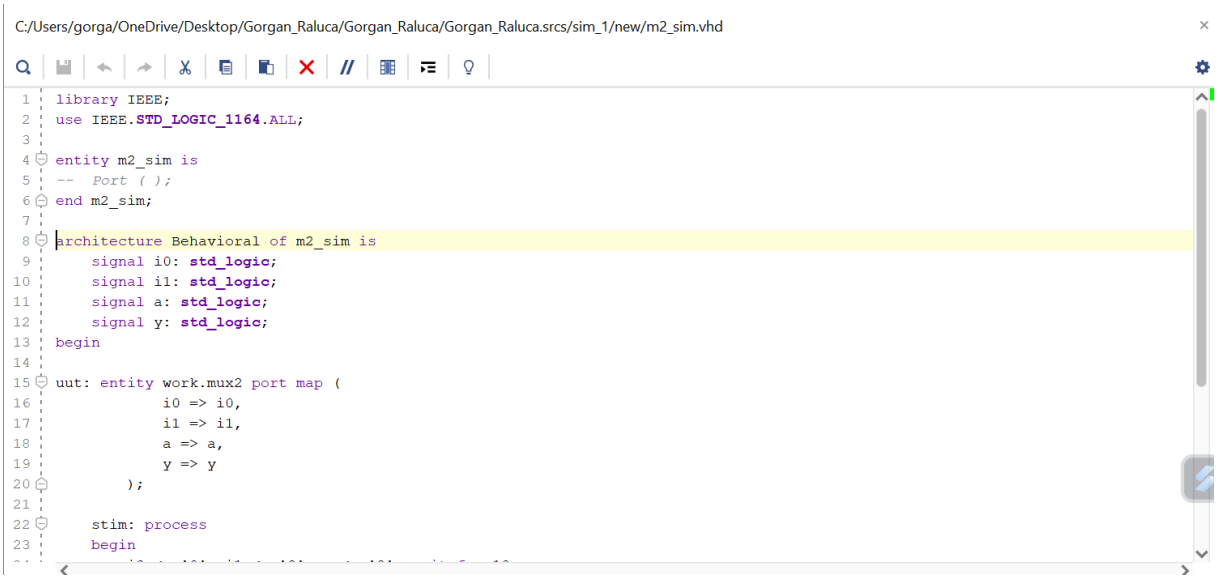
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.std_logic_unsigned.all;
use IEEE.std_logic_arith.all;

entity mux4 is
    Port (
        i0, i1, i2, i3 : in  std_logic;
        a1, a0         : in  std_logic;
        y              : out std_logic
    );
end mux4;

architecture Behavioral of mux4 is
begin
    process (i0, i1, i2, i3, a1, a0)
    begin
        if (a1 = '0' and a0 = '0') then
            y <= i0;
        elsif (a1 = '0' and a0 = '1') then
            y <= i1;
        elsif (a1 = '1' and a0 = '0') then
            y <= i2;
        else
            y <= i3;
        end if;
    end process;
end Behavioral;
```

SIMULARE



MUX2:1 + SIMULARE



```
    begin
        i0 <= '0'; i1 <= '0'; a <= '0'; wait for 10 ns;
        i0 <= '0'; i1 <= '0'; a <= '1'; wait for 10 ns;
        i0 <= '0'; i1 <= '1'; a <= '0'; wait for 10 ns;
        i0 <= '0'; i1 <= '1'; a <= '1'; wait for 10 ns;
        i0 <= '1'; i1 <= '0'; a <= '0'; wait for 10 ns;
        i0 <= '1'; i1 <= '0'; a <= '1'; wait for 10 ns;
        i0 <= '1'; i1 <= '1'; a <= '0'; wait for 10 ns;
        i0 <= '1'; i1 <= '1'; a <= '1'; wait for 10 ns;

    end process;

end Behavioral;

```

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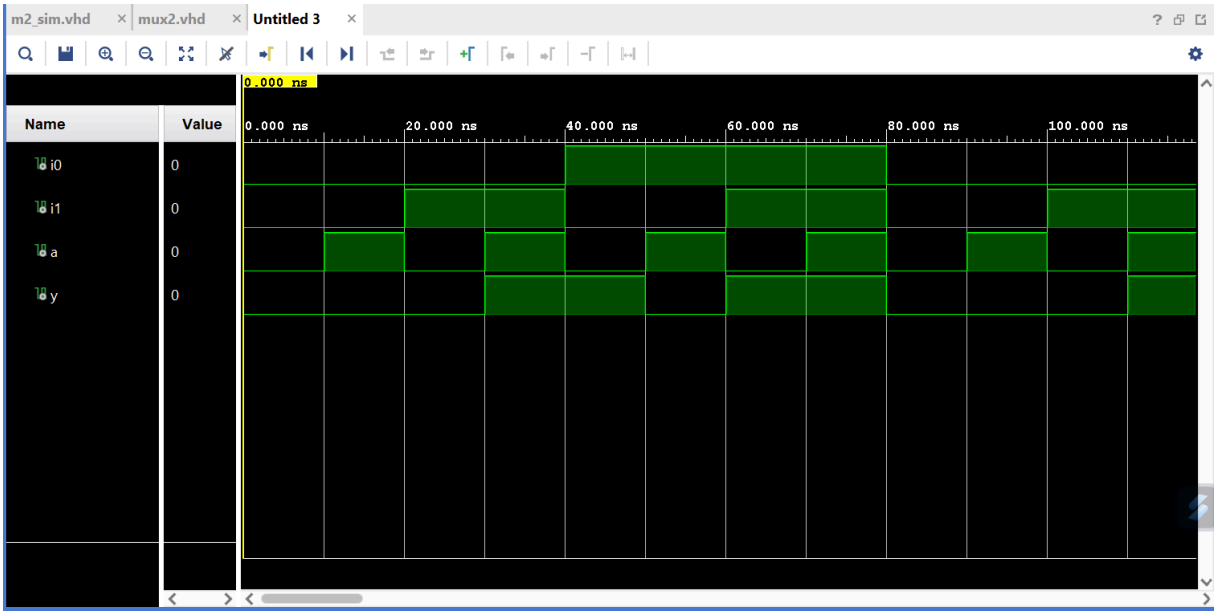
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mux2 is
    Port (
        i0 : in STD_LOGIC;
        i1 : in STD_LOGIC;
        a : in STD_LOGIC;
        y : out STD_LOGIC
    );
end mux2;

architecture Behavioral of mux2 is
begin
    process(i0, i1, a)
    begin
        case a is
            when '1' =>
                y <= i1;
            when others =>
                y <= i0;
        end case;
    end process;


    end process;
end Behavioral;

```

SIMULARE



PASUL 3:BISTABIL D + SIMULARE

C:/Users/gorga/OneDrive/Desktop/Gorgan_Raluca/Gorgan_Raluca/Gorgan_Raluca.srcs/sim_1/new/d_sim.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity d_sim is
5  --  Port ( );
6  end d_sim;
7
8  architecture Behavioral of d_sim is
9  signal d: std_logic;
10     signal clk: std_logic;
11     signal r: std_logic;
12     signal q: std_logic;
13     signal qn: std_logic;
14
15 begin
16
17 T: entity work.bistD port map (
18             d => d,
19             clk => clk,
20             r => r,
21             q => q,
22             qn=> qn
23         );
```

```
clk_gen: process
    begin
        clk <= '0';
        wait for 5 ns;
        clk <= '1';
        wait for 5 ns;
    end process;

stim: process
    begin
        -- Assert reset
        r <= '0';
        wait for 10 ns;
        r <= '1';
        wait for 10 ns;

        -- Toggle d every 10 ns
        d <= '0';
        wait for 10 ns;
        d <= '1';
        wait for 10 ns;
        d <= '0';
        wait for 10 ns;
```

```
    end process;

end Behavioral;
```

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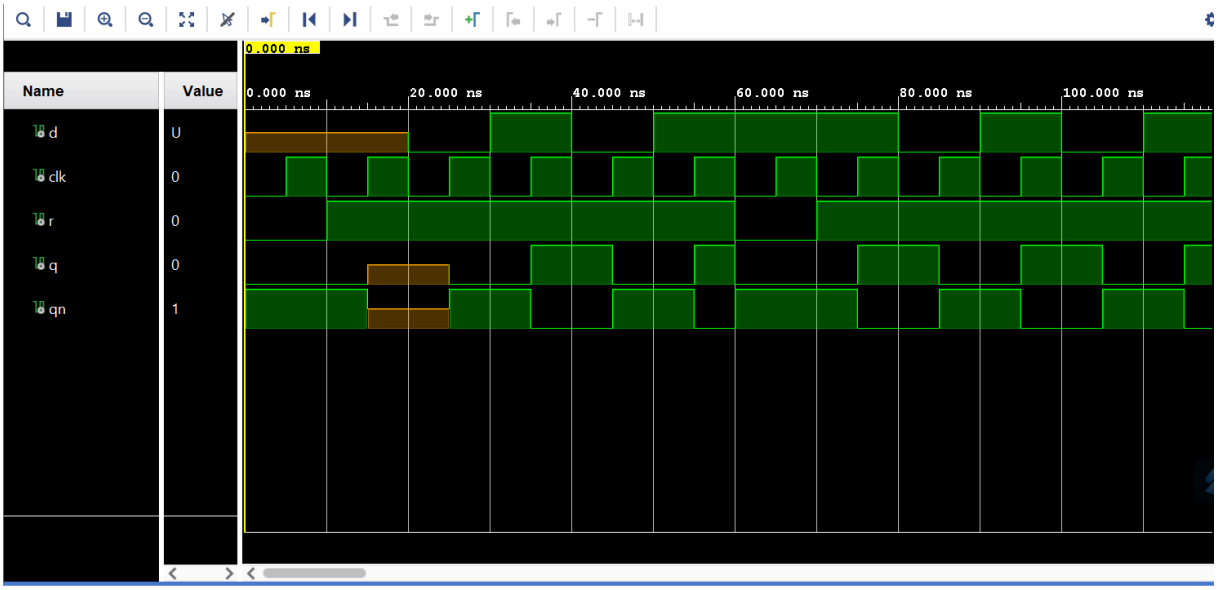
```
use IEEE.STD_LOGIC_1164.ALL;

entity bistD is
    Port ( d : in STD_LOGIC;
           clk : in STD_LOGIC;
           r : in STD_LOGIC;
           q : out STD_LOGIC;
           qn : out STD_LOGIC);
end bistD;

architecture Behavioral of bistD is

signal qint : std_logic;

begin

process(r, clk)
begin
    if r = '0' then
        qint <= '0';
    elsif rising_edge(clk) then
        qint <= d;
    else
```

```
    else
        qint <= qint;
    end if;
end process;

q <= qint;
qn <= not qint;

end Behavioral;
```

SIMULARE



PASUL 4:AUTOMAT + SIMULARE

C:/Users/gorga/OneDrive/Desktop/Gorgan_Raluca/Gorgan_Raluca/Gorgan_Raluca.srcs/sources_1/new/automat.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity automat is
5      Port ( clk : in STD_LOGIC;
6             r : in STD_LOGIC;
7             q : out STD_LOGIC_VECTOR (2 downto 0));
8  end automat;
9
10 architecture Behavioral of automat is
11
12     component bistD is
13         Port ( d : in STD_LOGIC;
14                clk : in STD_LOGIC;
15                r : in STD_LOGIC;
16                q : out STD_LOGIC;
17                qn : out STD_LOGIC);
18     end component bistD;
19
20     component mux4 is
21         Port (
22             i0, i1, i2, i3 : in  std_logic;
23             a1, a0         : in  std_logic;
```

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```
            y               : out std_logic
        );
    end component mux4;

    component mux2 is
        Port ( i0 : in STD_LOGIC;
               i1 : in STD_LOGIC;
               a : in STD_LOGIC;
               y : out STD_LOGIC);
    end component mux2;

    signal d0, d1, d2, net1, net2:std_logic;
    signal qint: std_logic_vector(2 downto 0);

begin

    q<=qint;

    B2: bistD port map(clk=>clk,
                r => r,
                d=>d2,
                q=>qint(2)
               );
```

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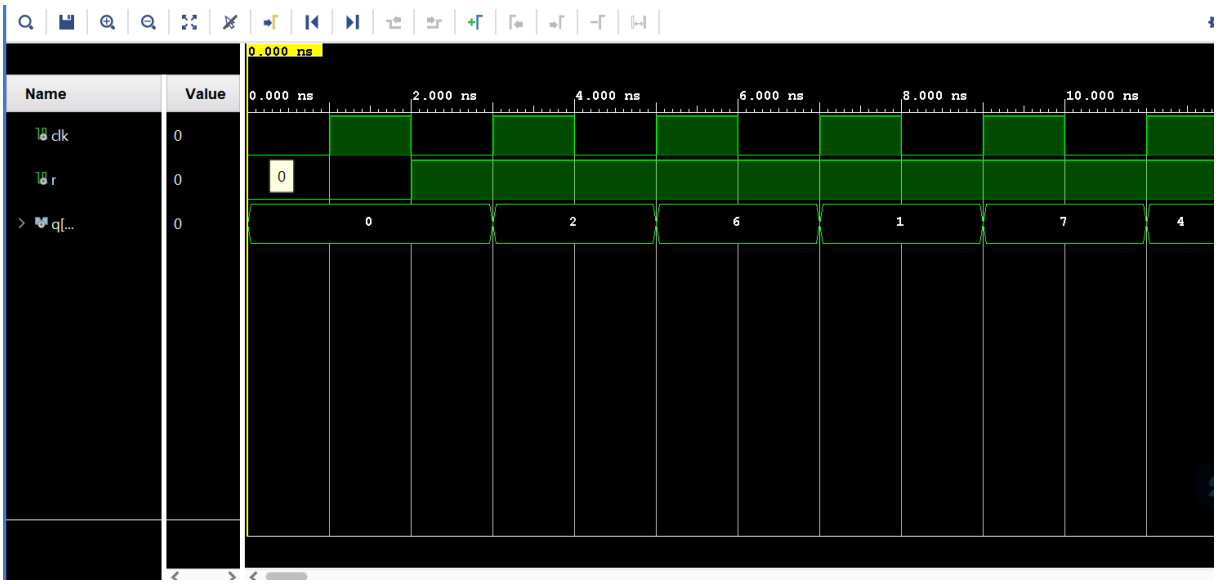
```
                q=>qint(2)
               );

    B1: bistD port map(clk=>clk,
                r => r,
                d=>d1,
                q=>qint(1)
               );

    B0: bistD port map(clk=>clk,
                r => r,
                d=>d0,
                q=>qint(0)
               );


    M2: mux2 port map (i0=> net1, i1=> qint(0), a=>qint(2), y=> d2);
    M21: mux4 port map (i0=> '0', i1=>'1', i2=> '1', i3=>'1', a1=> qint(1), a0=>qint(0), y=>net1);
    M1: mux2 port map (i0=> '1', i1=> '0', a=>qint(2), y=> d1);
    M0: mux2 port map (i0=> qint(0), i1=> net2, a=>qint(2), y=> d0);
    M01: mux4 port map (i0=> '0', i1=>'0', i2=> '1', i3=>'0', a1=> qint(1), a0=>qint(0), y=>net2);


end Behavioral;
```

C:/Users/gorga/OneDrive/Desktop/Gorgan_Raluca/Gorgan_Raluca/Gorgan_Raluca.srcs/sim_1/new/test.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity test is
5    -- Port ();
6  end test;
7
8  architecture Behavioral of test is
9
10   component automat is
11     Port (
12       clk : in  STD_LOGIC;
13       r   : in  STD_LOGIC;
14       q   : out STD_LOGIC_VECTOR (2 downto 0)
15     );
16   end component automat;
17
18   signal clk, r: std_logic;
19   signal q: std_logic_vector(2 downto 0);
20
21 begin
22
23   UUT: automat port map (clk, r, q);
```

```
23   UUT: automat port map (clk, r, q);
24
25   process
26
27   begin
28
29     clk <= '0';
30     wait for 1 ns;
31     clk <= '1';
32     wait for 1 ns;
33
34   end process;
35
36   r <= '0' after 0 ns, '1' after 2 ns;
37
38 end Behavioral;
```

SIMULARE


0.000 ns
Name
Value
clk
0
r
0
q[...
0
0.000 ns
2.000 ns
4.000 ns
6.000 ns
8.000 ns
10.000 ns
0
0
2
6
1
7
4