ECE546 Milestone-1 Report

Team Members-

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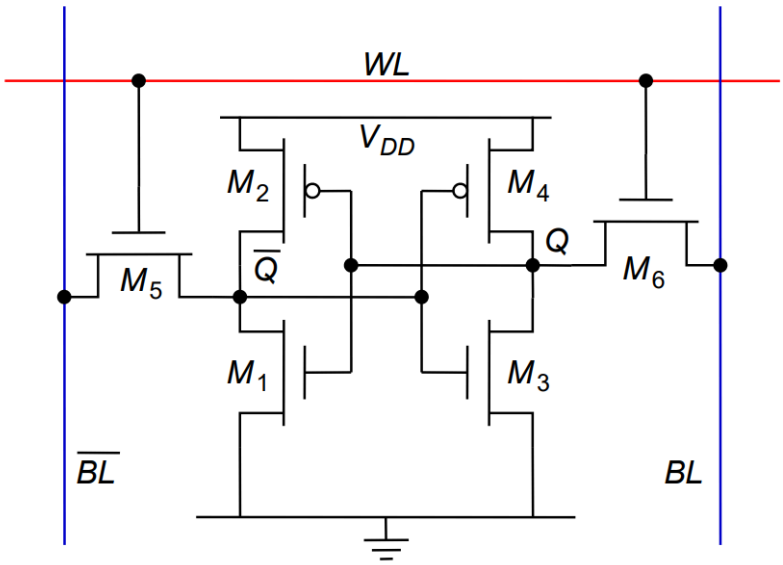
Introduction-

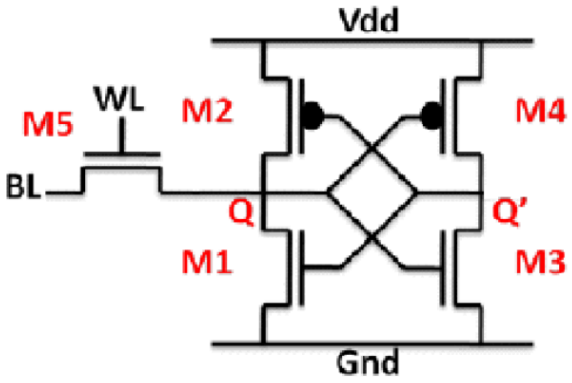
This project aims to build a 28 bit (32x4) Synchronous SRAM with the Inputs-Address(A<4:0>), Write data(D<3:0>), Write-Enable Bar(WENB- low indicates write) and Clock(CLK) and Outputs-Read data(Q<3:0>). The design is tested using a randomly generated set of values which are being stored and retrieved from the circuit. The Synchronous SRAM is being designed using 3nm technology. The project also focuses on developing a layout for the design. This layout is being tested using the same set of test vectors from the RC tree extracted from the layout.

Design options being considered-

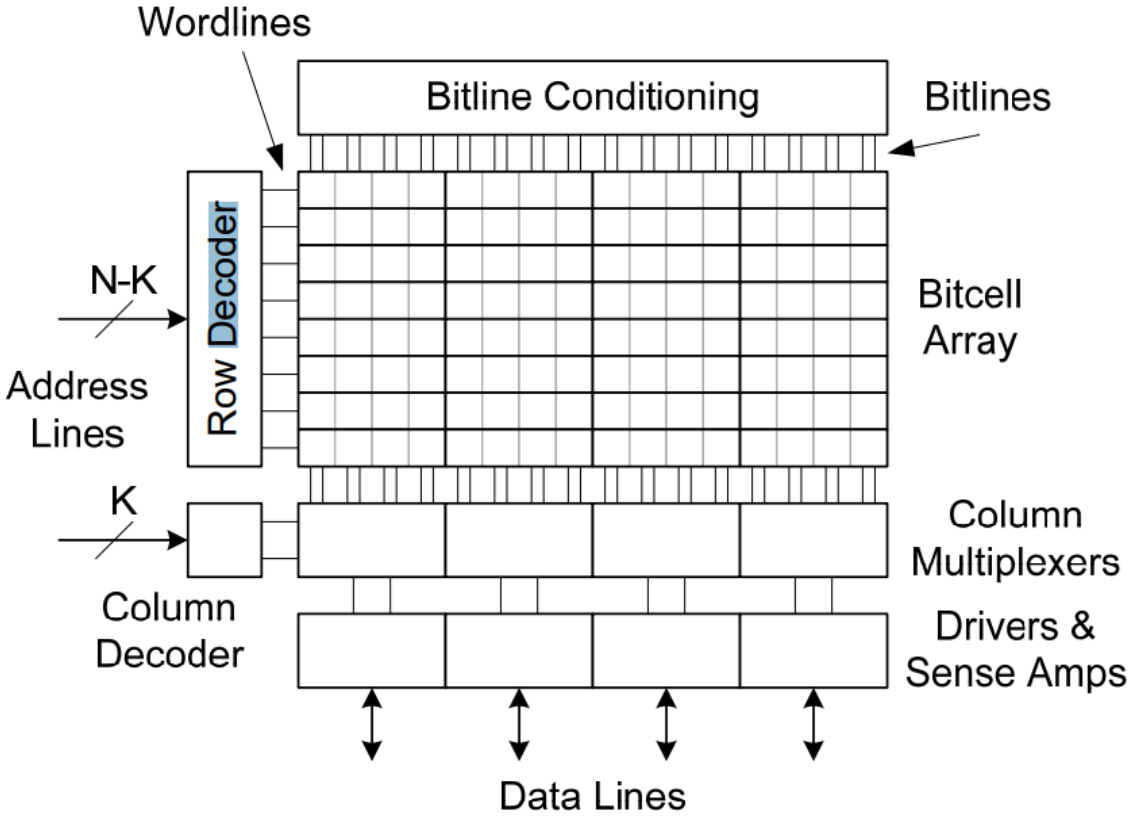
Bit-cells- 6-transistor CMOS SRAM Cell



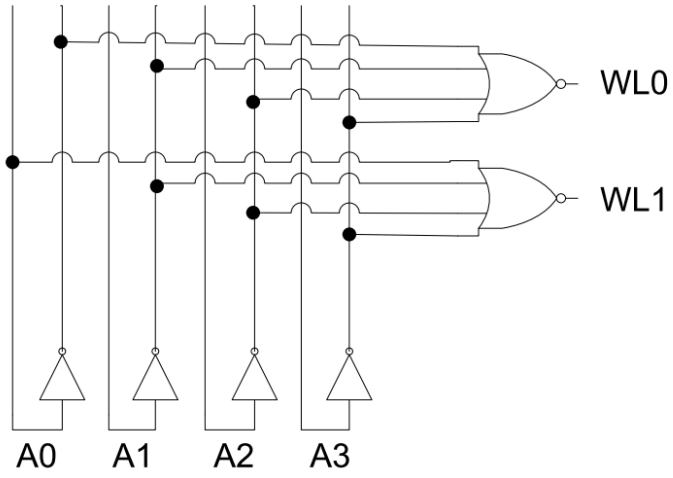
5-transistor CMOS SRAM Cell



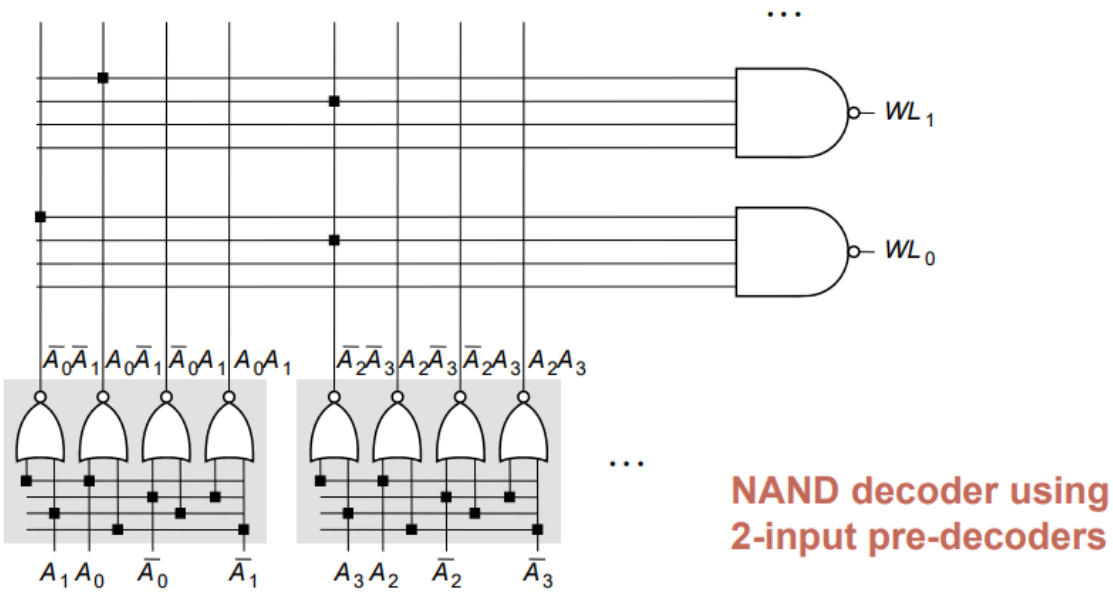
Architecture Overview-



Row Decoders-Traditional Decoder

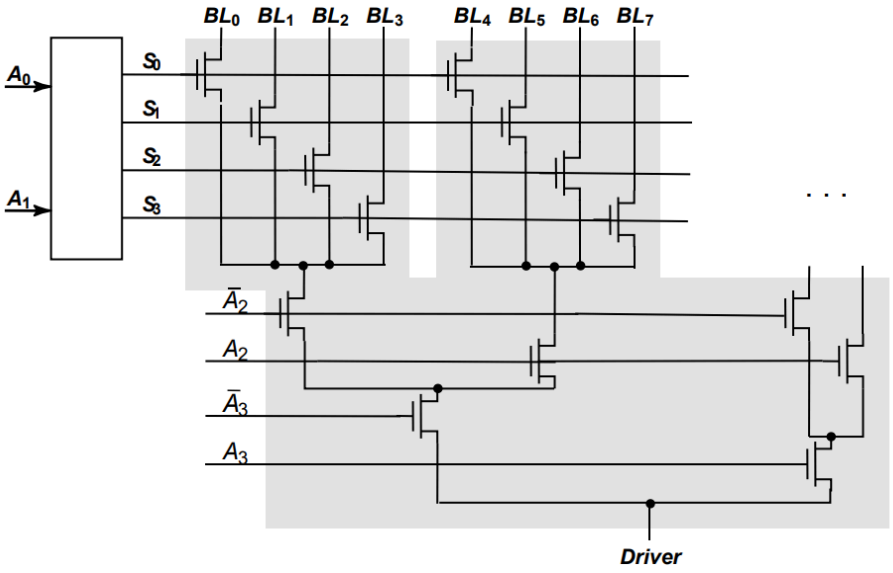


Row Decoders- Hierarchical Decoders



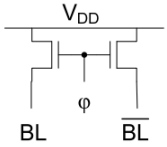
NAND decoder using
2-input pre-decoders

Column Decoder - Pre-decoded Column Decoder + Mux

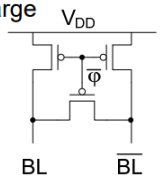


Bit-line Conditioning:

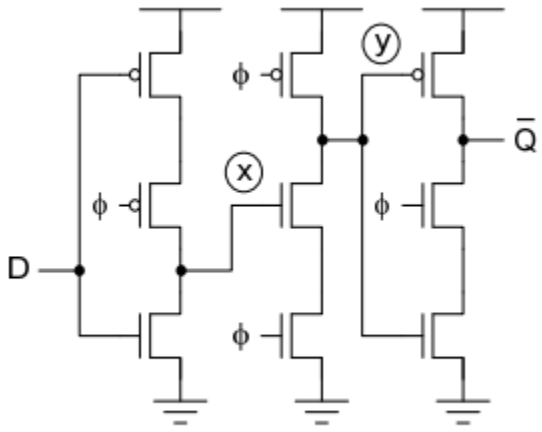
- NMOS
  - Faster sensing
  - Smaller noise margin



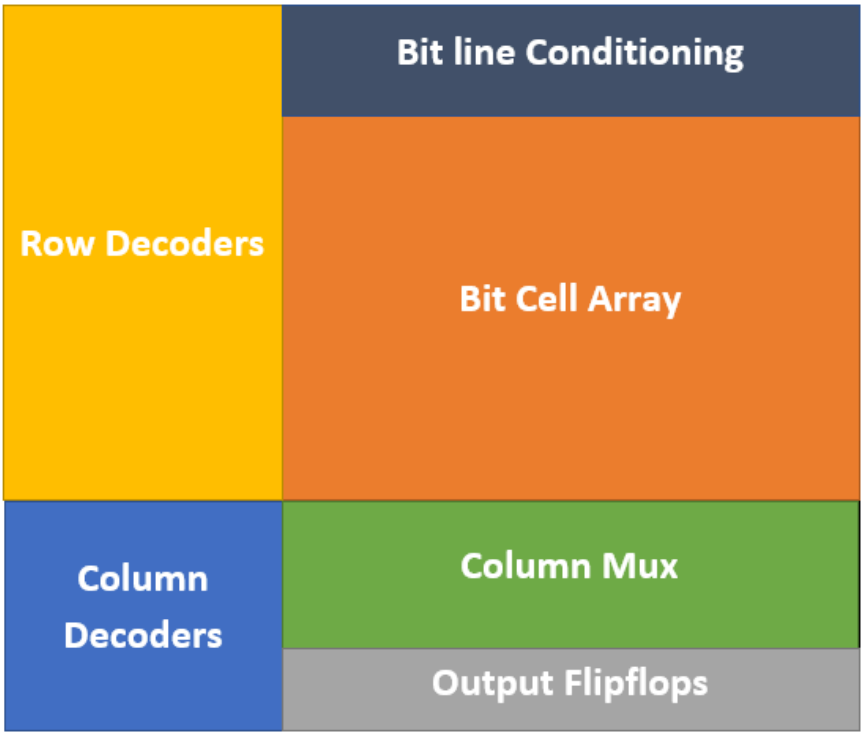
- Equalizer
  - Better noise margin
  - Fast precharge & sensing



Flip-flops: TSPC positive edge-triggered flip flop



Rough Floor Plan



Plan of work:

Major Tasks	**Assignment**
Bit Cell and Cell array design and testing.	Vaishnavi Avadhanam
Row Decoders design and testing.	Zachary Murray
Column Decoders and Flip Flop design and testing.	Ramachandran Sekanipuram Srikanthan

References:

1. Dachineni Bharath Satyanarayana, Kakarlapudi Pradeep, Tsr Prasad, T Ravi, 2012, A Proposed Five Transistor CMOS SRAM Cell For High Speed Applications, INTERNATIONAL JOURNAL OF ENGINEERING RESEARCH & TECHNOLOGY (IJERT) Volume 01, Issue 09 (November 2012),

2. Rabaey, Jan M. Digital Integrated Circuits: A Design Perspective. Prentice-Hall, 2003.