ECE 546 Final Report Group 7

16 Bit (4x4) SRAM

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Introduction

The design which we have presented is 16 bit (4X4) 2-port SRAM using 15nm technology. Our main focus is to optimize the design with respect to Energy*Delay*Area(EDA) product. In order to do this, we are using 6 transistor bit cell with 2 access transistors which will ensure that it will eliminate the read upset problem and will also ensure the value doesn't get flipped. Another advantage of using 6T bit-cell is less transistors which will help us to optimize the Area term in EDA product.

Design Description

SRAM

The block diagram for the SRAM is shown in Figure 1 and uses the basic components of an SRAM design. The bitcell array consists of 4 words that contain 4 bits each creating an overall 16 bit SRAM. This is ideal for the final layout as this provides a dense, square design.

BITCELL

The bitcell as described in the introduction is a 6 transistor bit cell with 2 access transistors as described in [1]. This cell is a 2 port read/write and write cell, however the read/write wordline is used only for writes. Apart from the access transistors, the transistors are of a 2-fin design to keep area down. While this leads to a higher resistance to a change during a write operation, the row decoder is properly sized to allow for correct operation. The access transistors are large at 10 fins to overpower the read bit conditioning when pulling the read bit line to ground. As the read bit condition is 4 fins, a 10 fin design can decrease charge quick enough to properly store the result.

ROW DECODER

The row decoder is of a simple static design with NAND gates and inverters. This provides a stable output and quick charging and discharging of word lines. There are two row decoders in the design, one for the read word line and one for the write word line.

FLIP-FLOP

The flip flop used in the design is a TSPC Positive Edge Triggered Flip Flop. This design is optimal from an operational point as the output of the register is inverted[2]. This is ideal as the read bitline from the bitcell is inverted. This reduces area as there is no need for an extra inverter. All transistors are 4 fins except for M7, which is 2 fins, to reduce output glitching. M4 and M1 are also 5 fins to help output.

READ BIT CONDITIONING

Read Bit Conditioning is of pseudo-nmos type to provide a reliable precharge. In order to make sure that the bitline could be discharged while the transistor was still on, we kept 4 fins for the conditioning so that the access transistors of the bitcell could overpower it

WRITE BIT CONDITIONING

Write Conditioning takes the data to be written and inverts it for the inverse bitline and connects it to a buffer for the other bitline to maintain the data. The outputs of the inverter and buffer are connected to 8 fin pmos transistors to enable quick writes when write enable is low.

RESULTS

The design was run at 0.8V with the clock period of 0.1 nanoseconds. The output waveforms are shown in Fig . We have measured total energy and got 1.109picoJoules. The total delay for our design is around 0.2 nanoseconds and the area is 70.15 square micrometers.

DIVISION OF LABOR

Craig Skvoretz	Flip flop and SRAM schematic and layout
Shreedhar Devendra Kolhe	Read and write bit conditioning schematic and layout. Bit cell schematic
Vaibhavi Nejkar	Row decoder schematic and layout Bit cell layout.

Table 1: Division of Labor

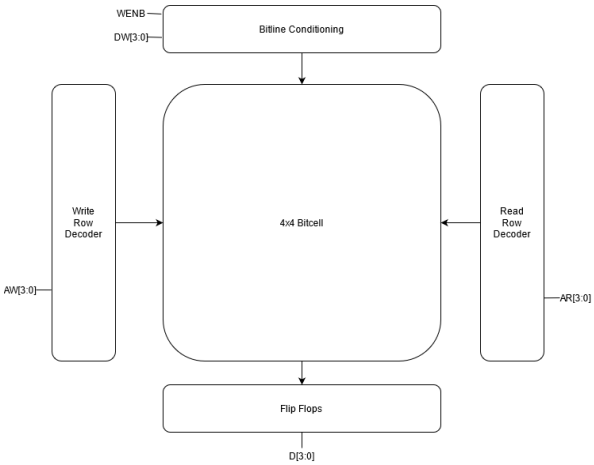

Figure 1: Block Diagram

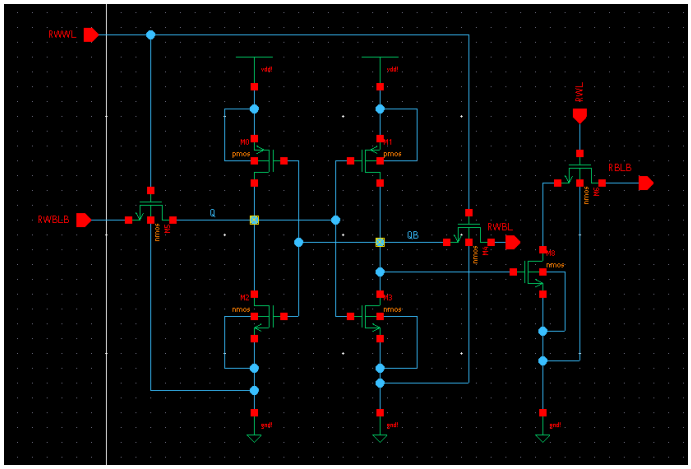

Figure 2: Bit Cell Schematic

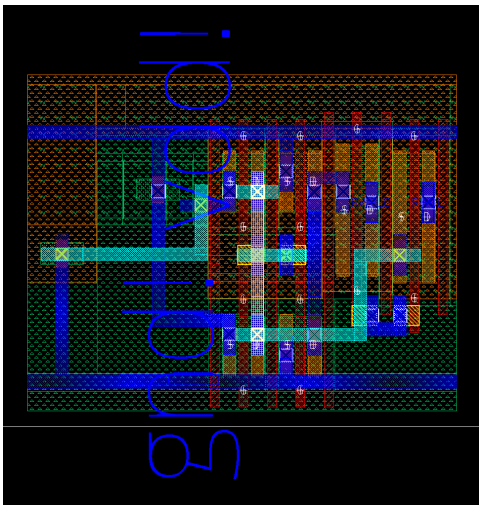

Figure 3: Flip Flop Layout

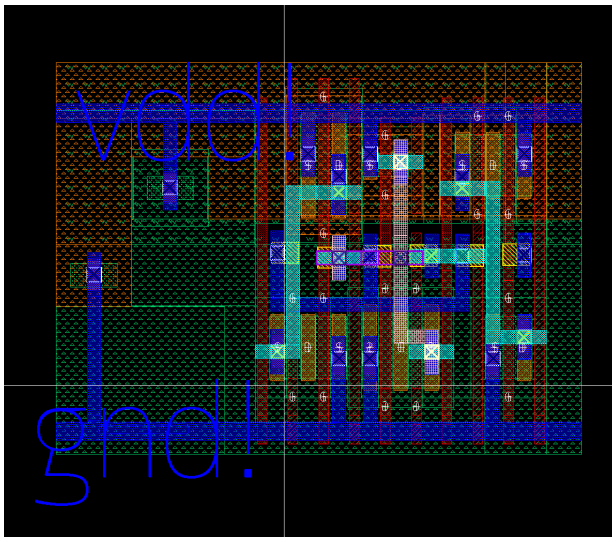

Figure 4: Bit Cell Layout

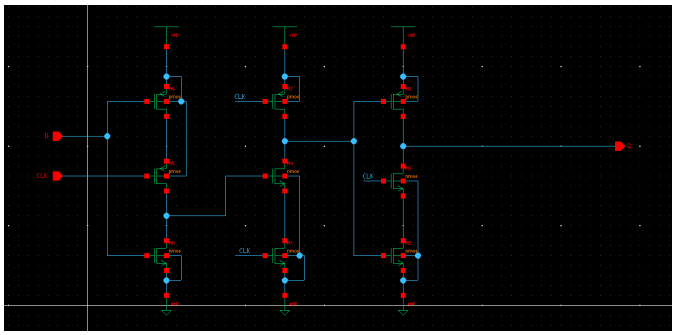

Figure 5: Flip Flop Schematic

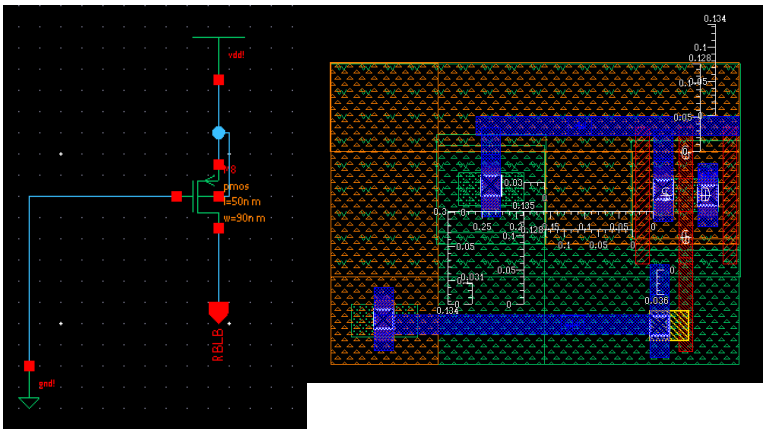

Figure 6: Read Bit Conditioning Schematic and Layout

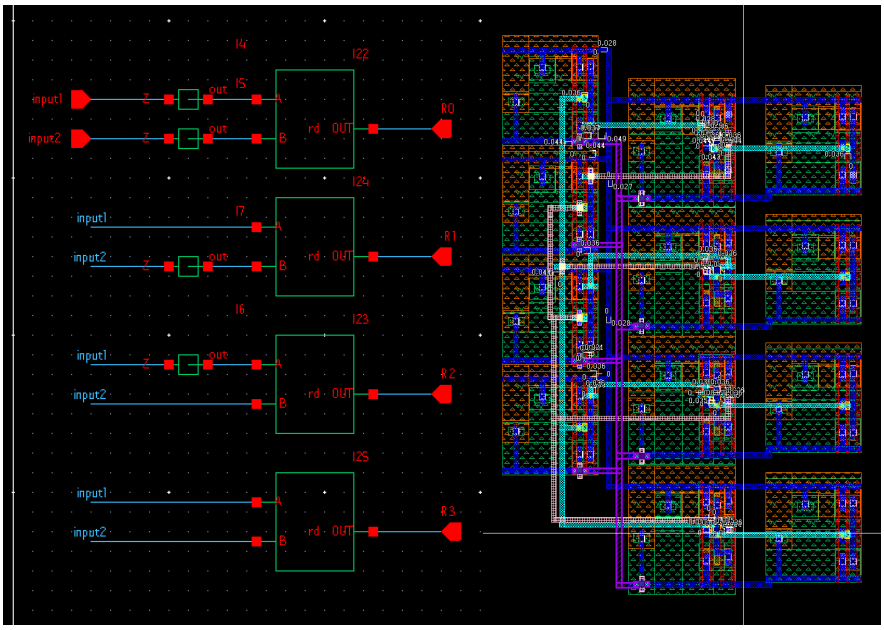

Figure 7: Row Decoder Schematic and Layout

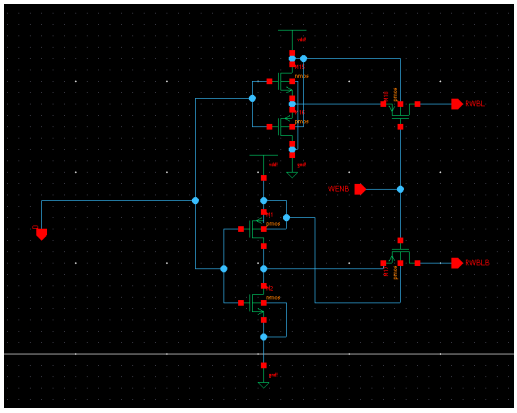

Figure 8: Write Bit Conditioning Schematic

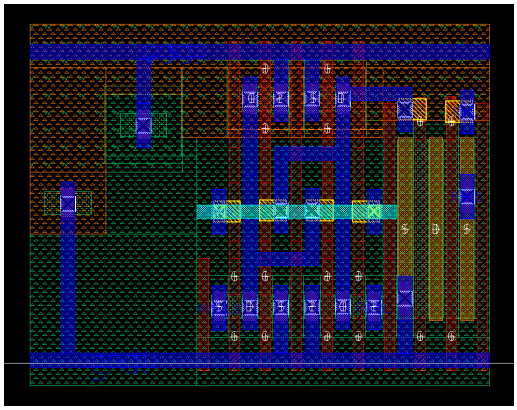

Figure 9: Write Bit Conditioning Layout

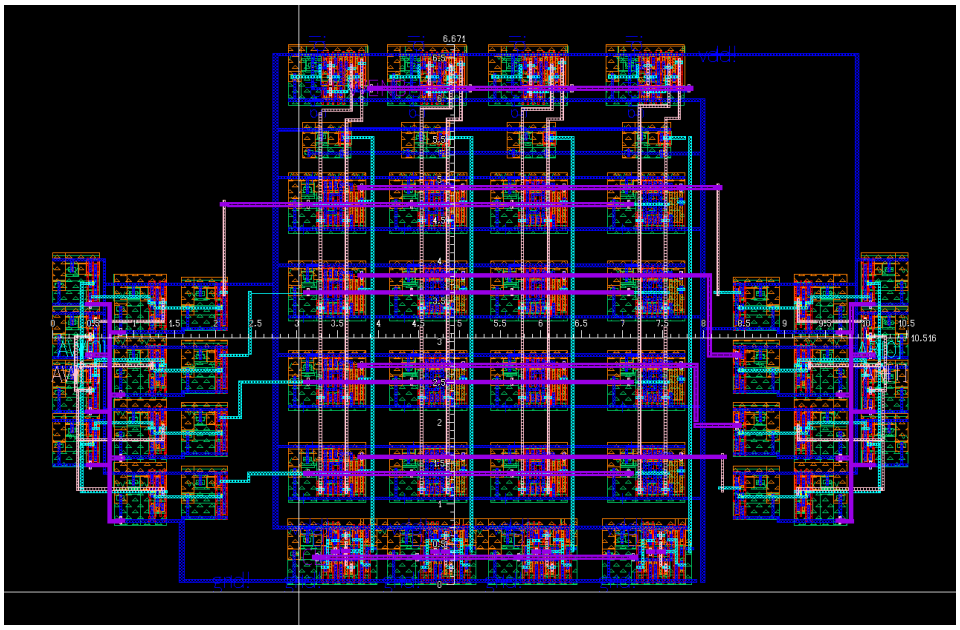

Figure 10: Overall SRAM Layout

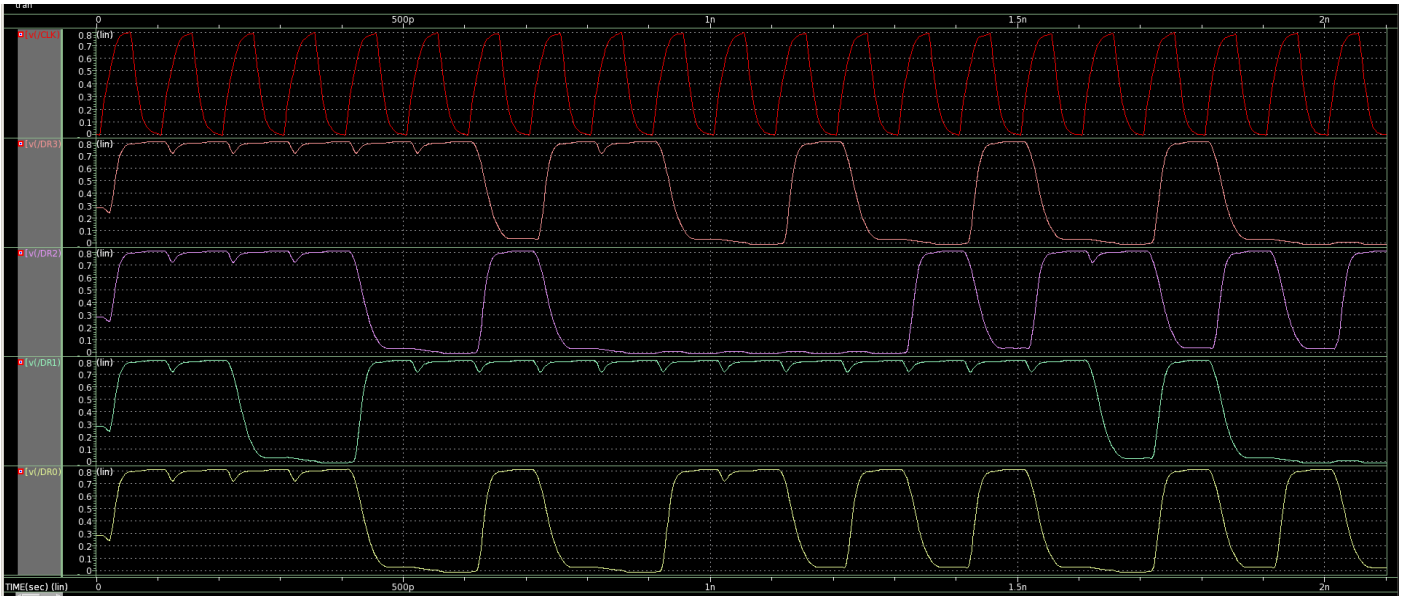

Figure 11: Output Waveforms

Min Clock Period	0.1ns
Supply Voltage	0.8 V
Total Energy	1.109 pJ
Total Transistors	256
Area	70.15 um^2
Transistors per Area	3.65 transistors/um^2
Design Time	75 hours

Table 2: Design Statistics

REFERENCES

[1] Class Notes “ECE 546” , Dr. W.R. Davis
[2] Digital Integrated Circuits: A Design Perspective: Rabaey, Chandrakasan, and Nikolic