```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE IEEE.numeric_std.all;

entity Instruction_Memory is
port (
 pc: in std_logic_vector(31 downto 0);
 instruction: out  std_logic_vector(31 downto 0)
);
end Instruction_Memory;

architecture Behavioral of Instruction_Memory is

 type ROM_type is array (0 to 63 ) of std_logic_vector(31 downto
0);

constant rom_data: ROM_type:=(
   "00010001100010010000000000010101",
      "00000000000000000000000000000000",
   "10001101011011000000000000000000",
   "10001101011011010000000000000001",
      --"00000000000000000000000000000000",
      "00000000000000000000000000000000",
      "00000000000000000000000000000000",
      "00000000000000000000000000000000",
   "00000101100011010111000000100000",
      "00000000000000000000000000000000",
      "00000000000000000000000000000000",
      "00000000000000000000000000000000",
      "00000000000000000000000000000000",
   "10101101011011100000000000000001",
   "00000101100000010110000000100000",
      "00000000000000000000000000000000",
      "00000000000000000000000000000000",
      "00000000000000000000000000000000",
      "00000000000000000000000000000000",
   "10101101011011000000000000000000",
   "00000100000000000000000000011111",
   "00000000000000000000000000000000",
   "00000000000000000000000000000000",
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   "00000000000000000000000000000000",
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   "00000000000000000000000000000000",
   "00000000000000000000000000000000",
   "00000000000000000000000000000000",
   "00000000000000000000000000000000"
  );
begin
  instruction <= rom_data(to_integer(unsigned(pc(5 downto 0))))
when pc < x"00000029" else x"00000000";

end Behavioral;
```