## Paper Reading List

1. Samajdar, A., Joseph, J. M., Zhu, Y., Whatmough, P., Mattina, M., & Krishna, T. (2020, August). A systematic methodology for characterizing scalability of dnn accelerators using scale-sim. In 2020 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) (pp. 58-68). IEEE.

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Link: https://ieeexplore.ieee.org/abstract/document/9238602

2. Venkataramani, S., Srinivasan, V., Wang, W., Sen, S., Zhang, J., Agrawal, A., ... & Gopalakrishnan, K. (2021, June). RaPiD: Al accelerator for ultra-low precision training and inference. In 2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA) (pp. 153-166). IEEE

Authors: Swagath Venkataramani, Vijayalakshmi Srinivasan, Wei Wang, Sanchari Sen, Jintao Zhang, Ankur Agrawal

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3. Zhang, H., Ning, A., Prabhakar, R. B., & Wentzlaff, D. (2024, June). LLMCompass: Enabling Efficient Hardware Design for Large Language Model Inference. In 2024 ACM/IEEE 51st Annual International Symposium on Computer Architecture (ISCA) (pp. 1080-1096). IEEE.

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4. Kothari, G., & Ghose, K. (2023, October). Thermally-Aware Multi-Core Chiplet Stacking. In 2023 IEEE/ACM International Conference on Computer Aided Design (ICCAD) (pp. 1-9). IEEE.

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Venue: 2015 IEEE Trustcom/BigDataSE/ISPA

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Link: <a href="https://ieeexplore.ieee.org/abstract/document/7345265">https://ieeexplore.ieee.org/abstract/document/7345265</a>

6. **[Demo Paper]** Luo, H., Tu, Y. C., Bostancı, F. N., Olgun, A., Ya, A. G., & Mutlu, O. (2023). Ramulator 2.0: A Modern, Modular, and Extensible DRAM Simulator. IEEE Computer Architecture Letters.

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