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FIFO

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Introduction to FIFO

What , Why and How?

What is FIFO?

- First In First Out
- Queue based data structure where the first item placeed into the queue is the one that is removed first.
- Used especially in data management, data buffering, Clock Domain Crossing
- Crucial for both hardware and software systems

Why FIFO is important in VLSI?

- Buffering data
- Timing synchronization
- Flow control
- Ensuring Data Integrity
- Prevention of Data Overrun and Underrun
- System efficiency
- Pipelining and Staging
- Error Handling and Recovery

FIFO In VLSI Design

- **Purpose:** In VLSI design, FIFO is critical for transferring data between components like processors, memory blocks, and I/O interfaces. It ensures that data is not lost during high-speed data transmission or when there are different timing constraints between components.

- **Applications in VLSI:**
  - ***High Speed Data Transfer*** → Communication interfaces, network processors
  - ***Buffering between clock domains*** →cross clock domain data transfer(Asynchronous FIFO)
  - ***Streaming data Applications*** →Video processing, audio streaming, sensor data processing
  - ***Efficient memory Utilization*** → by circularly allocating memory space
  - ***Prevents overflow and underflow*** → by generating full flag and empty flag
  - ***Design Flexibility***

Types of FIFO

- **Synchronous FIFO:**
  - Single clock pulse for both data read and write i.e., read and write operations are performed at same rate
  - Depth/Words : Number of rows
  - Width/ Word Length : Number of bits in each row

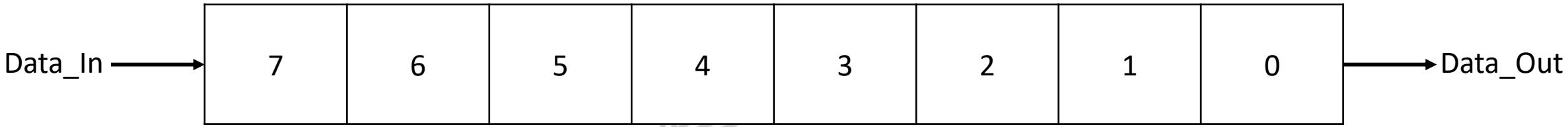
- **Asynchronous FIFO:**
  - Data values are written to and read from the same FIFO at different rates but at the same time.
  - Used to synchronize data flow between the systems.
  - Used to pass the data from one clock domain to another clock domain.

Flags in FIFO

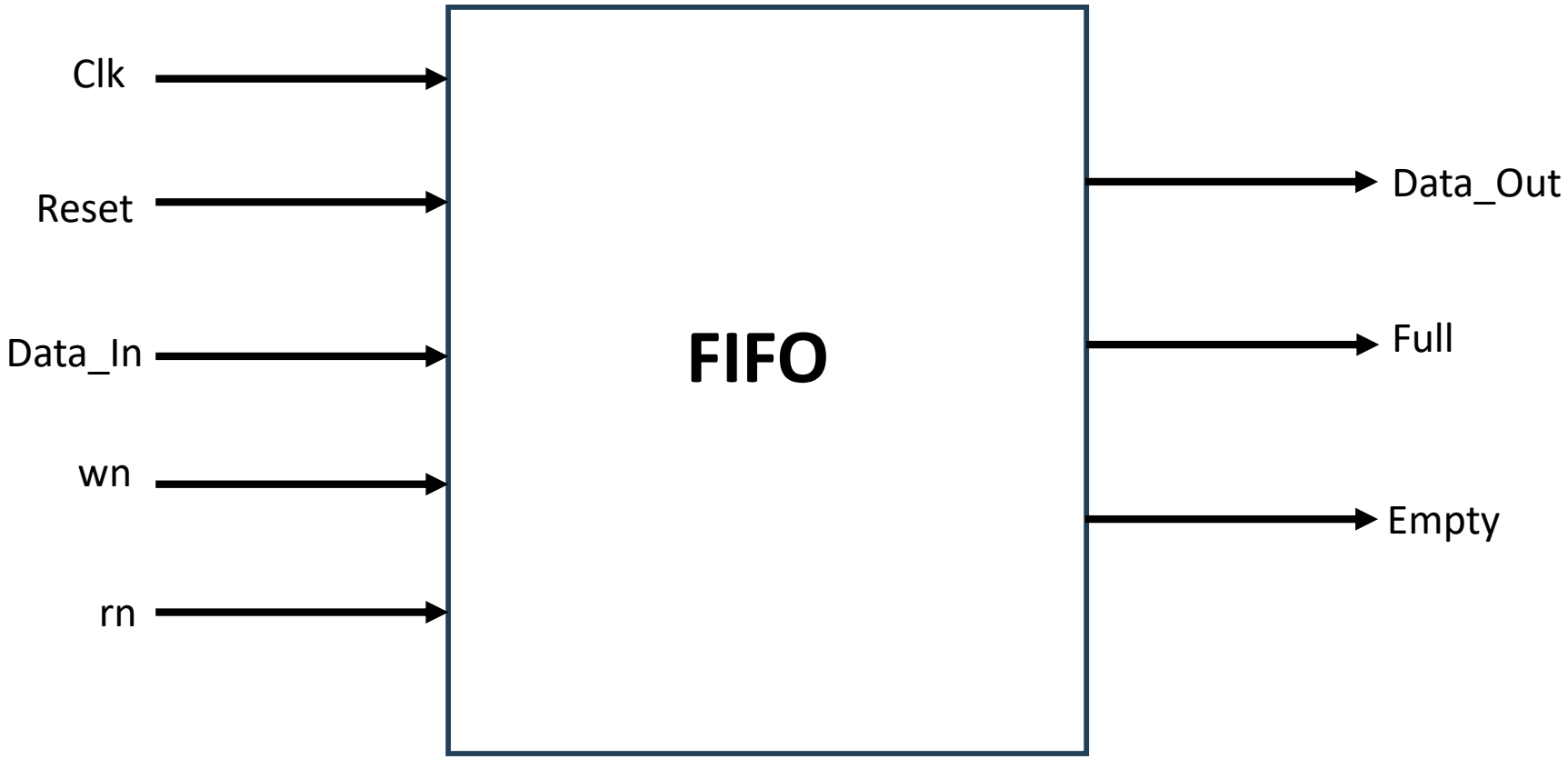
- **EMPTY FLAG:**
  - Empty flag is set when the FIFO is already empty and there is a request for a read operation.

- **FULL FLAG:**
  - Full flag is set when the FIFO is already full and there is a request for a write operation.

FIFO Architecture



FIFO Architecture



References

1. "FPGA Prototyping with Verilog examples" by Pong P. Chu
2. “Digital Logic Design Using Verilog” by Vaibhav Taraate


Thank You