RAMAIAH
SKILL ACADEMY

SERIAL PERIPHERAL INTERFACE

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Introduction to SPI

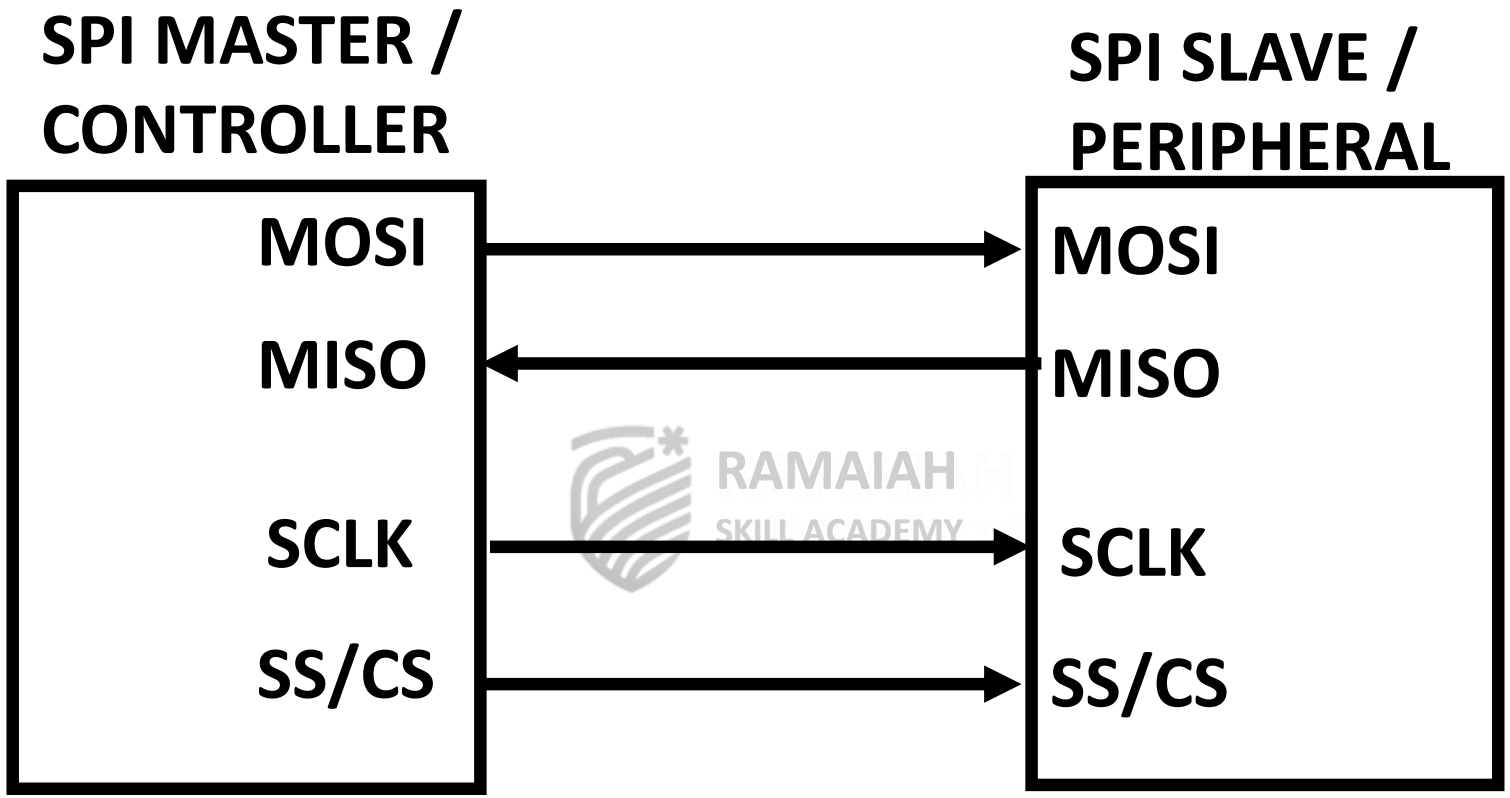
- SPI is a Serial Bus communication Protocol developed by Motorola in late 1980s
- It is a Synchronous, Full Duplex protocol and most used protocol for short distance communication
- Used in microcontrollers, sensors, EEPROMS, ADCs, DACs etc
- Has a simple hardware interface
- Provides high-speed data transfer
- Supports single or multiple slave devices but has only one master that controls all communications

Basic SPI Architecture

- **Master-Slave Configuration**
  - One master controls the communication
  - One or more slaves respond to the master

- **There are Four main signals:**
  - ***MOSI (Master Out Slave In)*** → used for sending data from Master to Slave
  - ***MISO (Master In Slave Out)*** → used for sending data from Slave to Master
  - ***SCLK (Serial Clock)*** → used to clock the signal
  - ***SS/CS (Slave Select / Chip Select)*** → used by master to send the data by selecting a particular slave. It is used when there are multiple slaves in the design

Basic SPI Architecture



Working Principle

→Clock Synchronization: where Master generates the clock SCLK

- All data transfers are synchronized to this clock.
- Data Shifts occur on clock edges determined by SPI mode.

→Data Transfer

- Master sends data to the slave vis MOSI
- Slave responds with data via MISO
- Transfer happens in full duplex mode i.e., simultaneous read and write operations

→Chip Selection

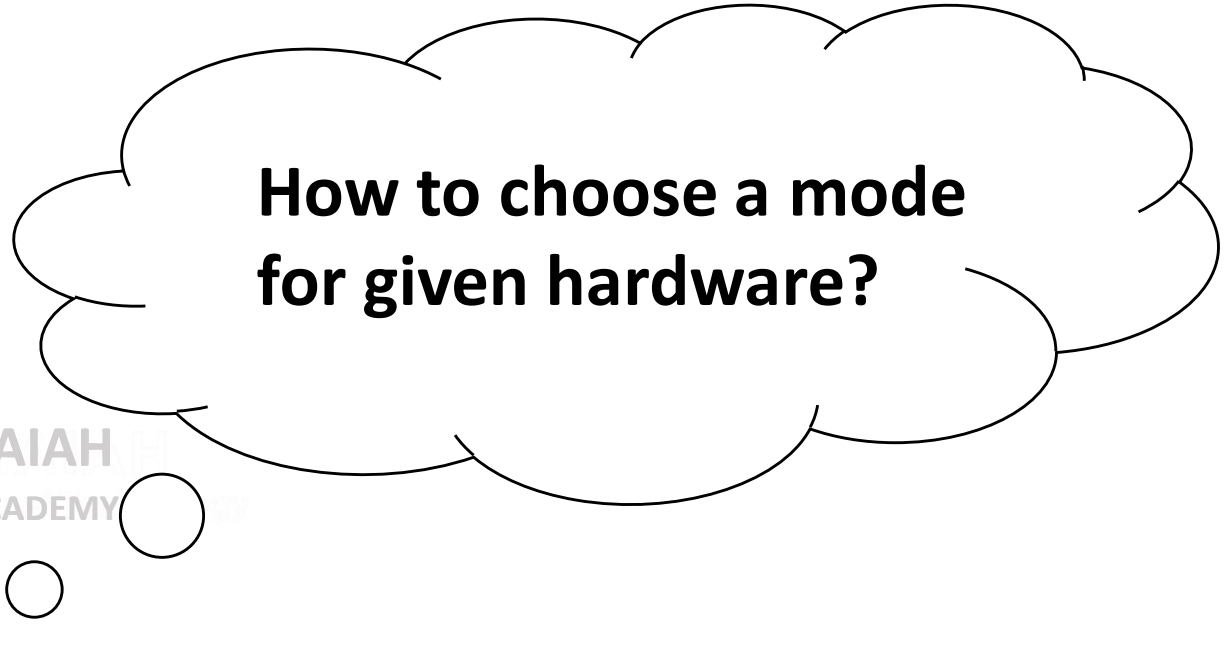
- SS is driven low to select a slave
- If a particular slave is not selected, it remains inactive and ignores SCLK and MOSI.

→Data Frame

- SPI uses a shift register based data frame
- Data is typically transferred as 8 bits at a time but it can be extended

SPI Modes (Clock Polarity and Phase)

- Mode 0 :
  →CPOL = 0, CPHA = 0
  →Data is sampled on rising edge
- Mode 1 :
  →CPOL = 0, CPHA = 1
  →Data is sampled on falling edge
- Mode 2 :
  →CPOL = 1, CPHA = 0
  →Data is sampled on falling edge
- Mode 3 :
  →CPOL = 1, CPHA = 1
  →Data is sampled on rising edge



Timing Diagram

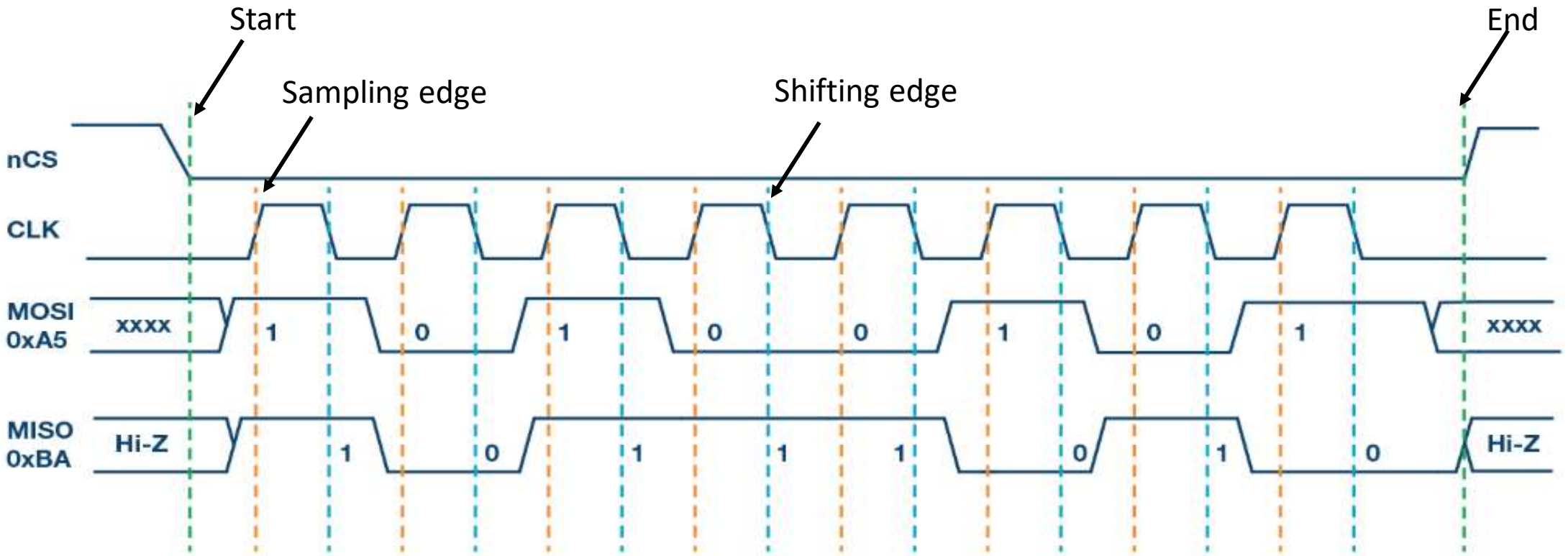


Figure 2. SPI Mode 0, CPOL = 0, CPHA = 0: CLK idle state = low, data sampled on rising edge and shifted on falling edge.

Reference: www.analog.com

Timing Diagram

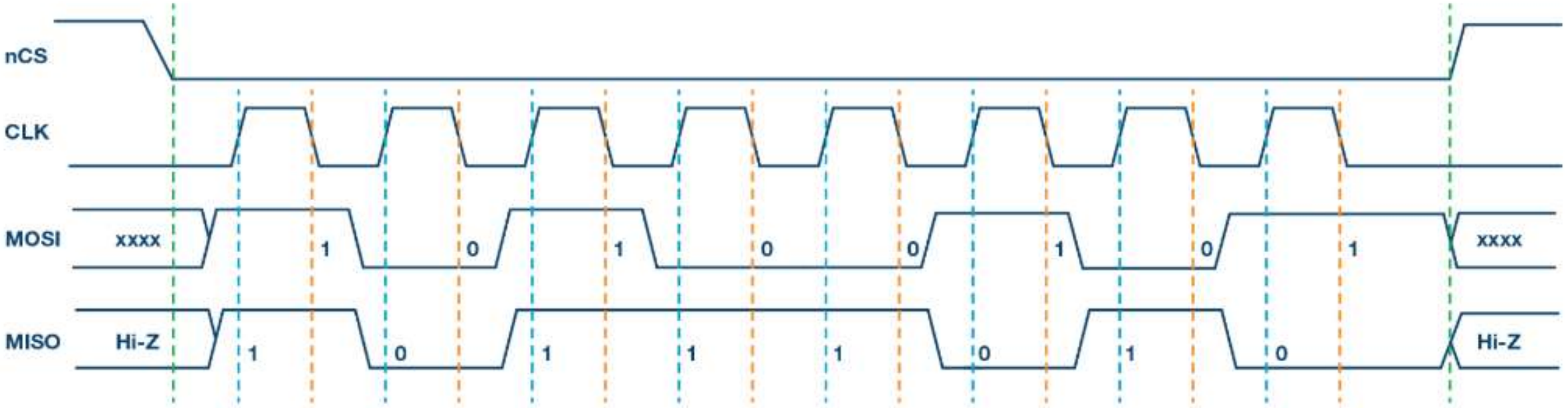


Figure 3. SPI Mode 1, CPOL = 0, CPHA = 1: CLK idle state = low, data sampled on the falling edge and shifted on the rising edge.

Reference: www.analog.com

Timing Diagram

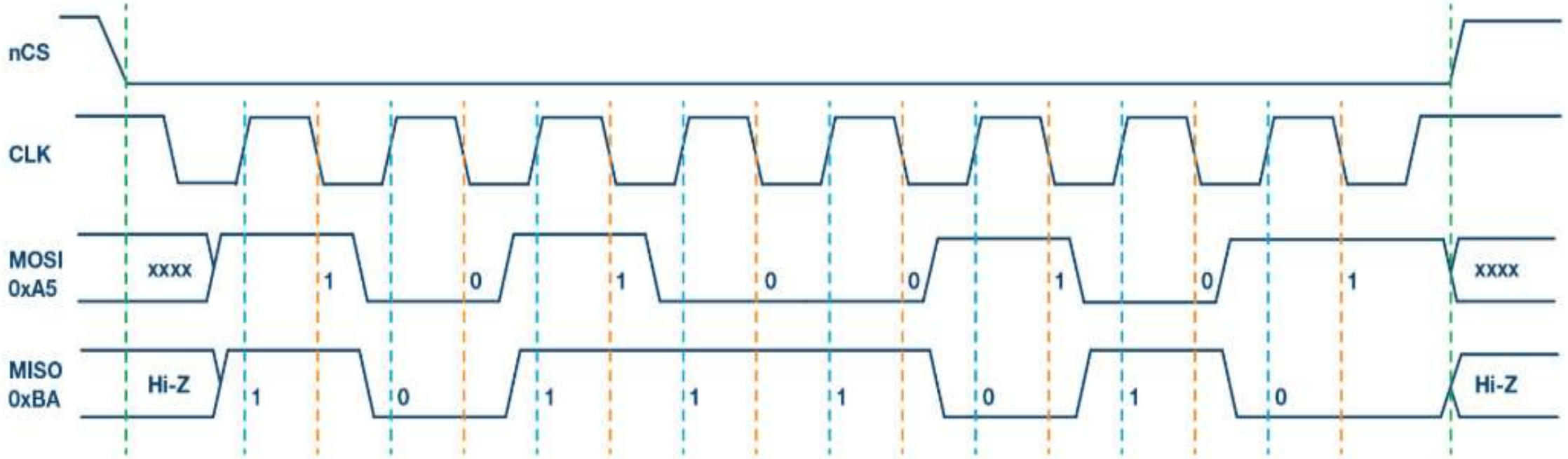


Figure 4. SPI Mode 2, CPOL = 1, CPHA = 0: CLK idle state = high, data sampled on the falling edge and shifted on the rising edge.

Reference: www.analog.com

Timing Diagram

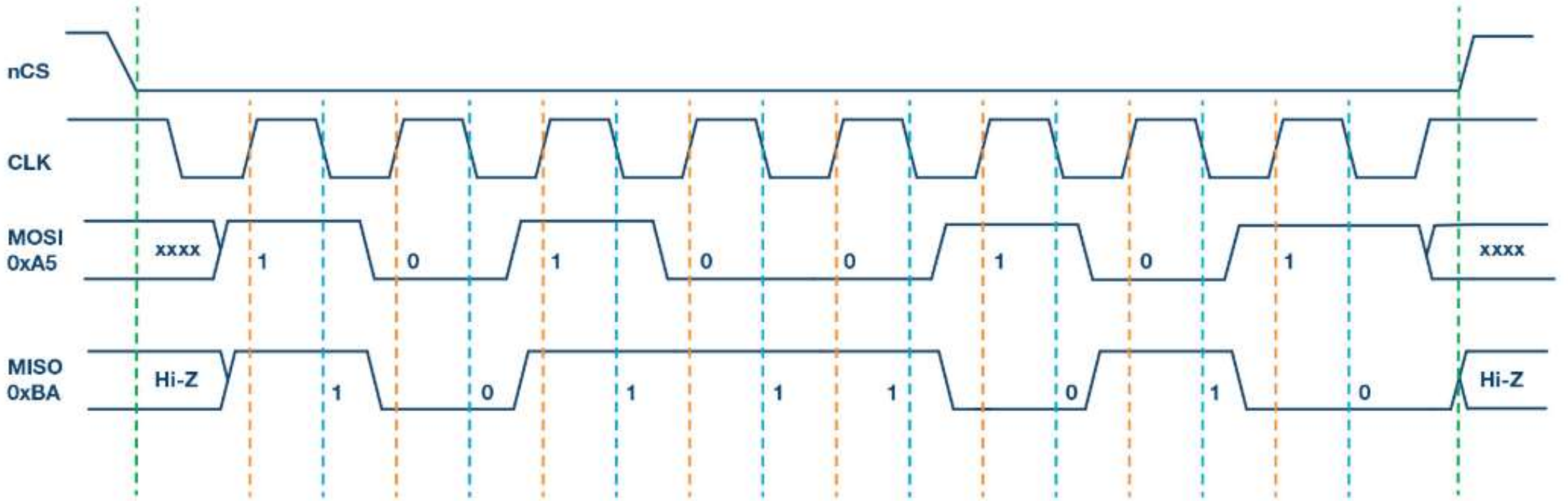


Figure 5. SPI Mode 3, CPOL = 1, CPHA = 1: CLK idle state = high, data sampled on the rising edge and shifted on the falling edge.

Reference: www.analog.com

Advantages of SPI

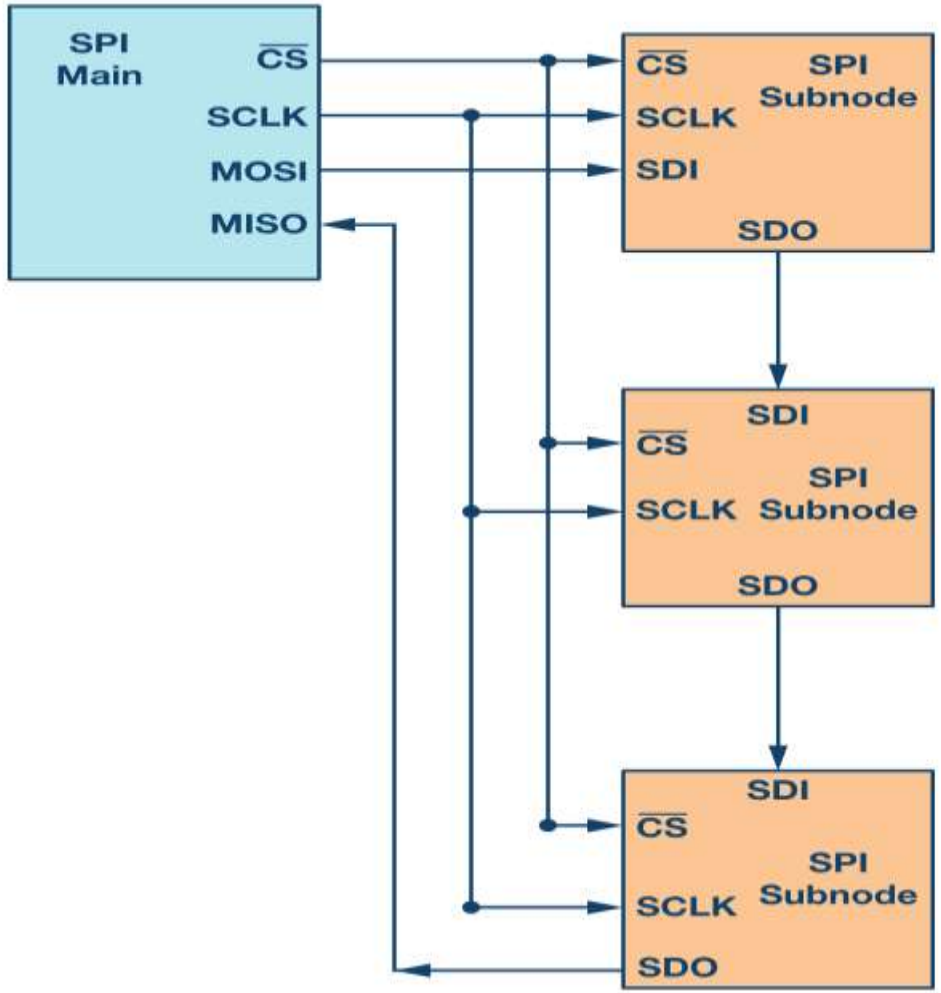
- High speed data transfer
- Simple Implementation
- Full-duplex communication
- Low power consumption
- Easy to daisy-chain multiple devices

Limitations of SPI

- No formal standard
- Limited to short distances
- Requires more pins than I2C
- Only one master at a time
- Handling multiple slaves requires extra control logic

Multi-Slave Configuration

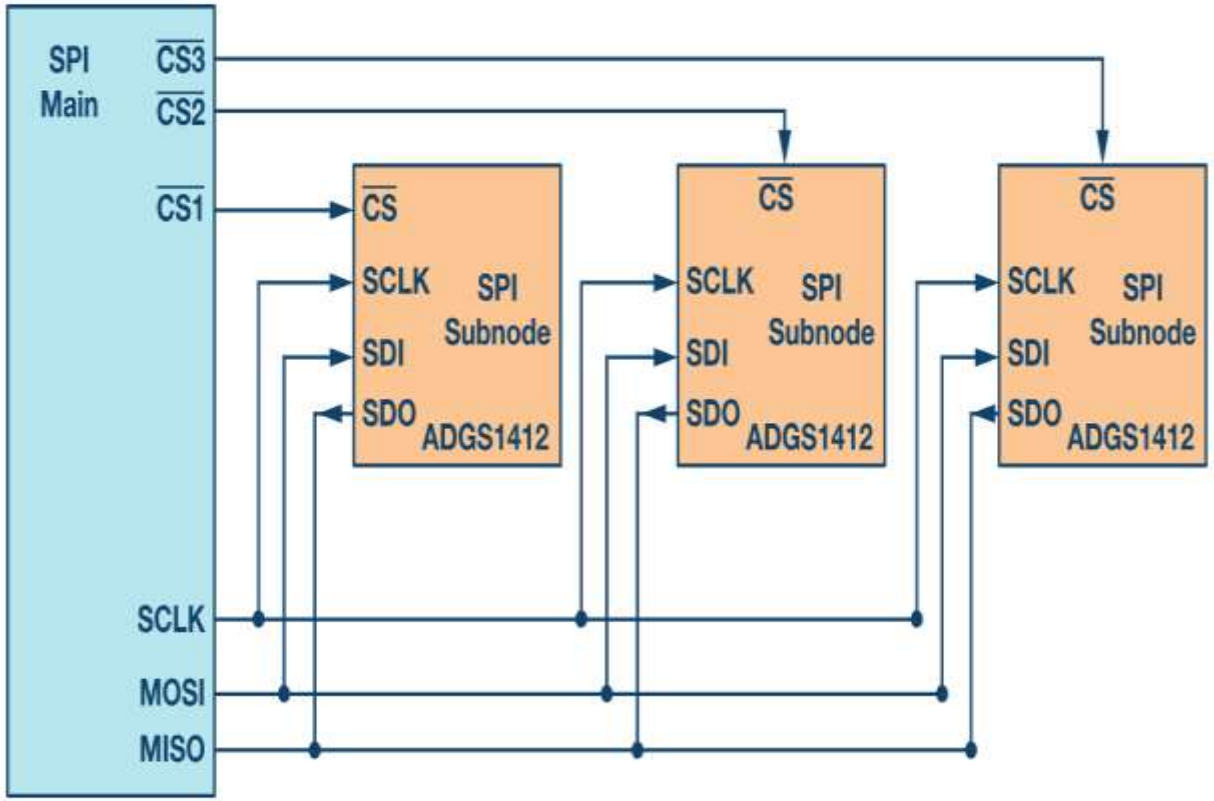
- Daisy-Chain:
  - Single data line for all slaves
  - Advantages:
    - Reduces number of SS lines
    - Simple hardware connections
  - Disadvantages:
    - Slower due to cascading delays
    - Single point of failure



Reference: www.analog.com

Multi-Slave Configuration

- Individual SS Lines:
  - Each slave has a dedicated SS line
  - Advantages:
    - Faster Communication
    - Better Fault Isolation
  - Disadvantages:
    - Requires more GPIO pins
    - Complex hardware wiring for large systems



Comparison with other Protocols

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Feature	SPI	I2C	UART	CAN
Speed	High	Moderate	Moderate	Low
Number of Wires	4 (min)	2	2	2
Full Duplex	Yes	No	No	No
Master-Slave	Single Master, Multi-Slave	Multi-Master, Multi-Slave	Point-to-Point	Multi-Master, Multi-Slave
Addressing	No	Yes	No	Yes
Robustness	Low	Medium	Medium	High
Range	Short	Short-Medium	Medium	Long

Applications

- Consumer Electronics:
  - SD Cards, Touch screens
- Industrial:
  - Sensors, Actuators
- Automotive:
  - ECU communication

Assignment

- Design an SPI module in Verilog that includes both spi_master and spi_slave functionalities.
  - Implement 8-bit data transfer with support for all four SPI modes (CPOL, CPHA).
  - Ensure the master generates the clock (SCLK) and the slave communicates based on the Slave Select (SS) signal.
  - Write a testbench to verify full-duplex communication for a given sequence of data bytes and validate correct operation through simulation waveforms.
  - Explain how your design would handle scenarios where the clock speed of the SPI master is higher than the capability of the slave.

References

1. "Serial Communication Protocols: Principles and Applications" by Robert J. Anderson, Wiley, 2020.

2. "Microcontroller Systems: Advanced Design Techniques" by John H. Davies, Elsevier, 2019.