RAMAIAH
SKILL ACADEMY

LIBRARIES

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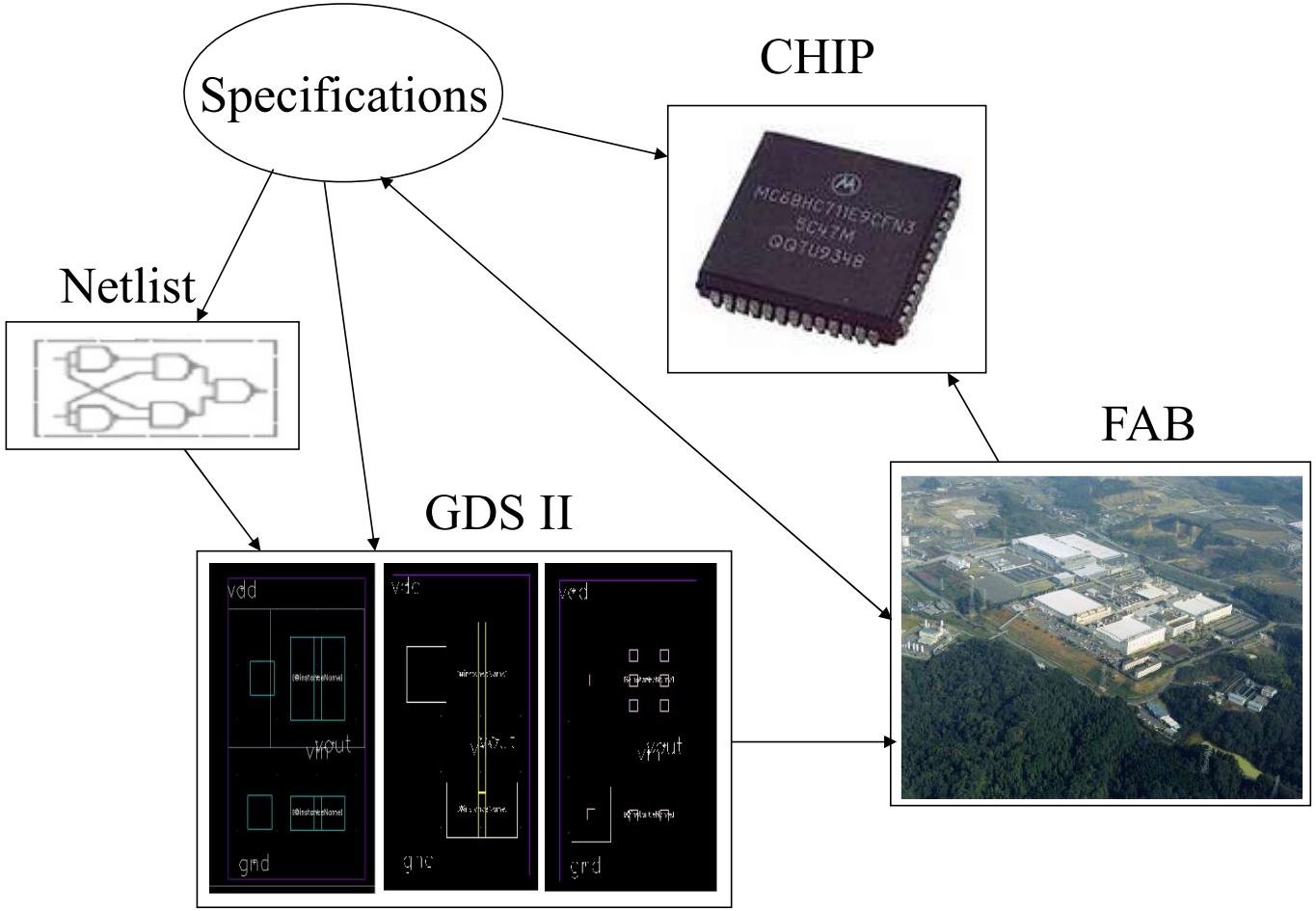
Foundry



Kinds of Libraries

- Physical libraries
  - Standard Cell
  - IO
- Memory Libraries
    - RAM / ROM
- Analog Libraries
  - PLL
  - VCO
  - ADC / DAC
- IP Libraries
  - DesignWare

Kinds of Libraries

- Logical Libraries
  - Contains logic synthesis relevant information such as area, timing, power, functionality of
    - Standard Cells
    - IOs
- Simulation Libraries
  - Contains timing and functional information for post synthesis simulation in different formats such as
    - VITAL
    - Verilog Model
- Symbol Libraries
  - Used to view the schematics of generated netlists

Logic Libraries / Technology Libraries

- Provided by fabrication house
- Is a collection of standard cells with their logical synthesis relevant information
- No physical information present in these libraries
- Generally a compilation of information extracted after the development of standard cell/IO layouts
- Typically in the “.lib” format
  - .lib : logic library
  - .plib : physical library
  - .slib : schematic library
  - .sldb : synthetic library
  - .v : verilog model file

Technology Libraries

- Libraries consist broadly of 3 parts
  - Standard Cells
  - Environmental Variables
  - Library Level Attributes
    - Specifies default units of various parameters such as time, power, capacitance, resistance, current
    - Constant through out the library
    - Used while calculating delays and specifying constraints
    - Example

```
library (tsmc28nm) {
technology (cmos);
delay_model          : table_lookup ;
date                 : “Feb 29,2000” ;
Revision             : “1.17” ;
current_unit         : “1µA” ;
time_unit            : “1 ns” ;
voltage_unit         : “1V” ;
```

Environment description

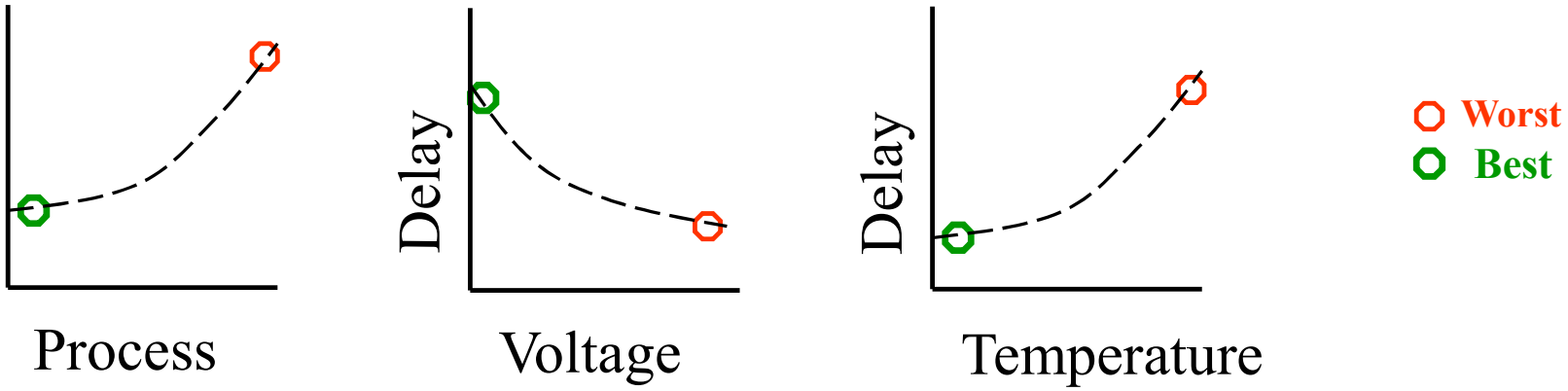
- Attributes defined in the library to model the variations in the environment
- Library is characterized for a particular environment
  - Known as Operating Conditions
  - Consist of 3 parameters PVT
    - Process : Signifies the manufacturing process.
      Depends on doping concentration, oxide thickness, device length etc
    - Voltage : Signifies the Voltage at which chip is expected to work
    - Temperature : Signifies the working temperature
- Typically three kinds of Operating Condition exist
  - Min, Max, Typical
  - Also known as best case, worst case and nominal

Environment description

- Sets of operating conditions defined in the library specify the process, temperature, voltage and the RC tree model
- These are used during synthesis and timing analysis of the design
- Library developers may define any number of operating conditions in the library
- A library is characterized using one set of operating conditions
- During synthesis or timing analysis if another set of operating conditions are specified then K factors are used to derate the delay values

$$d_{NEW} = d_{NOMINAL} * (1 + \delta_P * K_P) * (1 + \delta_V * K_V) * (1 + \delta_T * K_T)$$

PVT



- Process varies around 1
- Voltage variation depends on technology being used
- Temperature varies normally between 0 – 125^0c

PVT

operating_conditions (WORST) {
process : 1.3 ;
temperature: 100.0 ;
voltage: 2.75 ;}

operating_conditions (NOMINAL) {
process : 1.0 ;
temperature: 25.0 ;
voltage : 3.00 ;}

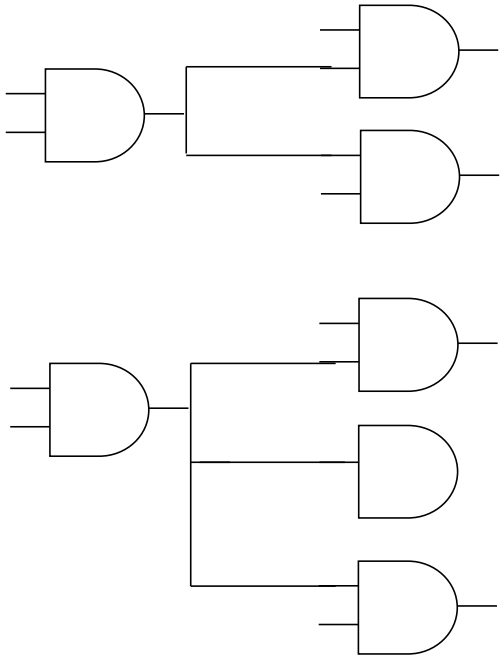
operating_conditions (BEST) {
process : 0.7 ;
temperature: 0.0 ;
voltage: 3.25 ;}

Wire delays

- Synthesis results in a netlist to meet certain specifications
- Netlist is a collection of cells AND wires
- Almost accurate delays of cells are available from the libraries
- Interconnect lengths are unknown at the pre-placement stage
- Wire delays constitute a substantial part of the total delay in a circuit
- With no exact means of knowing the wire lengths a estimate needs to be done
- Interconnect delays can be extracted from comparative study of similar designs which are already fabricated
- Available as WLM in the library
- The only means of estimating wire delays in the pre-placement stage

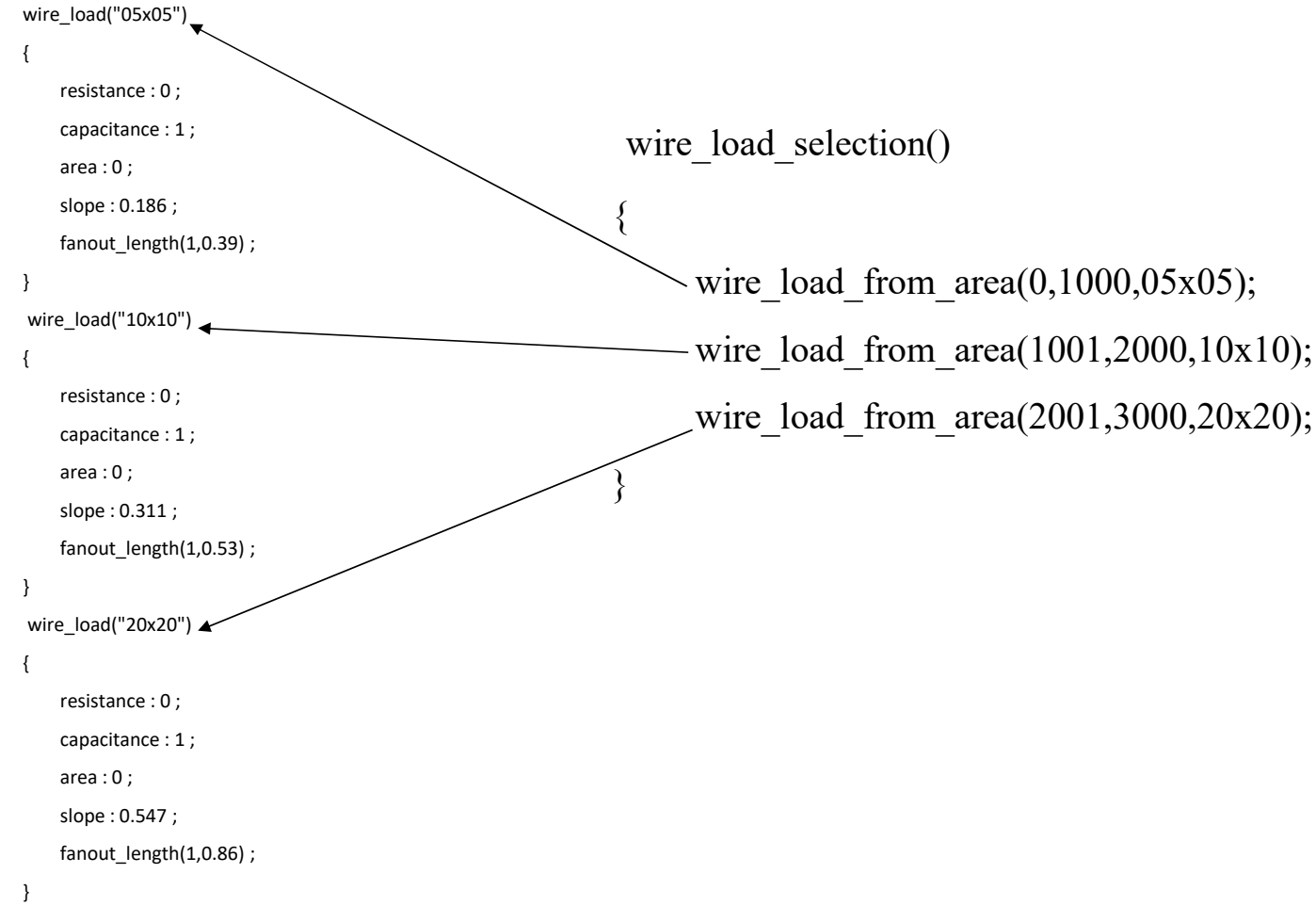
Wire load models

- Many WLM available in a library for various design areas
- They define area, capacitance & resistance of interconnects

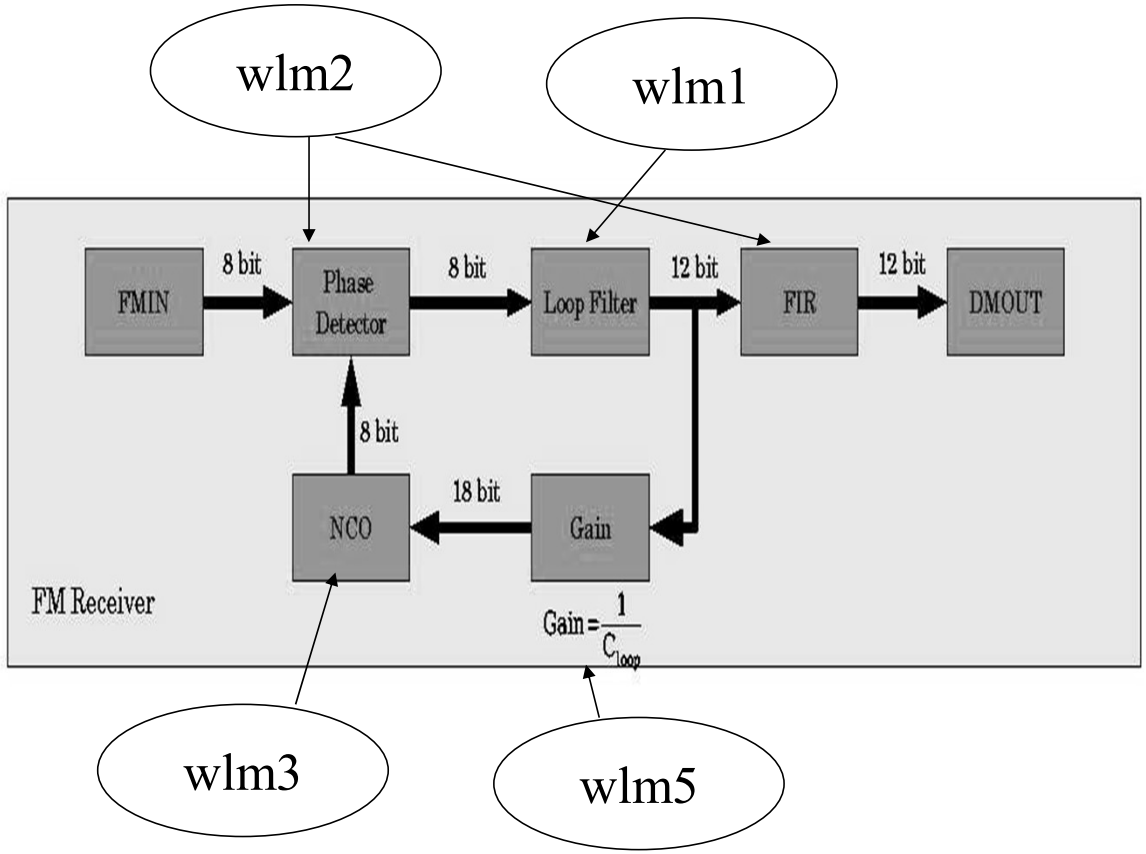


- Two nets having same length can have different delays
- Delay does not depend on only length of net
- Length of net depends on other factors

Wire load models



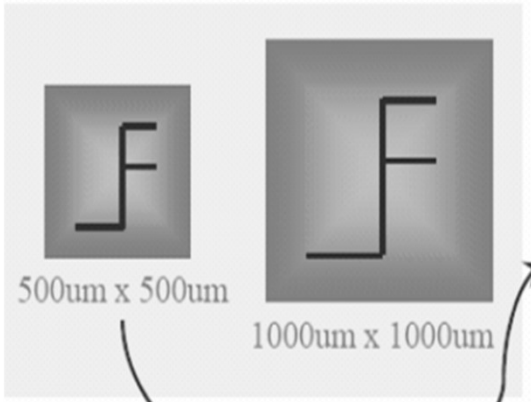
Wire load models



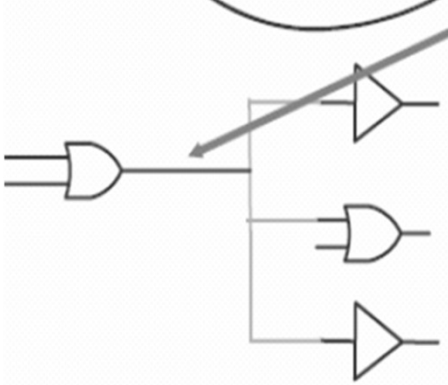
Sub - Blocks	Area(sq micron)
FM Core	2250
Loop Filter	250
NCO	800
Phase Detector	600
FIR	500

```
wire_load_selection()
  {
     wire_load_from_area(0,250,wlm1);
     wire_load_from_area(251,600,wlm2);
     wire_load_from_area(601,1000,wlm3);
     wire_load_from_area(1001,1600,wlm4);
     wire_load_from_area(1601,2400,wlm5);
  }
```

Wire delay calculation




```
wire_load ("500") (
resistance : 3.0          /* R per unit length*/
capacitance: 1.3          /* C per unit length */
area: 0.04                /* area per unit length */
slop: 0.15                /* extrapolation slope*/
fanout_length ( 1 , 2.1 ) /* fanout-length pairs */
fanout_length ( 2 , 2.5)
fanout_length ( 3 , 2.8)
fanout_length ( 4 , 3.3)
```



C_{wire} = (fanout=3, length =2.8) x capacitance coefficient (1.3) = 3.64 load units

R_{wire} = (fanout=3, length =2.8) x resistance coefficient (3.0) = 8.4 resistance units

$Area_{Net}$ = (fanout=3, length =2.8) x area coefficient (0.04) = 0.112 net area units

Standard Cells

- Assortment of cells exist in a library
  - and , nand, nor, or, exor, xnor, ff, latch
  - Complex cells such as : aor, aoi, oai
- For each particular kind of cell there exists variety of types
  - diverse 2 input ‘and’ gates with various drive strengths
- Cells with balanced rise and fall
  - especially inverters and buffers
- Synchronous / asynchronous, positive edge / negative edge triggered Flip-flops
  - Single or multiple outputs available with each flip-flop

Standard Cells

- The logic synthesis relevant information of cells such as
  - area
  - power
  - pin capacitance
  - functionality
    - Either in terms of boolean equation or state table
  - timing info

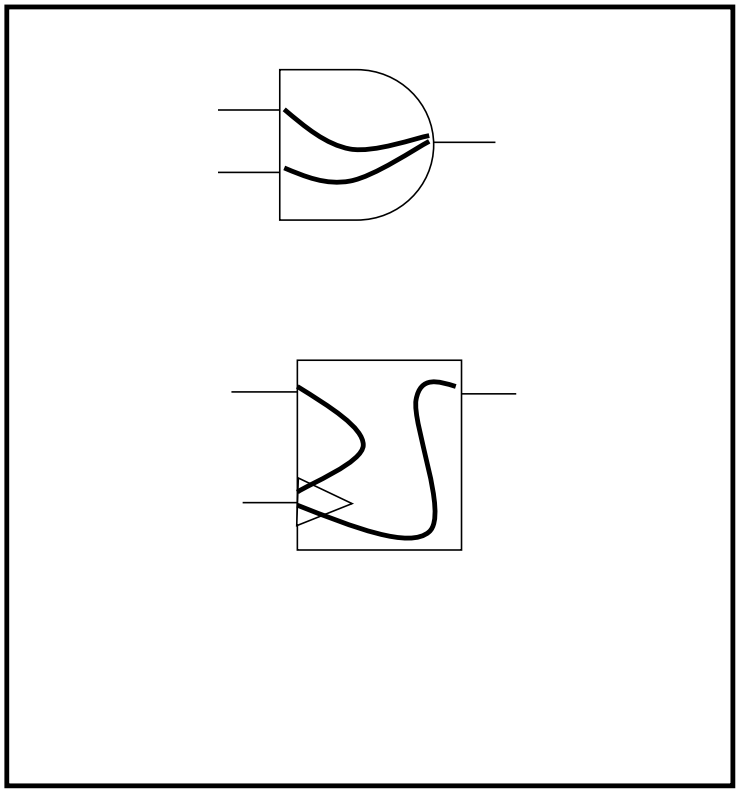
Propagation Delay

- Propagation delay is constituted of 3 parts
  - Intrinsic Delay
    - The delay through the element independent of the load
  - Slope Delay
    - The delay incurred from input pin to output pin due to transition time of the input pin
  - Transition Delay
    - The delay due to capacitive loading at the output pin
- Total Delay = $D_{Intrinsic} + D_{Slope} + D_{Transition}$

Timing Sense

- Timing Sense specifies how an input transition affects the output
  - Positive Unate :
    - A rising / falling transition at the input leads to a rising / falling transition at the output
  - Negative Unate :
    - A rising / falling transition at the input leads to a falling / rising transition at the output
  - Non Unate :
    - The output transition can not be determined from the input transition

Timing Arcs



- Pin-Pin timing information of
  - Combination logic
    - Input - output
  - Flip-Flops
    - Input – Clock
    - Clock – Output