RAMAIAH
SKILL ACADEMY

Low Power and UPF

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Why Low Power

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- Battery

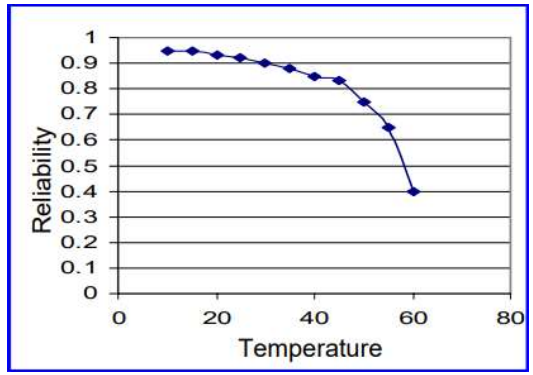
- Packaging

- ~1W : inexpensive plastic package
- ~10 W : Ceramic Package
- ~10W / cm2 : convection cooling
- ~50 W / cm2 : forced air cooling

  - Data from Pentium days

- Cooling

- Reliability



- Environment

Why Low Power

- 2 Billion mobile phones can be charged with 100 Mega Watts
- Equivalent to 2 large wind-farms

- 1 Billion PCs being on for 9 hours per day require 95000 Mega Watts
- Equivalent to ~100 coal-fired power stations

Necessary

- Consumer Needs
  - More Features
  - Longer Battery life
    - Battery Technology not catching up
- How to address
  - Software management
    - Manage different states efficiently
  - Architecture and IP
  - Libraries
  - EDA Software
  - Power supply management
  - Process technology

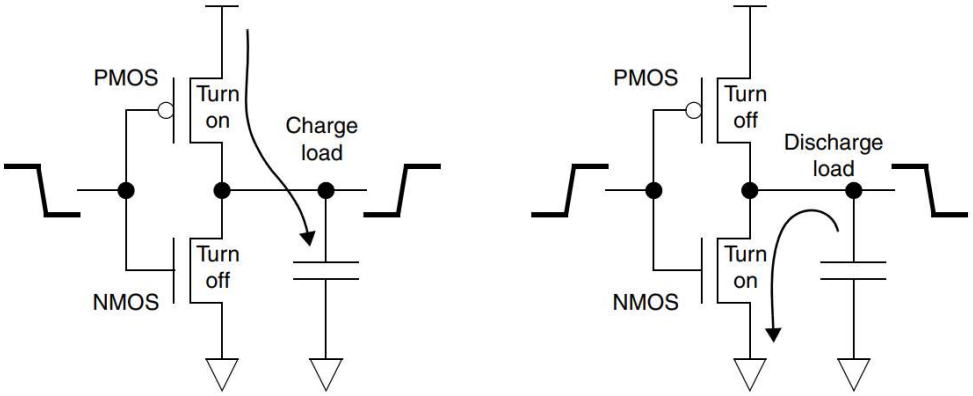
What constitutes Power ?

- Dynamic Power
  - Switching power
  - Short-Circuit Power
    - Crowbar current
- Leakage Power

$$P_{total} = C_L V_{DD}^2 f_{clk} a_{0\rightarrow 1} + V_{DD} I_{short\text{-}circuit} + V_{DD} I_{leakage}$$

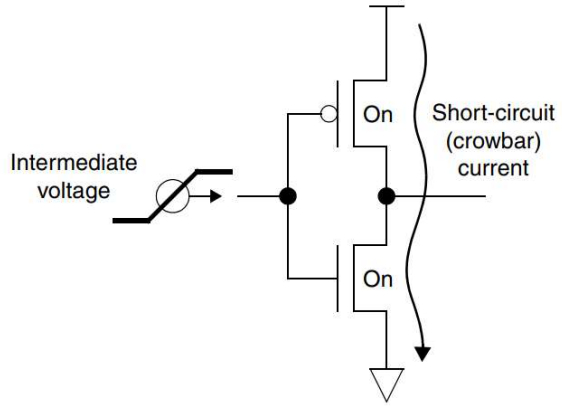
- Reduce
  - Voltage, Load, Frequency, Switching , Current

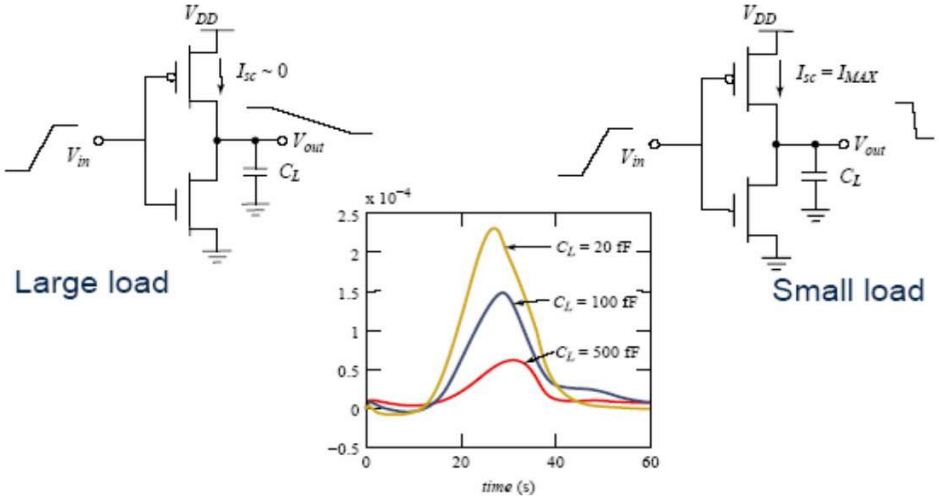
Dynamic Power



- Dynamic power dissipation can be affected by the following factors
  - V_{DD}
  - Switching
  - Short Circuit Current
    - Transition
  - Clock Gating
  - Operand Isolation
  - Other arch solutions
  - DFS, DVFS, AVS

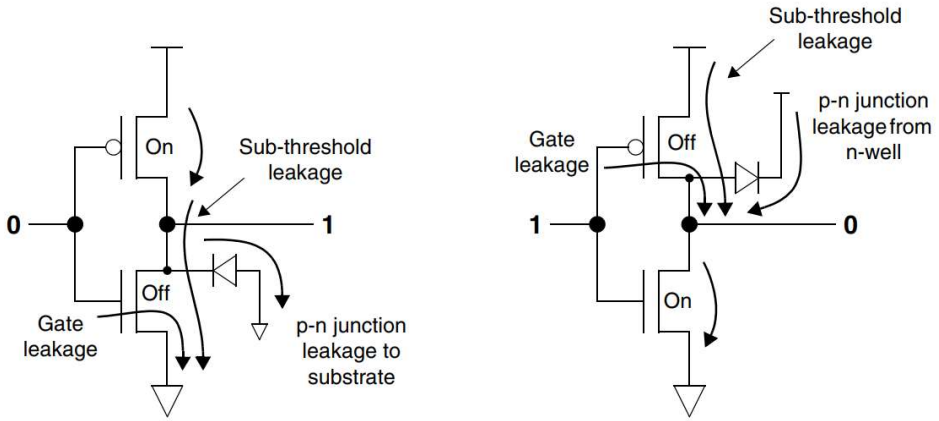
Short Circuit Current

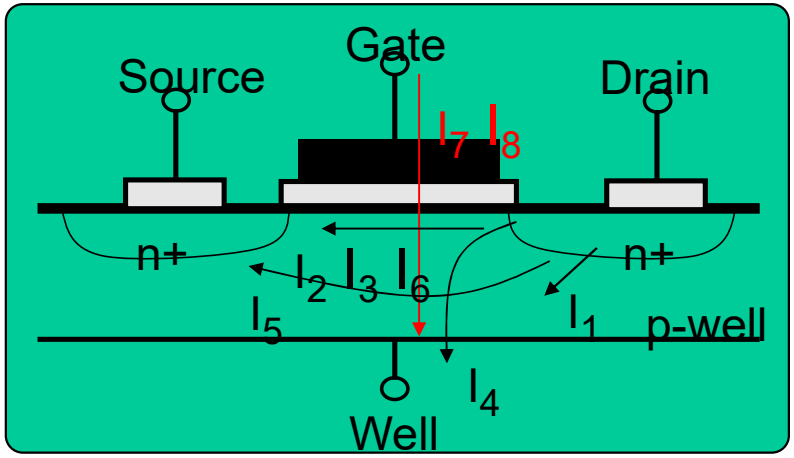




- Internal power consumed during the short period of time when both PMOS and NMOS are On
- Depends on ratio of input to output transition times.
  - Higher the ratio, more is the time for which both devices are On
- Can be minimized by balancing the input and output rise / fall times

Leakage Current



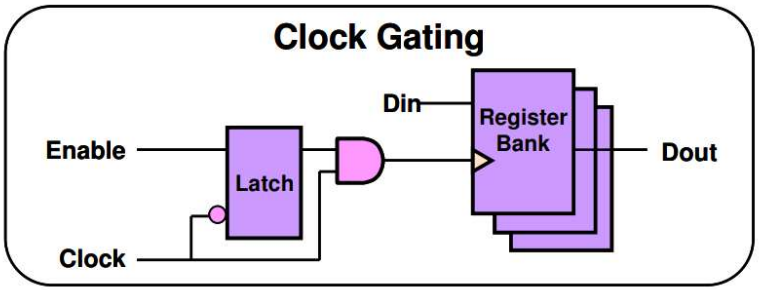


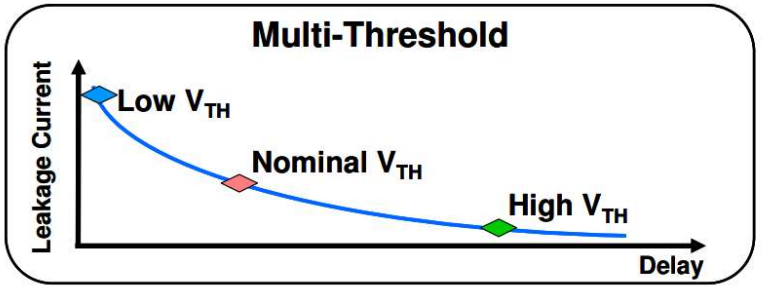
- I_1 – Reverse Bias Diode
- **I_2 – Weak Inversion**
  - *Due to ever reducing V^{TH}*
- I_3 – Drain Induced Barrier Lowering (DIBL)
- I_4 – Gate Induced Barrier Lowering (GIDL)
- I_5 – Punchthrough
- I_6 – Narrow Width Effect
- I_7 – Gate Oxide Tunneling
- I_8 – Hot Carrier Injection

- Gate leakage also becoming significant due o thinning of gate oxide

Power reduction methods

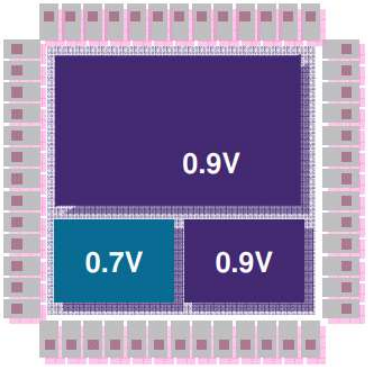
- Common

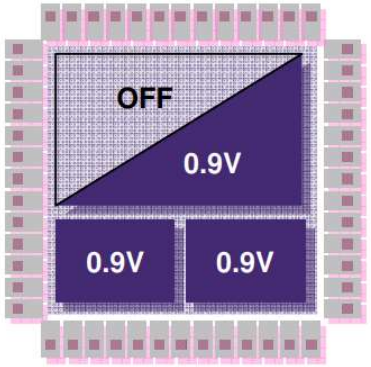


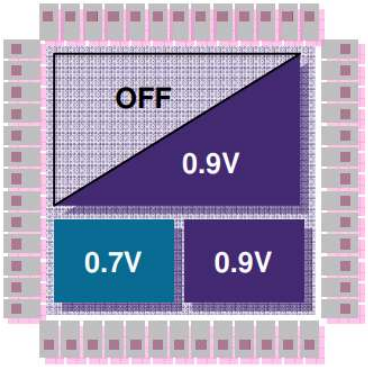


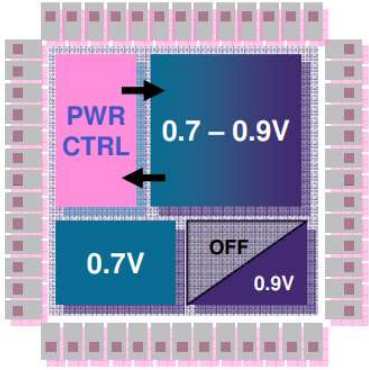
- MV
- PG
- MV with PG
- DVFS

- Advanced

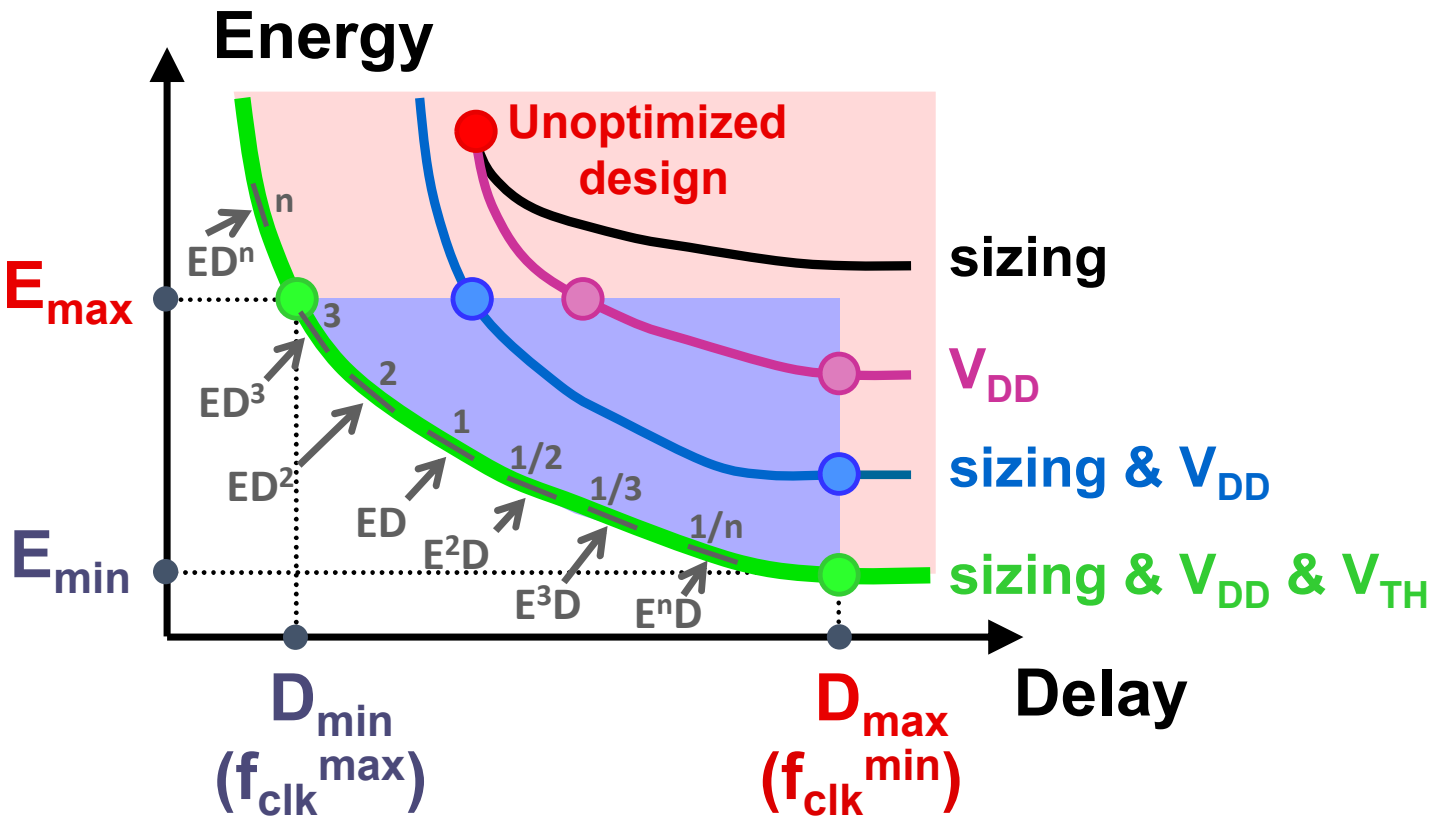








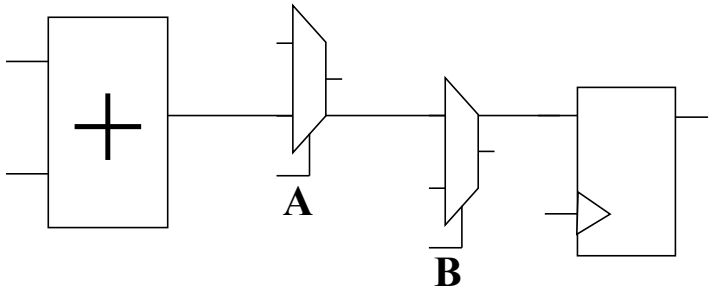
Power – Delay Optimization



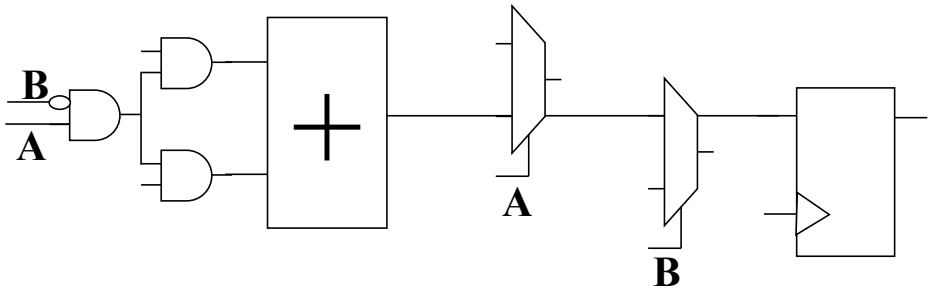
Power Optimization

- Major component of dynamic power dissipation is due to switching
- The transitions of signal from high-low and vice versa causes capacitances to charge and discharge
- Power dissipation is huge during these cycles
- This kind of power can be optimized by ensuring minimum switching
- Should be accounted for at the architecture level

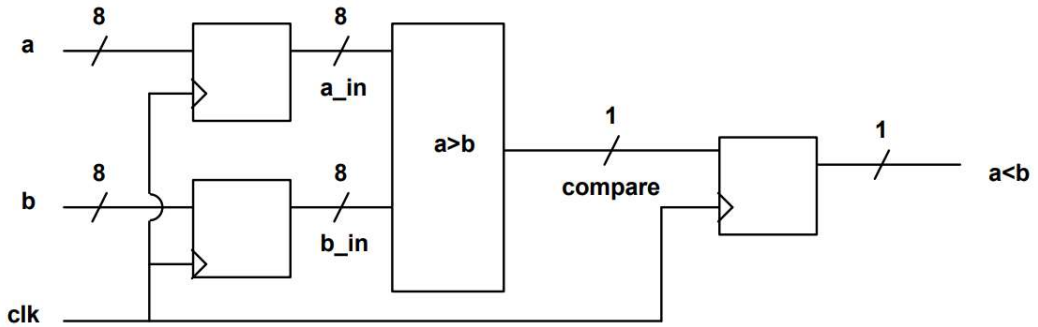
Operand Isolation



- Most designs are datapath intensive
- Computations in the data path contributes to a large portion of dynamic power dissipation
- Unnecessary computations need to be eliminated



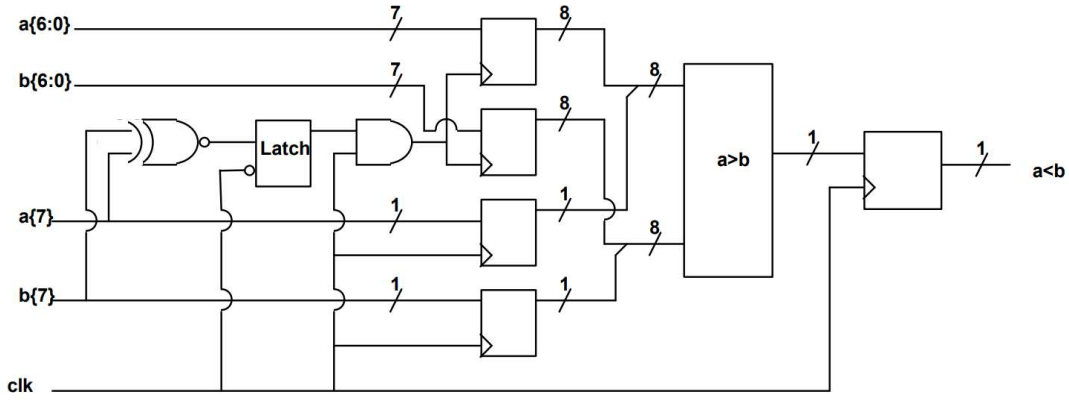
Precomputation



Entire function is computed

Smaller function is computed

Enable is precomputed



Right Architecture

Topology	Delay	Power	PDP	Area
Ripple Carry	1	1	1	1
Constant Block Width Carry Skip	0.56	1.06	0.59	1.27
Variable Block Width Carry Skip	0.44	1.29	0.57	1.88
Carry Look Ahead	0.44	1.59	0.70	2.04
Carry Select	0.36	2.24	0.81	3.38
Conditional Sum	0.41	3.18	1.30	4.38

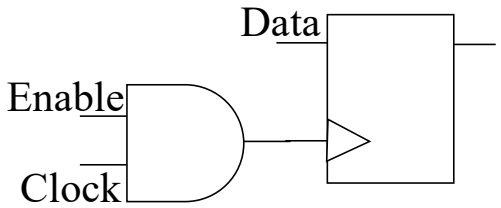
Adders normalized to Ripple Carry

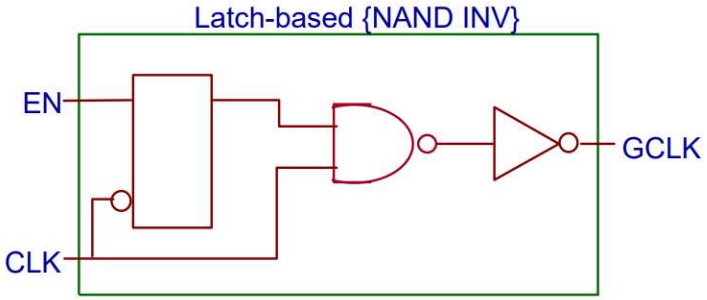
Multipliers normalized to Array

Topology	Delay	Power	PDP	Area
Array	1	1	1	1
Split Array	0.68	0.87	0.59	1.43
Wallace Tree	0.58	0.74	0.43	1.93
Modified Booth	0.49	0.95	0.47	2.02

Clock Gating

- During the operation of a circuit all registers are not active all the time
- Clock transition also contributes largely to power dissipation
- The clock to those flops which are not active can be switched of by clock gating
- By far the most dominant power optimization technique used

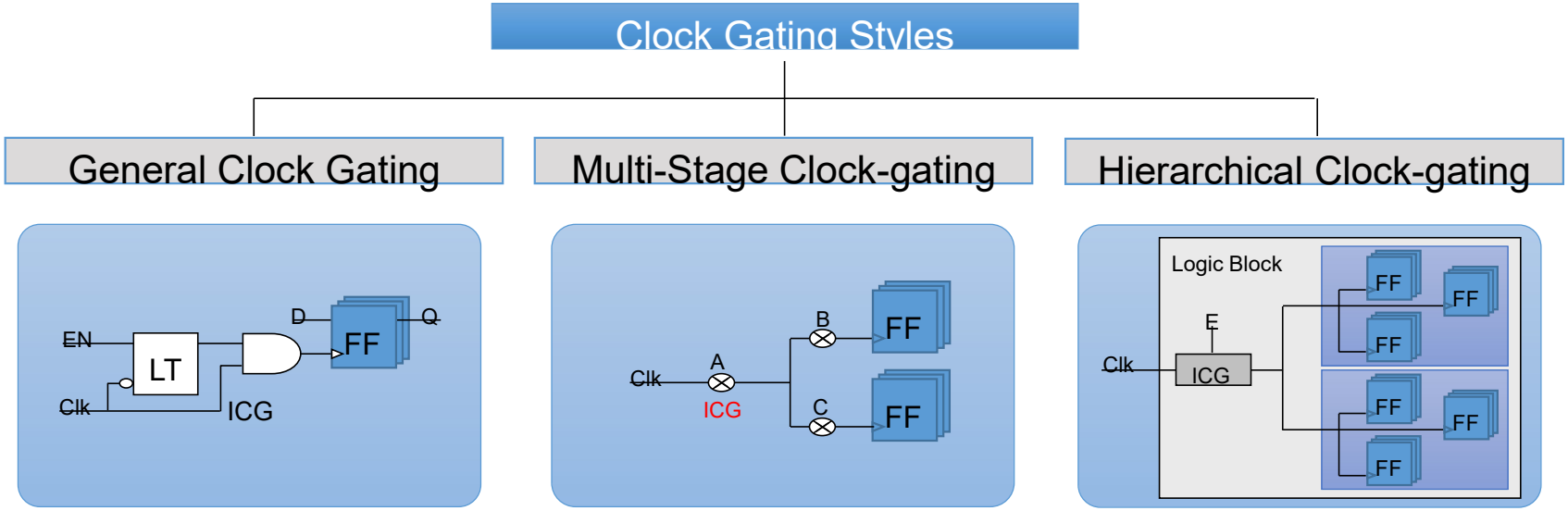




- Challenges
  - Enable signal timing
  - Insertion delay increase
  - Peak power during ON/OFF of clock
  - Verification impact

Clock Gating

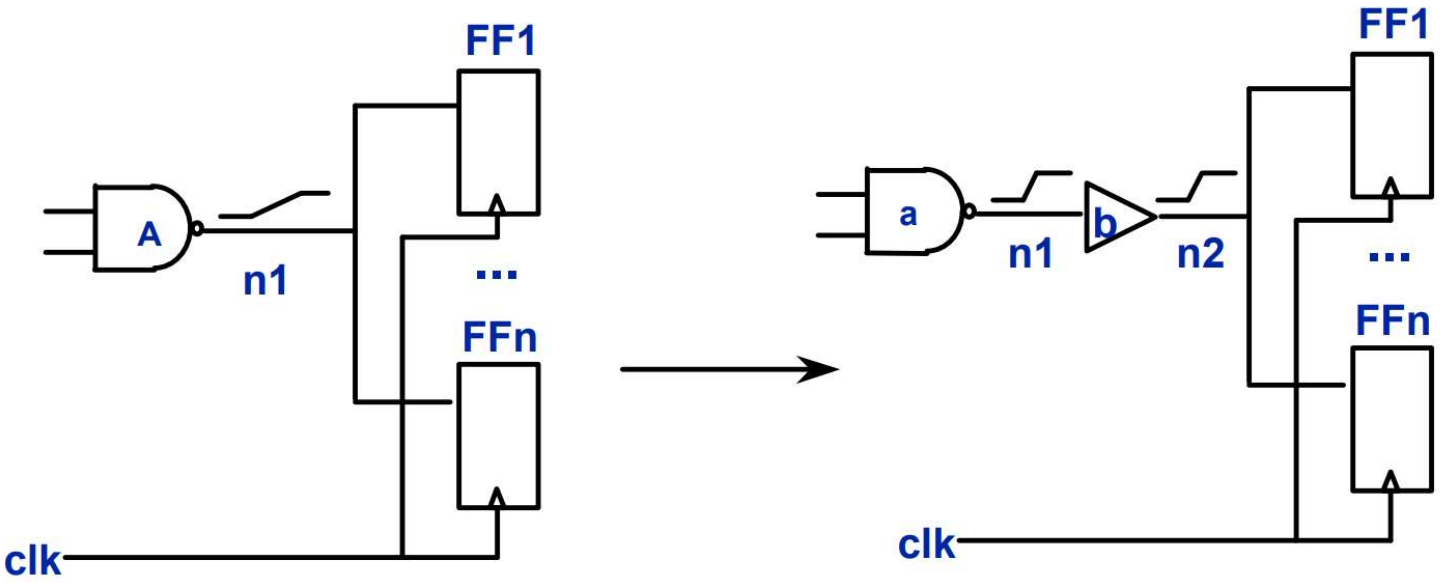
- Some guidelines to be followed for Clock Gating are
  - The enable signal should not be a constant value
  - The enable signal should not be generated from a flip-flop whose clock is different from the that of the flip-flop which is being gated
  - For automatic clock gating, enable should not be from the input port



Synthesis for Power

- Clock gating is the user controlled low power techniques that can be utilized during synthesis
- Any flip-flop which has a enable signal is a prime candidate for clock gating
- The enable signal instead of enabling the data enables the clock
- A mux and a flip-flop can be replaced by a clock and flip-flop
- The flip-flop is not active until the clock is enabled
- Switching activity of the clock and internal power of flip-flop is decreased
- Area of the design decreases

Buffer Insertion



A = 3, FF1,2 = 5, Total : 13

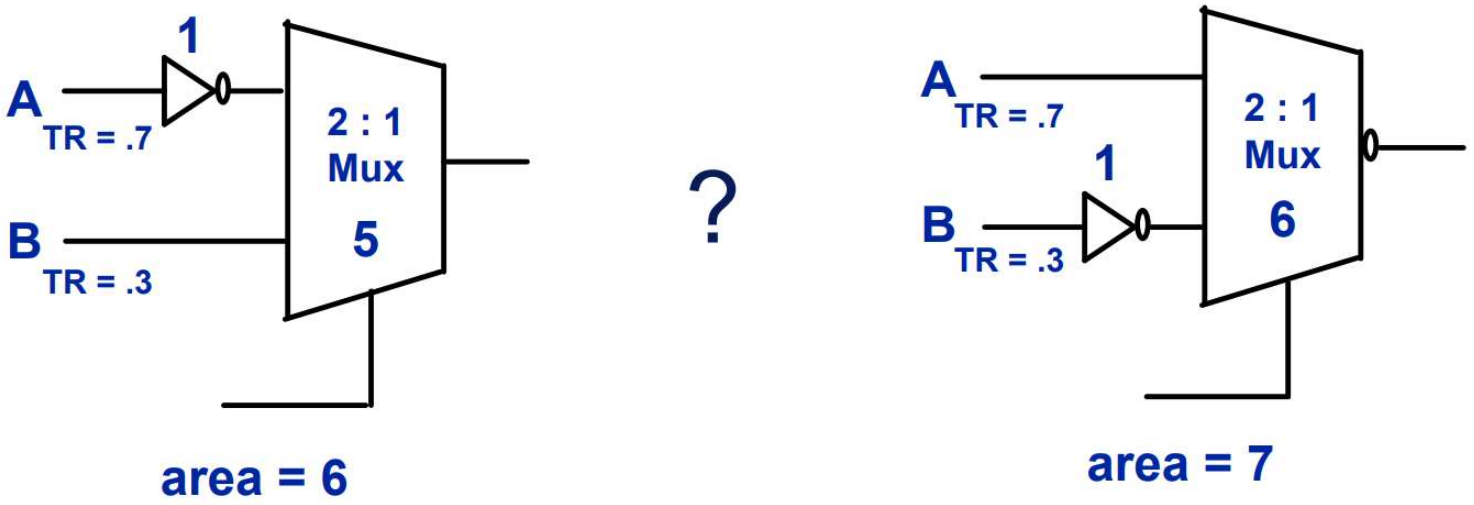
Transition Time , n1 = 4

A = 2.5, FF1,2 = 4.5, Buf = 1

Total : 12.5

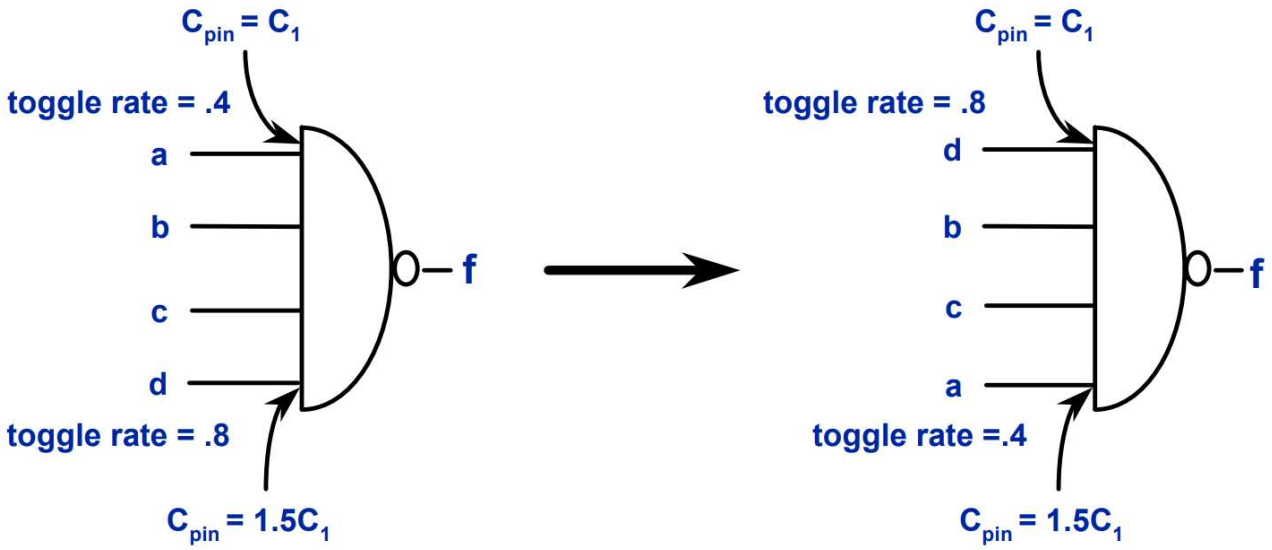
Transition Time , n1,n2 = 2

Phase assignment



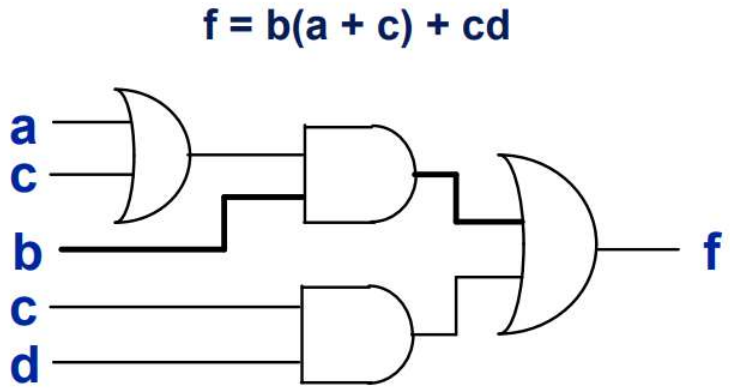
Need to know actual toggle rates

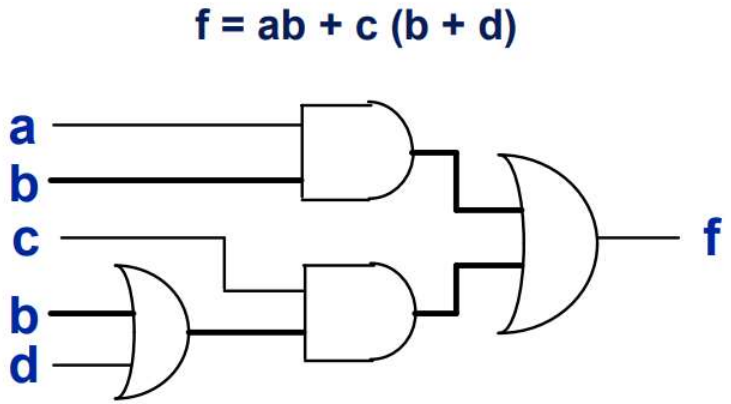
Pin Swapping



Need to know actual toggle rates

Factoring





F = ab + bc + cd

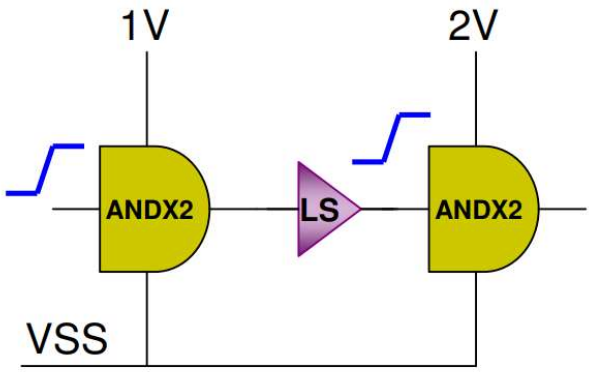
Signal B is high activity net

Leakage Power

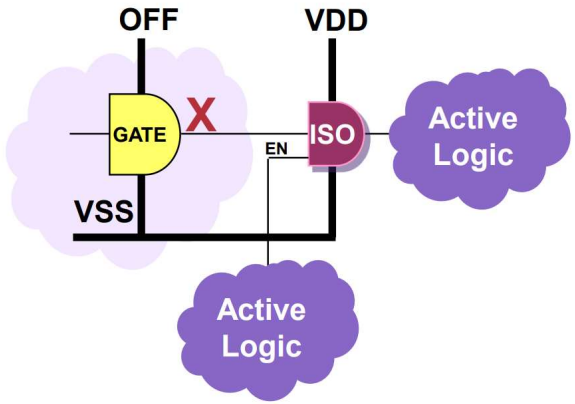
- At VDSM technologies Leakage power constitutes a large percent of the total power dissipation
- Leakage power dissipation can be reduced by increasing threshold Voltage
- Increase in threshold voltage leads to increase in delay of the cell
  - Fine balance has to be created
- By ensuring that blocks which are not functionally required are switched off leakage current can be minimized
  - Known as power gating
  - Isolation cells , retention registers required

Low Power Cells

- Level Shifters
  - Connecting 2 power domains at different voltage levels will cause issues
    - Timing inaccuracy
    - Signals not propagated

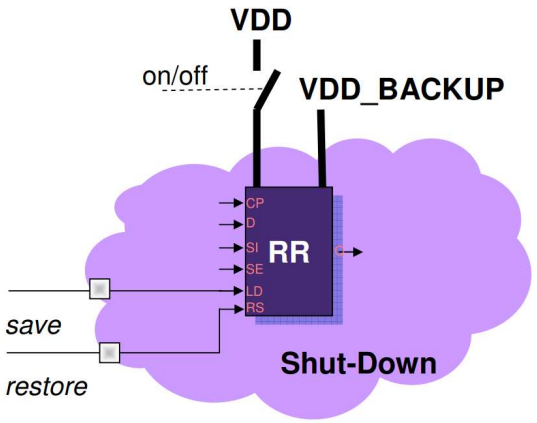


- Isolation Cells
  - Connecting shutdown and active logic will cause issues
    - Spurious signal propagation
    - Crow bar current
    - Provides protection during shutdown

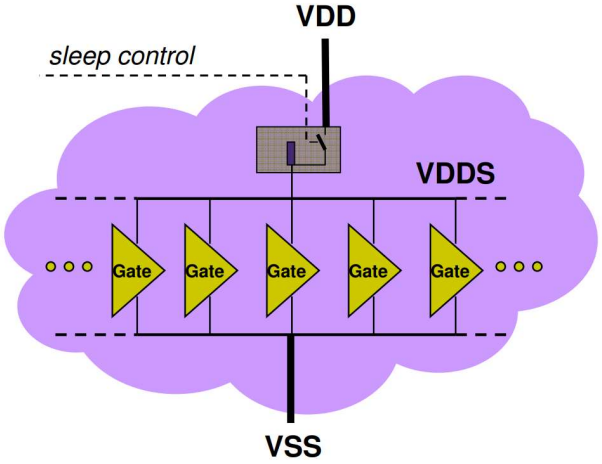


Low Power Cells

- Retention Registers
  - Value of few registers in shut down mode needs to be preserved
    - Master-Slave
    - Balloon

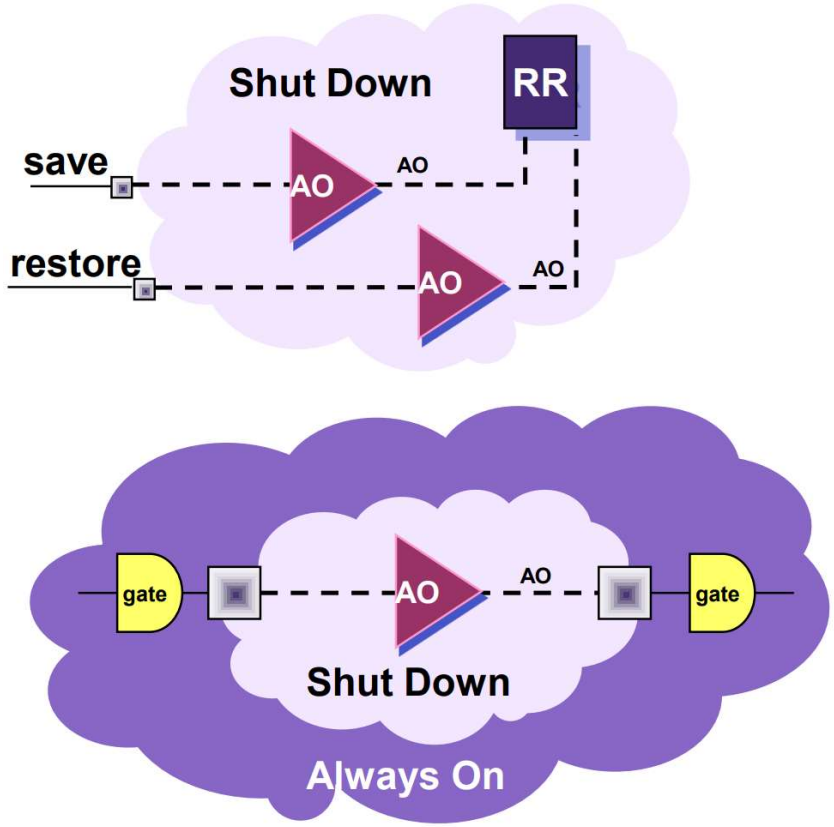


- Power switches
  - Turn of inactive logic to remove leakage power
  - Multi-Threshold CMOS
    - In active mode: SL=0, MP and MN are “on”
    - VDDV and VSSV almost function as VDD and VSS.
  - In standby mode: SL=1, MP and MN are “off” and leakage is suppressed

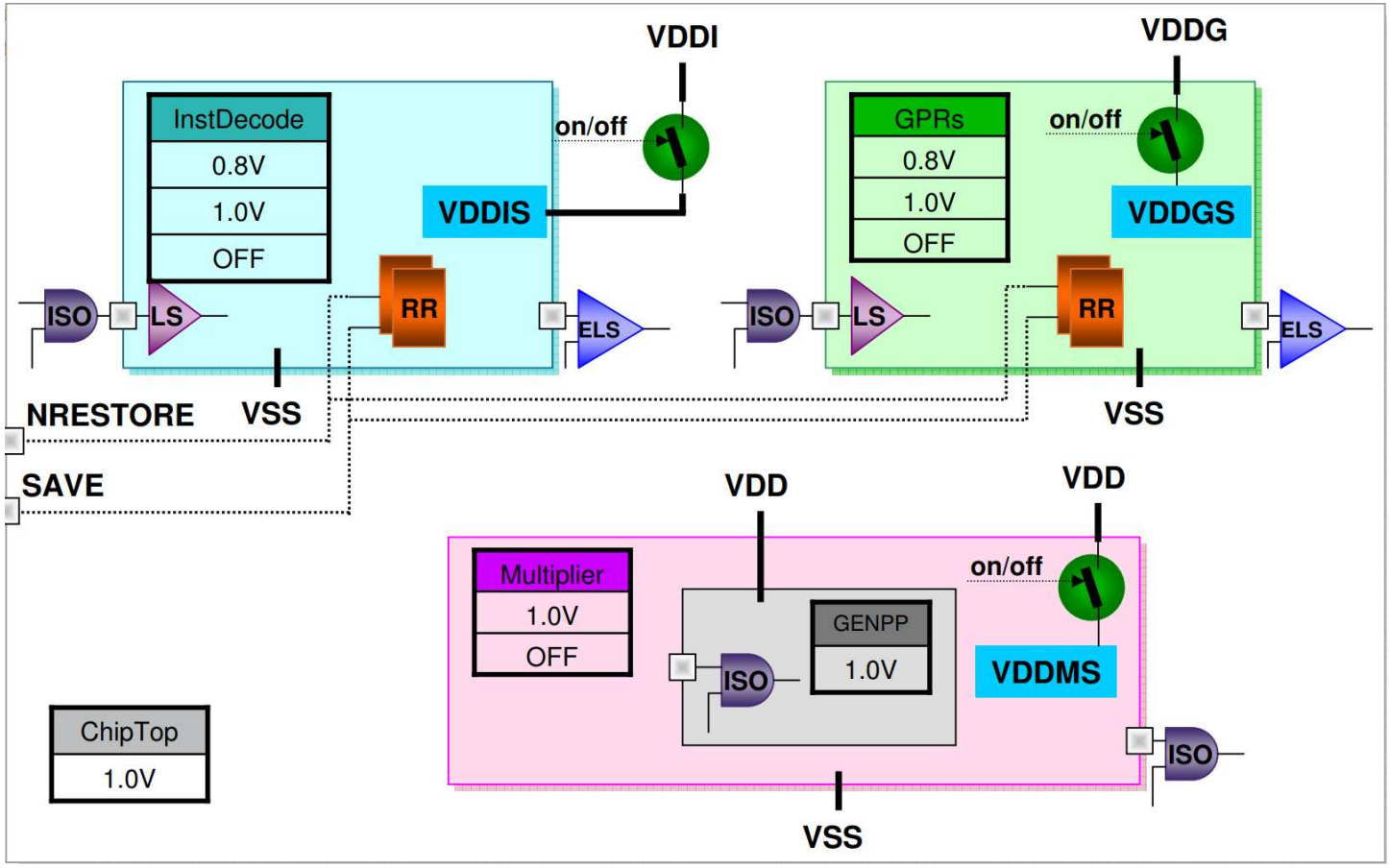


Low Power Cells

- Always On
  - Some logic needs to stay On during shut down
    - Power switches
    - Retention Registers



Low Power Management



Low Power Management

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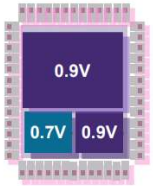
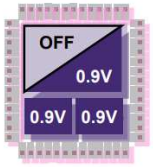
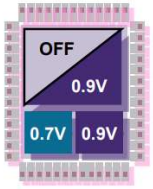
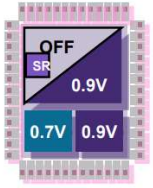
	Level Shifters	Isolation Cells	Power Switches (MTCMOS)	Retention Registers	Always-on Logic
 Multiple Voltage (MV) Domains	✓				
 Power Gating (shutdown) Single Voltage No State Retention		✓	✓		
 MV Domains Power Gating No State Retention	✓	✓	✓		
 MV Domains Power Gating w/ State Retention	✓	✓	✓	✓	✓

Low Power Management

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Power reduction technique	Leakage power	Dynamic power	Timing penalty	Area penalty	Implement. impact	Synth, Formal & Test Impact	Verification impact
Area optimization	1.1X	10%	0%	-10%	None	None	None
Multi-Vt optimization	6X	0%	0%	2 to -2%	Low	None	None
Clock gating	0X	20%	0%	<2%	Low	Low	None
Multi-supply voltage (MSV)	2X	40-50%	0%	<10%	Medium	Medium	Low
Power shut-off (PSO)	10-50X	~0%	4-8%	5-15%	Medium-high	High	High
Dynamic and Adaptive Voltage Frequency Scaling (DVFS and AVS)	2-3X	40-70%	0%	<10%	High	High	High

Synthesis for Power

- Among all the low power methodologies discussed so far it can be seen that power optimization requires
  - usage of proper libraries
  - efficient architecture
  - appropriate materials
- It can be seen that at the synthesis level scope for power optimization is limited
- The major power optimizations done during synthesis are
  - Clock Gating
  - Multi V_{TH} Synthesis

Synthesis Commands

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set_clock_gating_style	• sets the clock gating style used for clock gate insertion and replacement.
insert_clock_gating	• performs clock gating on an appropriately prepared GTECH netlist.
propagate_constraints -gate_clock	• propagates timing constraints from lower levels of the design hierarchy to the current design.
report_clock_gating <-hier> <-ungated>	• reports information about clock gating performed by Power Compiler.
compile –exact_map –gate_clock	• Compiles with clock gating

Challenges

- Power domain architecture
- Shutdown strategy
  - Isolation, retention
- Power control unit
- Power switch configuration
  - On chip /off chip
  - Switch layout, control (HW/SW), hookup
- Always-on synthesis
- DFT, CTS
  - Power domains introduce new boundaries
- Timing, power, and rail analysis
  - Multi-corner, multi-mode
  - In-rush current, dynamic IR drop

- Isolation/Level shifting bugs
- Control sequencing bugs
- Retention scheme/control errors
- Retention selection errors
- Electrical problems like memory corruption
- Power sequencing/Voltage scheduling errors
- Hardware-software deadlock
- Power gating failure/dysfunction
- Power-on-reset/bring-up problems
- …

These must be considered throughout the flow!