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Synthesis & Constraints

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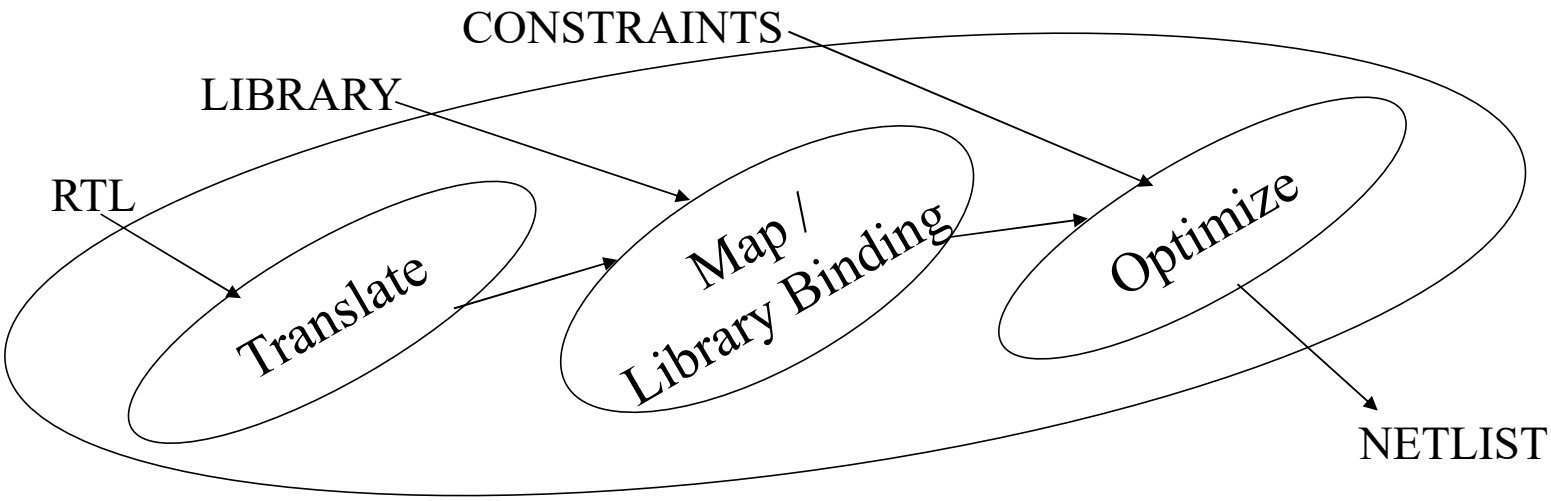
Synthesis Process

- Synthesis is a 3 step process
  - The first where the code gets translated
  - The second where the translated code gets bound by the library
  - The third where the netlist is optimized



Synthesis Process

- Translate:
  - A process where RTL is converted to equation format
  - A basic boolean optimization is carried out to reduce the literals
  - An completely independent code is made tool dependent
- Map
  - The obtained equations from step above are directly mapped to the technology library
  - Hence the name technology / library binding
  - Now design is bound to particular tool as well as technology

Synthesis Process

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- Optimize
  - The design obtained after map is now optimized according to the specifications
  - Various timing algorithms and architectures are involved in making the design meeting the spec
  - Most of the times the design is primarily optimized to meet timing specifications

Design Objects

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- Design
  - It corresponds to the circuit description that performs some logical function
  - The design may be stand-alone or may include other sub-designs
- Port
  - These are the primary inputs,outputs or inouts of the design
  - In other words the interfaces of a design
- Cell
  - It is the instantiated name of the sub-design in the design

Design Objects

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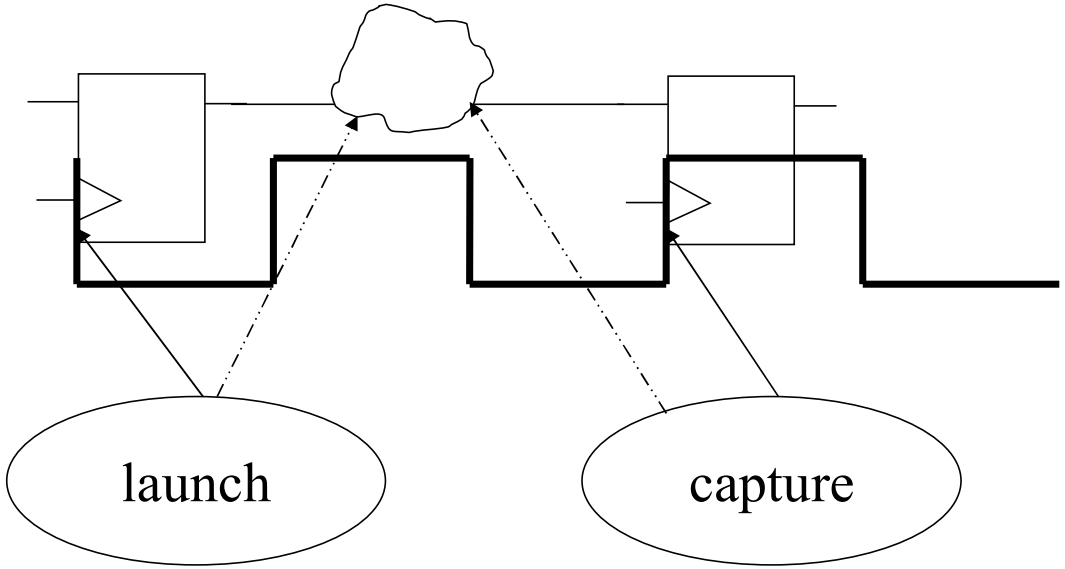
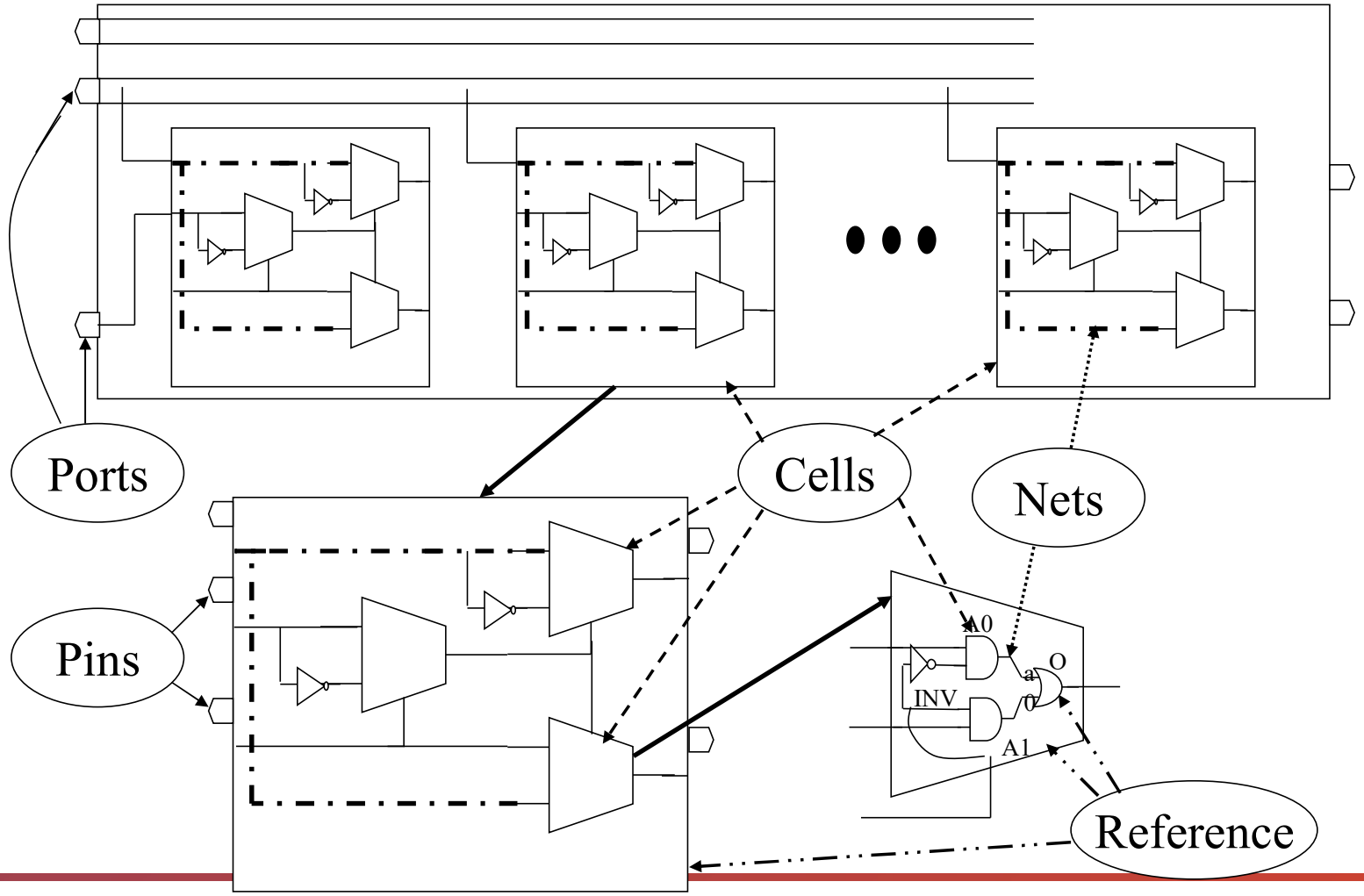
- Reference
  - This is the definition of the original design to which the cell or instance refers
- Pin
  - It corresponds to the inputs,outputs or IO ’ s of the cells in the design
- Net
  - The wires that hook up the design together by connecting ports to pins and/or pins to each other

Design Objects

- Clock
  - The port or pin through which the clock signal propagates in the design



Design Objects



Timing Paths

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- Synthesis process can be considered as a ‘timing’ based selection of gates to meet a particular function
- ‘Timing’ refers to the time taken by data to travel from one point to the other
- The point at which data is expected to commence / originate is considered a ‘start point’
  - Input Port
  - Clock Pin of sequential elements
- The location at which data terminates is considered as the stop point
  - Output Port
  - Data Pin of sequential elements

Propagation Delay

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- Delay of a cell depends on many factors such as
  - Operating Conditions
  - Functionality of the cell
  - Type of Inputs
- Based on the factors above a cell can propagate data either quickly or slowly
- Depending on the kind of analysis being done at any point of time one needs to consider either minimum delays or maximum delays

Violations

- When the setup and hold time requirements are not met the design is said to fail the timing specifications
- This can happen due to various reasons such as

	Causes for setup violations	Remedies
Data	Slow	Fast
Launch Clock	Slow	Fast
Capture Clock	Fast	Slow

Contamination Delay

- Contamination delay t_{CD} is the lower bound between invalid inputs and invalid outputs
- Propagation delay t_{PD} is the upper bound between new valid inputs and new valid outputs