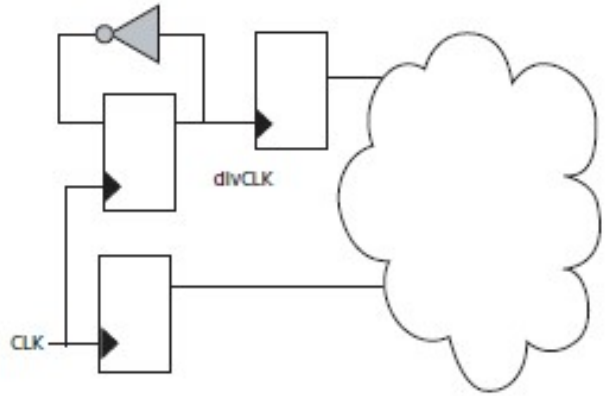
RAMAIAH
SKILL ACADEMY

Clock Domain Crossing

Vasudev Murthy

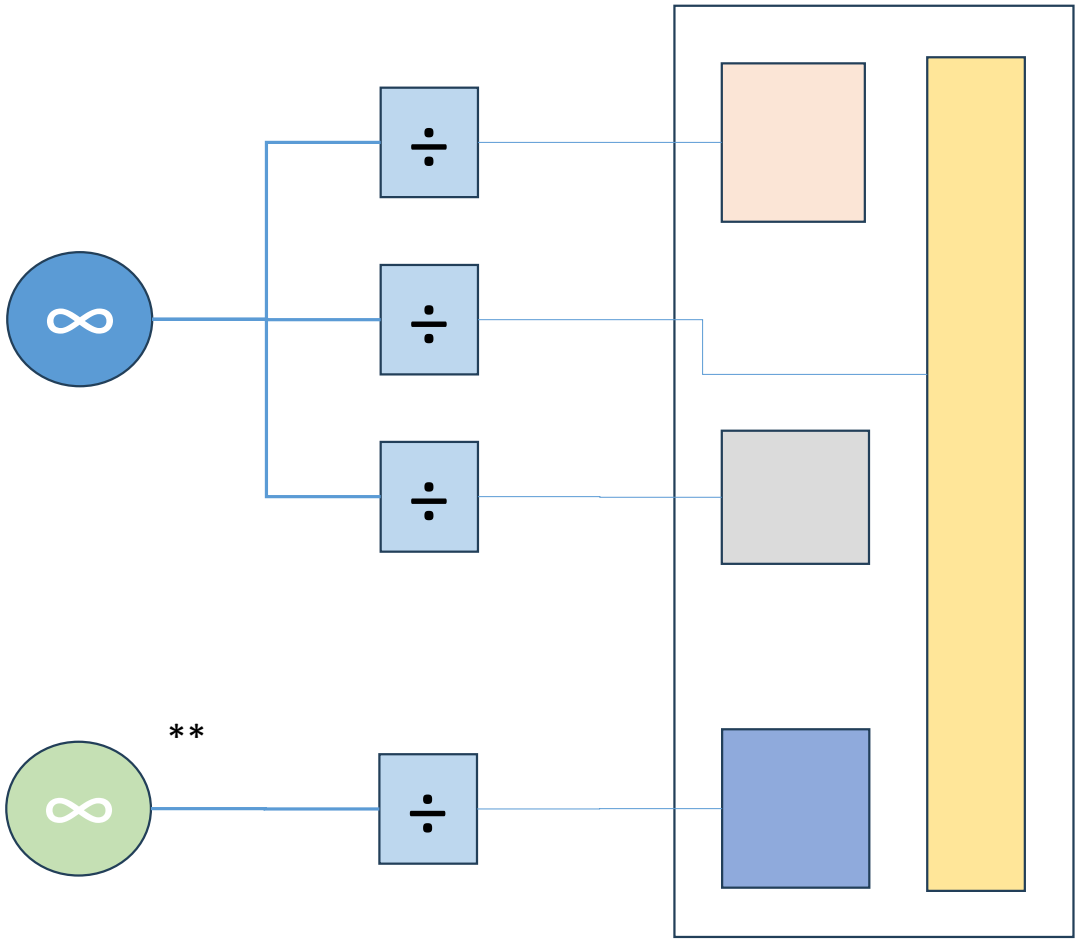
Clock Domain

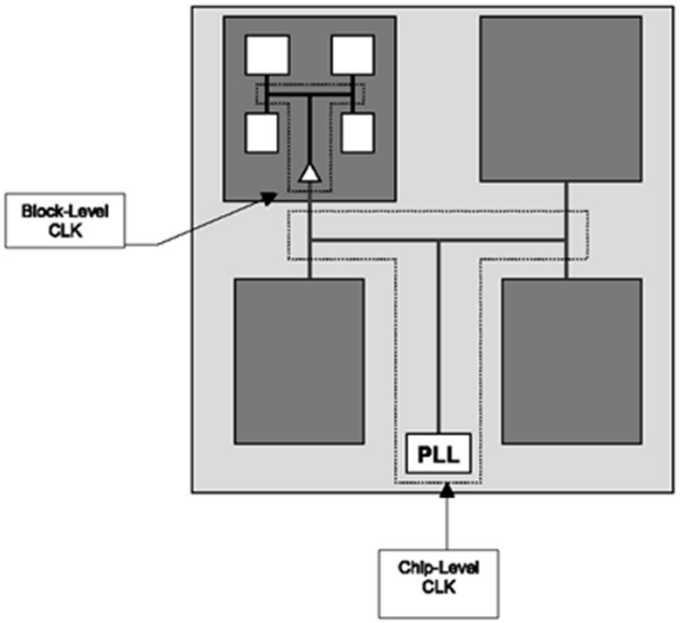
- **Clock Domain** : All flops clocked by the same clock are said to be in the same domain



- **Synchronous Clock** : All clocks which are phase aligned are said to be synchronous to each other
  - Clocks with different frequencies can still be synchronous to each other
  - Clocks with same frequency can still be asynchronous
  - Typically clocks from same source are synchronous **

Clock Domain

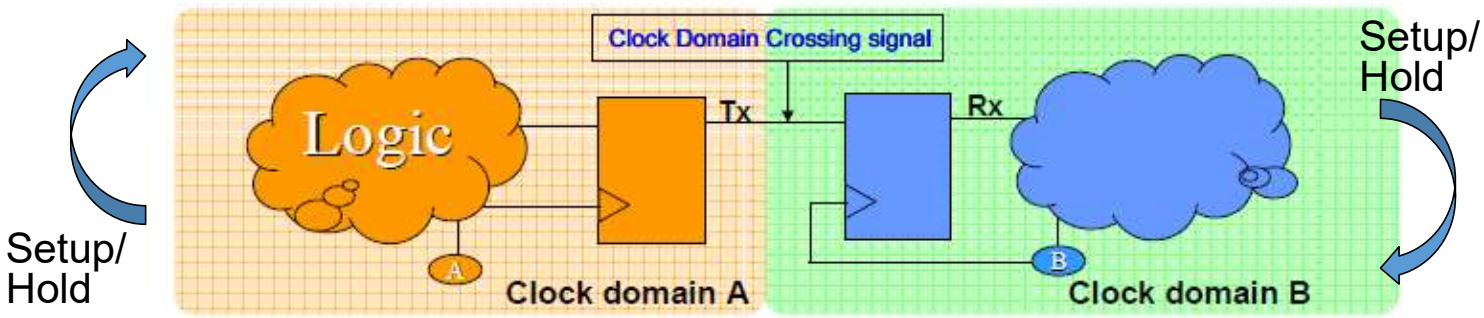




Clocks from same source can be considered and built as asynchronous to reduce clock tree balancing complexities

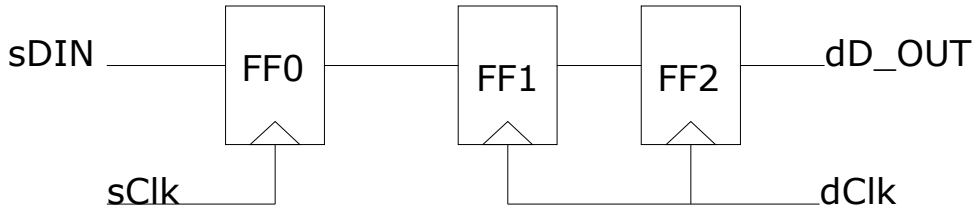
Clock Domain Crossing

- **CDC** : Clock domain crossing occurs when data is transferred across async clock domains
- STA Checks ensure setup and hold are honoured in sync clock domains
- No timing checks done on CDC paths
- Metastability will occur in async paths and need to be addressed
- STA cannot identify CDC issues, though simulation can mimic
- CDC issues cannot be fixed through SW fixes

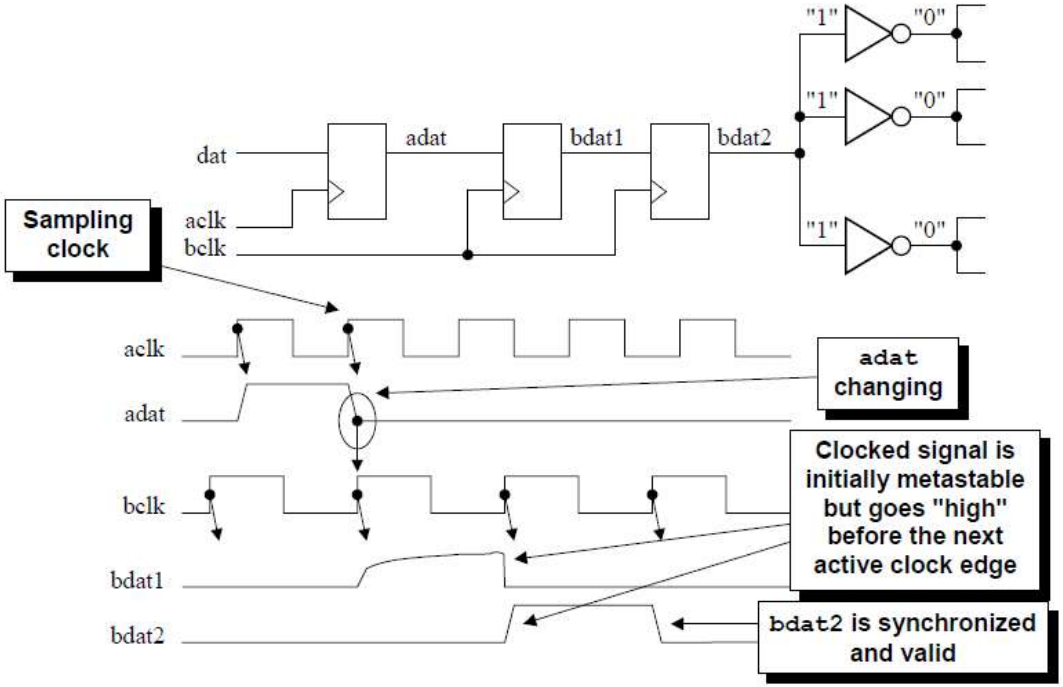


Synchronizers

- **Synchronizers** are specially built cells / logic to reduce the probability of metastability
- These logic are able to withstand any metastability locally and ensure a stable output for the rest of the design
- The most common synchronizer logic is the 2 FF synchronizer
- FF1 will go meta-stable, but FF2 does not look at data until a clock period later, giving FF1 time to stabilize



Synchronizers



- If data is changing too fast we might have to consider adding 1 more FF.
- This structure used for single and multi bit control signals and single bit data signals

MTBF

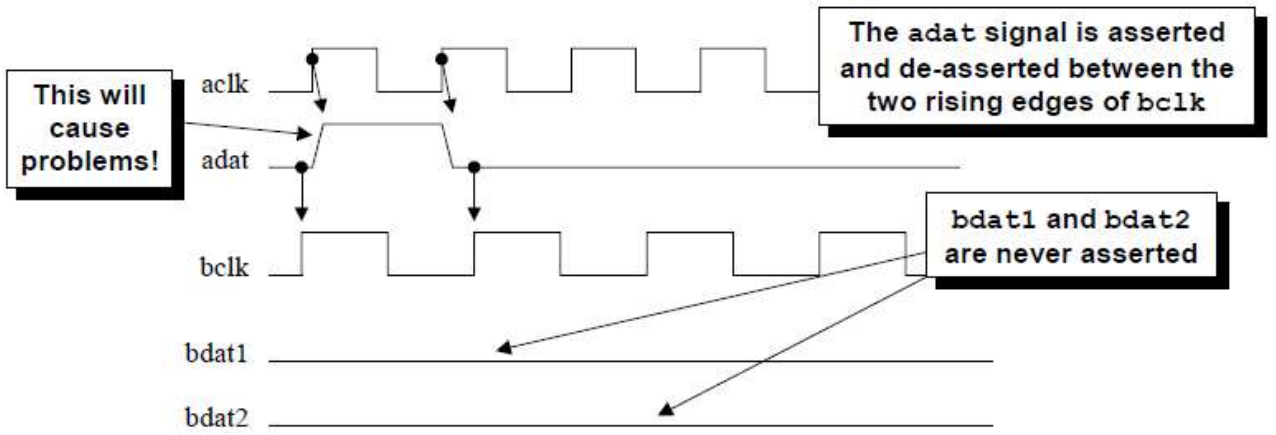
- **Mean Time Before Failure**
  - Attribute of merit for a sync FF related to metastabilty.
  - Inversely proportional
    - Frequency of receiving clock domain
    - The rate of change of data

$$MTBF(t_r) = \frac{e^{(t_r/\tau)}}{T_o f a}$$

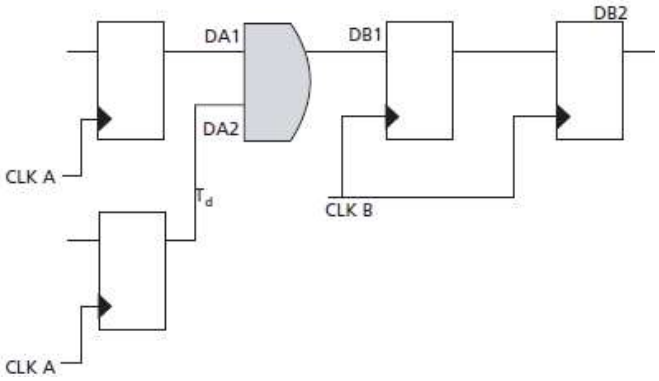
t_r resolution time (time since clock edge)
f sampling clock frequency
a asynchronous event frequency
τ and T_o FF parameters

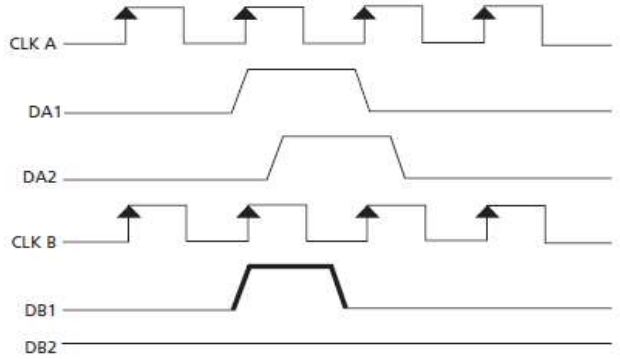
Slow-Fast ; Fast-Slow Clocks

From	To	Issues
Slower Clock	Faster Clock	The faster clock signal will sample the slower signal one or more times
Faster Clock	Slower Clock	Signal must be wider than the cycle time of the slower clock



Issues

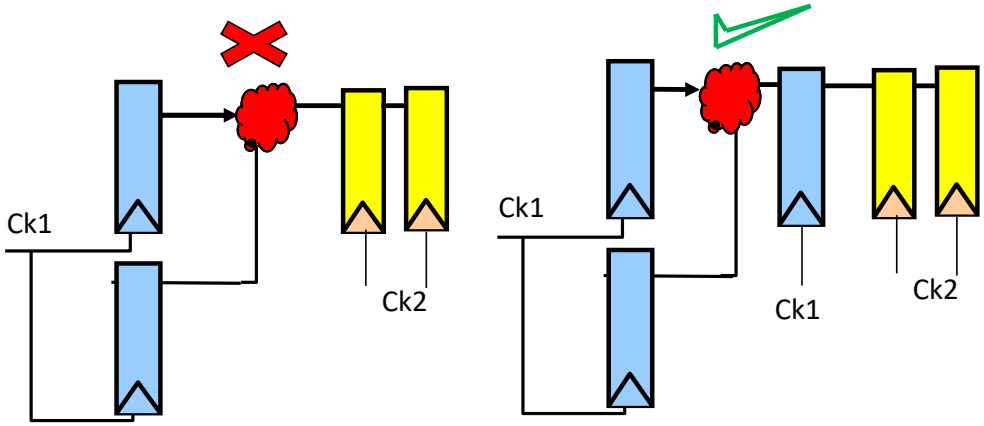


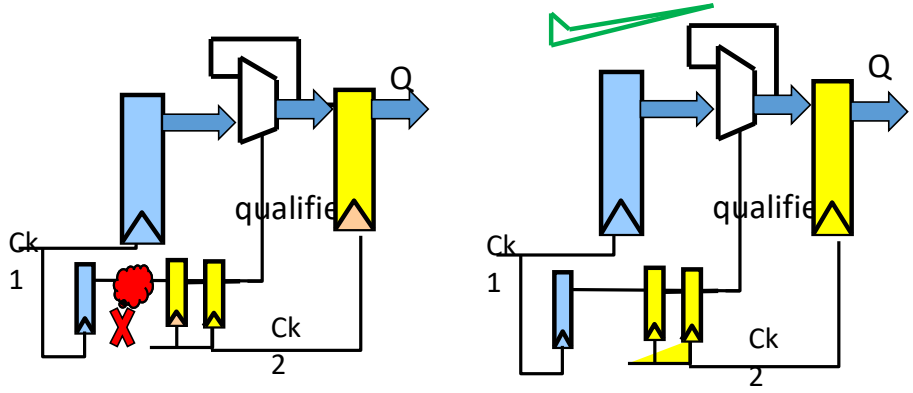


- Unconstrained path has delay imbalance, leading to loss of data & glitches.
- Multiple signals converging through Combo logic leads to glitch
- Convergence / Divergence

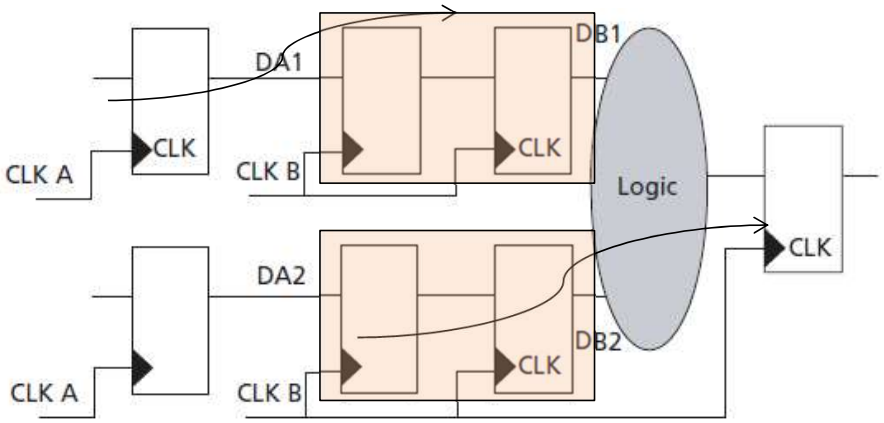
Issues

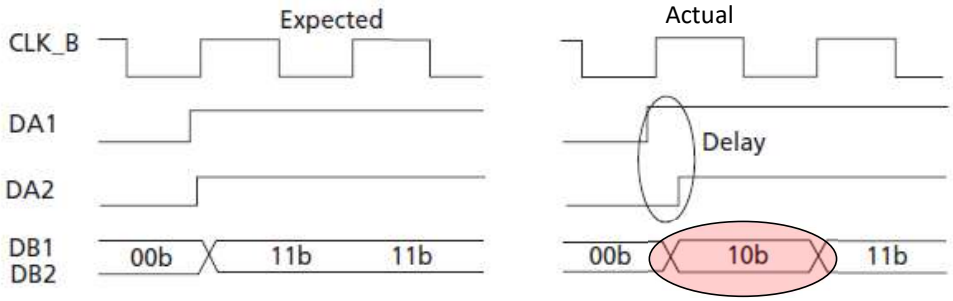
Don’t use combinational logic on data / control path





Reconvergence





Compute the controls & then do one transfer across domain

Gray Coding

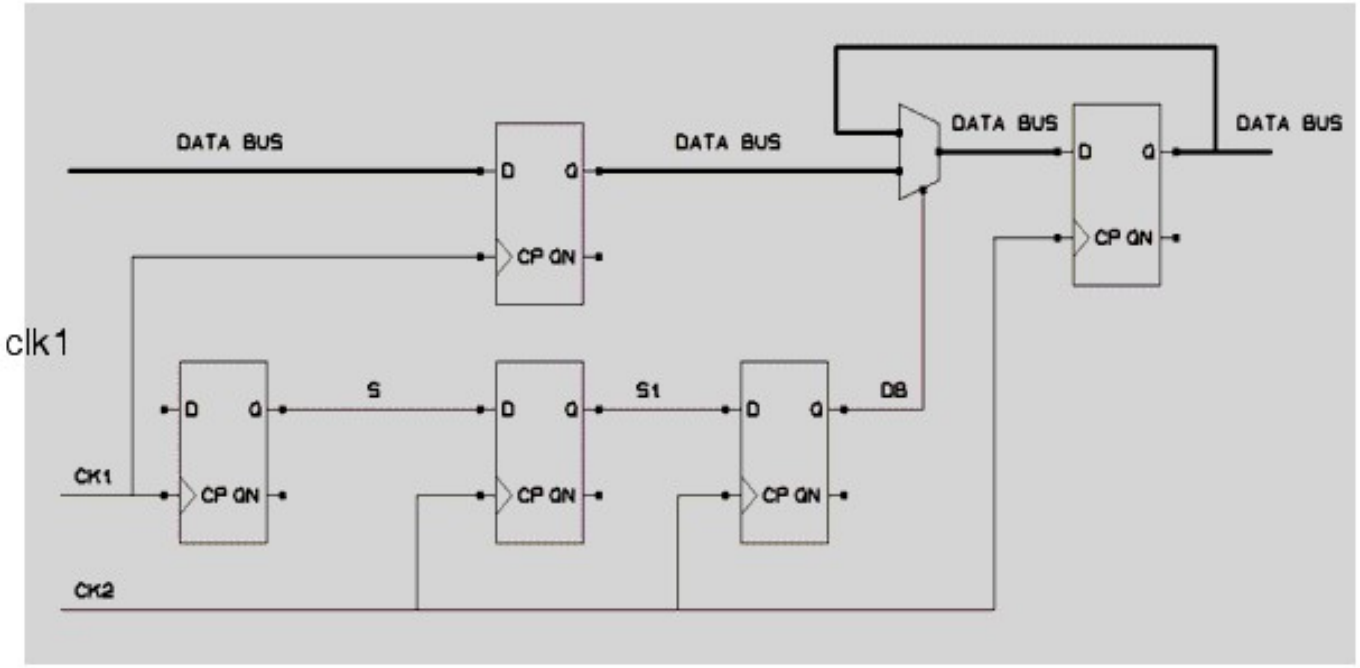
- Use Gray code when crossing a clock domain boundary.
- A Gray code ensures that only a single bit changes as the bus counts up or down.
- Gray code – Unit distance code
- Applicable only for control signals as it may not be possible to Gray-encode the data busses

	Binary count	Gray count
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100

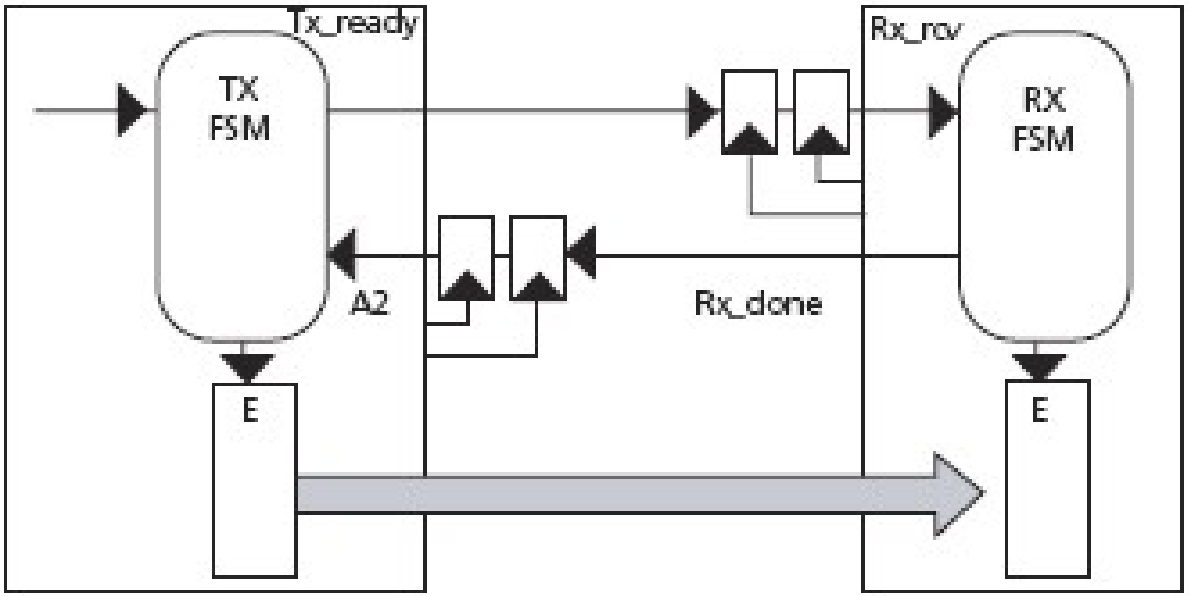
Bad gray code if count to 5

Good gray code if count to 7

Mux based Synchronization



Hand Shake based



- Clock freq maybe configurable / unknown
  - Hard to design previous syncs for all cases
  - Hard to properly check for all cases
- Solution: handshake protocols

False Negatives

- Common False Negatives
  - Constant signals (VSS, VCC)
  - Near Constant Signals
    - Parameters set during reset and never changed
    - Reset pins
  - Alternate mode signals
    - Valid in only some operating modes including clock
    - Scan and some ultra slow interfaces

Other Synchronizers

- Other Synchronizers
  - Pulse Synchronizer
  - Word Synchronizer
  - Null Synchronizer
  - Reset Synchronizers
  - FIFO