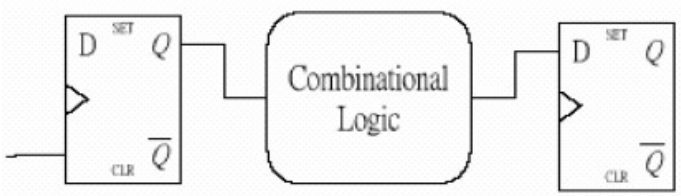
RAMAIAH
SKILL ACADEMY

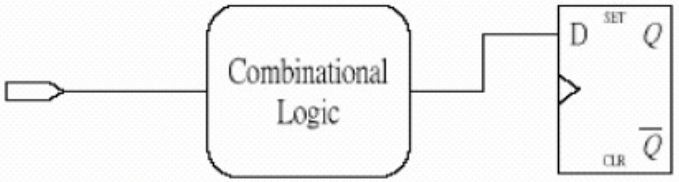
TIMING BASICS

Vasudev Murthy

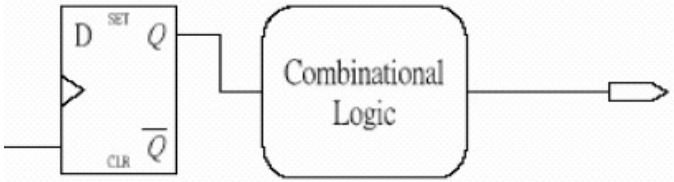
Timing paths



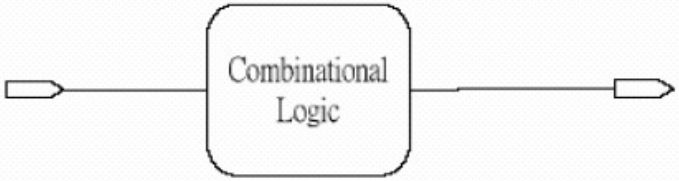
Start Point:
clock pin of sequential device
End Point:
data input pin of sequential devices



Start Point:
primary input port
End Point:
data input pin of sequential devices

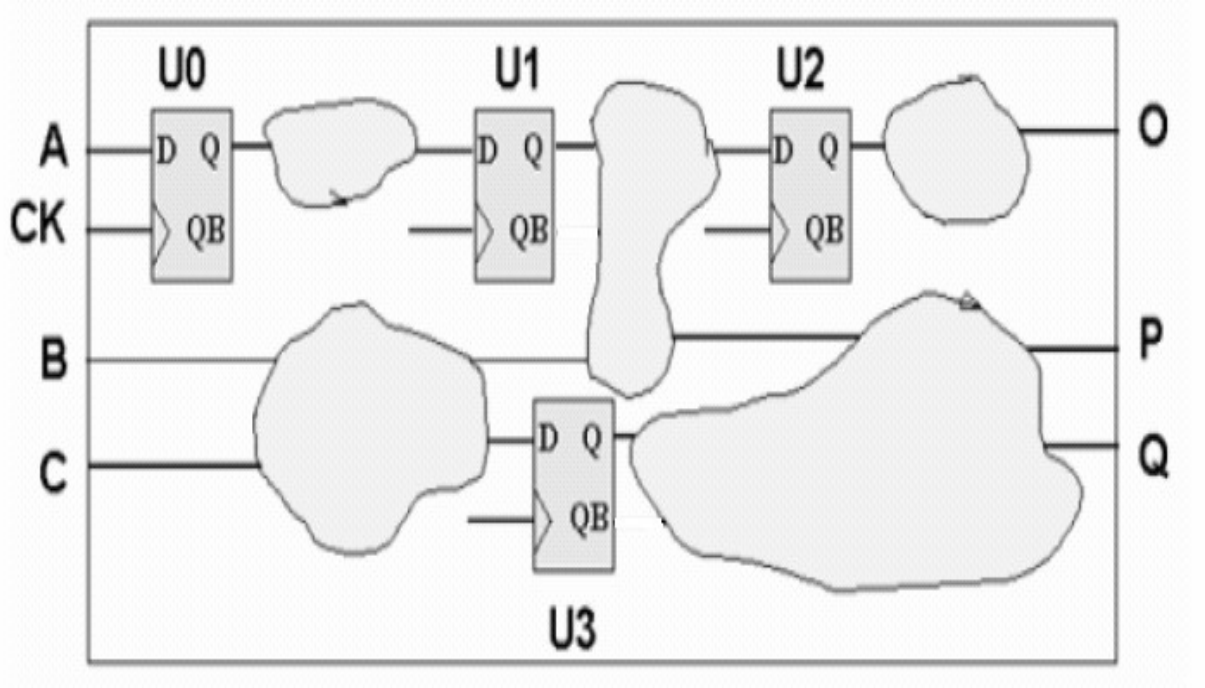


Start Point:
clock pin of sequential device
End Point:
primary output port



Start Point:
primary input port
End Point:
primary output port

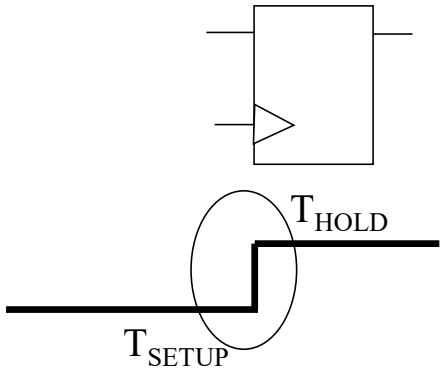
Timing paths



- This circuit has
- How many start points ?
- How many end points ?
- How many paths ?

Timing Terminologies

- Setup Time : Time for which data should be stable at the input of the ff **before** the arrival of clock at the ff's clock pin
- Hold Time : Time for which data should be stable at the input of the ff **after** the arrival of clock at the ff's clock pin



Timing Terminologies

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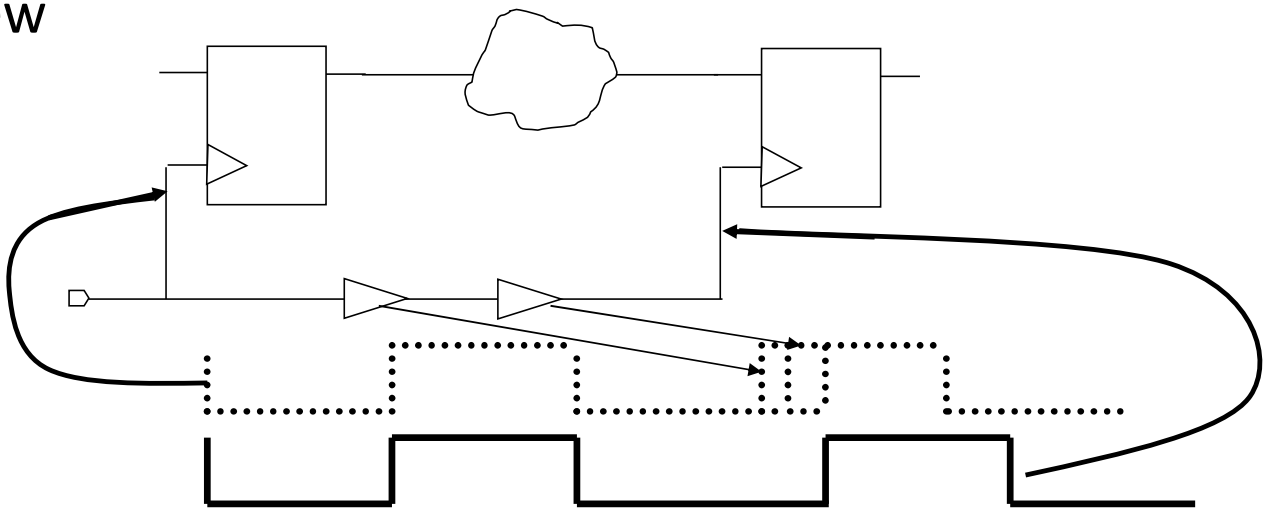
- Critical Path : Theoretically path which has maximum delay
- Arrival Time : Time taken by data to reach a particular end point from a specific start point. Depends on complexity of logic through which data traverses
- Required Time : Time at which data is required at a particular end point. Depends on the requirements / specifications
- Slack : Difference in required time and arrival time. For a design to work the slack value should always be positive

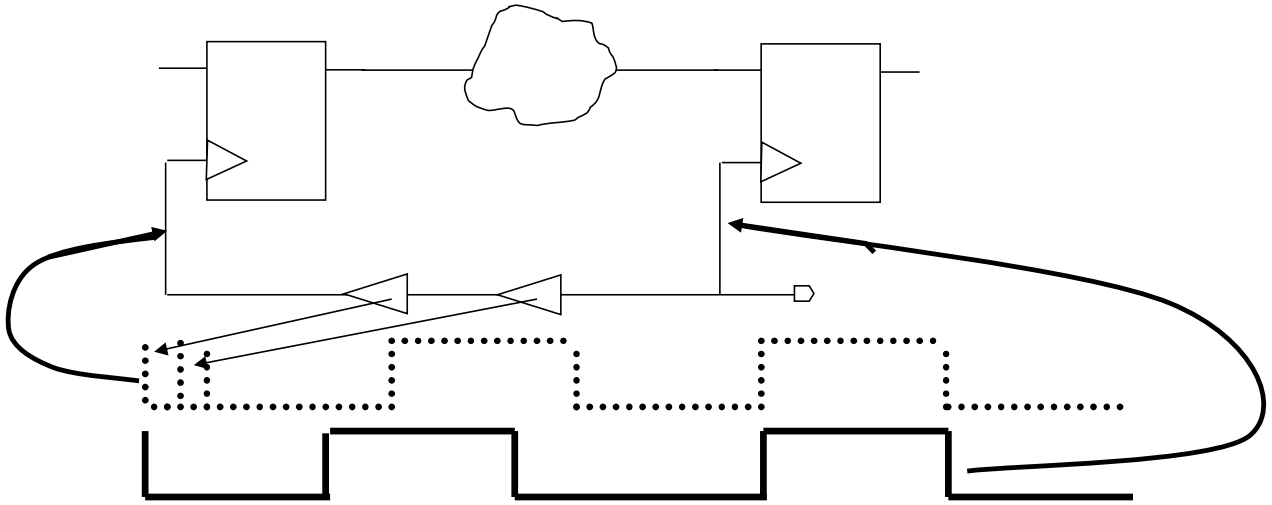
Clock Skew

- Clock feeds multimillion flip-flops
- Theoretically clock should arrive at same instance at all flip-flops – Practically impossible
- Frequency of clock may vary from cycle to cycle
- Variation in arrival of clock at clock pin of subsequent / consecutive flip-flops is known as skew



Clock Skew

- The difference in arrival of clock at different flip-flops could be due to
  - Jitter – cycle to cycle variation in clock period due to aging of oscillator, anomalies in the pll etc
  - Clock network delay – Uncertainty in arrival of clock due to clock network and clock network component delays

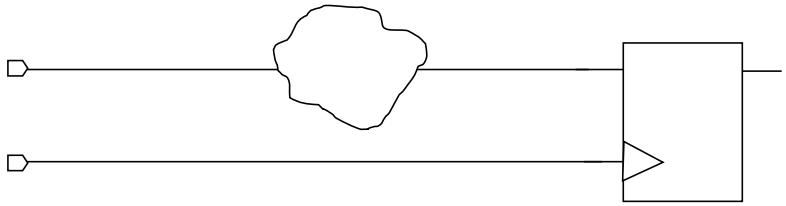


Clock Skew

- Skew can be considered to be of two types
  - When clock arrives earlier than expected – generally known as negative skew
  - When clock arrives later than expected – generally known as positive skew
- +ve skew can occur when data & clock travel in same direction
- -ve skew can occur when data & clock travel in opposite directions

Frequency Calculation

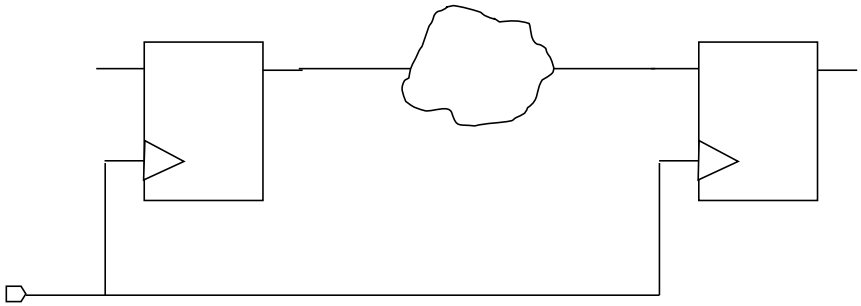
- Arrival Time = $T_{COMBO, Max}$



- Required Time = $T_{CP} + T_{Clock\_Insertion\_Delay} - T_{SETUP}$
  - Since there is only one clock here instead of skew the possible delay on the clock line is denoted as insertion delay

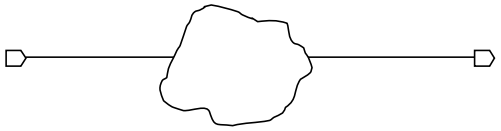
- Arrival Time : $T_{Clk\text{-}Q} + T_{Combo, MAX}$

- Required Time = $T_{CP} + T_{Clock\_Skew} - T_{SETUP}$
  - Due to presence of 2 clocks the possible difference in arrival of clock is denoted as skew



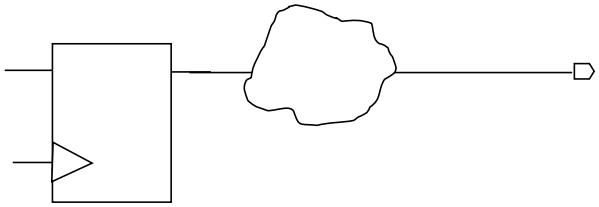
Frequency Calculation

- Arrival Time : $T_{Combo, MAX}$



- Required Time : Explicit Timing Constraint
  (If Specified)

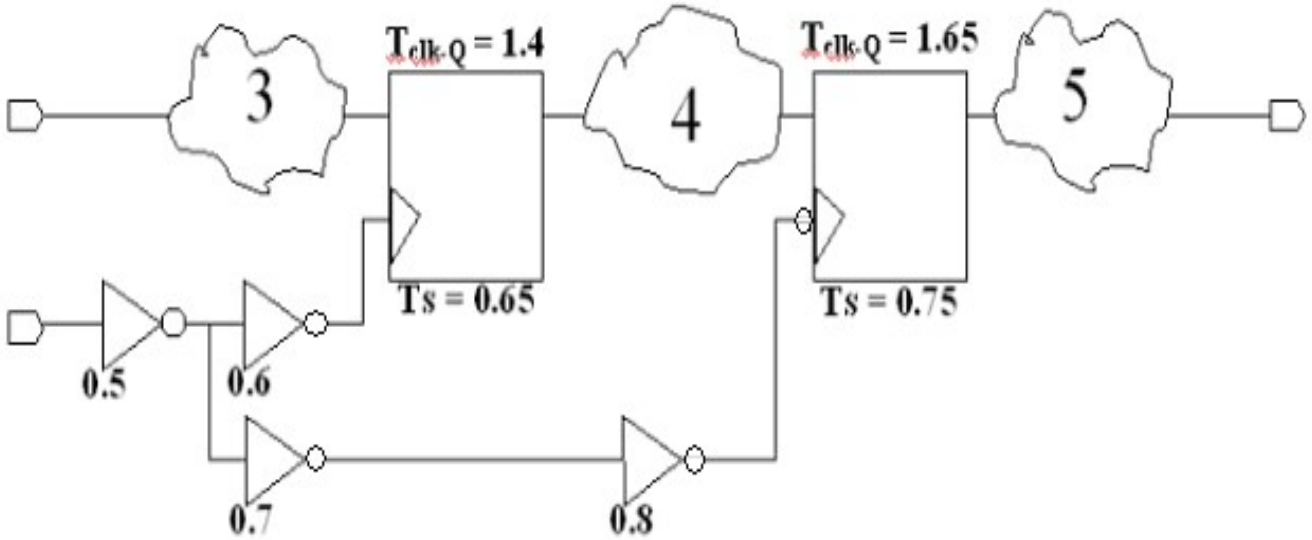
- Arrival Time = $T_{Clk\text{-}Q} + T_{Combo, MAX}$



- Required Time = Typically Unconstrained Path
  (Has no requirement set)

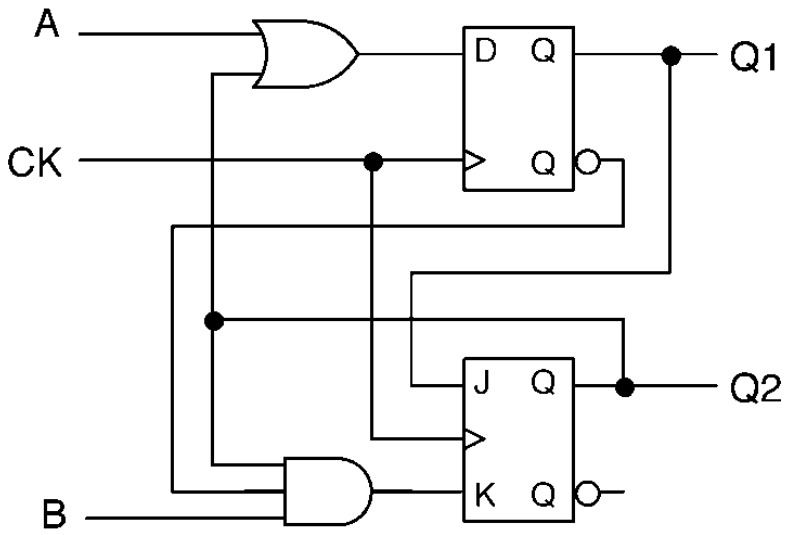
Max Frequency Calculation

- Find The maximum Frequency for the circuit shown in figure below



Max Frequency Calculation

- Find The maximum Frequency for the circuit shown in figure below



	t_P	t_{su}
D Flip-Flop:	20 ns	5 ns
JK Flip-Fllp:	25 ns	10 ns
AND Gate:	12 ns	
OR Gate:	10 ns	

Max Frequency Calculation

- Find the maximum Frequency for the circuit shown in figure below