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Constraints

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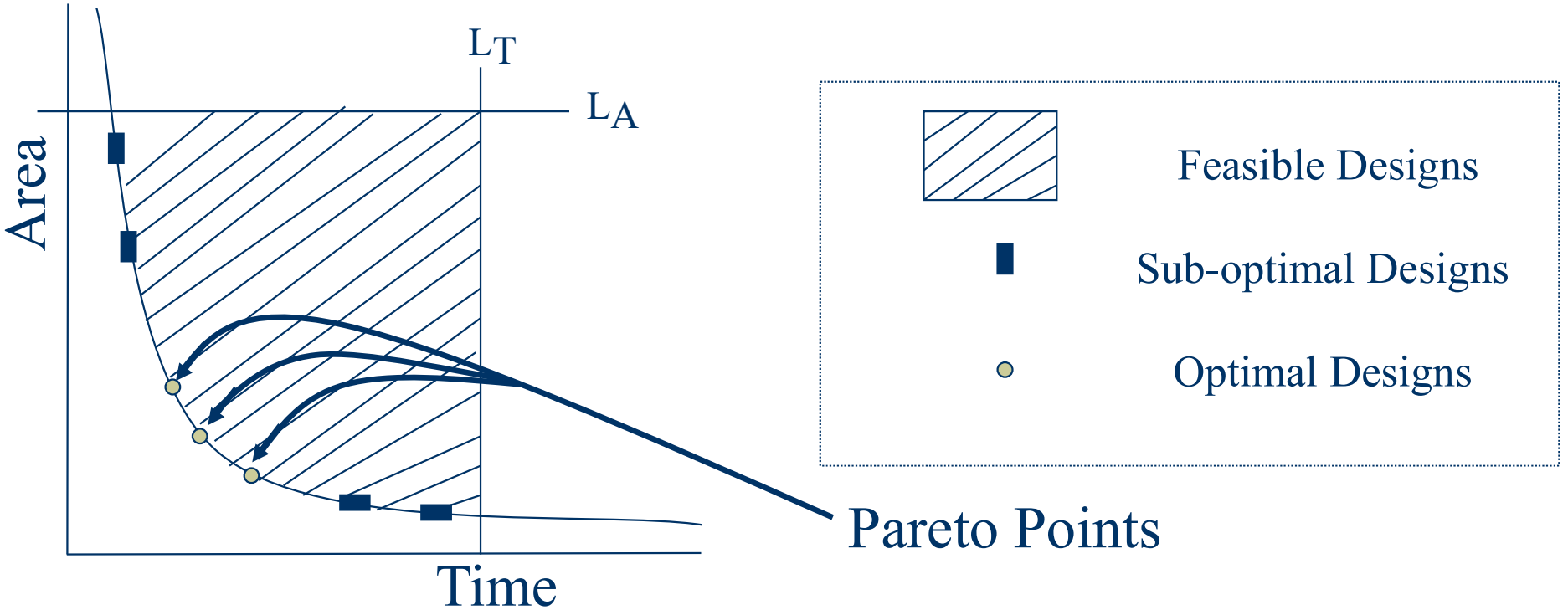
Trade-Off

- Synthesis comprises of developing some hardware to meet certain specifications
- But rarely are all specifications met
- *"You can meet some specifications all of the time, all specifications for some time, but never all specifications all the times"* – adapted from ***Abraham Lincoln***



Constraints

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- Constraints are what ‘specifications’ are normally known as
- They specify the requirements or the expectations from a manufactured device
- Some constraints are technology dependent and exist by default while others are design dependent and decide by the engineer
- Constraints can be broadly categorized under two heads
  - Optimization
  - Design Rule

Environment

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- The characteristics of a Chip depends highly on the environment in which it is working
- The environment restrictions exist on a design but the designer can choose an appropriate one from many
- The environment chosen decides the characteristics of the cells being used
- The three environment constraints are
  - Operating Condition
  - Wire Load Models
  - Wire Load Mode

Operating Condition

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- The effect of PVT the operating conditions on a design has been already seen
- When a IC is being designed it should be ensured that the chip works for both the extremes of the permissible operating conditions
- The power, delay aspects of the design are checked at both the worst and best case conditions
- To ensure that both setup and hold are met both the best and worst operating conditions should be specified
- Operating Condition can be considered as the first and foremost constraint

Wire Load Models

- The delays due to interconnects can account upto 65% of the composite delay of the chip
- The appropriate wire load model chosen is a major factor in calculating wire delays
- Many a times designers use ‘zero wire delay’ model for rapid and easy calculations of net delays
  - Which is as good as ignoring the wire delays
- Wire load models are selected by default based on the area of the circuit being designed
- The ASIC designer can choose a optimistic or pessimistic wire load model from the many available in the libraries

Wire Load Modes

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- The wire delays mainly depend on the wire load mode in consideration
- For hierarchal designs the wire load modes specify as to which wire load model is to be chosen for delay calculation
- Though there may exist a default wire load mode in the library the ASIC designer can again change the wire load mode from one of the below as per the analysis being carried out
  - Top
  - Segmented
  - Enclosed

DRC

- For the proper functioning of a circuit some physical characteristics should be satisfied
- These are known as design rules
- Layouts have design rules like minimum width, minimum spacing etc
- For synthesis to be successful some electrical and physical characteristics should be met such as
  - Transition
  - Fanout
  - Capacitance

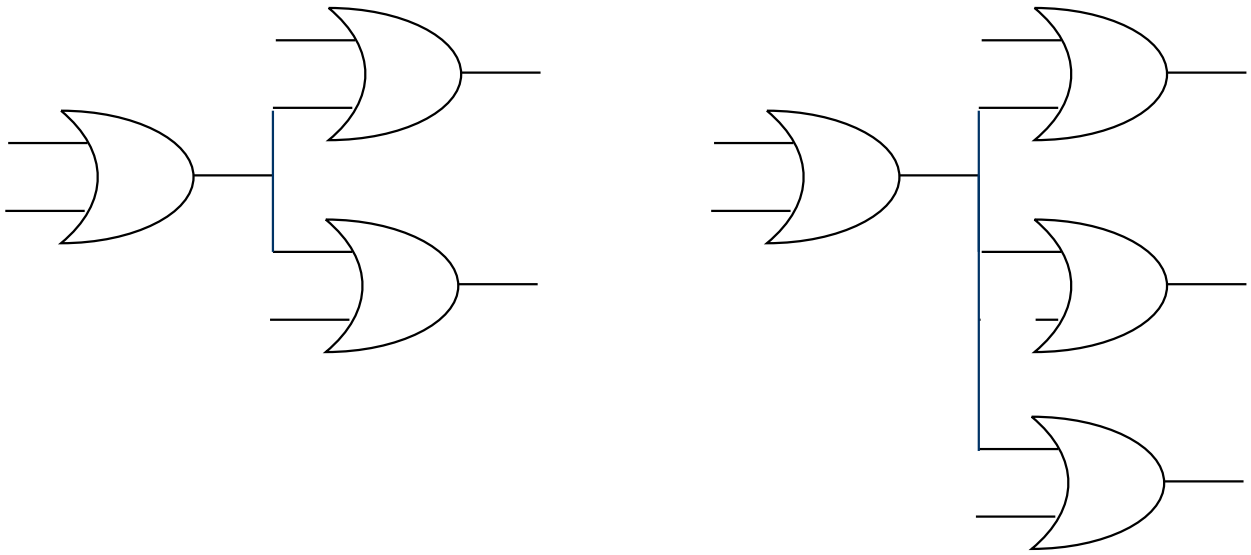
Transition

- The propagation delay of a gate is very much dependent on the time taken for data to switch from high to low or vice-versa
- The time taken for data to switch from high-low or vice-versa known as transition time depends mainly on
  - Load Capacitance
  - Wire length / characteristics - RC
  - Junction Capacitance of cell

Transition

- If the allowable transition time is restricted the design performance will increase significantly
- Every Gate and wire will have its own transition time
- By specifying appropriate constraint we can ensure that only those components are chosen that transit faster

Fanout



- In the above figure assuming that the same kind of ‘OR’ gates being used throughout
  - If input were provided at time 0 which of the 5 outputs would be faster?

Fanout

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- The delay of a system depends on the type of cells that are being used in the circuit
- Cells with high drive strength are required to efficiently drive high loads
- Cells with high drive strengths have more width and hence offer more capacitance

Limiting Fanout

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- Layman explanation
  - *The number of gates a the output pin of cell can drive*
  - *The number of 'nand' gates that a cell can drive*
  - *The number of 'equivalent' gates that a cell can drive*
- Fanout is the measure of the ability of a logic gate output to drive a number of inputs of some other logic gates
- Every input pin of a gate has a *'fanout_load'* attribute specified in the library

Limiting Fanout

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- Every output pin of a gate has a *'max_fanout'* attribute specified
- The sum of all the fanout_loads of all the driven cells should not exceed the max_fanout attribute of the output pin of the driving cell
- It can be ensured that only specific cells are chosen which have a lower max_fanout attribute

Capacitance

- The transition as well as the fanout capacity are explicitly or implicitly dependent on the capacitance of the components
- By limiting the maximum capacitance in the circuit there can be made an attempt in improving the delay
- Capacitance, Transition and Fanout are the major Design rule constraints which need to be taken care of during synthesis
- They monitor the buffering of the design

Optimization Constraints

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- The DRC exists on a design inherently
- When a designer does not specify DRC explicitly the values from the libraries are used while choosing the cells
- DRC constraints are imposed upon the design by requirements specified in the technology library
- Optimization constraints are the ones which convey the specifications of the design
  - Area
  - Power
  - Timing

Area Constraints

- In ASIC front end process ‘area’ refers to the sum of the cell areas + sum of wire areas
- Chip area depends on placement of cells and routing area
- Placement and routing are done down the flow hence can not be estimated up-front

Area Constraints

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- Every cell has an area attribute set in the library
- Design area is actually sum of all such cell areas and nett wire area (if provided in the library)
- The maximum as well as minimum limit on the area of a design can be set
- It has the least priority of all constraints

Low Power

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- Two kinds of Power needs to be looked into
  - Dynamic
  - Static / Leakage
- Dynamic power dissipation can be affected by the following factors
  - V_{DD}
  - Material Used
  - Switching
  - Short Circuit Current
  - Clock Gating
  - Operation Isolation

Power Optimization

- Leakage Power can be optimized by
  - Multiple Threshold Voltages
  - Power Gating
- Power Depends on supply Voltage
- By reducing supply voltage power dissipation can be reduced
  - But decrease in supply voltage leads to increase in delay
  - Fine balance has to be created
  - Level shifters required
- Power depends on material used to fabricate the IC
- New technologies like Silicon-On-Insulator help in power optimization

Power Optimization

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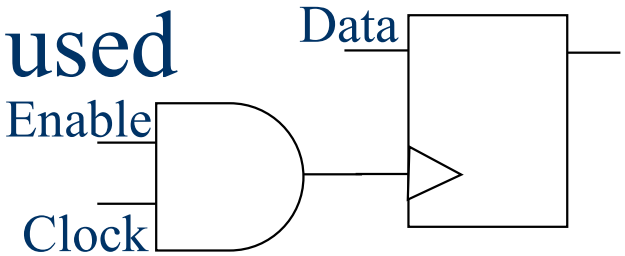
- Major component of power dissipation is due to switching
- The transitions of signal from high-low and vice versa causes capacitances to charge and discharge
- Power dissipation is huge during these cycles
- Depending on the rate of transition short circuit current also contributes to power dissipation
- This kind of power can be optimized by ensuring minimum switching
- Can be accounted for at the architecture level

Power Optimization

- During the operation of a circuit all registers are not active all the time
- Clock transition also contributes largely to power dissipation
- The clock to those flops which are not active can be switched of by clock gating
- By far the most dominant power optimization technique used



Leakage Power

- At VDSM technologies Leakage power constitutes a large percent of the total power dissipation
- Leakage power dissipation can be reduced by increasing threshold Voltage
- Increase in threshold voltage leads to increase in delay of the cell
  - Fine balance has to be created
- By ensuring that blocks which are not functionally required are switched off leakage current can be minimized
  - Known as power gating
  - Isolation cells , retention registers required

Constraints for Low Power

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- Among all the low power methodologies discussed so far it can be seen that power optimization requires
  - usage of proper libraries
  - efficient architecture
  - appropriate materials
- It can be seen that at the synthesis level scope for power optimization is limited
- The major power optimizations done during synthesis are
  - Clock Gating
  - Multi V_{TH} Synthesis

Timing Constraints

- Synthesis can be considered as the process of choosing appropriate cells that meet the required specifications
- Unless otherwise specified the goal of synthesis is Timing Optimization
- Synthesis is timing driven and among all optimization constraints timing has highest priority
- All designs are sequential in nature and invariably have a clock
- Among all timing constraints the most important is that concerning the clock

Clock

- The most important aspect of the clock is its frequency
- Clock is that net which runs throughout the design and feeds all the flip-flops
- The load on the clock being huge a real clock will not be square wave in nature but will have a finite transition time
- Again due to the load as well as due to other reasons the time at which clock arrives at two flip-flops will not be the same – Skew
- Skew can be advantageous as well as disadvantageous depending on the kind of analysis being carried out
- The clock may either come early or late

Insertion Delay

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- Many modules together comprise a design
- Each of them may have their own clocks or share the same clock
- Designs will not have many oscillators / PLLs
- Same oscillator / PLL will be used to generate multiple clocks and then fed to the modules

Insertion Delay

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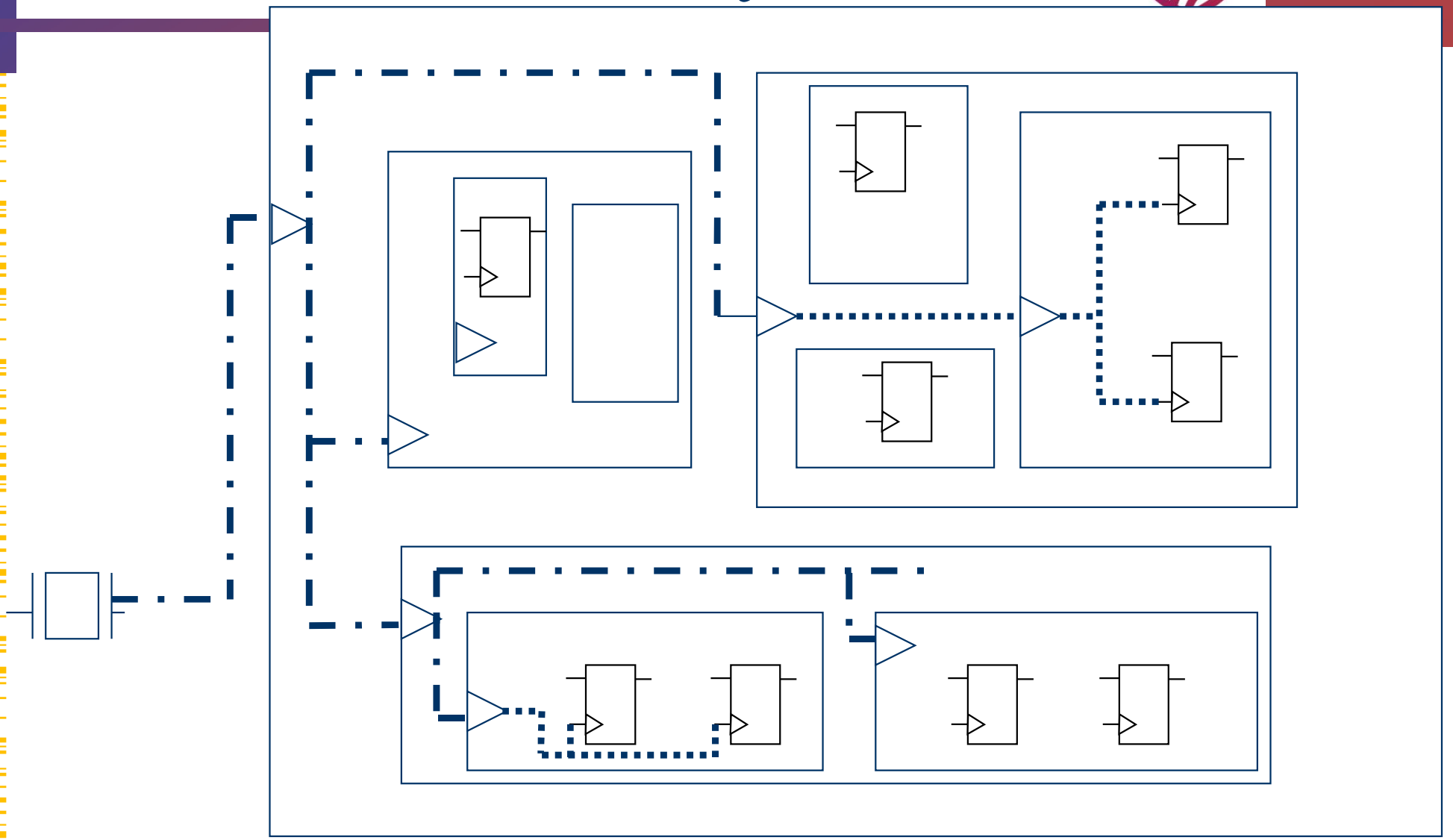
- The difference in arrival of clock from the point of origin to the point of definition is known as clock insertion delay
- The difference (when external to the module being designed) is called as clock source insertion delay
- The difference (when internal to the module being designed) is known as clock network insertion delay

Insertion Delay



Source Insertion Delay

Network Insertion Delay

Clock Constraint

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- The clock related constraints that should be provided are
  - Frequency
  - Duty Cycle
- The clock related information that can be provided are
  - Transition
  - Skew
    - Early
    - Late
  - Insertion Delay
    - Source
    - Network

External Delay

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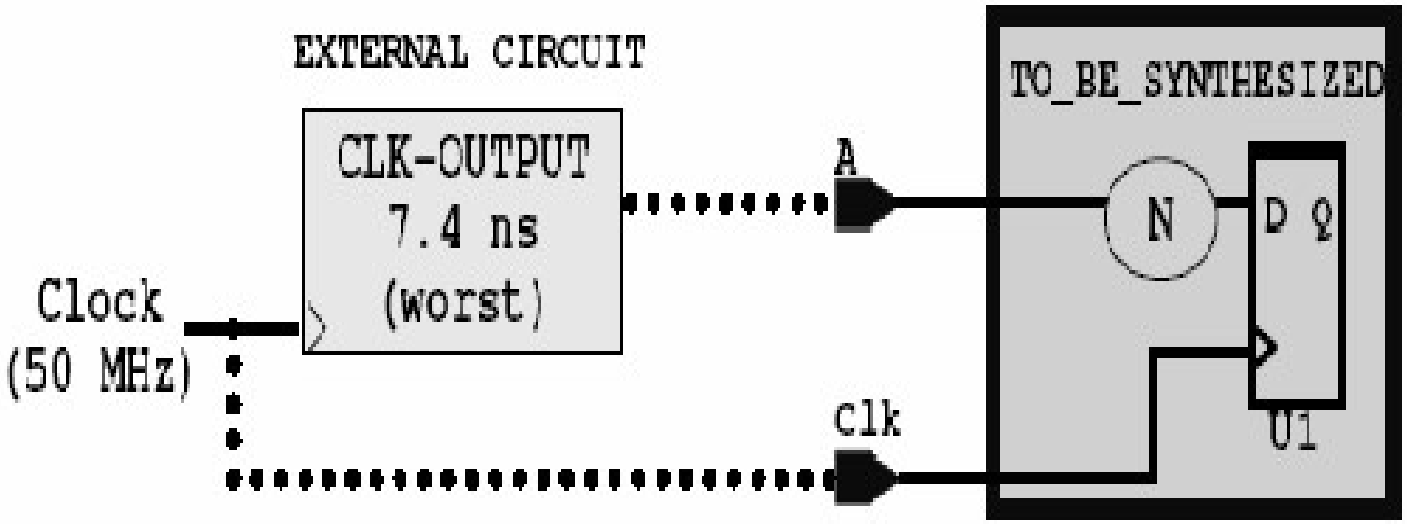
- Complete IC need not be synthesized by same team or at the same time
- Modules designed one after the other
- A module might work well in isolation – not sufficient
- Should work well even after top level integration
- External delay information needs to be provided while synthesizing the design
- The external delay could be both at the input as well as the output of the circuit being designed
- Both Input external delay as well as output external delay information need to be provided

Input External Delay

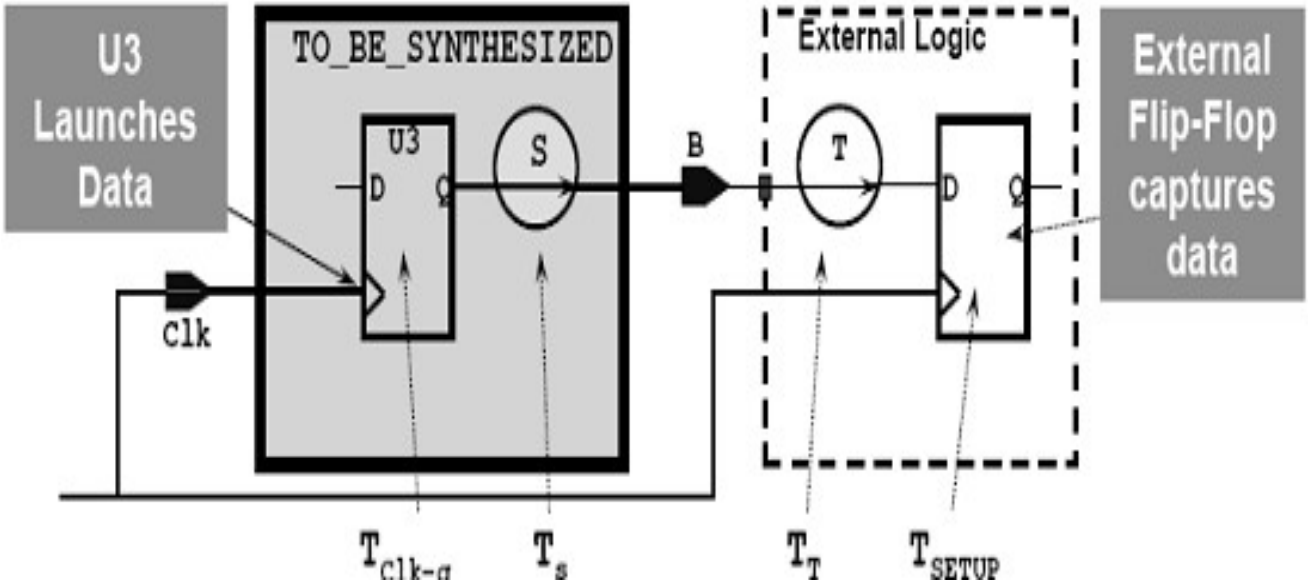
- A input external delay information helps in optimizing the logic between the input and the first flip-flop
- Typically affects input -> reg paths



- In design above an optimization will be attempted on logic ‘N’ so that it can accommodate the external delay of 7.4 ns

Output External delay

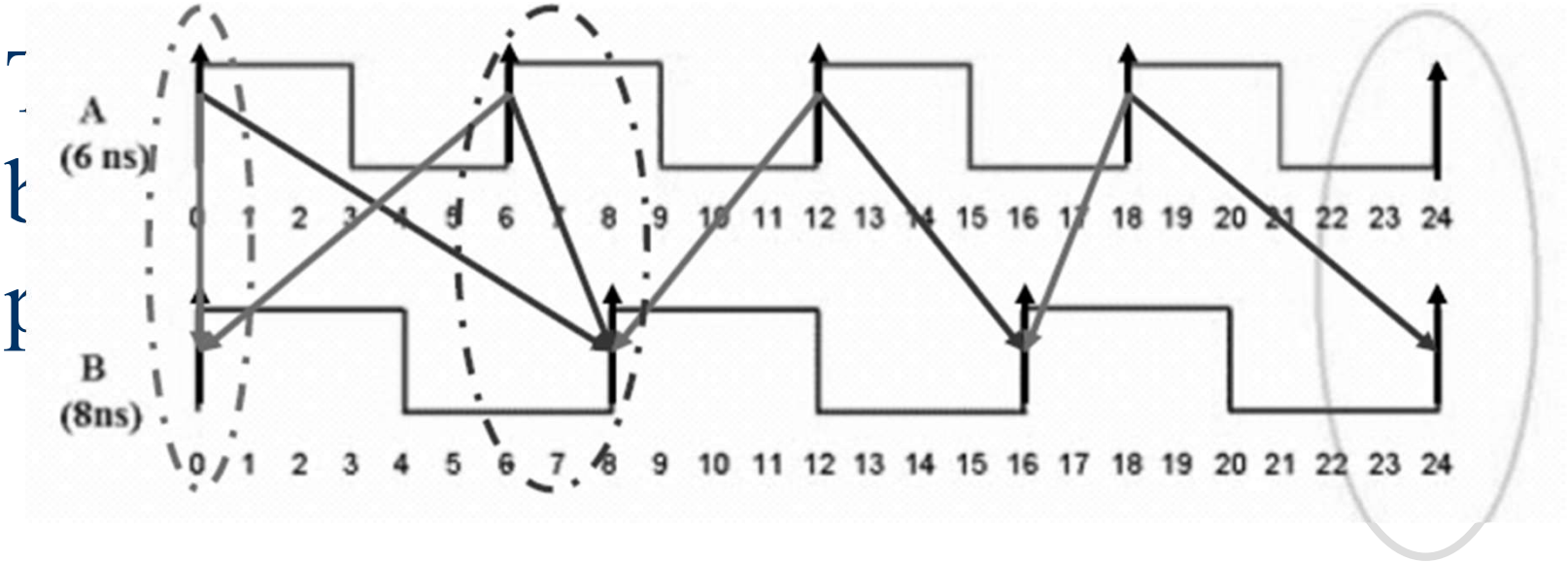
- An output external delay information helps in optimizing the logic between the last flip-flop / register bank and the output
- May affect reg -> Out paths



- In design above an optimization will be attempted on logic ‘S’ so that it can accommodate the external delay provided by the logic ‘T’

Multiple Clock Analysis

- Determine the least common multiple (LCM) of the 2 clock periods first
- The setup relationship is the closest distance between the launching clock edge (A) and the capturing clock edge (B)
- T
  k
  l



Timing Exceptions

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- In any given design the data once launched at the start point is expected at the end point within one clock cycle
- All paths are considered as single cycle paths
- There may be times where it may be required for data to arrive much earlier than the normal single clock cycle
- Any path which has a more restrictive timing constraint than one clock cycle is known to be having Timing exception

Point - Point Exceptions

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- When the exception is between Input -> reg known as point – clock exception
- When the exception is between reg -> out path known as clock – point exception
- When the exception is between input –> output known as point – point exception

DRC Constraints

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- Environment
  - set_min_library tcb013ghplvtwc.db –min_version tcb013ghplvtbc.db
  - set_operating_conditions WCCOM
  - set_wire_load_model FORQA
  - set_wire_load_mode TOP
- DRC
  - set_max_transition 0.01 [current_design]
  - set_max_fanout 5 [current_design]
  - set_max_capacitance 0.05 [current_design]

Optimization Constraints

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- Area
  - set_max_area 3000
  - set_min_area 0
- Power
  - set_max_dynamic_power 20 mw
  - set_max_leakage_power 10 uw
- Timing
  - create_clock –period 4 –waveform {1 0} –name master_clock
  - set_clock_transition 0.04 master_clock
  - set_clock_uncertainty –setup 0.4 master_clock
  - set_clock_uncertainty –hold 0.2 master_clock
  - set_clock_latency –network 0.35 master_clock

Hierarchy of constraints

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- The following are the hierarchy of constraints
  - Min Capacitance
  - Max Transition
  - Max Fanout
  - Max Capacitance
  - Max Delay
  - Min Delay
  - Max Power
  - Max Area

Exceptions

- Exceptions
  - set_max_delay 3 –from [all_inputs] –to [all_outputs]
    - applies to all the logic which lies in the path from input to output
    - If there is no path from input to output constraint is ignored
  - set_max_delay 2 –from [all_inputs]
    - applies to all paths which start from the input
    - Can be input to output path as well as input -> reg path
  - set_max_delay 1.8 –to [all_outputs]
    - applies to all paths ending at the output
    - can be input to output paths as well as reg -> output paths
- External Delay Information
  - set_input_delay 1 [all_inputs]
  - set_output_delay 1 [all_outputs] –clock master_clock

Constraints