

ECE132: Basic Electrical and Electronics Engineering Lab

Experiment 9:

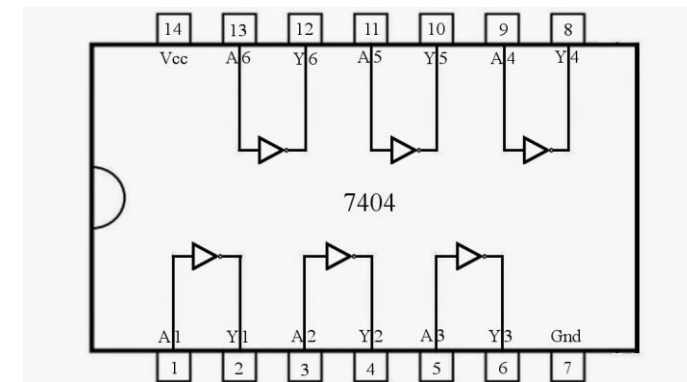
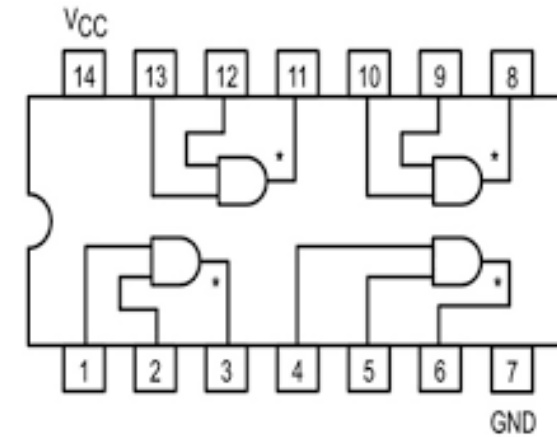
To understand Truth table of Logic gates and verifying the Boolean equations.

Introduction to Logic Gates







- Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship between the input and the output is based on a certain logic. Based on this, logic gates are named as AND gate, OR gate, NOT gate etc.

Introduction to Logic Gates

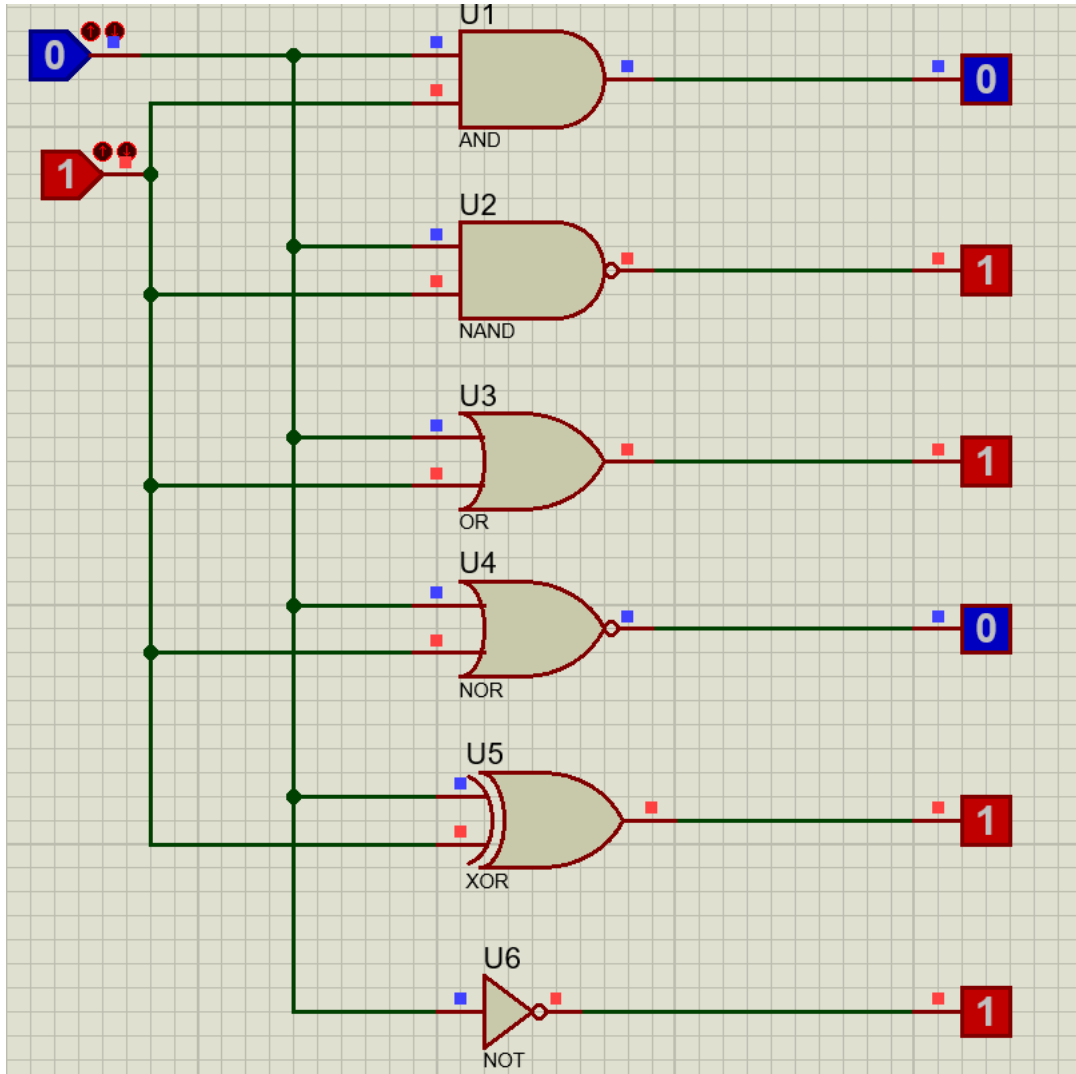
| Sr. No. | Component | Specification |
|---------|-----------|---------------|
| 1 | AND Gate | IC7408 |
| 2 | OR Gate | IC 7432 |
| 3 | NOT Gate | IC7404 |
| 4 | NAND Gate | IC7400 |
| 5 | NOR Gate | IC7402 |
| 6 | XOR Gate | IC7486 |



Introduction to Logic Gates

| Logic | Schematic | Boolean Expression | Truth Table | English Expression | | | | | | | | | | | | | | | |
|-------|---|----------------------------|--|--------------------|---|---|---|---|--|--|---|--|---|---|--|---|---|--|---|
| AND |  | $A \bullet B=Y$ | <table><tr><th>A</th><th>B</th><th>Y</th></tr><tr><td>0</td><td>0</td><td></td></tr><tr><td>0</td><td>1</td><td></td></tr><tr><td>1</td><td>0</td><td></td></tr><tr><td>1</td><td>1</td><td></td></tr></table> | A | B | Y | 0 | 0 | | 0 | 1 | | 1 | 0 | | 1 | 1 | | The only time the output is positive is when all the inputs are positive. |
| A | B | Y | | | | | | | | | | | | | | | | | |
| 0 | 0 | | | | | | | | | | | | | | | | | | |
| 0 | 1 | | | | | | | | | | | | | | | | | | |
| 1 | 0 | | | | | | | | | | | | | | | | | | |
| 1 | 1 | | | | | | | | | | | | | | | | | | |
| OR |  | $A+B=Y$ | <table><tr><th>A</th><th>B</th><th>Y</th></tr><tr><td>0</td><td>0</td><td></td></tr><tr><td>0</td><td>1</td><td></td></tr><tr><td>1</td><td>0</td><td></td></tr><tr><td>1</td><td>1</td><td></td></tr></table> | A | B | Y | 0 | 0 | | 0 | 1 | | 1 | 0 | | 1 | 1 | | The output will be positive when any one or all inputs are positive. |
| A | B | Y | | | | | | | | | | | | | | | | | |
| 0 | 0 | | | | | | | | | | | | | | | | | | |
| 0 | 1 | | | | | | | | | | | | | | | | | | |
| 1 | 0 | | | | | | | | | | | | | | | | | | |
| 1 | 1 | | | | | | | | | | | | | | | | | | |
| XOR |  | $A\oplus B=Y$ | <table><tr><th>A</th><th>B</th><th>Y</th></tr><tr><td>0</td><td>0</td><td></td></tr><tr><td>0</td><td>1</td><td></td></tr><tr><td>1</td><td>0</td><td></td></tr><tr><td>1</td><td>1</td><td></td></tr></table> | A | B | Y | 0 | 0 | | 0 | 1 | | 1 | 0 | | 1 | 1 | | The only time the output is positive is when the inputs are not the same. |
| A | B | Y | | | | | | | | | | | | | | | | | |
| 0 | 0 | | | | | | | | | | | | | | | | | | |
| 0 | 1 | | | | | | | | | | | | | | | | | | |
| 1 | 0 | | | | | | | | | | | | | | | | | | |
| 1 | 1 | | | | | | | | | | | | | | | | | | |
| NOT |  | $\bar{A}=Y$ | <table><tr><th>A</th><th>Y</th></tr><tr><td>0</td><td></td></tr><tr><td>1</td><td></td></tr></table> | A | Y | 0 | | 1 | | The output is the opposite of the input. | | | | | | | | | |
| A | Y | | | | | | | | | | | | | | | | | | |
| 0 | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | |
| NAND |  | $\overline{A \bullet B}=Y$ | <table><tr><th>A</th><th>B</th><th>Y</th></tr><tr><td>0</td><td>0</td><td></td></tr><tr><td>0</td><td>1</td><td></td></tr><tr><td>1</td><td>0</td><td></td></tr><tr><td>1</td><td>1</td><td></td></tr></table> | A | B | Y | 0 | 0 | | 0 | 1 | | 1 | 0 | | 1 | 1 | | The output is positive provided all the inputs are not positive. |
| A | B | Y | | | | | | | | | | | | | | | | | |
| 0 | 0 | | | | | | | | | | | | | | | | | | |
| 0 | 1 | | | | | | | | | | | | | | | | | | |
| 1 | 0 | | | | | | | | | | | | | | | | | | |
| 1 | 1 | | | | | | | | | | | | | | | | | | |
| NOR |  | $\overline{A+B}=Y$ | <table><tr><th>A</th><th>B</th><th>Y</th></tr><tr><td>0</td><td>0</td><td></td></tr><tr><td>0</td><td>1</td><td></td></tr><tr><td>1</td><td>0</td><td></td></tr><tr><td>1</td><td>1</td><td></td></tr></table> | A | B | Y | 0 | 0 | | 0 | 1 | | 1 | 0 | | 1 | 1 | | The only time the output is positive is when all the inputs are negative. |
| A | B | Y | | | | | | | | | | | | | | | | | |
| 0 | 0 | | | | | | | | | | | | | | | | | | |
| 0 | 1 | | | | | | | | | | | | | | | | | | |
| 1 | 0 | | | | | | | | | | | | | | | | | | |
| 1 | 1 | | | | | | | | | | | | | | | | | | |

Simulation



Observation and Calculation

Truth Table

| Input A | Input B | Output |
|---------|---------|--------|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

THANKS TO ALL