Unit -6

Memory

PLD

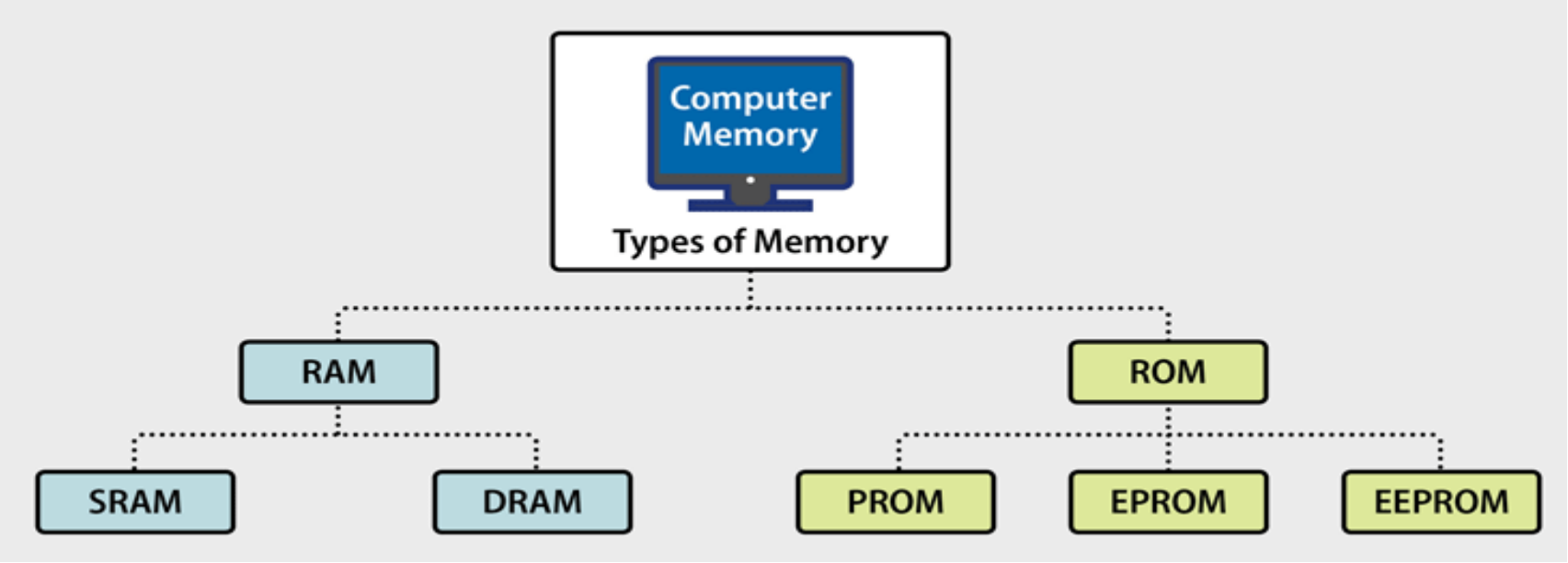
Converters ADC-DAC

Memory

Memory is the most essential element of a computing system because without it computer can’t perform tasks.

Computer memory is of two basic type – Primary memory(RAM and ROM) and Secondary memory(hard drive, CD,etc.)

Random Access Memory (RAM) is volatile memory and Read Only Memory (ROM) is non-volatile memory.



Random Access Memory (RAM)

Read write memory

The programs and data that the CPU requires during execution of a program are stored in RAM

It is a volatile memory as the data loses when the power is turned off.

Further classified into two types-

SRAM (Static Random Access Memory)

DRAM (Dynamic Random Access Memory)

Read Only Memory (ROM)

Stores crucial information essential to operate the system, like the program essential to boot the computer.

It is non volatile.

Always retains its data.

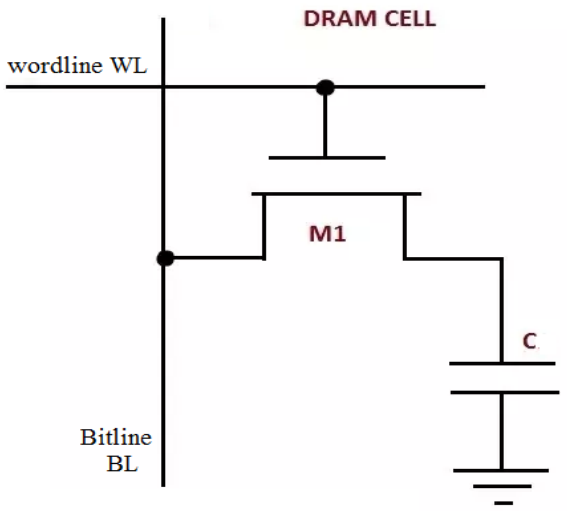
Used in embedded systems or where the programming needs no change.

Used in calculators and peripheral devices.

ROM is classified into 4 types- *ROM*, *PROM*, *EPROM*, and *EEPROM*.

RAM	ROM
1. Temporary Storage.	1. Permanent storage.
2. Store data in MBs.	2. Store data in GBs.
3. Volatile.	3. Non-volatile.
4.Used in normal operations.	4. Used for startup process of computer.

DRAM Cell – Read Write



DRAM Cell single transistor that is paired with a capacitor (1T1C)

DRAMs store data in cells that depend on capacitors, which need to be 'refreshed'

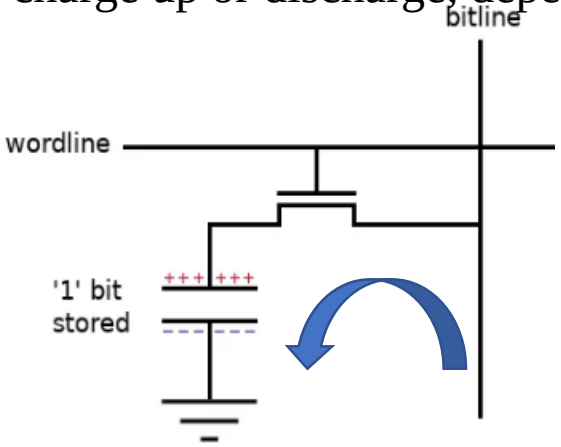
A bit in DRAM can be stored as the presence or absence of charge on a capacitor.

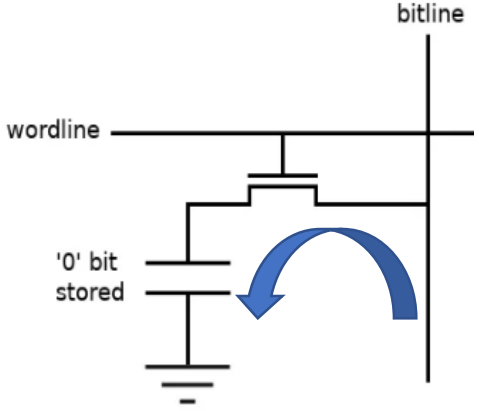
DRAM IC has address lines, data lines, and control lines.

Word lines identify the location of the memory cell to be read from or written Bit lines contain the value of the data read or being written

Write operation

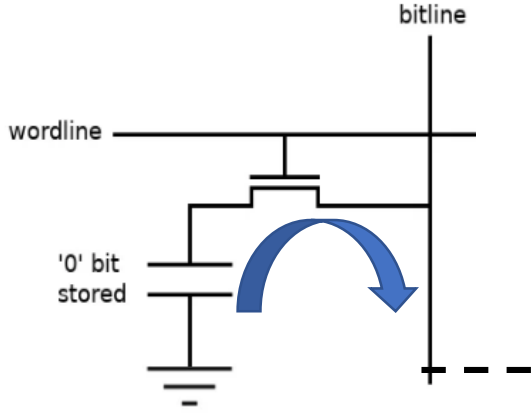
Data to be written ('1' or '0') is provided at the 'bit' line
word line turns on the transistor and allows the capacitor to charge up or discharge, depending on the state of the bit line.



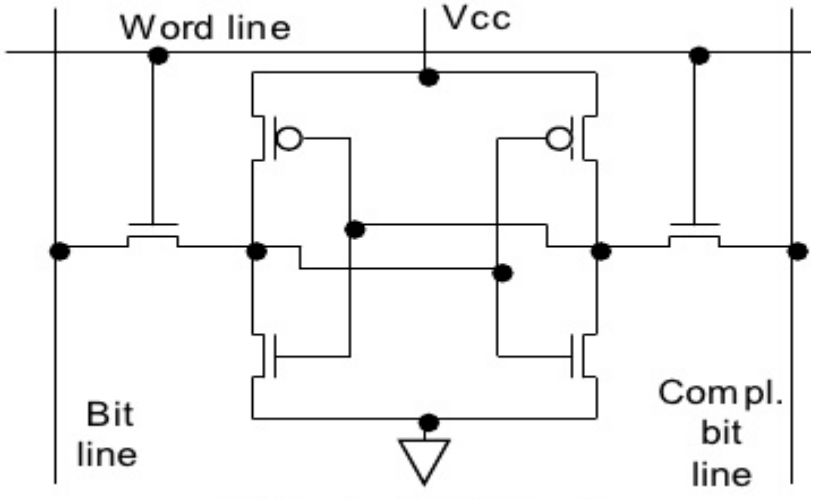


Read operation

Word line turns on the access transistor.
Transistor allows the voltage on the capacitor to be read by a sensitive amplifier circuit through the 'bit' line.
sense circuit determine whether a '1' or '0' in the memory cell by comparing the sensed capacitor voltage against a threshold



SRAM Cell Read Write



6 Transistor (6T Cell)

stored data can be retained indefinitely, as long as the power supply is on, without need for periodic refresh operation

one-bit memory cell

Read

1. WL = 1
2. Access transistors are turned ON
3. BL and BL_bar values are read by Sense Amplifier

Write

1. WL = 1
2. Access transistors are turned ON
3. BL and BL_bar values are stored in cell

Parameter	SRAM	DRAM
Construction	Complex	Simple
Number of Transistors Required	6	1
Charge Leakage	No	Yes
Refreshing	Not Required	Needed periodically
Speed	Faster	Slower
Size	Smaller	Larger
Cost	Expensive	Cheap
Application	Cache Memory	Main Memory
Power Consumption	Higher	Lower
Density	Low	High
Capacity	LOw	High

PLD (Programmable Logic Devices)

An electronic component used to build reconfigurable digital circuits

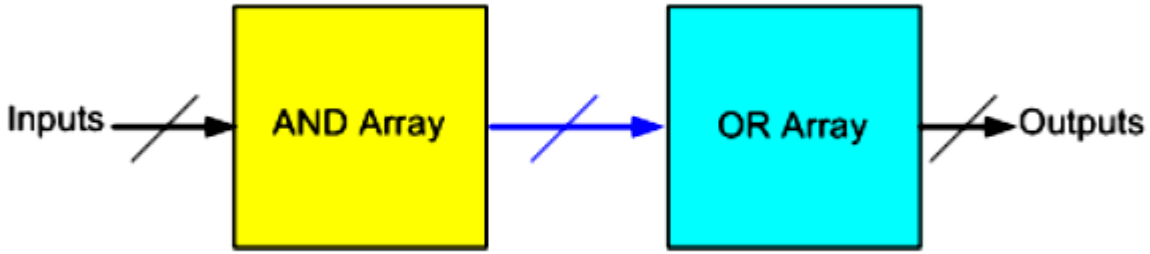
Contain an array of AND gates & another array of OR gate with programmable features

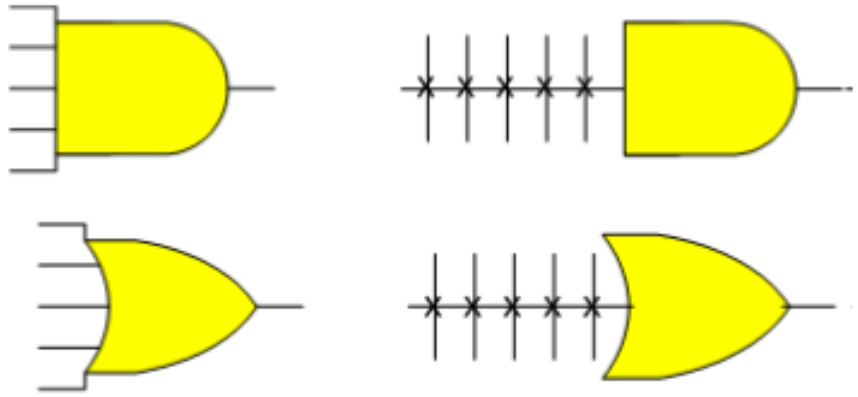
internal logic gates or connections of PLDs can be changed or configured by a programming process

simplest programming technologies is **to use fuses**

3 Type of PLD are

- Programmable Array Logic
- Programmable Logic Array
- Programmable Read Only Memory





Advantages of using PLDs

less board space, faster, lower power requirements, less costly assembly processes, higher reliability, availability of design software

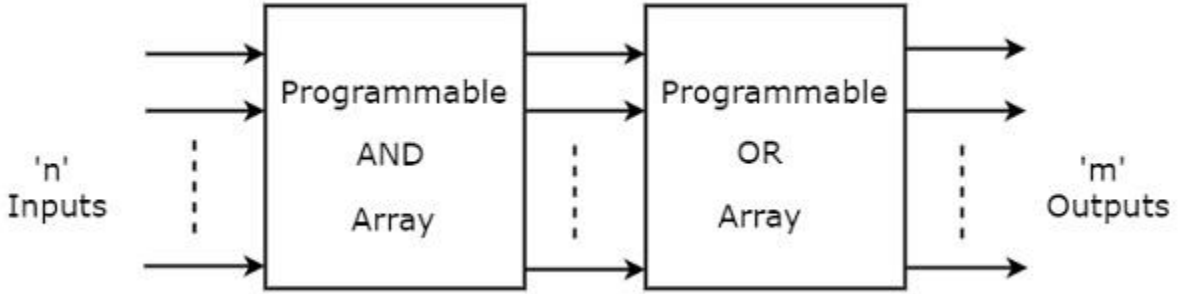
Programmable Logic Array PLA

Both Programmable AND array & Programmable OR array

Programmable AND array generates product term and programmable OR array generate sum term

A PLA output in SOP format

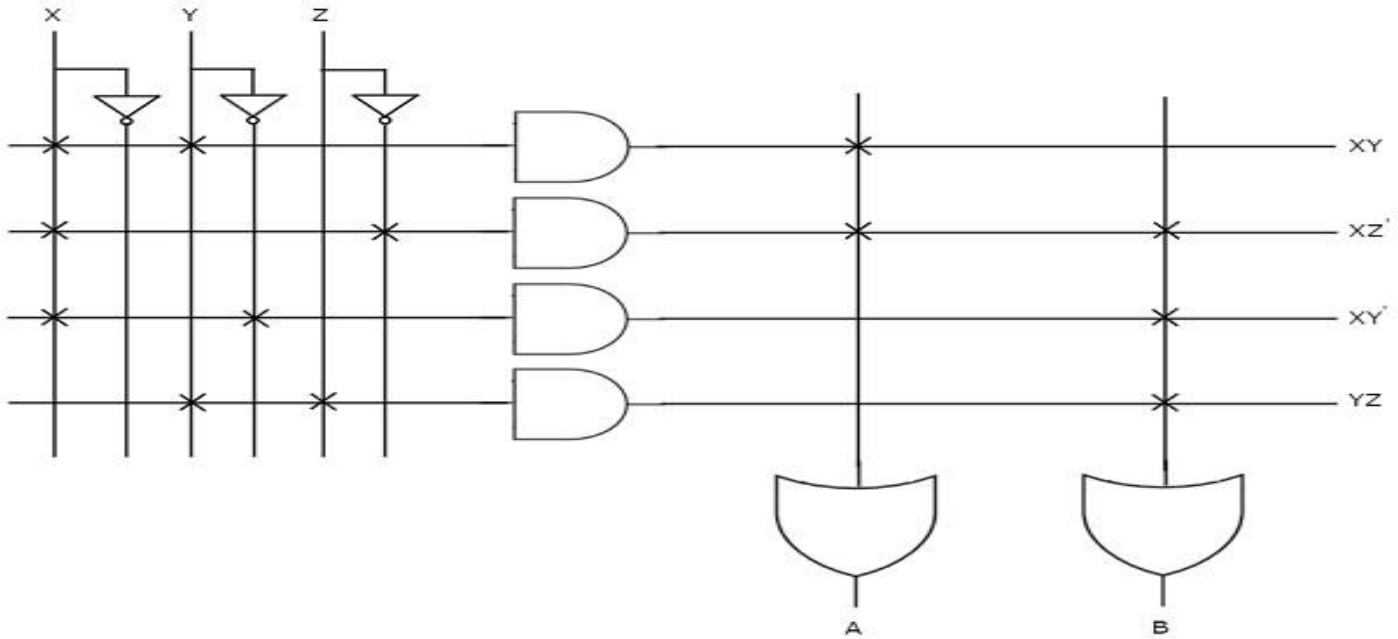
The symbol ‘X ’ is used for programmable connections



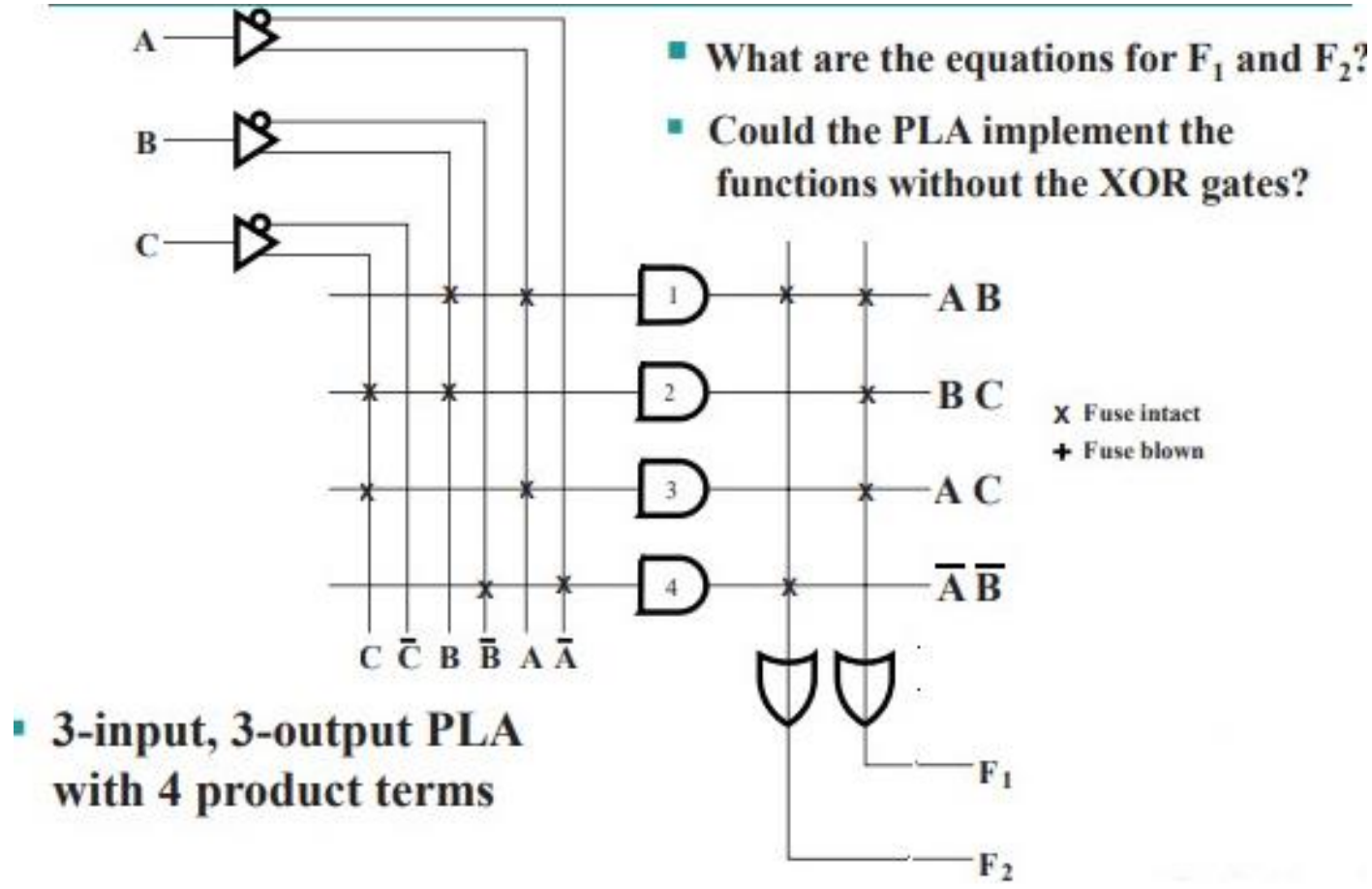
Implement the following equation using PLA

A=XY+XZ’

B=XY’+YZ+XZ’



PLA Example



- What are the equations for F_1 and F_2?
- Could the PLA implement the functions without the XOR gates?

- 3-input, 3-output PLA with 4 product terms

Implement the following functions using PLA

F0 = A + B' C'
F1 = A C' + A B
F2 = B' C' + A B
F3 = B' C + A

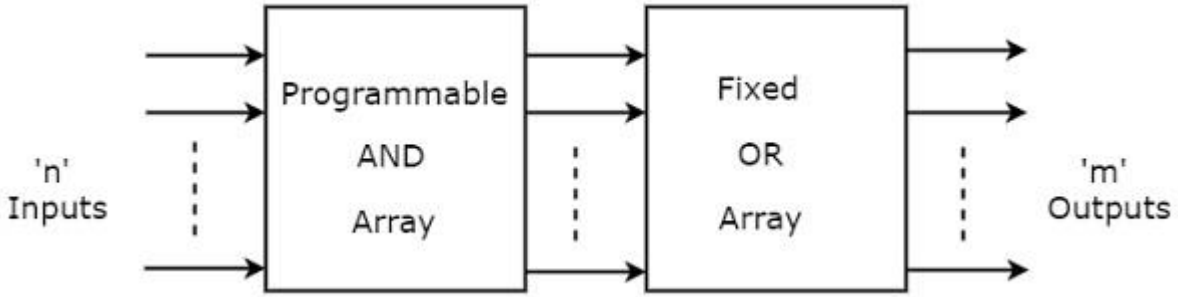
Programming Array Logic

Programmable AND array generates product term

Fixed OR array generates sum

Output of PAL are SOP

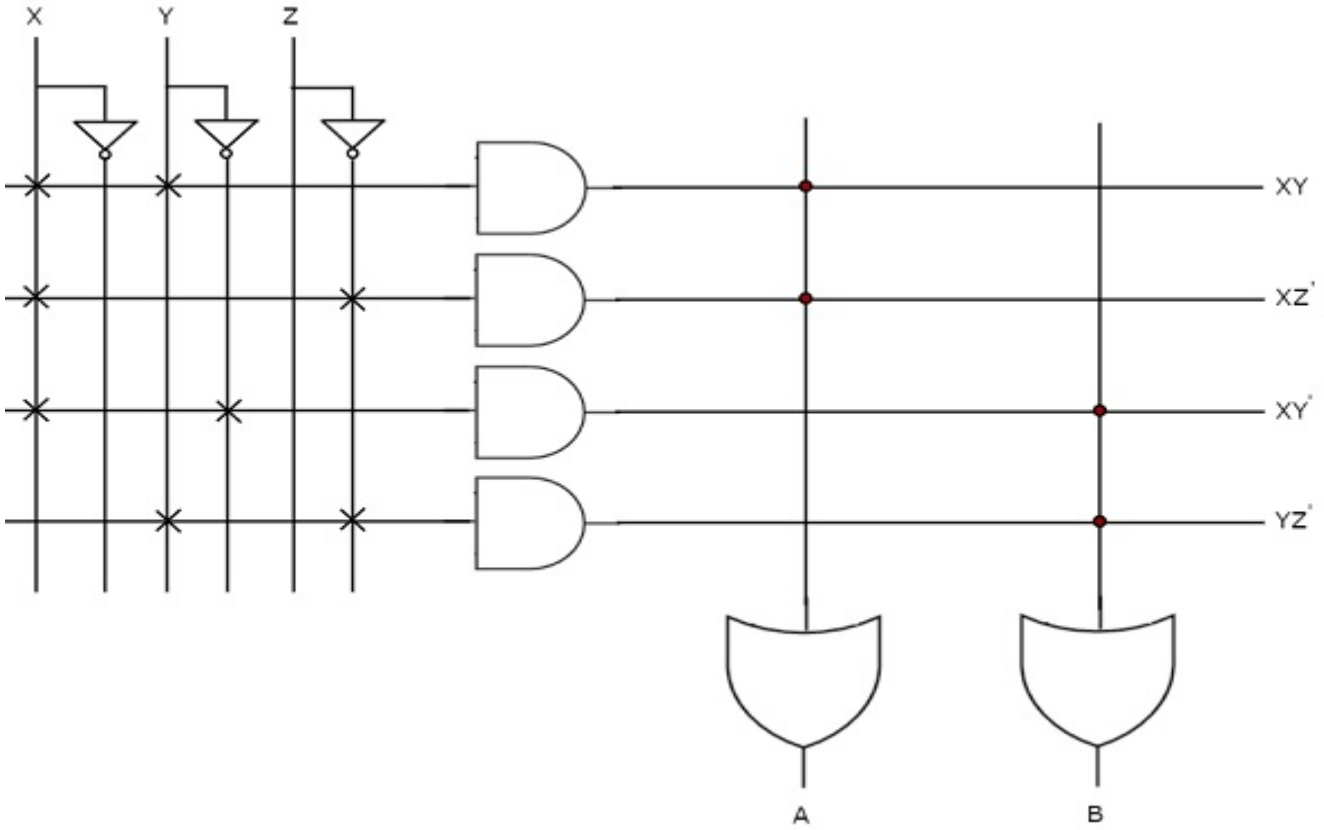
The symbol '.' is used for fixed connections



Implement following equation using PAL

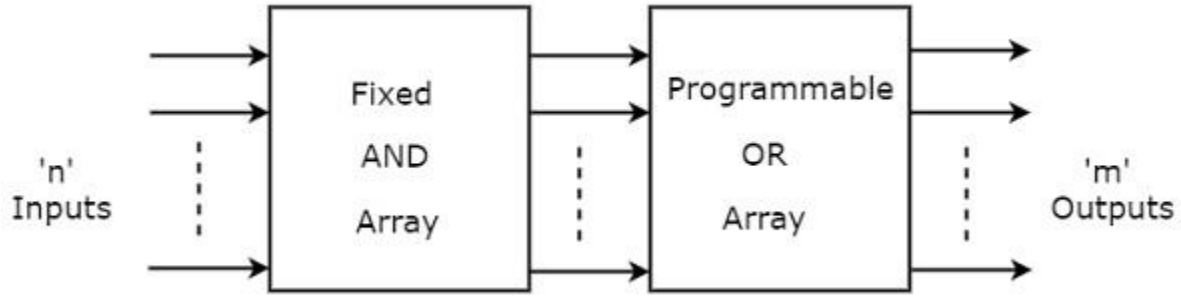
A=XY+XZ′

B=XY′+YZ′

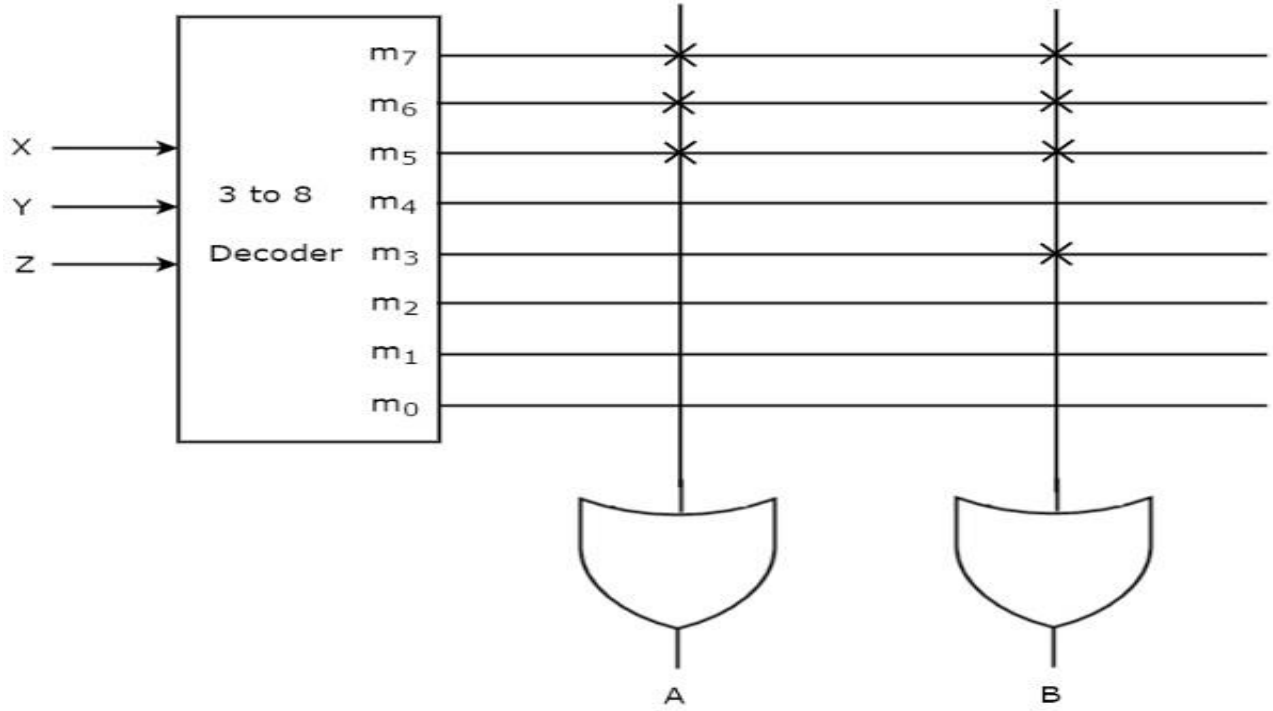


Programmable Read Only Memory PROM

Stores the binary information permanently
User has the flexibility to program the binary information electrically once by using PROM programmer
Fixed AND array (Decoder) & Programmable OR array.



Implement following using PROM
$A(X,Y,Z)=\sum m(5,6,7)$
$B(X,Y,Z)=\sum m(3,5,6,7)$



	PLA	PAL
1.	PLA stands for Programmable Logic Array.	While PAL stands for Programmable Array Logic.
2.	PLA speed is lower than PAL.	While PAL's speed is higher than PLA.
3.	The complexity of PLA is high.	While PAL's complexity is less.
4.	The cost of PLA is also high.	While the cost of PAL is low.
5.	Programmable Logic Array is less available.	While Programmable Array Logic is more available than Programmable Logic Array.

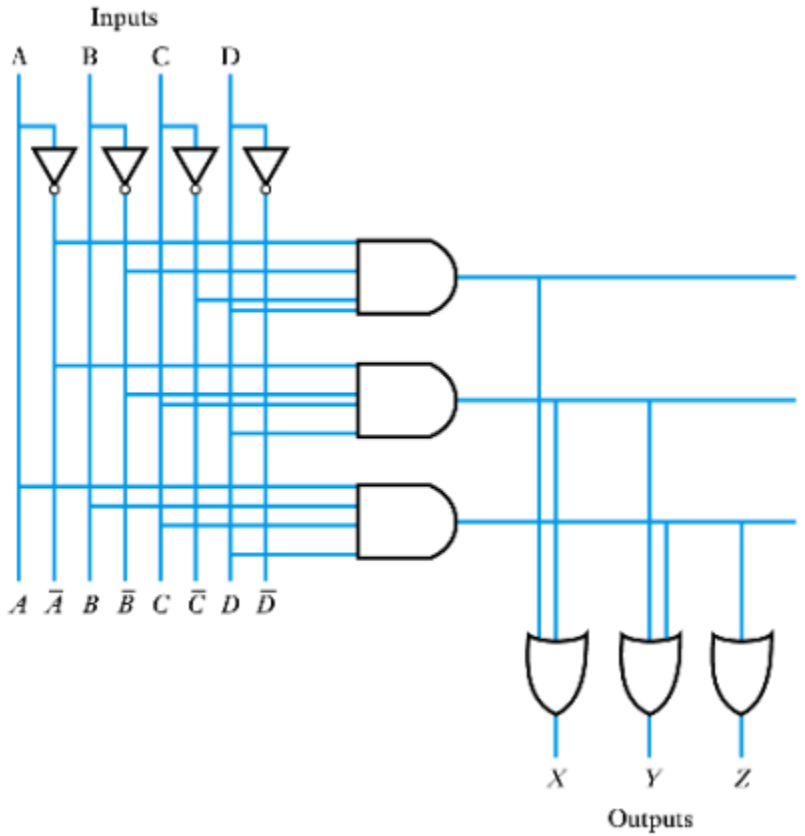
- In the following PLA, which output implements the logic function ABCD?

a. X

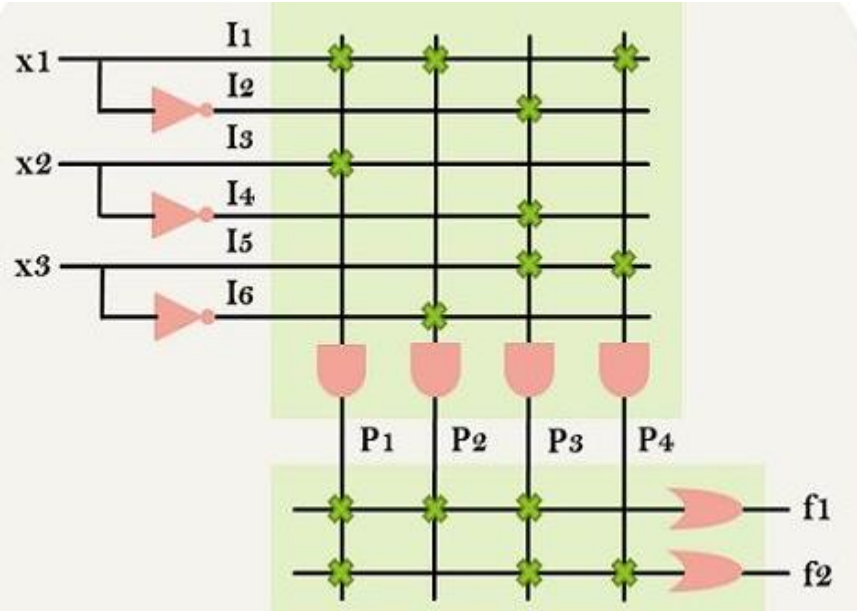
b. Y

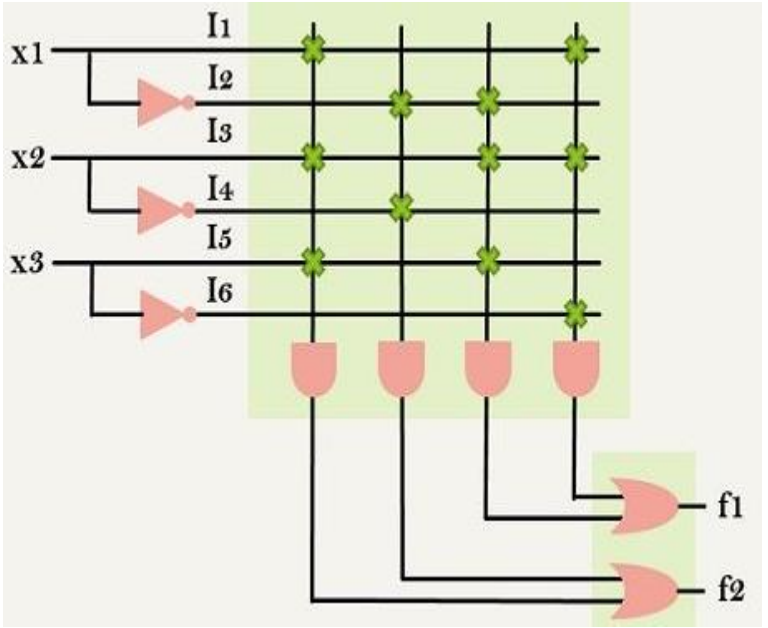
c. Z

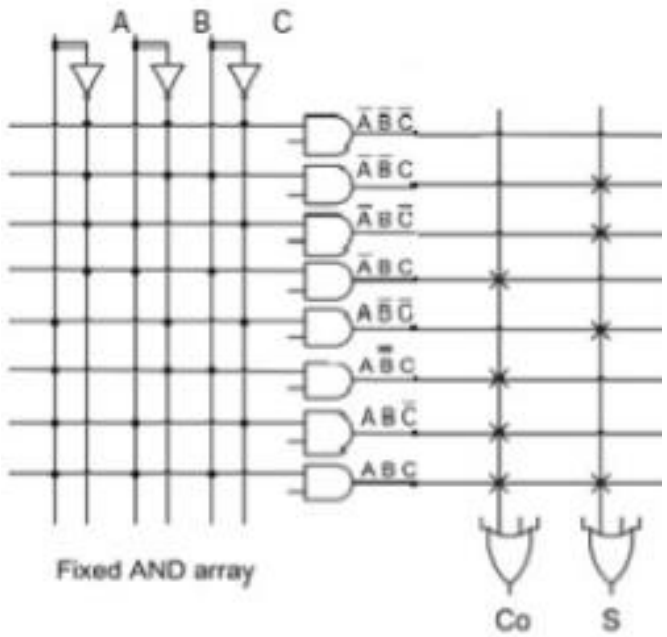
d. both X and Y



Identify the circuit and find equation







FPGA (Field Programmable Gate Array)

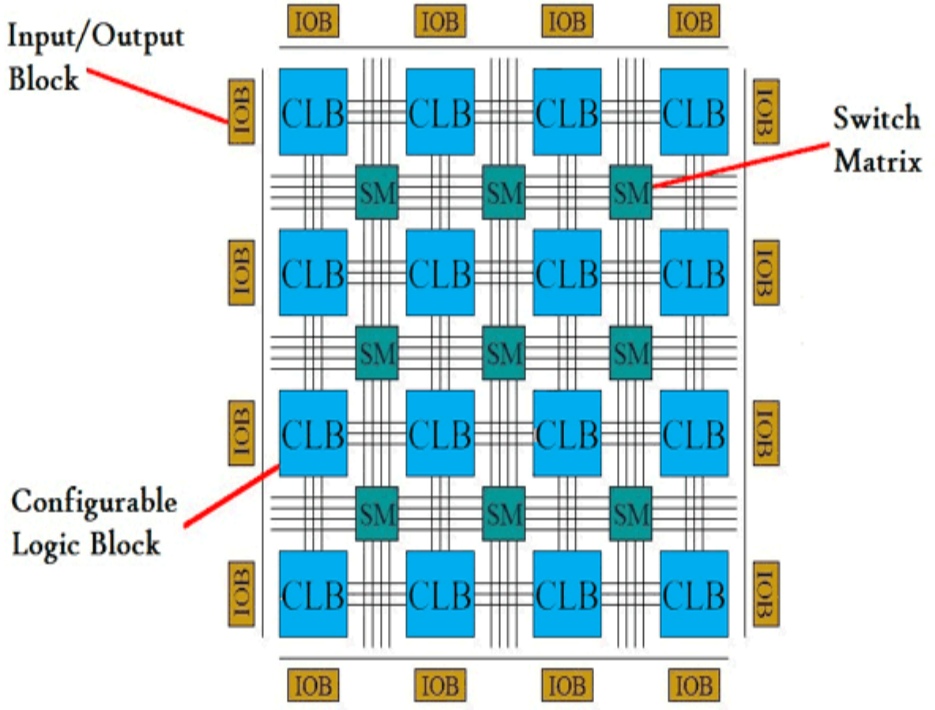
Arrays of logic blocks which are programmable.

It is surrounded by PROGRAMMABLE ROUTING RESOURCES, which allows the user to define the interconnections between the logic blocks.

It has lots of very flexible input and output circuits

Programmable Logic Device can programmed by HDLs

2 major players in the FPGA domain: Xilinx and Altera



- Logic blocks implement the logical functions required by the design and consist of various components such as transistor pairs, look-up tables (LUTs), flip flops, and multiplexers.
- Programmable interconnection is used for allocating resources among configurable logic blocks (CLBs)
- CLB is tied to a switch matrix to access the general routing structure.
- I/O blocks (IOBs) are used to interface the CLBs and routing architecture to the external components.

MCQ

- Most FPGA logic modules utilize a(n) _____ approach to create the desired logic functions.

a. AND array

b. Look-up table

c. OR array

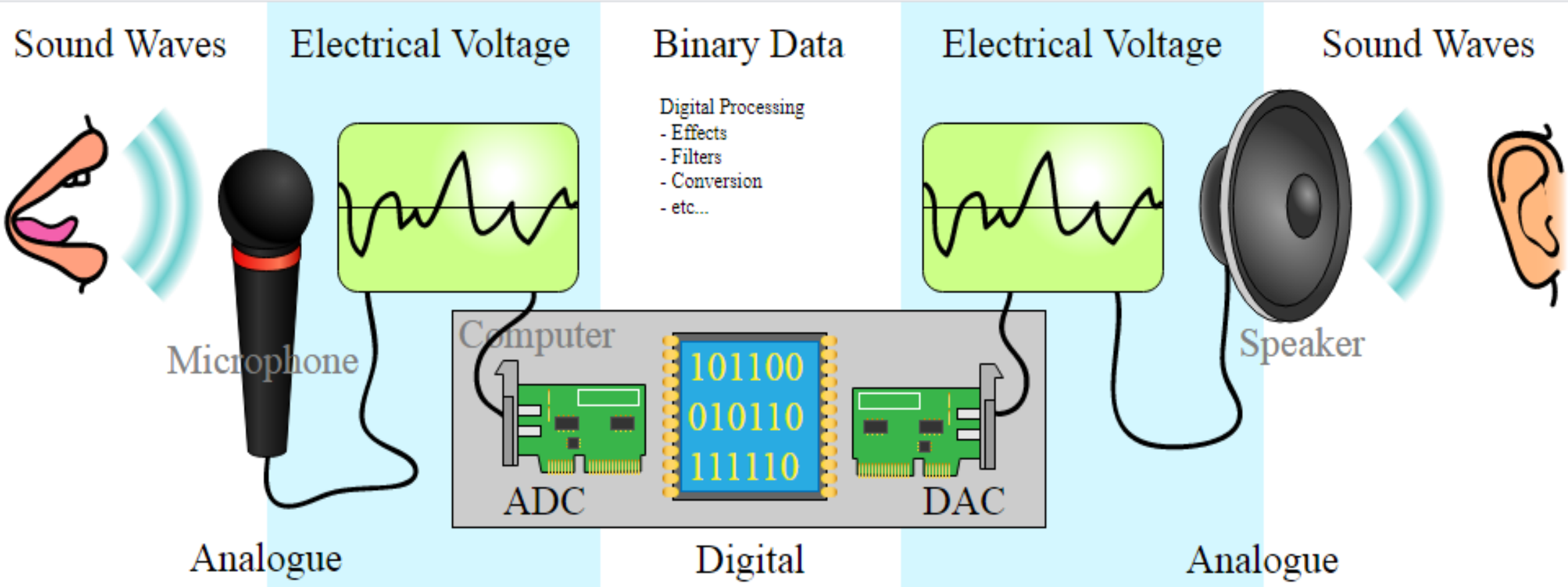
d. AND and OR array

MCQ

- In FPGA, vertical and horizontal directions are separated by _____

a) A line
b) A channel
c) A strobe
d) A flip-flop

Data Converter

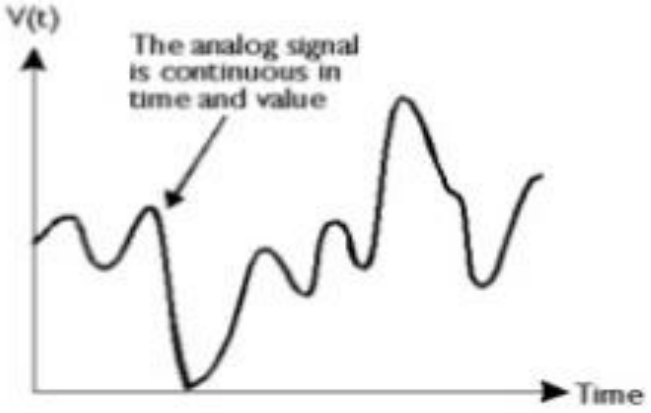


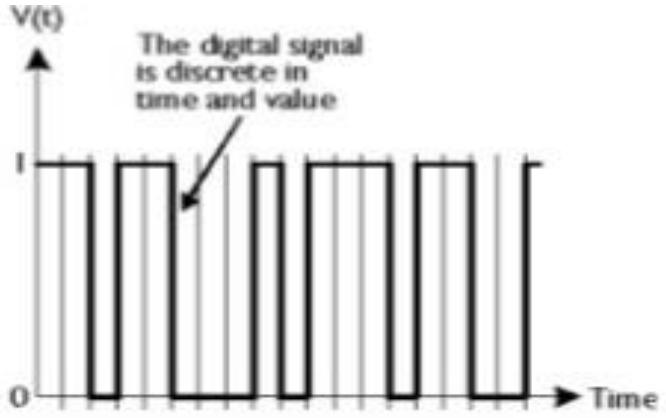
ADC – Analog to Digital Convertor
DAC – Digital to analog Converter

Analog to Digital Converter (ADC)

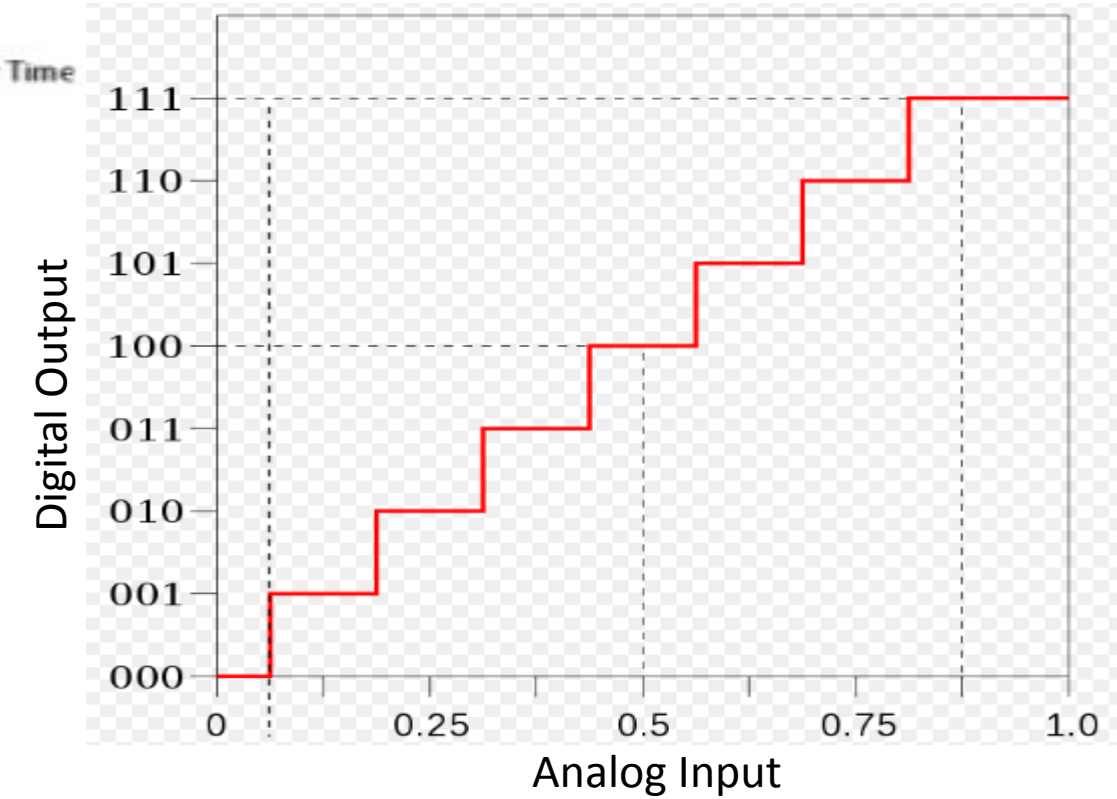
An electronics circuit converts a continuous analog input signal to discrete digital number (binary)

two discrete states, a logic “1” (HIGH) or a logic “0” (LOW).





conversion involves quantization of the input



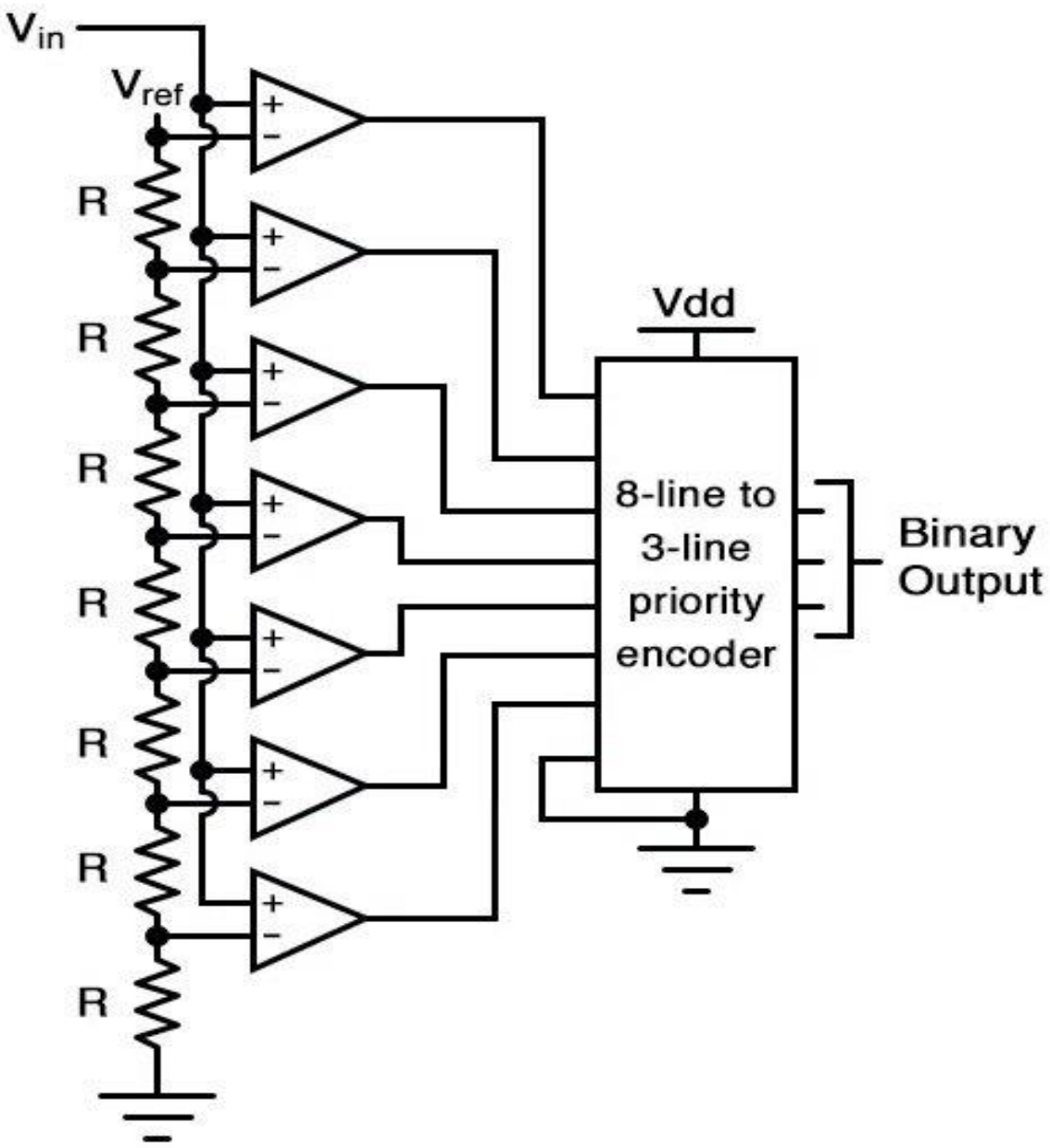
Type of ADC

Flash Type / Comparator Type Parallel ADC

- A series of comparators, resistor ladder and a priority encoder
- Each comparator compares the input signal to a unique reference voltage.
- The comparator outputs inputted of a priority encoder circuit, produces a binary output

Fastest type of ADC
Minimum conversion time

No. of Comparator = 2^n -1
No. of Resistor = 2^n
No. of priority encoder =1



MCQ

The flash type A/D converters are called as
a) Parallel non-inverting A/D converter
b) Parallel counter A/D converter
c) Parallel inverting A/D converter
d) Parallel comparator A/D converter

MCQ

How many comparator required for 4 bit flash type ADC?

(a)4

(b)8

(c) 15

(d) 16

MCQ

- What is the advantage of using flash type A/D converter?
  a) High speed conversion
  b) Low speed conversion
  c) Nominal speed conversion
  d) None of the mentioned

Successive Approximation ADC

Analog input converts into digital output using successive approximation algorithm

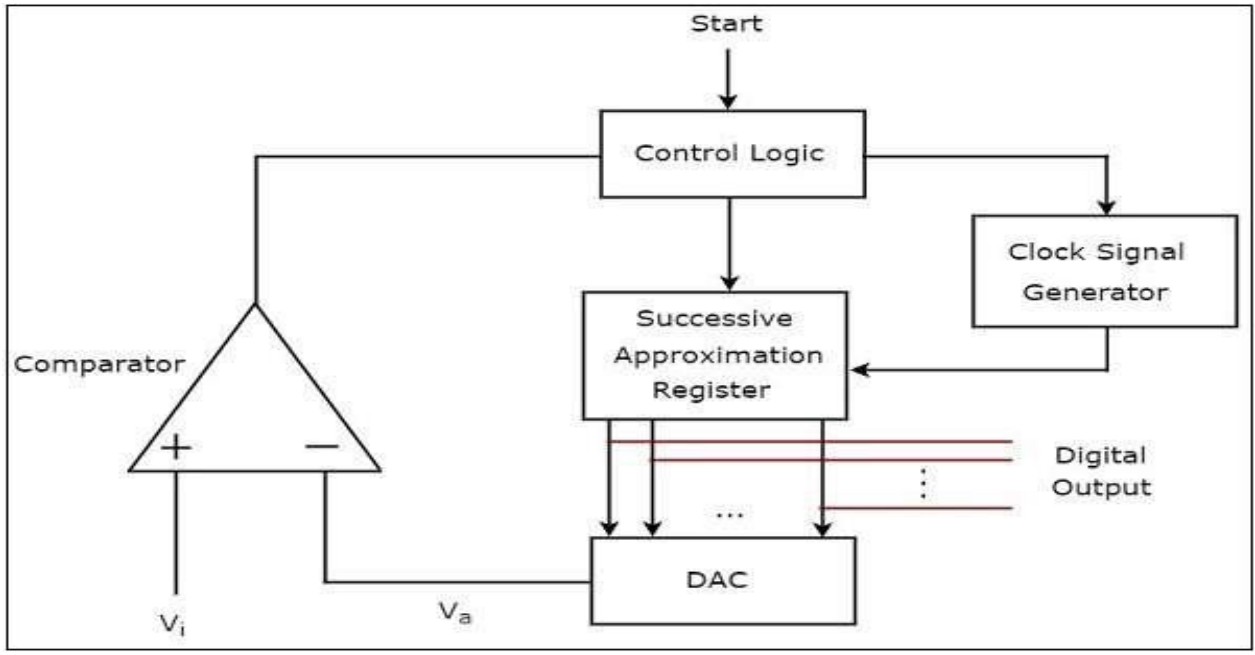
Contains Clock signal generator,

Successive Approximation Register (SAR)

DAC

Comparator

Control logic



- **control logic** resets all the bits of SAR

  enables the clock signal generator, after start

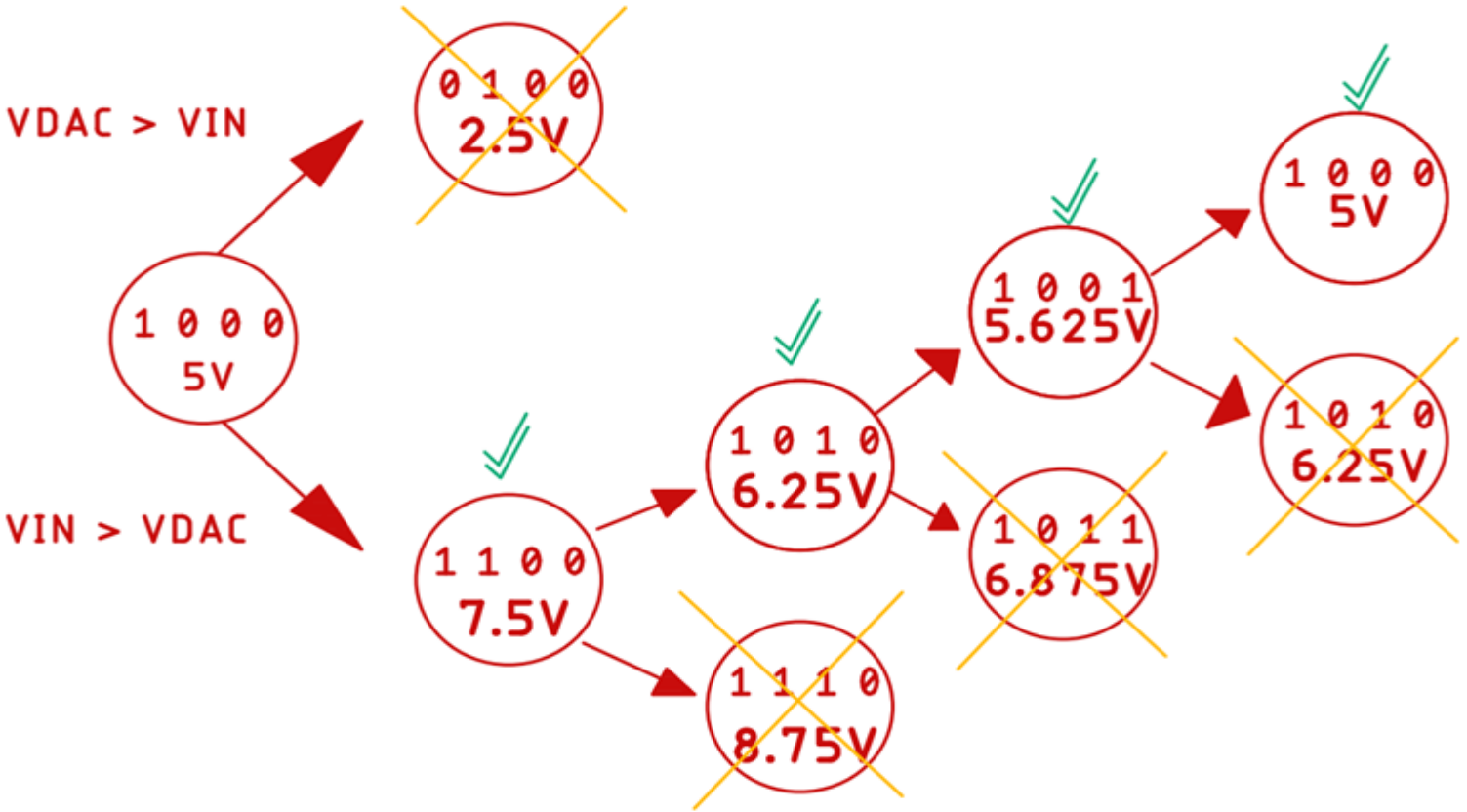
The binary (digital) data present in **SAR** will be updated for every clock pulse based on the output of comparator. The output of SAR is applied as an input of DAC.

- **DAC** converts the received digital input, which is the output of SAR, into an analog output.
- The comparator compares this analog value Va with the external analog input value Vi
- The **output of a comparator** will be '1' as long as Vi is greater than Va.
- Similarly, the output of comparator will be '0', when Vi is less than or equal to Va
- The operations mentioned in above steps will be continued until the digital output is a valid one.

4-bit SAR ADC with input signal **is 5.8V** and reference **is 10V**

conversion starts, with sets the most significant bit to 1 and all other bits to zero
DAC will produce a value of 5V
Now this voltage will be compared to the input voltage and based on the comparator output

Vin > Va (DAC output), MSB will stay as it is, and the next bit will be set for a new comparison.
Vin < Va (DAC output), MSB will set to zero, and the next bit will be set to 1 for a new comparison.



Conversion Time:

N bit SAR ADC, take N clock cycles,

conversion time of SAR ADC➔ Tc = N x Tclk

How many clock pulses do a successive approximation converter requires for obtaining 5 bit a digital output.

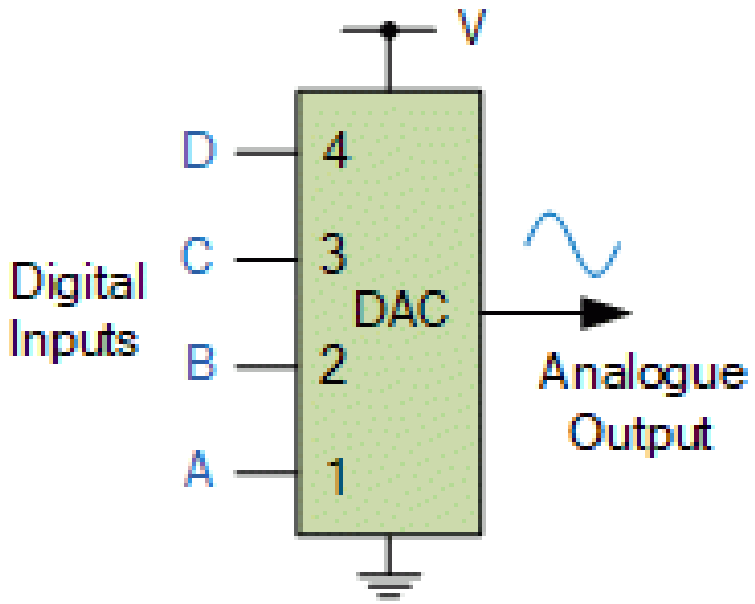
a) 1
b) 5
c) 32
d) 10

Digital to Analog Converter(DAC)

Accepts n-bit binary input and produces proportional analog signal

Analog output = K × digital input

K-propotionality factor



DAC's convert binary or non-binary numbers into analogue ones with its output voltage (or current) being proportional to the value of its digital input number

Type of DAC

1. Binary weighted resistors

Contains OP-AMP, Digital Switch, 2^n resistors

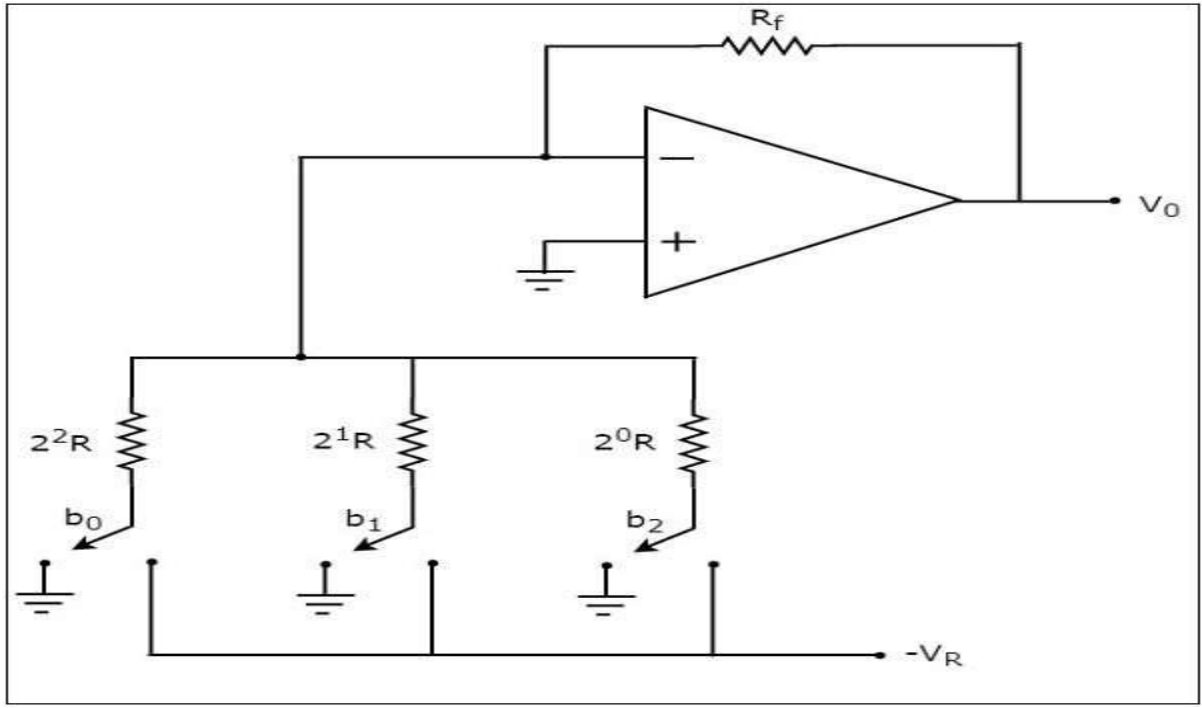
3-bit binary input is b2b1b0

digital switches connected to ground for input bits '0'.

connected to the VR for input bits '1'

non-inverting input terminal of an op-amp is connected to ground

virtual ground concept, the voltage at the inverting input terminal of opamp is same as that of the voltage at its non-inverting input terminal



$$\frac{0+V_R b_2}{2^0 R}+\frac{0+V_R b_1}{2^1 R}+\frac{0+V_R b_0}{2^2 R}+\frac{0-V_0}{R_f}=0$$

Substituting, $R = 2R_f$ f in above equation.

$$=> \frac{V_0}{R_f}=\frac{V_R b_2}{2^0 R}+\frac{V_R b_1}{2^1 R}+\frac{V_R b_0}{2^2 R}$$

$$=> V_0=\frac{V_R R_f}{R}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

$$=> V_0=\frac{V_R R_f}{2R_f}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

$$=> V_0=\frac{V_R}{2}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

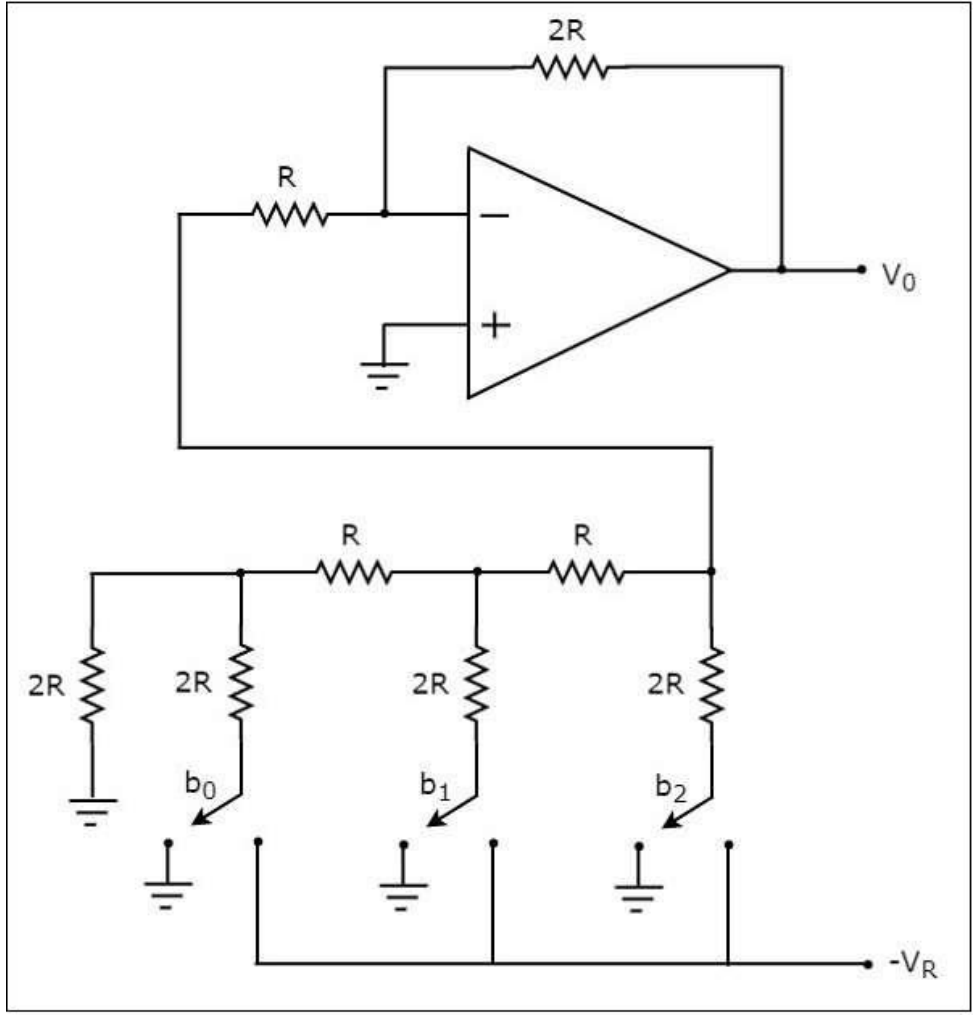
2. R-2R Ladder DAC

Contains R-2R resistor ladder, OP-AMP and digital switch

Only two value of resistor

digital switches connected to ground for input bits ‘0’.

connected to the VR for input bits ‘1’



$$V_0 = \frac{V_R}{2}\left\{\frac{b_{N-1}}{2^0} + \frac{b_{N-2}}{2^1} + \ldots + \frac{b_0}{2^{N-1}}\right\}$$

MCQ

A 4-bit R/2R digital-to-analog (DAC) converter has a reference of 5 volts. What is the analog output for the input code 0101.

A 0.325 V
B 3.125 V
C 0.78125 V
D –3.125 V

DAC Specification

1. Resolution- Number of different analog output values can provided by DAC

n-bit DAC Resolution =2^n

Resolution also defined as

Ratio of change in output voltage due to change in 1 LSB at digital input

$$\text{Resolution} = \frac{V_{oFS}}{2^n - 1}$$

VoFS = Full Scale Voltage

Full scale voltage of 8-bit DAC is 10.2 V

Resolution = 2^8 = 256

Resolution = 10.2 / (2^8 -1) = 10.2 /255 = 40 mV/LSB

1 LSB change in digital input produces 40 mV analog output

Output voltage of DAC **Vo = Resolution * Decimal value of Digital input**

2. Accuracy - Difference between actual output voltage and expected output voltage

Accuracy of DAC 1/2LSB

3. Conversion Time - Time taken for the output to settle within a specified band

settling time ranges from 100 ns to 10 µs

Digital input for a 4-bit DAC is (0110)2
Calculate its final output voltage for full scale output 15V

Solution : For given DAC,

$$n = 4$$

$$\therefore \quad V_{oFS} = 15 \text{ V}$$

$$\therefore \quad \text{Resolution} = \frac{V_{oFS}}{2^n - 1} = \frac{15}{2^4 - 1} = 1 \text{ V/LSB}$$

$$\therefore \quad V_o = \text{Resolution} \times D$$

$$\text{Now} \quad D = \text{Decimal of } (0110)_2 = 6$$

$$\therefore \quad V_o = 1 \text{ V/LSB} \times 6 = \mathbf{6 \text{ V}}$$

8-bit DAC have resolution 20 mV/LSB , Find full scale output and If input in (10000000)2

Solution : $\text{Resolution} = \frac{V_{oFS}}{2^n - 1}$

$$\therefore \quad 20 = \frac{V_{oFS}}{2^8 - 1}$$

$$\therefore \quad V_{oFS} = \mathbf{5.1 \text{ V}}$$

$$D = \text{Equivalent of } (10000000)_2 = 128$$

$$\therefore \quad V_o = \text{Resolution} \times D = 20 \times 128 = \mathbf{2.56 \text{ V}}$$

12-bit DAC has a step size 8 mV, determine the full scale voltage and % resolution. Also find the output voltage for the input (010101101101)2

Solution : For 12-bit DAC, step size is 8 mV.

$$V_{oFS} = 8\text{ mV} \times 2^{12} - 1 = \mathbf{32.76\ V}$$

$$\%\ \text{Resolution} = \frac{8\text{ mV}}{32.76\text{ V}} \times 100 = \mathbf{0.02442}$$

The output voltage for the input $(010101101101)_2$ is $= 8\text{ mV} \times (1389)_{10} = \mathbf{11.112\ V}$

A 5-bit DAC has a current output. For a digital input of 101000, an output current of 10mA is produced. What will IOUT be for a digital input of 11101?

digital input (10100)2 is equal to decimal 20. Since IOUT = 10 mA for this case, the proportionality factor as 0.5 mA

(11101)2 = (29)10 as follows : IOUT = (0.5mA) × 29 = 14.5 mA