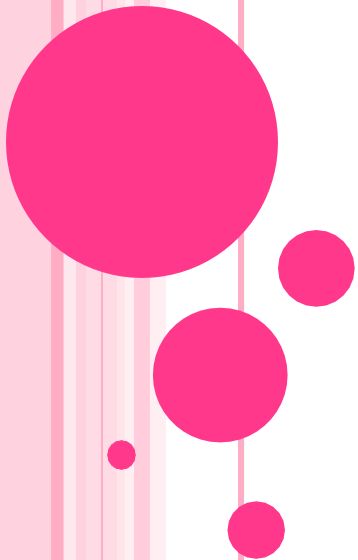


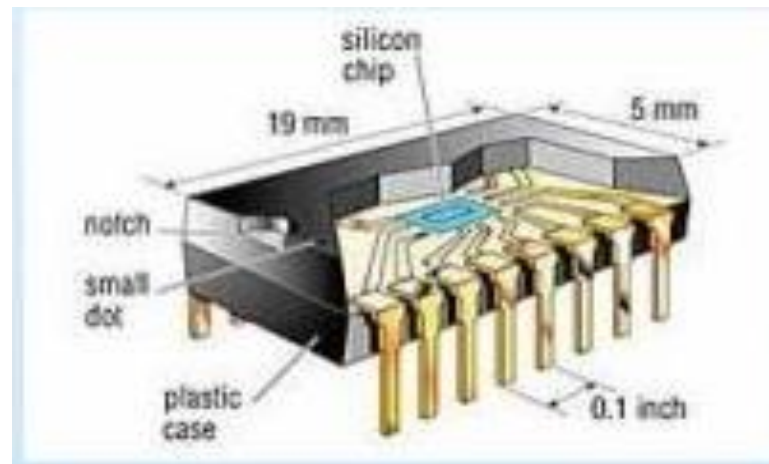
Unit-3:

Logic Families

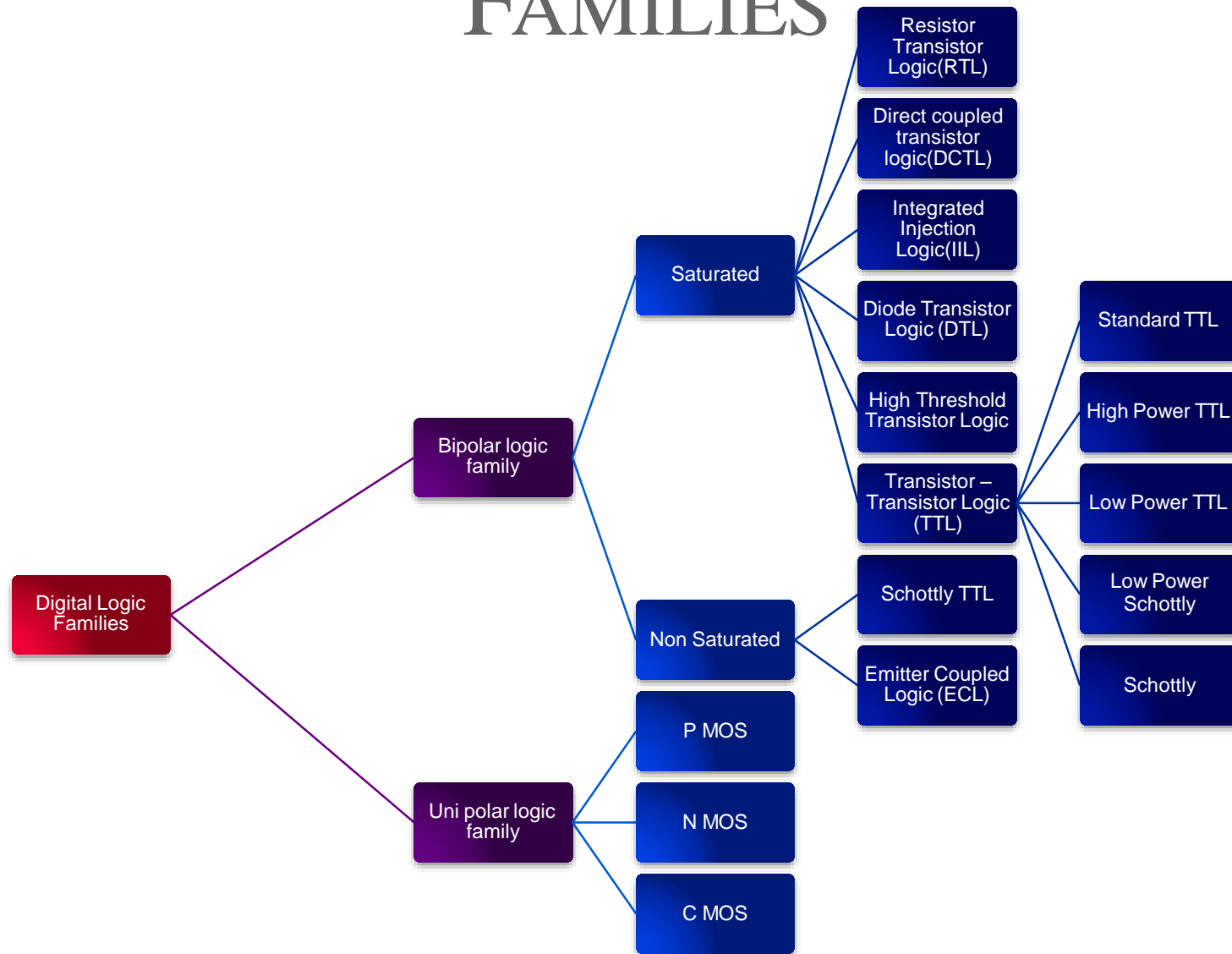


1. INTRODUCTION

- Logic gates are available in the form of Integrated circuit(IC's)
- As per the level of integration, the IC's can accommodate more number of logic gates and digital functions.
- These forms are referred as logic family.



2. CLASSIFICATION OF LOGIC FAMILIES



3. IMPORTANT POINTS

- The digital family is categorized by two types
 - (i) Bipolar and
 - (ii) Unipolar
- In Saturated Bipolar logic families, the transistor in the IC is driven into saturation.

In Non Saturated Bipolar logic families, the transistor in the IC is not driven into saturation
- In PMOS & NMOS Unipolar logic family only P & N channel MOSFETs are used. CMOS Unipolar logic family both P & N-channel MOSFETs are used.
- All family same logic level & same Voltage.



Logic Families

OBSOLETE ONES:

1. Diode Logic.
2. Diode Transistor Logic (DTL).
3. Resistor Transistor Logic (RTL).

CURRENT ONES:

1. TTL (Transistor Transistor Logic)
2. ECL (Emitter Coupled Logic)
3. CMOS (Complementary Metal Oxide Semiconductor)



4. LEVEL OF INTEGRATION

- Number of gates fabricated in single IC
- There are 4 generation
 - Small Scale Integration (SSI) = 12 gates in 1 Chip
 - Medium Scale Integration (MSI) = 12 to 100 gates
 - Large Scale Integration (LSI) = 100 to 1000 gates
 - Very Large Scale Integration (VLSI) = Up to 1,00,000 or more



5. SPECIFICATION OF DIGITAL IC's

- Different types of ICs are manufactured, based on the components used and their interconnections.
- These ICs are compared using certain performance specifications.

1. Power Dissipation

2. Propagation Delay

3. Fan-In

4. Fan-Out

5. Input Logic Level

6. Output Logic Level

7. Compatibility

8. Noise Margin

9. Speed – Power Product



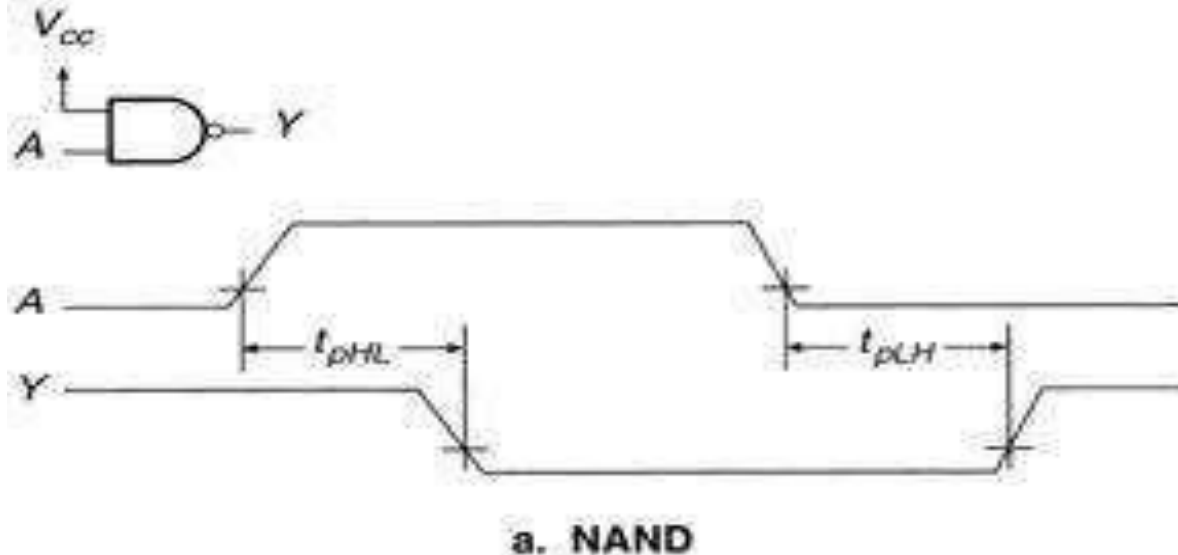
1. POWER DISSIPATION

- This is **the mean power of logic circuit draws from the supply** during one complete cycle.
- This parameter is very important because if the power dissipation is large, then the life period of the IC is reduced.
- It should be noted that in one complete cycle, the IC is in logic '1' for half the time and in logic '0' during the remaining half.
- The power dissipation of a logic gate is equal to the dc supply voltage (V_{CC}) times the average supply current (I_C).



2. PROPAGATION DELAY

- This parameter characterizes the **speed of a logic circuit**.
- The propagation delay of IC is the mean time required for a pulse to pass through the IC.
- It is thus defined as the time interval between a change in input and the resulting change in the output of an IC.
- It is represented by t_{pd} .



3. FAN-IN

Fan in of a logic circuit gives the **maximum number of inputs** that can be connected to the logic circuit without impairing other primary parameters.

4. FAN-OUT

Fan-out of a logic circuit **is the maximum number of outputs** the circuit may have and still operate properly. The fanout is the limiting factor which determines the number of loads that the given data can drive.

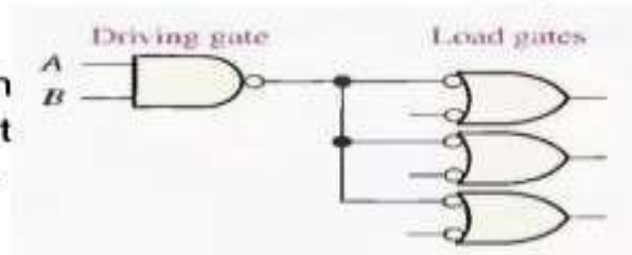
Fan in and Fan out

Fan-in:

Number of inputs a gate has. For example, a two input gate will have fan-in equal to 2

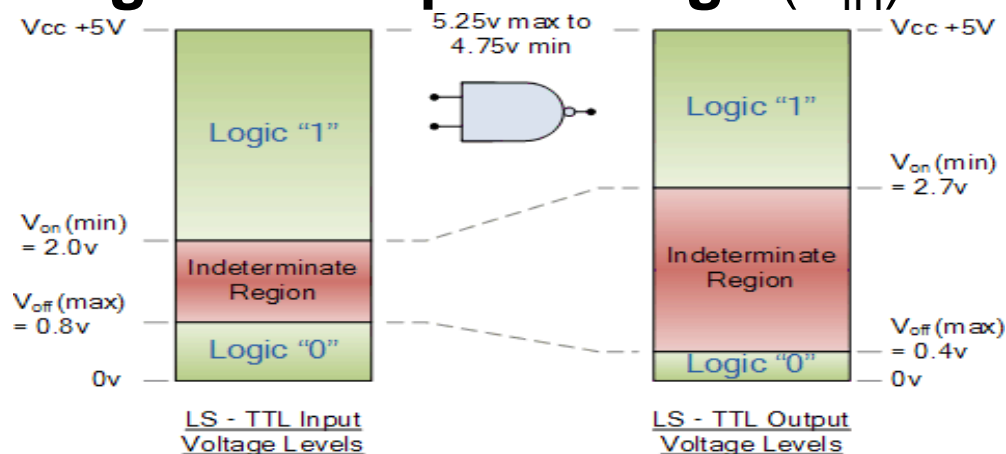
Fan-out:

Maximum
family t
outside



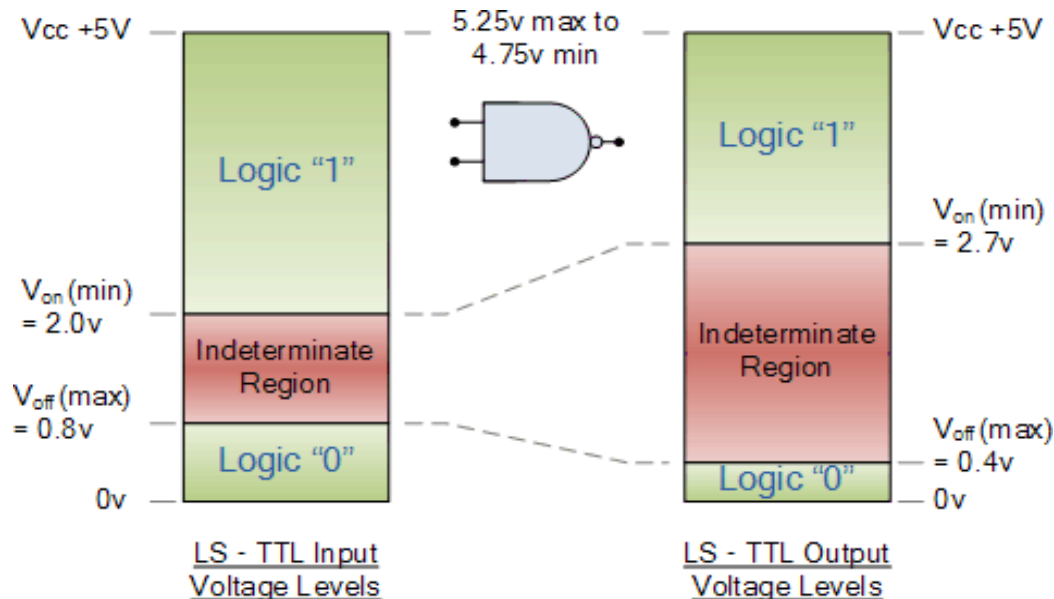
5. INPUT LOGIC LEVEL (V_{IL} & V_{IH})

- If the input voltage level changes without changing the output, this is known as **Input Logic Level**.
- The input is either in logic 0 – low(0V) or logic 1 – High(+5 V)
- some tolerance is allowed to the input voltage.
- Eg: If the input voltage may change from 0V to 0.8V without changing the output level. This voltage of 0.8V is defined as the **Maximum low input voltage** (V_{IL}).
- If the logic 1 may change from + 5V to + 2V without affecting, the output level, then the + 2V is known as the **Minimum high level input voltage** (V_{IH}).



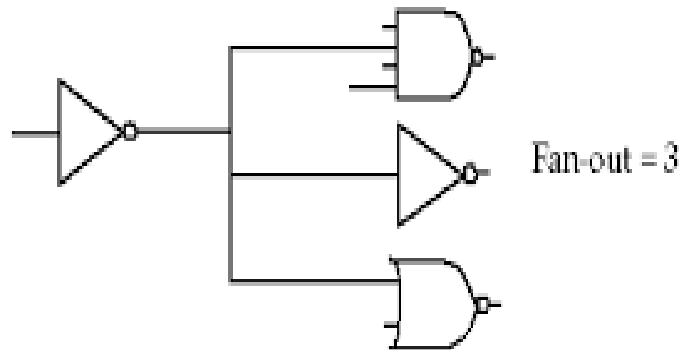
6. OUTPUT LOGIC LEVEL

- The output voltage is at 0V for logic 0 and at 5V for logic 1.
- Eg: In supply voltage variations, voltage drop across resistors etc., so these voltages tend to vary. Thus any voltage say, from 0V to 0.4V is considered as low output.
- Similarly any voltage from 2.7V to 5V is considered as logic 1.
- Thus the worst-case output voltages are the **Maximum low level output voltage** (V_{OL}) and the **Minimum high level output voltage** (V_{OH}).



7. COMPATIBILITY(ABILITY TO WORK WITH ANOTHER)

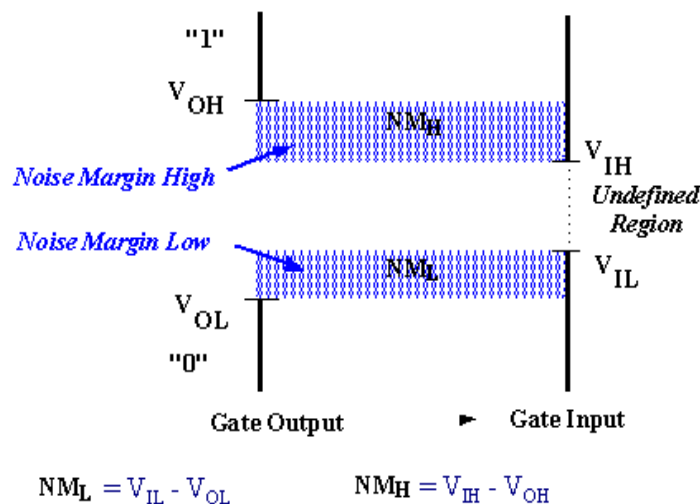
- Compatibility is defined as the **ability of one device to drive the input of another device.**
- If the output of one device is connected to the input of another device, for both the devices the the Input Logic Level and Output Logic Level must be same, then these two devices are compatible .



8. NOISE MARGIN

- There is a minimum permissible variation between the **drive device and the load device** this difference is known as the noise margin.
- As long as the noise level of any stray interference picked by the various leads of the device is within this value of 0.4V the input of the load device is not affected

Definition of Noise Margins



9. SPEED – POWER PRODUCT

- It is specified by the manufacture as a measure of the performance of a logic circuit based on the product of the propagation delay time and the power dissipation at a specified frequency.
- It is expressed in the units of joules (J).

Speed-Power Product

- Desirable properties:
 - Short propagation delays (high speed)
 - Low power dissipation
- Speed-power product measures the combined effect.



REVIEW OF SPECIFICATION OF DIGITAL IC'S

1. Power Dissipation
2. Propagation Delay
3. Fan-In
4. Fan-Out
5. Input Logic Level
6. Output Logic Level
7. Compatibility
8. Noise Margin
9. Speed – Power Product



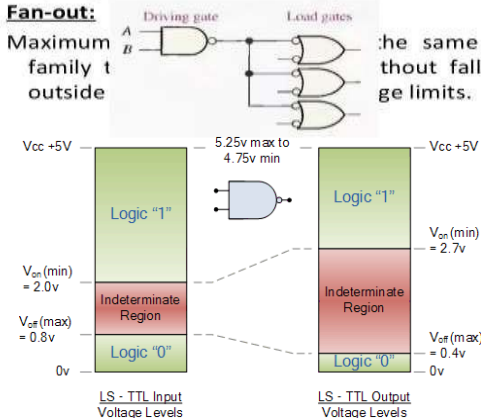
Fan in and Fan out

Fan-in:

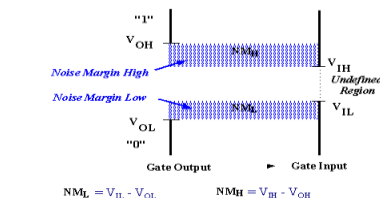
Number of inputs a gate has. For example, a two input gate will have fan-in equal to 2

Fan-out:

Maximum number of load gates that can be connected to the output of a driving gate without falling outside the specified limits.

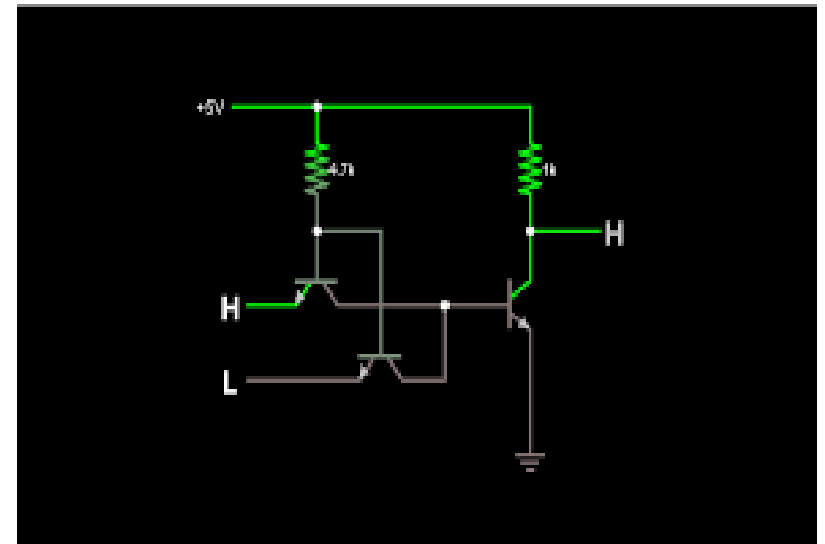


Definition of Noise Margins



TRANSISTOR –TRANSISTOR LOGIC(TTL) CIRCUIT

- The most widely used logic family is Transistor – Transistor Logic (TTL)
- It has Bipolar Transistor
- High Speed($t_p = 10$ ns)
- Low power dissipation
- Fan – In from 12 -14
- Fan out equals to 10 or more



TTL IC Family

● Transistor-Transistor Logic Families:

- ✦ **74L** **Low power**
- ✦ **74H** **High speed**
- ✦ **74S** **Schottky**
- ✦ **74LS** **Low power Schottky**
- ✦ **74AS** **Advanced Schottky**
- ✦ **74ALS** **Advance Low power Schottky**



ECL IC Family

- PROS: Fastest logic family available ($\sim 1\text{ns}$)
- CONS: low noise margin and high power dissipation
- Operated in emitter coupled geometry (recall differential amplifier or emitter-follower), transistors are biased and operate near their Q-point (never near saturation!)
- Logic levels. “0”: -1.7V . “1”: -0.8V
- Such strange logic levels require extra effort when interfacing to TTL/CMOS logic families



MOS/ CMOS CIRCUIT

- Metal Oxide Semiconductor(MOS) field effect transistor.
There are 3 types
 - P MOS- P- Channel MOSFET – slowest
 - N MOS – N Channel MOSFET – Microprocessor & Memories
 - C MOS (Complementary MOS) – both N& P Channel
 - ADVANTAGES:
 - LOW POWER DISSIPATION
 - LOW NOISE
 - HIGH FAN OUT
 - HIGH SWITCHING SPEED
 - BETTER COMPATIBILITY



TTL vs CMOS

● TTL

- ✦ faster (some versions)
- ✦ strong drive capability
- ✦ rugged

● CMOS

- ✦ lower power consumption
- ✦ simpler to make
- ✦ greater packing density
- ✦ better noise immunity



CMOS as a Switch

PMOS

ON → Gate input Low

OFF → Gate input High



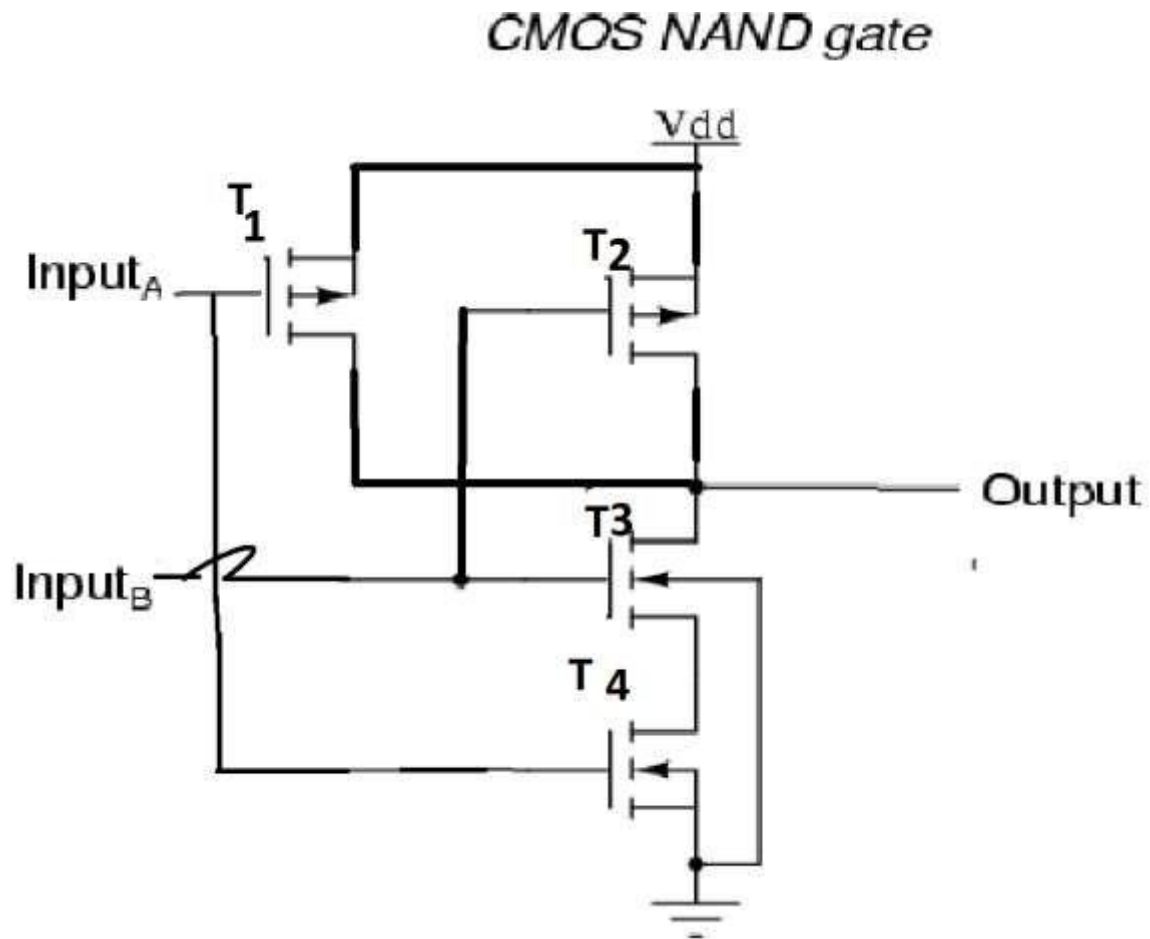
NMOS

OFF → Gate input Low

ON → Gate input High

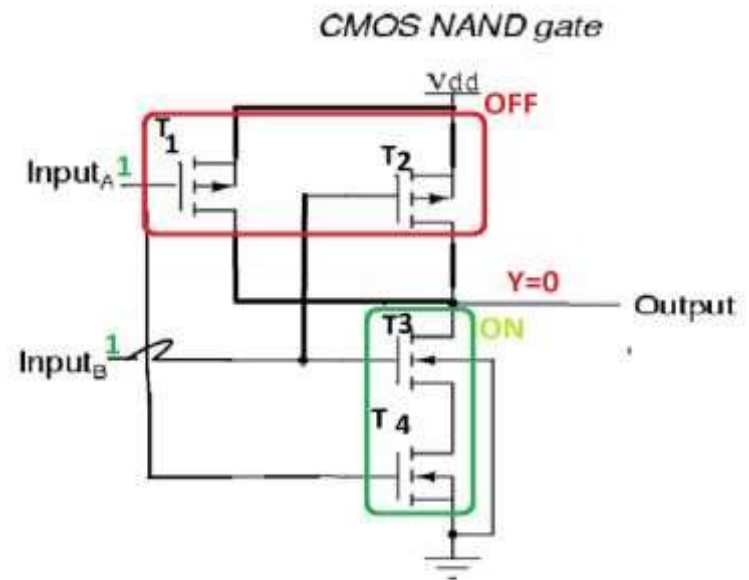
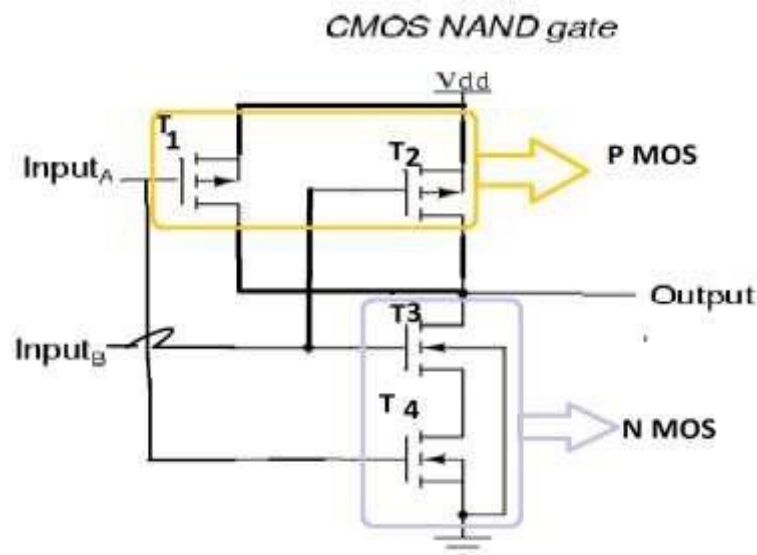


CMOS NAND GATE



8. CMOS NAND GATE OPERATION

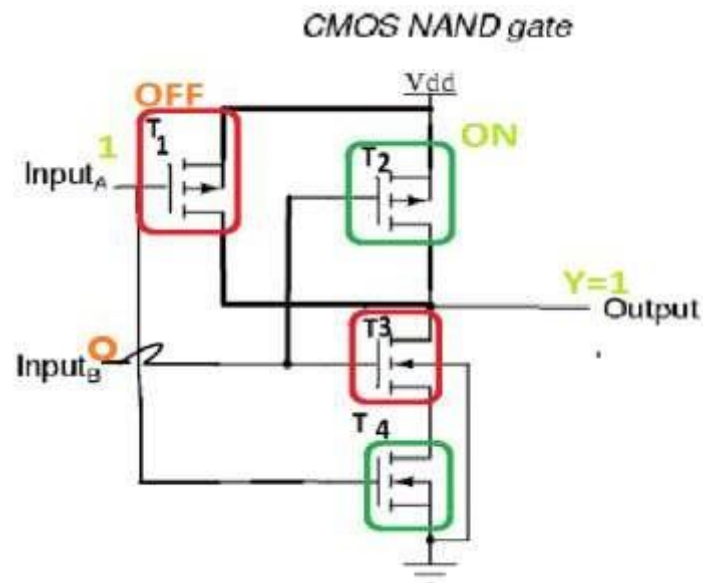
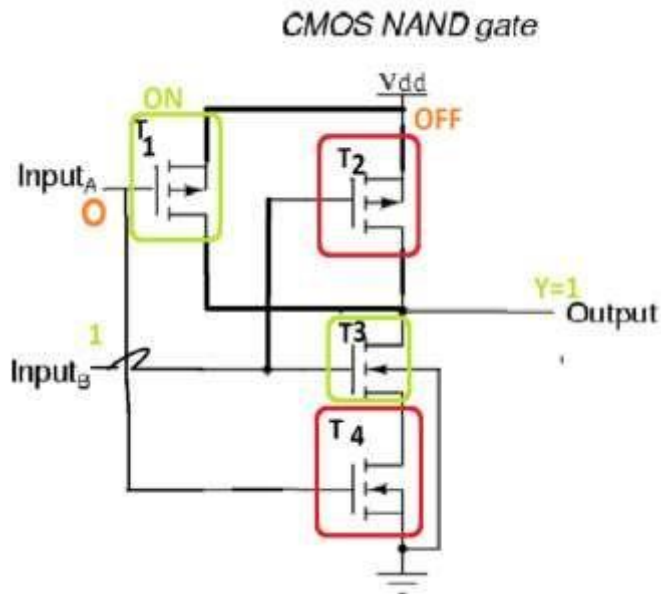
- Complementary MOSFET
- T1 & T2 are p-channel MOSFET
- T3 & T4 are n-channel MOSFET
- If inputs are high '1' then p-channel MOSFET (T1 & T2 – OFF), n-channel MOSFET (T3 & T4 – ON), so the output is low.



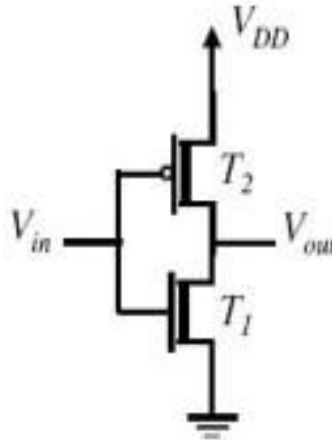
8. CMOS NAND GATE OPERATION

- If any one of the input is high then the pmos transistor is OFF & its Combinational nmosTransistor is On
- For Eg:

INPUT	T1	T2	T3	T4	OUTPUT
0,0	ON	ON	OFF	OFF	1/HIGH
0,1	ON	OFF	ON	OFF	1/HIGH
1,0	OFF	ON	OFF	ON	1/HIGH
1,1	OFF	OFF	ON	ON	0/ LOW

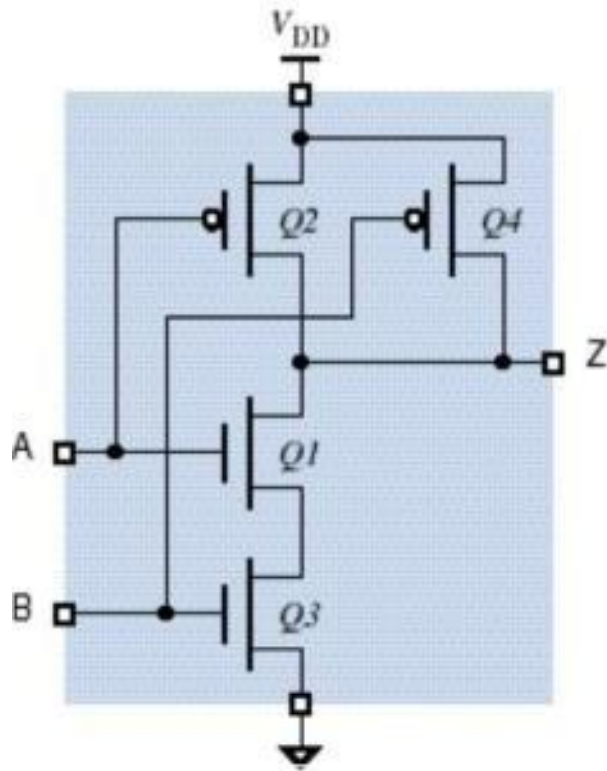


CMOS as a NOT Gate

Truth Table	Integrated Circuit												
<table><tr><th>V_{in}</th><th>T_1</th><th>T_2</th><th>V_{out}</th></tr><tr><td>0</td><td>off</td><td>on</td><td>1</td></tr><tr><td>1</td><td>off</td><td>off</td><td>0</td></tr></table>	V_{in}	T_1	T_2	V_{out}	0	off	on	1	1	off	off	0	
V_{in}	T_1	T_2	V_{out}										
0	off	on	1										
1	off	off	0										



CMOS as a NAND Gate

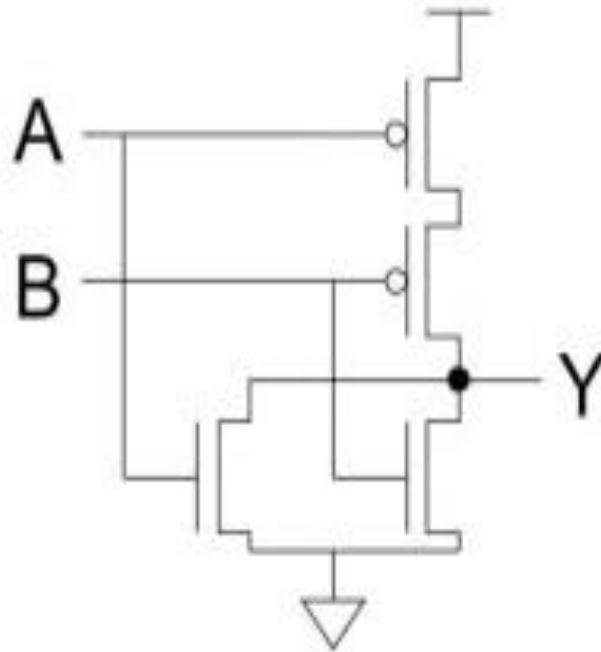
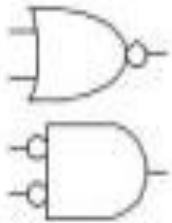


A	B	$Q1$	$Q2$	$Q3$	$Q4$	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L



CMOS as a NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



10. COMPARISON OF TTL, CMOS & ECL LOGIC FAMILY

Parameter	CMOS	TTL	ECL
Basic gate	NAND/NOR	NAND	OR/NOR
Fan-out	>50	10	25
Power per gate (mW)	1 @ 1 MHz	1 - 22	4 - 55
Noise immunity	Excellent	Very good	Good
t_{PD} (ns)	1 - 200	1.5 - 33	1 - 4



MCQ

. If a logic circuit has a fan out of 4 then the circuit

- A. 4 input
- B. has 4 outputs
- C. can drive maximum of 4 inputs
- D. gives output 4 times the input

A RTL consists of

- A. Resistor ,transistor and inductors
- B. Resistors,diodes and bipolar junction transistor
- C. Resistors,capacitors and diodes
- D. Resistors and transistors



Which of the following logic family dissipates minimum power?

A. CMOS

B. ECL

C. TTL

D. DTL

