Flip Flop

Flip Flop

- A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs.
- Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

(a) Response to positive level

(b) Positive-edge response

(c) Negative-edge response

QUICK QUIZ (POLL)

Flip flops are:

a) Level sensitive
b) Positive edge triggered
c) Negative edge triggered
d) Both b and c

Difference between Latch and Flip Flop

Latch	Flip flop
Level sensitive	Edge sensitive
A latch doesn’t contain any clock signal	A flip-flop contains a clock signal
The structure of Latches is built with logic gates	FFs are designed with latches by adding an extra clock signal.
Asynchronous	Synchronous
Faster	Slower

QUICK QUIZ (POLL)

Which of the following is an synchronous sequential circuit

a) NAND based SR latch
b) NOR based SR latch
c) Clocked SR flip flop
d) D latch

Types of Flip Flop

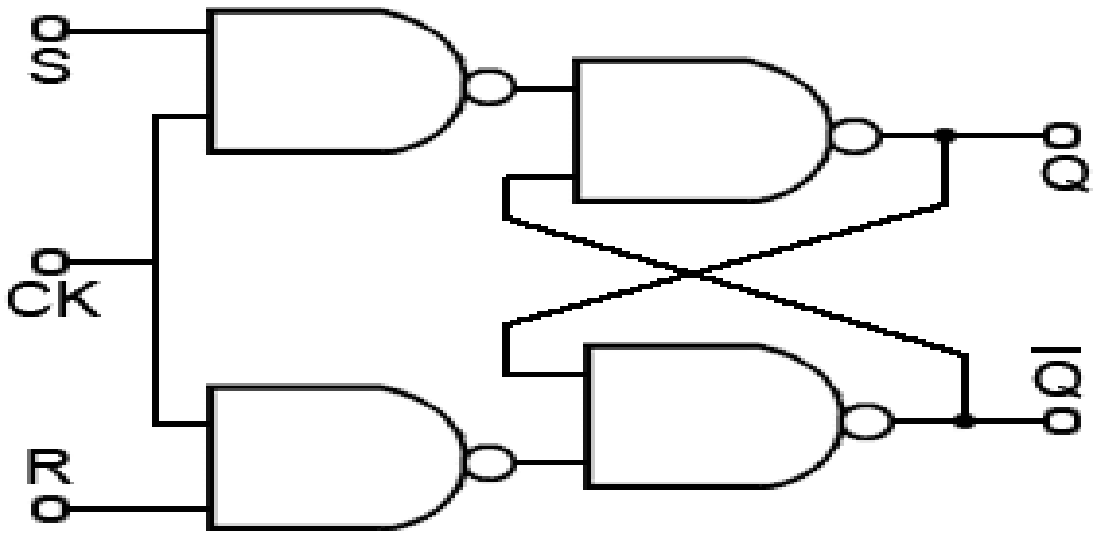
SR flip flop

D flip flop

JK flip flop

T flip flop

SR Flip Flop



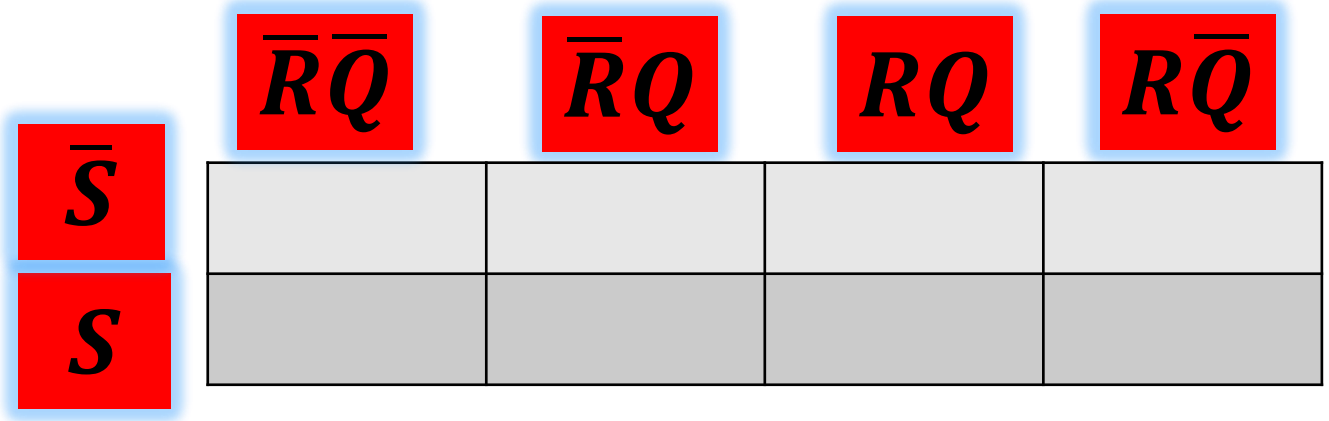
Characteristic Table:

CLK	S	R	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	×	Q_n	$\overline{Q_n}$
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

SR Flip Flop

Characteristic Table:

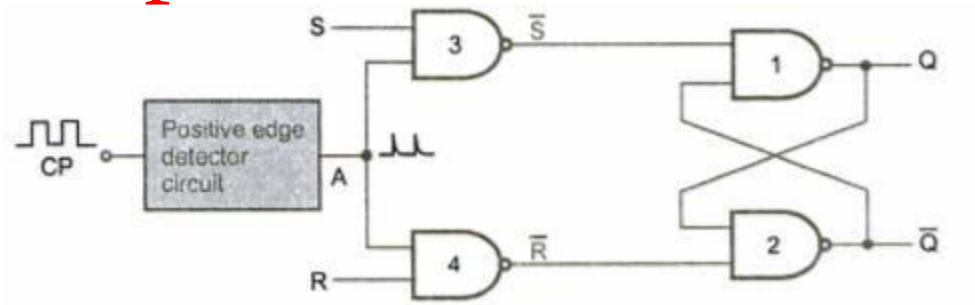
CLK	S	R	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	Indeterminate	
1	1	1	1	Indeterminate	

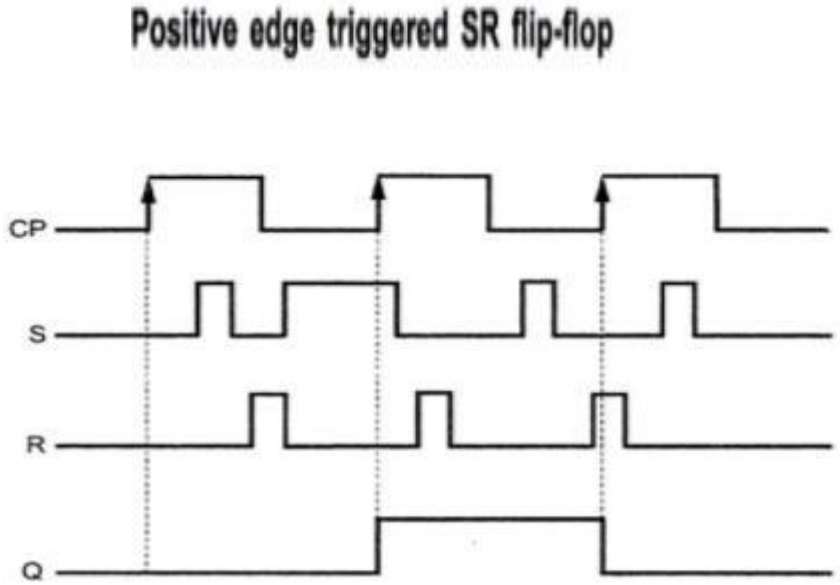


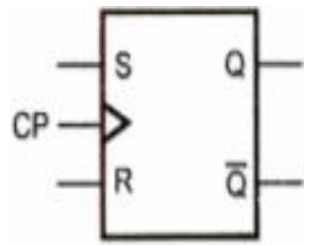
Excitation Table for SR flip-flop

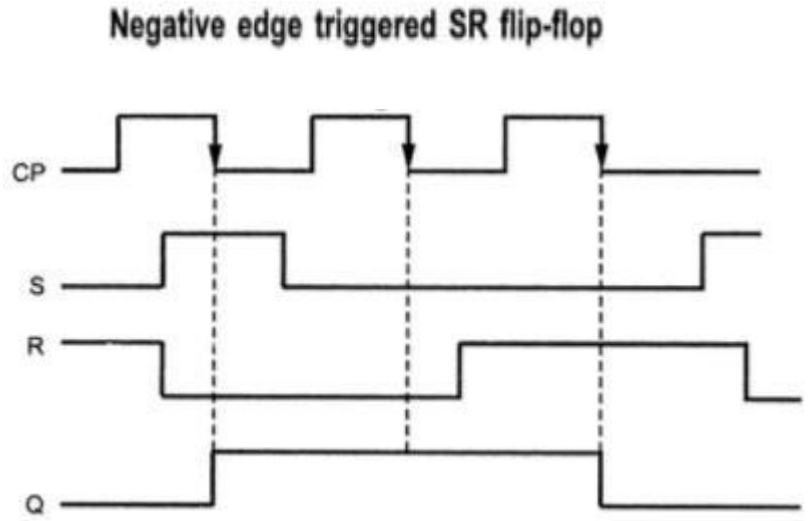
Outputs		Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

SR Flip Flop


S
3
$\overline{S}$
1
Q
CP
Positive edge detector circuit
A
4
$\overline{R}$
2
$\overline{Q}$
R


Positive edge triggered SR flip-flop
CP
S
R
Q


S
Q
CP
R
$\overline{Q}$


Negative edge triggered SR flip-flop
CP
S
R
Q

QUICK QUIZ (POLL)

What would be the output state in clocked SR flip flop when S=1, R=0 and CLK=0?

a) SET

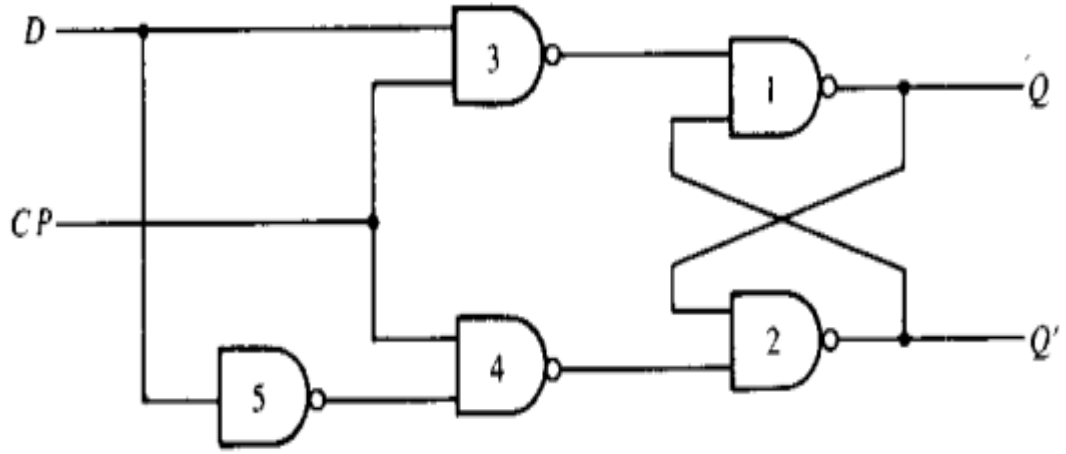
b) RESET

c) MEMORY

d) INVALID

D Flip Flop

D flip-flop can be used to create delay-lines which are used in digital signal processing systems.



Characteristic Table:

CLK	D	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	Q_n	$\overline{Q_n}$
1	0	0		
1	0	1		
1	1	0		
1	1	1		

D Flip Flop

Characteristic Table:

CLK	D	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

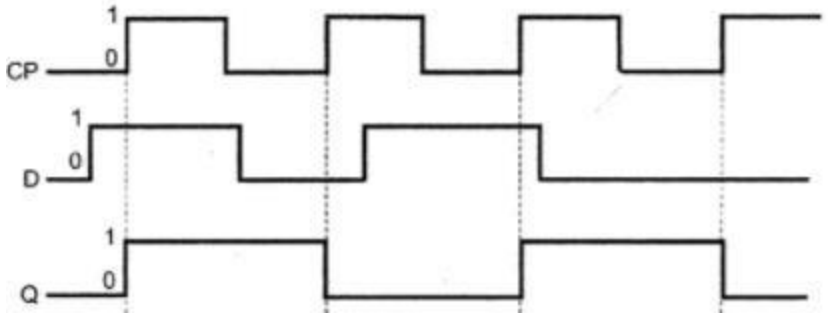
	$\overline{Q}$	Q
$\overline{D}$		
D		

Excitation Table for D flip-flop

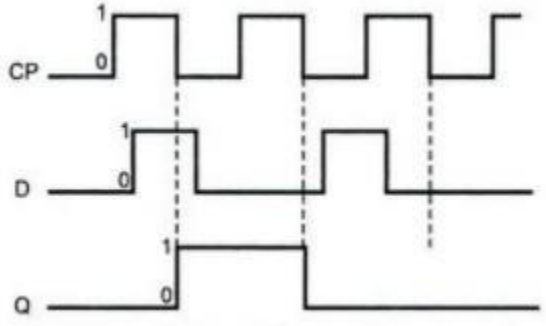
Outputs		Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

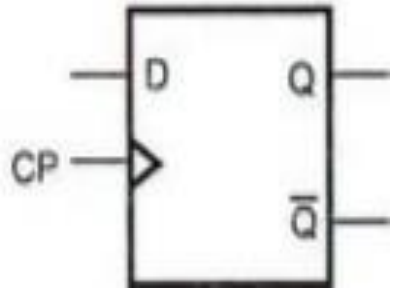
D-Flip Flop

Positive edge triggered D flip-flop



Negative edge triggered D flip-flop





CP	D	Q_{n+1}
↑	0	0
↑	1	1
0	X	Q_n

$Q_{n+1} = D$

QUICK QUIZ (POLL)

“The output is same as that of input, when clock is enabled”. This statement is true for

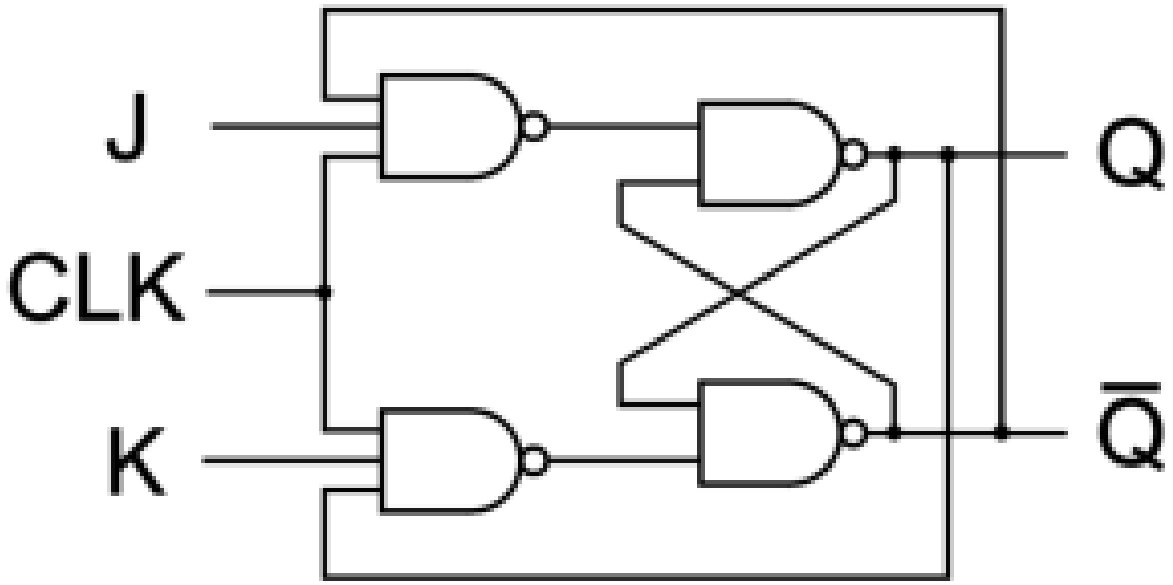
a) SR flip flop

b) D flip flop

c) JK flip flop

d) T flip flop

JK Flip Flop



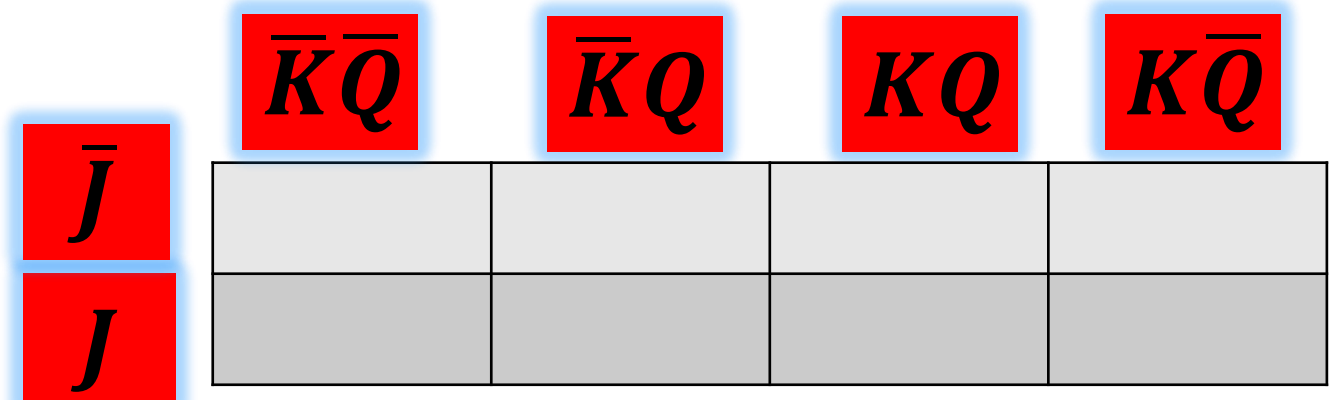
Characteristic Table:

CLK	J	K	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	×		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

JK Flip Flop

Characteristic Table:

CLK	J	K	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1



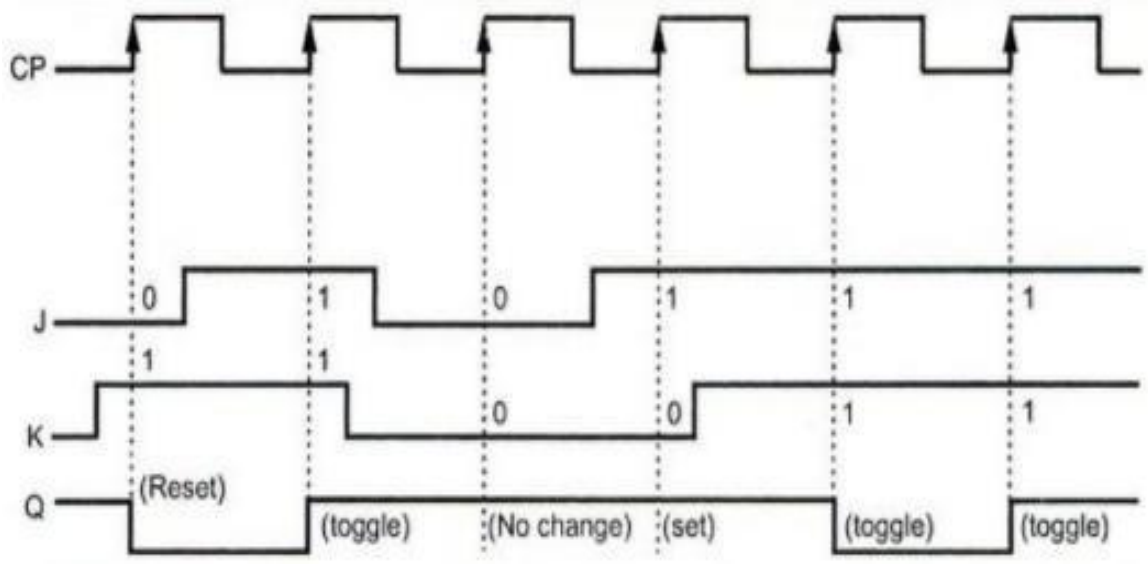
Excitation Table for JK Flip-Flop

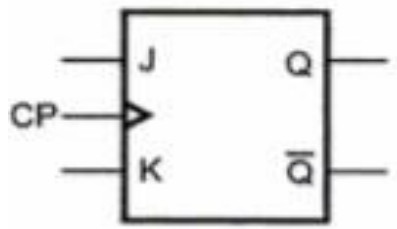
Outputs		Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

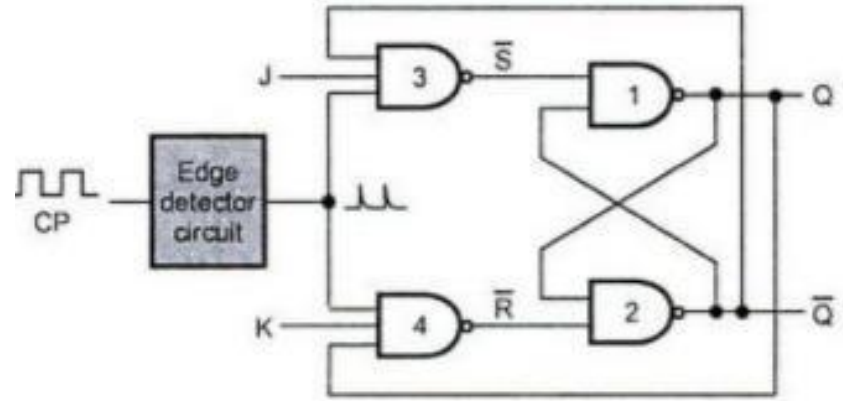
Application of JK FF

- Registers. A single **flip flop** can store a 1 bit word.
- Counters. Counter is a digital circuit used for a counting pulses or number of events and it is the widest **application** of **flip-flops** .
- Event Detectors- measures the contact failure phenomenon that occurs instantaneously due to vibration or temperature change of the connection parts when joining connectors.
- Data Synchronizers.
- Frequency Divider.

JK Flip Flop







Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

≡

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

QUICK QUIZ (POLL)

What would be the output state in clocked JK flip flop when J=1, K=1 and CLK=1?

a) SET

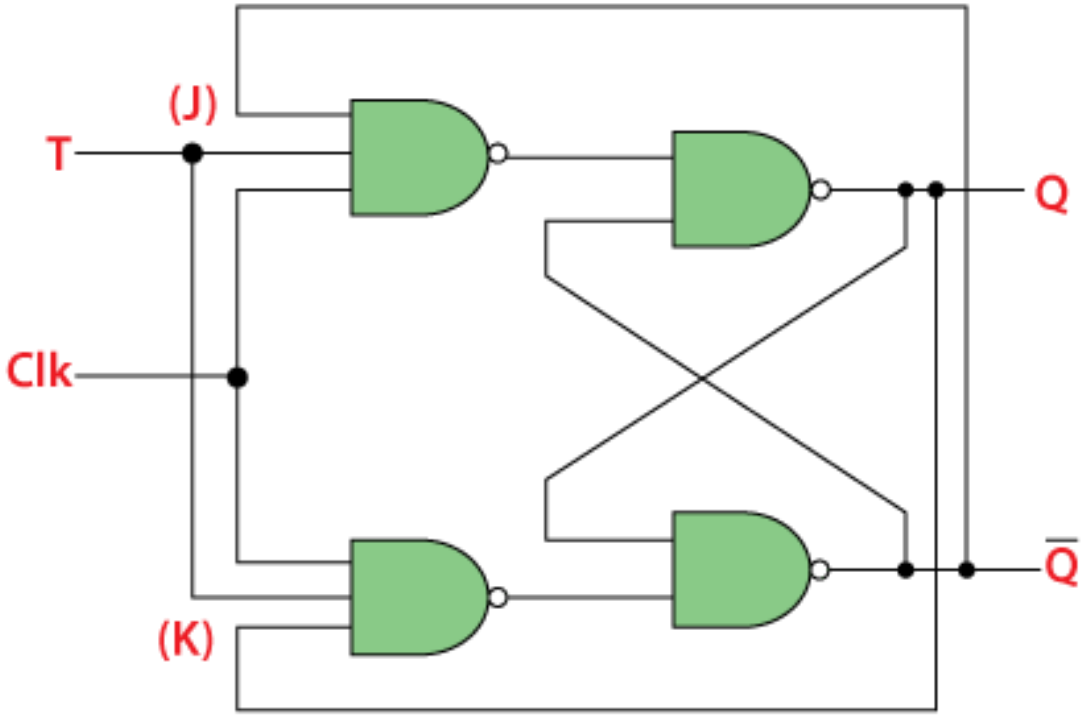
b) RESET

c) MEMORY

d) TOGGLE

T Flip Flop

major **applications of T flip-flop** are counters and control circuits.



Characteristic Table:

CLK	T	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	Q_n	$\overline{Q_n}$
1	0	0		
1	0	1		
1	1	0		
1	1	1		

T- Flip Flop

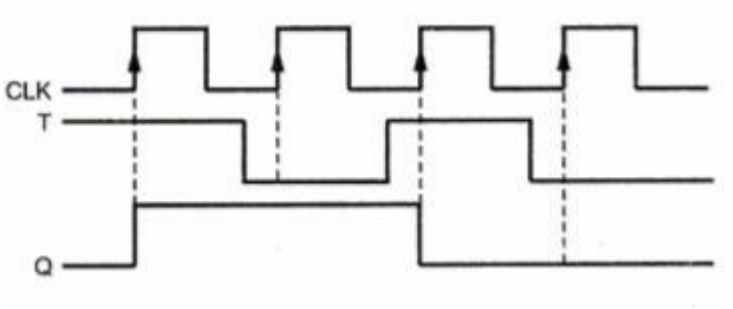
Characteristic Table:

CLK	T	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	×	×	Q_n	$\overline{Q_n}$
1	0	0	0	
1	0	1	1	
1	1	0	1	
1	1	1	0	

	$\overline{Q}$	Q
$\overline{T}$		
T		

Excitation Table for T Flip Flop

Outputs		Input
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0



QUICK QUIZ (POLL)

In a J-K flip-flop, if J=K the resulting flip-flop is referred to as _____

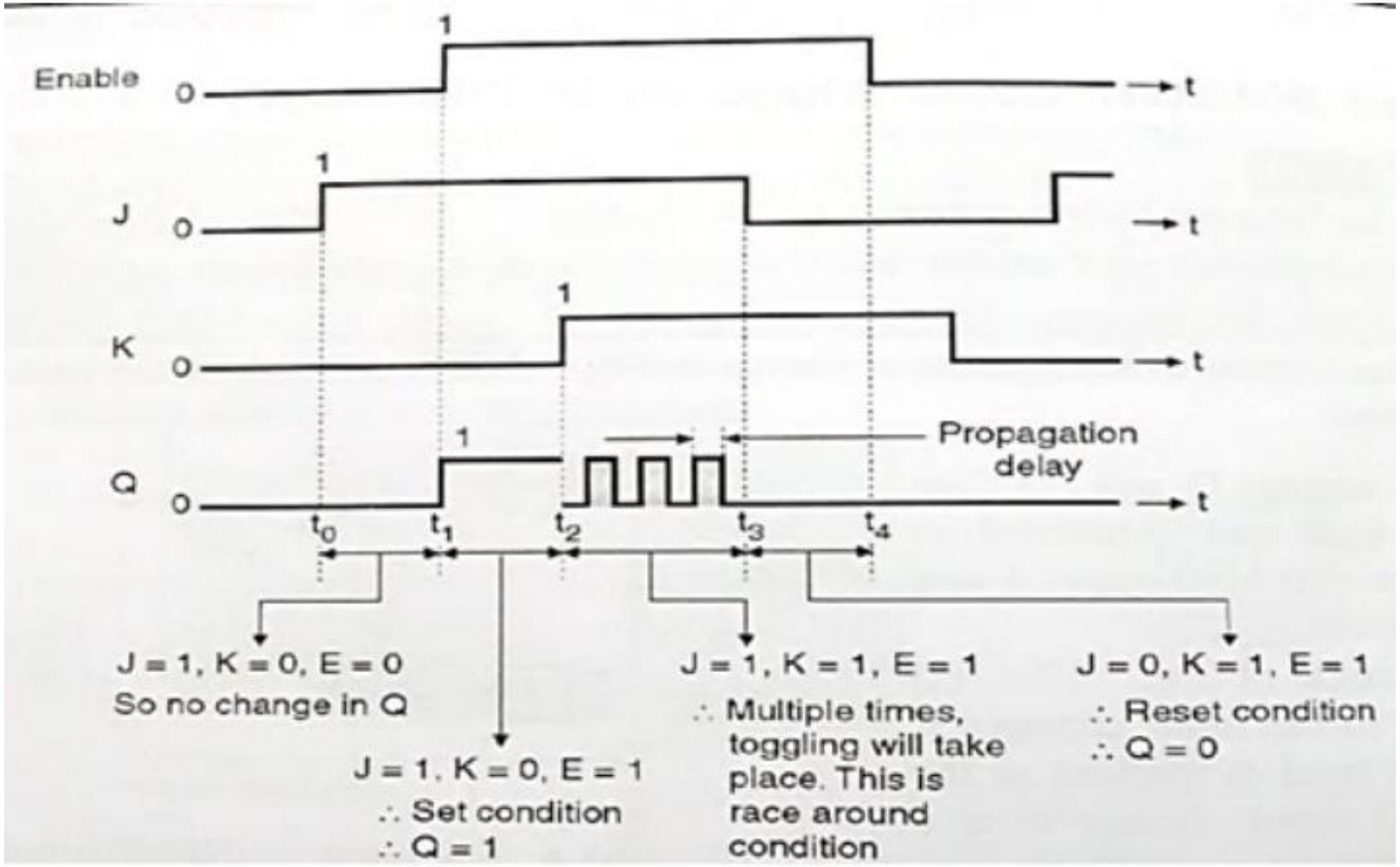
a) D flip-flop

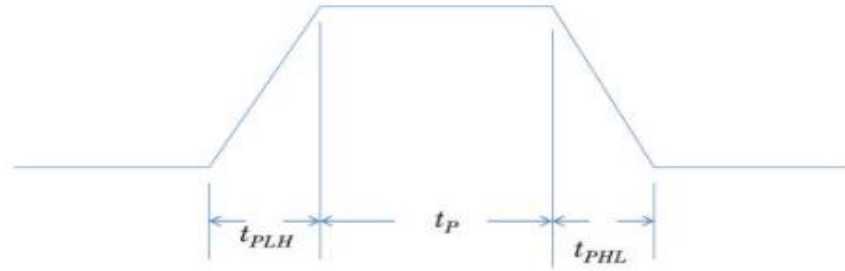
b) S-R flip-flop

c) T flip-flop

d) S-K flip-flop

Race Around Condition





RACE AROUND CONDITION

Now $t_{PLH} = t_{PHL} = \Delta t$ (Propagation delay time)

- The race-around condition (Problem) occurs when both the inputs of JK-Flip-flop are 1.
- If the width of the clock pulse t_P is too long, the state of the flip-flop will keep on changing from 0 to 1, 1 to 0 , 0 to 1 and so on, and at the end of the clock pulse, its state will be uncertain.
- This phenomenon is called the *rece around condition*.

Race Around Condition

- The *race around condition* occurs if $t_P >> \Delta t$.

How we can avoid race-around condition?

We can avoid race around condition by the following way.

1. If $t_P < \Delta t$.
2. By using edge triggering flip-flop.
3. By using Master-Slave JK Flip-flop.

MCQ

Which type of flip flop used to remove race around condition?

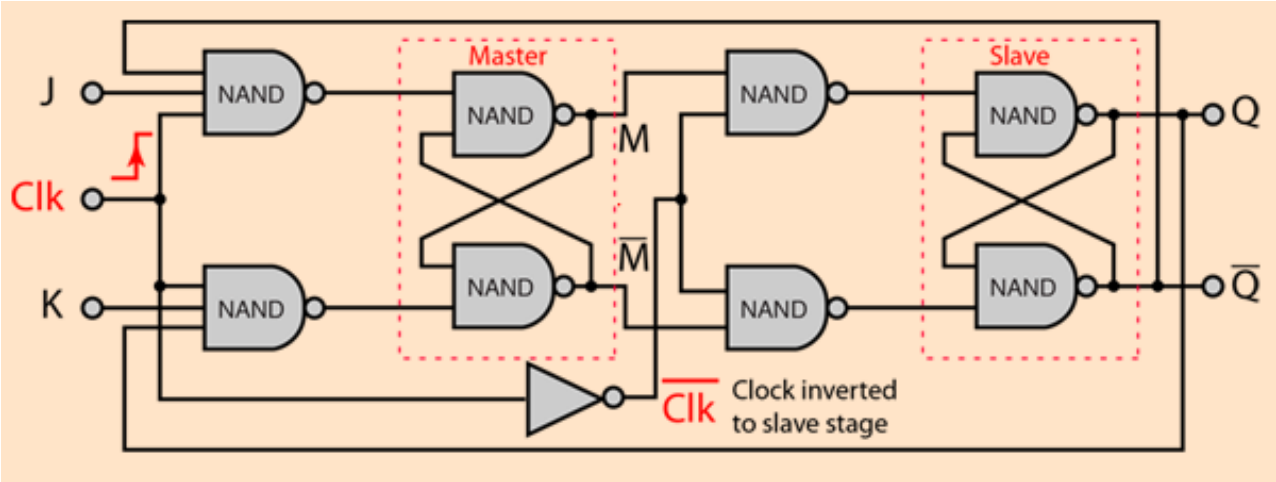
(a) SR flip flop

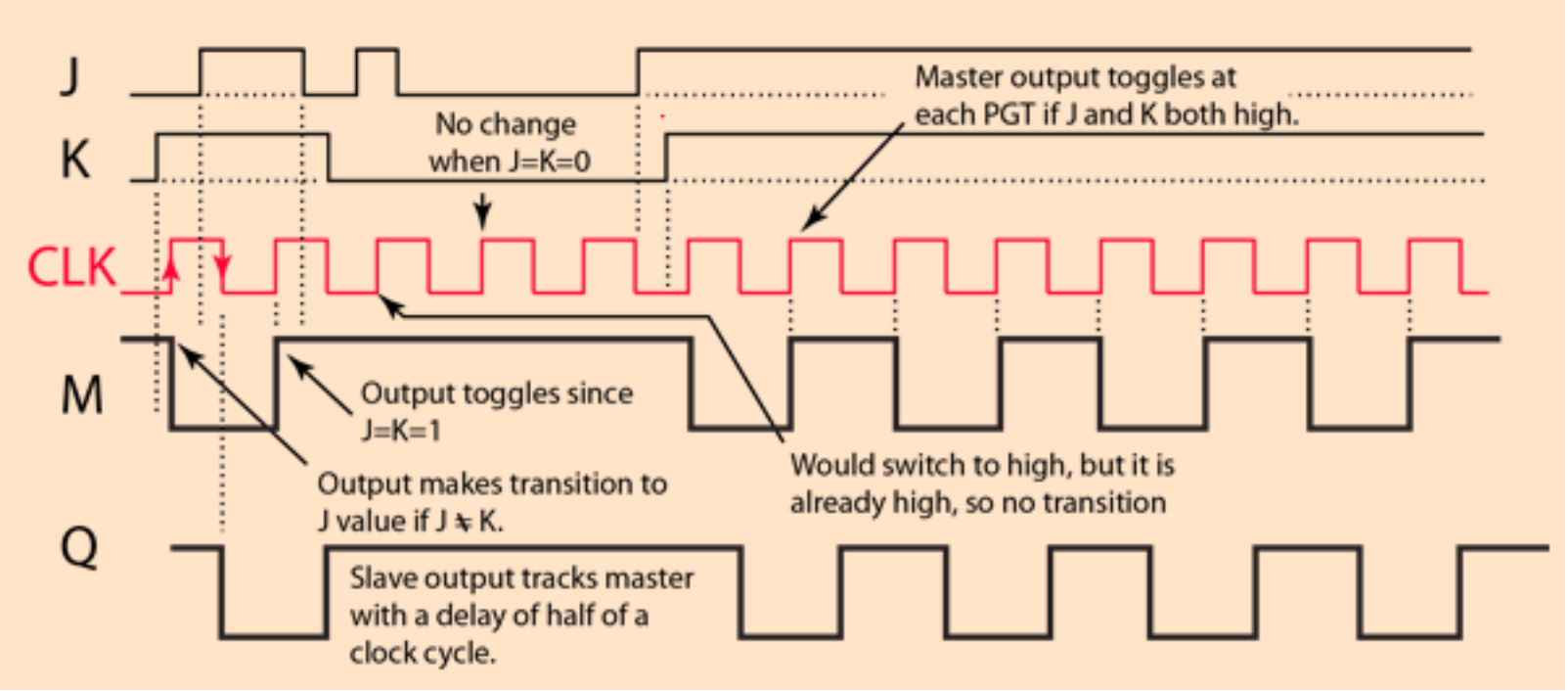
(b) JK flip flop

(c) T flip flop

(d) Master Slave flip flop

Master Slave





.MCQ

Which is true to remove race around condition?

(a) width of clock more than width of propagation delay of gate
(b) width of clock less than width of propagation delay of gate
(c) Master Slave flip flop
(d) both b and c