

**Dr Manoj kumar T**

**Assistant Professor,**

**Karpagam Institute of Technology, Coimbatore**

**Publication Details**

TITLE	CITED BY	YEAR
<a href="#">FPGA implementation of an optimized key expansion module of AES algorithm for secure transmission of personal ECG signals</a> PK TM Kumar Design Automation for Embedded Systems An International Journal	15*	2017
<a href="#">An optimized s-box circuit for high speed AES design with enhanced PPRM architecture to secure mammographic images</a> T Manojkumar, P Karthigaikumar, V Ramachandran Journal of Medical Systems 43 (2), 1-8	8	2019
<a href="#">A low area high speed FPGA implementation of AES architecture for cryptography application</a> TM Kumar, KS Reddy, S Rinaldi, BD Parameshachari, K Arunachalam Electronics 10 (16), 2023	7	2021
<a href="#">A novel method of improvement in advanced encryption standard algorithm with dynamic shift rows, sub byte and mixcolumn operations for the secure communication</a> KP Manoj Kumar T International Journal of Information Technology 12 (1), 825-830	3	2020
<a href="#">An Effective Software Based Method to Analyze SCA Countermeasures for Advanced Encryption Standard</a> T Manoj Kumar, P Karthigaikumar Wireless Personal Communications, 1-22		2021
<a href="#">Implementation of a High-Speed and High-Throughput Advanced Encryption Standard</a> TM Kumar, P Karthigaikumar INTELLIGENT AUTOMATION AND SOFT COMPUTING 31 (2), 1025-1036		2021
<a href="#">Implementation of Speed-Efficient Key-Scheduling Process of AES for Secure Storage and Transmission of Data</a> TM Kumar, KR Balmuri, A Marchewka, P Bidare Divakarachari, S Konda Sensors 21 (24), 8347		2021
<a href="#">Smart System for Monitoring Air Pollutants from Industries</a> DPK Manoj Kumar. T IJSART 2 (2), 192-195		2016
<a href="#">An Intelligent Traffic Monitoring System</a> TM Kumar International Journal of Advanced Research in Computer Science and Software ...		2015

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<b>An Efficient Performance Analysis of Different Adder Topologies</b> TM Kumar, S Navaneethan, AC Murugesapandian		2015
<b>COMPARISON ON VARIOUS ADDERS AND MULTIPLIERS IN DIFFERENT FPGA'S ARCHITECTURES AND ASIC AND THEIR PERFORMANCE STUDY</b> M Kumar T International Journal of Applied Engineering Research 10 (20), 19393-19398		2015
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<b>Analysis of DC Characteristics and short Channel effects in Junctionless FINFET</b> CJ Manoj Kumar.T International Conference on Knowledge Collaboration in Engineering 2014		2014
<b>Past,Present and Future of Nano CMOS Technologies</b> IEEE		2013
<b>A Bist Scheme for testing the SRAM based FPGA's Faults</b> M Kumar T International Conference on Recent Advancements in Engineering and ...		2013
<b>A Bist Scheme for testing the SRAM based FPGA</b> M Kumar T National Conference on Advanced computational Intellegience Systems 1, 501-506		2013
<b>A Bist scheme for testing the SRAM based FPGA's Faults</b> M Kumar T CAREER'13 1		2013
<b>A fast Low power Modulo 2n+1 multiplier</b> M Kumar T National level conference on Innovations in Engineering and Technology 1 ...		2012
<b>Transmission Lines and WaveGuides</b> NB Manoj Kumar.T Anuradha Publications		
<b>A BIST scheme for fault detection in SRAM based FPGA</b> M Kumar.T IEEE		