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List of publications

1. **Arun Samuel, TS**, Balamurugan, NB, Bhuvaneswari,S, Sharmila, D & Padmapriya, K 2013, 'Analytical modelling and simulation of single-gate SOI TFET for low-power applications', **International Journal of Electronics**, Publisher: **Taylor & Francis**, Vol. 101, No. 6, pp.779–788 (ISSN: 0020-7217 **Impact Factor: 0.737**).
2. **Arun Samuel, TS** & Balamurugan, NB, Sibitha,S, Saranya,R & Vanisri, D 2013, 'Analytical Modeling and Simulation of Dual Material Gate Tunnel Field Effect Transistors', **Journal of Electrical Engineering & Technology**, vol. 8, no. 6, pp. 1481-1486. (ISSN: 1975-0102 **Impact Factor: 0.579**).
3. **Arun Samuel, TS** & Balamurugan, NB 2013, 'An Analytical Modeling and Simulation of Dual Material Double Gate Tunnel Field Effect Transistor for Low Power Applications', **Journal of Electrical Engineering & Technology**, vol. 9, no. 1, pp. 247-253. (ISSN: 1975-0102, **Impact Factor: 0.579**)
4. **Arun Samuel, TS**, Balamurugan, NB 2014, Niranjana, T & Samyuktha, B 'Analytical Surface potential model with TCAD simulation verification for evaluation of Surrounding Gate TFET', **Journal of Electrical Engineering & Technology**, vol.9, no.2, pp. 655-661. (ISSN: 1975-0102, **Impact Factor: 0.579**)
5. **Arun Samuel, TS** & Balamurugan, NB 2014, 'Analytical Modeling and Simulation of Germanium Single Gate Silicon on Insulator TFET', **Journal of Semiconductors** Publisher: **IOP Science**, Vol.35, No.3, pp.034002-1-4 (ISSN: 1674-4926, **Impact Factor: 0.378**).
6. **Arun Samuel T.S** & Helen Ramya.J, 2015, 'Potential and electric field model for 18 nm Germanium based Dual Material Gate tunnel field effect transistor', **International Journal of Applied Engineering Research**, Publisher: **Research India Publications**, Vol.10, No.1, pp.253-257. (ISSN 0973-4562)
7. S.Rama Kalangiam and **T. S. Arun Samuel**, 2015, 'A QOS Based EQGOR Protocol for WSN and VANET', **International Journal of Applied Engineering Research**, Publisher: **Research India Publications**, Vol.10, No.55, pp.1762-1766. (ISSN 0973-4562)
8. Vanitha.P, Balamurugan.N.B, **ArunSamuel.T.S** 2015, "2-D Analytical Modeling and Simulation of Dual Material Surrounding Gate Tunnel FET (DMSGTFET) For Diminished SCES",**International Journal of Applied Engineering Research**,

Publisher: Research India Publications, Vol.10, No.7, pp. 18551-18564. (ISSN 0973-4562).

9. **T.S.Arun Samuel** and M.Karthigai Pandian 2016, “Comparative Performance Analysis of Multi Gate Tunnel Field Effect Transistors”, **Journal of Nano Research**, Vol. 41, pp 1-8). (ISSN: 1661-9897).
10. **T.S. Arun Samuel**, N. Arumugam and A. Shenbagavalli 2016, “Drain Current Characteristics Of Silicon Nanowire Field Effect Transistor”, **ICTACT Journal On Microelectronics**, Vol. 2, No.3, pp 284-287.
11. **T.S. Arun Samuel**, S. Darwin and N. Arumugam 2017, “Design of adiabatic logic based comparator for low power and high speed applications”, **ICTACT Journal On Microelectronics**, Vol.3, No.1, 365-369.
12. R. Anand, **T.S. Arun Samuel** and P. Melba Mary 2017, “Improved dynamic response of isolated full bridge DC to DC converter using BATA optimization tuned fuzzy sliding mode controller for solar applications”, **International Journal of Hydrogen Energy-Elsevier** Vol. 42, pp. 21648 -21658.
13. G. Rajakumar, A. Andrew Roobert, **T. S. Arun Samuel** & D. Gracia Nirmala, 2017 “Low power VLSI architecture design of BMC, BPSC and PC scheme” **Analog Integrated Circuits and Signal Processing-Springer**, Vol.93, pp.169-178.
14. **T.S.Arun Samuel**, N. Arumugam and S.Theodore Chandra 2017 “Analytical Approach and Simulation of GaN Single Gate TFET and Gate All around TFET”, **ECTI transactions on electrical eng., electronics, and communications**, Vol.15, No.02, pp. 1-7. (ISSN: 1685-9545).
15. G. Rajakumar, T.Ananth Kumar and **T.S. Arun Samuel**, 2018 “IOT Based Milk Monitoring System For Detection Of Milk Adulteration”, **International Journal of Pure and Applied Mathematics**, Vol.118, No.9, pp.21-32.
16. R. Solomon Roach, N.Nirmal Singh and **T. S. Arun Samuel**, 2018 “Resource Minimization and Power Reduction of ESPFFIR Filter Using Unified Adder/Subtractor”, **Analog Integrated Circuits and Signal Processing-Springer**, (published online), (ISSN: 0925-1030, **Impact Factor: 0.8**).
17. **T. S. Arun Samuel** and S. Komalavalli, 2018, Mathematical Modeling and TCAD Simulation of TMQG Tunnel Field Effect Transistors for Low Power Applications, **Journal of Nano Research**, Vol.54, pp.146-157, Aug 2018. (ISSN: 1661-9897, **Impact Factor: 0.8**).

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