B.E / B.Tech MODEL EXAMINATION NOVEMBER / DECEMBER 2020

Third Semester

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Branch : CSE

Subject Code : CS8382 – Digital system Laboratory.

DATE : 16/12/2020

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1) Using HDL simulate any one FlipFlop.

Aim

To design a ripple counter and verify its output using Verilog HDL

Tools Required:

Xilinx 8.1 ISE

Algorithm:

* Get input as "clk" and the outputs as 'qa', 'qb', 'qc', 'qabar', 'qbbar', 'qcbar',

*) The outputs are obtained using t-flipflop for T-flip flop:

(ii) Get the input at t, clk and output q, qbar

(iii) operation when t=0 → previous state

(iv) when t = 1 → q = ~q ; qbar = ~q

T- flip-flop is a flip-flop in which the state change (toggles) when transition occurs from 0 to 1. Ripple counter is asynchronous counter using T-flip-flop

Program

```
module ripplecounter(clk, qa, qb, qc, qabar,
qbbar, qcbar);
input clk;
output qa, qb, qc, qabar, qbbar, qcbar.
tflipflop g1(1, clk, qc, qcbar);
tflipflop g1(1, clk, qb, qbbar);
tflipflop g1(1, clk, qa,
                    qabar);
endmodule.
```

//t flipflop

```
module tflipflop(t, clk, q, qbar);
input t, clk;
output q, qbar;
reg q, qbar;
initial
    begin
        q=0;
        qbar;
    end
always @(negedge clk)
begin
    if(t==1)
        begin
            q = q;
            qbar = qbar;
        end
```

```
else
    begin
        q = ~q;
        qbar = ~qbar
    end
end
end module.
```

CircuitVerse - Digital Circuit Sim

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Paused

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tflipflop x | half adder x | half subtractor x

```
1  // Write Some Verilog Code Here!
2  module tflipflop( t, clk, q , qbar);
3      input t, clk;
4      output q, qbar;
5      reg q, qbar;
6    initial
7      begin
8        q=0;
9        qbar=1;
10
11     end
12     always@(negedgeclk)
13       begin
14         if (t == 1)
15           begin
16             q = q;
17             qbar = qbar;
18           end
19         else
20           begin
21             q = ~q;
22             qbar = ~qbar;
23           end
24       end
25 endmodule
```

VERILOG MODULE

Reset Code

Save Code

PROPERTIES

PROJECT PROPERTIES

Project:

Untitled

Circuit:

tflipflop

Clock Time (ms):

- 500 +

Clock Enabled:

Lite Mode:

Edit Layout

Delete Circuit

Result

Thus ripple counter is designed using HDL

(ii) Design and implement a combinational circuit using basic gates for arbitrary function like a half adder and half subtractor.

Aim

To Design and construct halt subtractor, half Adder using.

Procedure

Half Adder

* Design the half Adder using input & output element from the circuit element
* Now select input and output and by one select the properties and give the labels to input and output x, y, Sum & Carry
* Now click the empty region of canvas in Half adder circuit you'll get "Edit layout" in Properties click if you will half adder representation in block diagram from which you can change layout per requirements Then click 'save'.

Halt substractor.

(*) Follw the same procedure as Half Adder and design Half Substractor.

Half Adder Truth Table.

A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Halt substractor

A	B	Borrow	Difference
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

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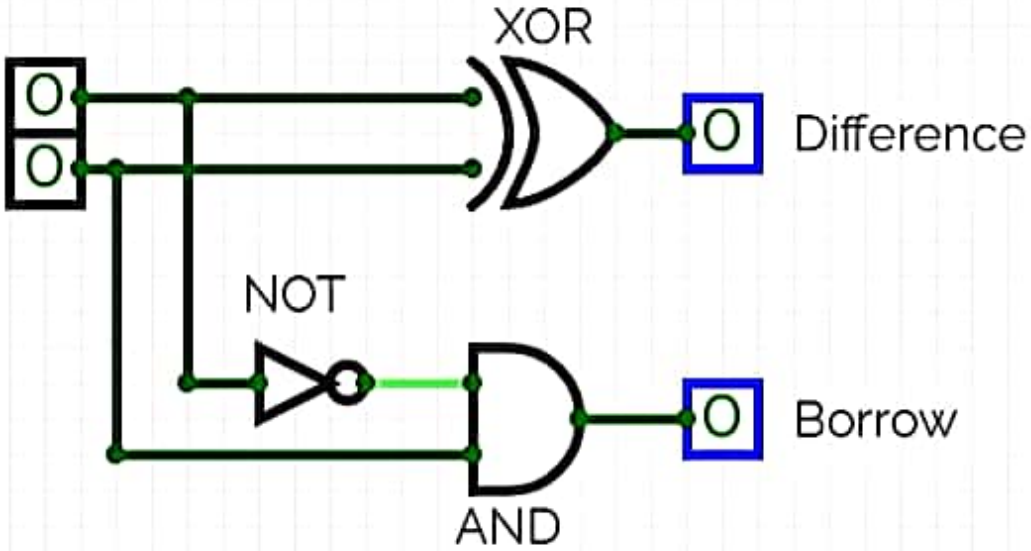
tflipflop x | half adder x | half subtractor x

CIRCUIT ELEMENTS

TIMING DIAGRAM



PROPERTIES

PROJECT PROPERTIES

Project:

Untitled

Circuit:

half subtractor

Clock Time (ms):

- 500 +

Clock Enabled:

Lite Mode:

Edit Layout

Delete Circuit

15:30
16-12-2020

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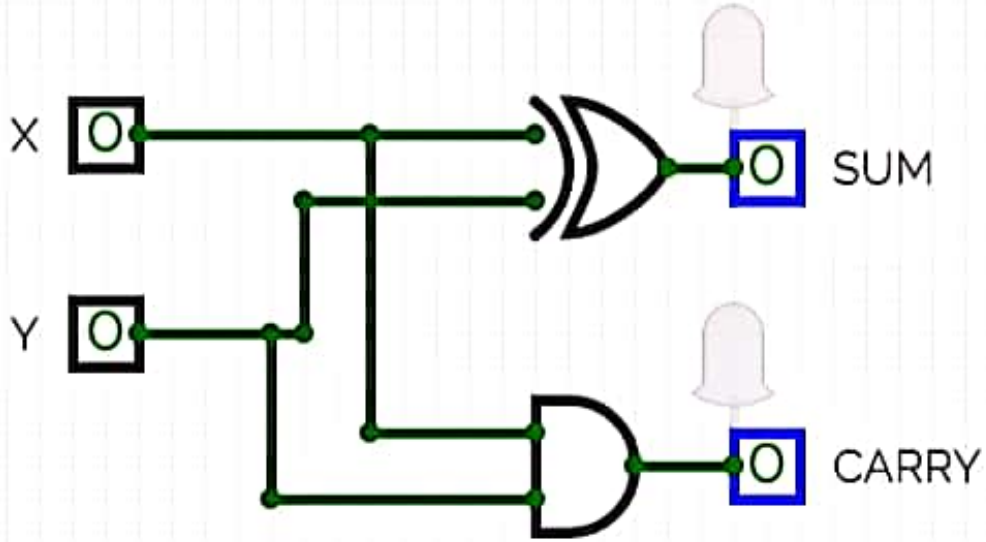
tflipflop x half adder x half subtractor x

CIRCUIT ELEMENTS

TIMING DIAGRAM



PROPERTIES

PROJECT PROPERTIES

Project:

Untitled

Circuit:

half adder

Clock Time (ms):

- 500 +

Clock Enabled:

Lite Mode:

Edit Layout

Delete Circuit

Result

Thus half adder, half substractor circuits are verified.