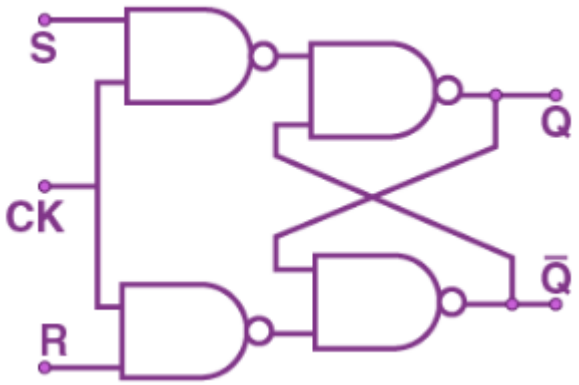
FLIP-FLOPS

S-R Flip Flop

Diagram:



Truth Table:

S	R	Qn+1	State
0	0	Qn	Hold
0	1	0	Reset
1	0	1	Set
1	1	X	Invalid

Block diagram:

SR Flip Flop basic Block diagram

Working of SR Flip Flop

- **Case 1**: Let's say, **S=0** and **R=0**, then output of both AND gates will be 0 and the value of Q and Q' will be same as their previous value, i.e, Hold state.
- **Case 2**: Let's say, **S=0 and R=1**, then output of both AND gates will be 1 and 0, correspondingly the value of Q will be 0 as one of input is 1 and it is a NOR gate so it will ultimately gives 0, hence Q gets 0 value, similarly Q' will be 1.
- **Case 3**: Let's say, **S=1 and R=0**, then output of both AND gates will be 0 and 1, correspondingly the value of Q' will be 0 as one of input to NOR gate is 1, so output will be 0 ultimately and this 0 value will go as input to upper NOR gate, and hence Q will become 1.
- **Case 4**: Let's say, **S=1 and R=1**, then output of both AND gates will be 1 and 1 which is invalid, as the outputs should be complement of each other.

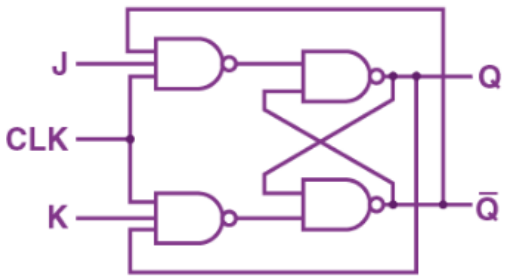
Applications of SR Flip Flop

There are numerous applications of SR Flip Flop in Digital System, which are listed below:

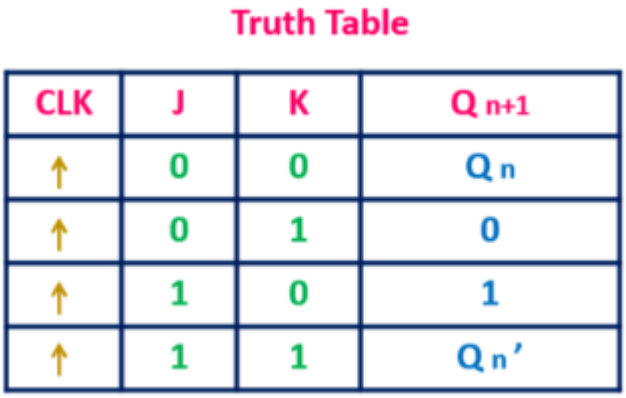
- **Register**: SR Flip Flop used to create register. Designer can create any size of register by combining SR Flip Flops.
- **Counters**: SR Flip Flops used in counters. Counters count the number of events that occurs in a digital system.
- **Memory**: SR Flip Flops used to create memory which is used to store data, when the power is turned off.
- **Synchronous System**: SR Flip Flops are used in synchronous systems which are used to synchronise the operation of different component.

J K Flip-Flop

Diagram:



Truth Table:



Working of JK-Flip Flops:

1. **Basic Structure**: A JK flip-flop is a digital circuit component that stores one bit of data. It has two inputs, J (set) and K (reset), and two outputs, Q (output) and Q' (complementary output).
2. **Truth Table**: The behavior of a JK flip-flop is defined by its truth table, which outlines the output (Q and Q') for all possible combinations of inputs (J and K) and the current state (Q).

J	K	Q (output)	Q' (complementary output)
0	0	Q	Q'
0	1	0	1
1	0	1	0
1	1	Q' (Toggle)	Q (Toggle)

3. **Operation**:
   - When both J and K inputs are LOW (0), the flip-flop maintains its current state. If Q is currently HIGH, it remains HIGH, and if it's LOW, it remains LOW.
   - When J is HIGH (1) and K is LOW (0), the flip-flop sets (or sets to 1) its output Q to HIGH (1).
   - When J is LOW (0) and K is HIGH (1), the flip-flop resets (or clears to 0) its output Q to LOW (0).
   - When both J and K are HIGH (1), the flip-flop toggles its output Q. If Q is currently HIGH, it switches to LOW, and if it's LOW, it switches to HIGH.
4. **Sequential Operation**: A series of JK flip-flops can be connected together to form sequential circuits like counters, shift registers, and memory units. In such circuits, the output of one flip-flop serves as the input to the next flip-flop.
5. **Clock Input (Optional)**: In some implementations, JK flip-flops may have an additional clock input. When the clock input changes state (e.g., rising edge, falling edge), the flip-flop will only respond to changes in the J and K inputs during that transition, allowing for synchronized operation.

Applications of JK Flip-Flop

We can simply implement a JK-flipflop using NAND gates. In that case two NAND gates need to be connected together and the output of that will be feed to the input which will create a stable state-holding circuit. The resulting circuit will be the NAND gate. So, by following this mechanism we can develop and use JK-flipflop for various application which are listed below.

- **Counters:** These are very essential components for the application of frequency dividers and event sequencers where there is a need of storing and propagating the count value. We can design binary synchronous and asynchronous counters using JK-flipflop.
- **Shift registers:** For data storage and manipulation, serial-to-parallel or parallel-to-serial data conversion the shift registers are widely used. Registers can store and shift the binary data in a sequential manner. We can design it by JK-flipflops.
- **Memory Units:** JK-flipflop itself act as a memory unit to store binary information. By making a sequential chain of JK-flipflops we can use it even as RAM.

Advantages of JK Flip-Flop

- **Versatility:** As discussed above, JK-flipflops can be used as a basic memory element or a primary building block of further complex memory design. It is very much adaptive as it can be operated in both synchronous and asynchronous modes.
- **Toggle Functionality:** The application which are required to get output as its complement of input that also can be developed by JK-flipflops as when J=K=1 it triggers toggle state which gives output which is complement with it's each clock pulse.
- **Error Detection and Correction:** We can use a complex circuit built by JK-flipflops which can detect and correct information during data-transmission.

Disadvantages of JK Flip-Flop

- **Complexity:** Compared to other types of flipflops(D,T, SR), JK flipflop requires additional logic gates to implement which consumes extra memory resources and increases complexity to operate.
- **Propagation Delay:** This is the major problem present in JK-FF. Propagation delay results a timing delay in certain application which are time-flow sensitive.
- **Race Problem:** This issue arises when the clock input's timing pulse isn't given enough time to turn "Off" before the output Q's state is altered.

D Flip-Flop:

D flip flop is an electronic devices that is known as “delay flip flop” or “data flip flop” which is used to store single bit of data.D flip flops are synchronous or asynchronous. The clock single required for the synchronous version of D flip flops but not for the asynchronous one.The D flip flop has two inputs, data and clock input which controls the flip flop. when clock input is high, the data is transferred to the output of the flip flop and when the clock input is low, the output of the flip flop is held in its previous state.

Working of D Flip Flop

D flip flop consist of a single input D and two outputs (Q and Q’). The basic working of D Flip Flop is as follows:

- When the clock signal is low, the flip flop holds its current state and ignores the D input.
- When the clock signal is high, the flip flop samples and stores D input.
- The value that was previously fed into the D input is reflected at the flip flop’s Q output.
    - If D = 0 then Q will be 0.
    - If D = 1 then Q will be 1.
- The Q’ output of the flip flop is complemented by the Q output.
    - If Q = 0 then Q’ will be 1.
    - If Q = 1 then Q’ will be 0.

D	CLK	$\bar{Q}$
0	1 (Raising Edge)	0
1	1 (Raising Edge)	1

Truth Table of D Flip Flop

Characteristic Table of D Flip Flop

The characteristic table of the D flip flop displays the behavior of the flip flop for each combination of input and current state. The characteristic table for a D flip flop is as follows.

D	Q(Current)	Q(n+1) (Next)
0	0	0
0	1	0
1	0	1
1	1	1

Characteristics table of D Flip Flop

- D is the input, and Q is current state, Qn + 1 is the next state outputs.
- Qn+1 will always be zero when D is 0, irrespective of current state of flip flop.
- When the input of the flip flop is 1, next state of flip flop will always be 1, regardless of the current state of flip flop.

Characteristic Equation of D Flip Flop

The characteristics equation of D flip flop consist of a Boolean expression that explains the relationship between the input and output of the flip flop. The characteristic equation for a D flip flop is as follows.

$$Q(n+1) = D(n)$$

Characteristics Equation of D Flip Flop

- Qn+1 represents the output of flip flop at the next clock cycle.
- Dn is the input to the flip flop at the current clock cycle, and n represents the current clock cycle.

- This characteristic equation of D flip flop states "**that the output of the flip flop at the next clock cycle will be equal to the input at the current clock cycle**".

D Flip Flop Excitation Table

Her, Qn represents the current state of the flip flop, and Dn represents the current input of the flip flop. Where as Qn+1 represents the next state of the flipflop.

- When the Qn is 0 and the Dn is also 0, then the Qn+1 becomes 0. This situation explains the condition of "hold" state.
- When the Qn is 0 but Dn is 1, then the Qn+1 becomes 1. This situation explains the condition of "reset" state.
- When the Qn is 1 but Dn is 0, then the Qn+1 becomes 0. This situation explains the condition of "hold" state.
- When the Qn is 1 and the Dn is also 1, then the Qn+1 becomes 1. This situation explains the condition of "reset" state.

Q(n)	D(n)	Q(n+1) (Next)
0	0	0
0	1	1
1	0	0
1	1	1

Advantages of D Flip Flop

- D flip flop is very simple to design.
- The computation speed of D flip flop is very fast compared to other flip flops.
- D flip flop requires very few components to design which makes it simple to understand.

Disadvantages of D Flip Flop

- D flip flops are glitch prone. When input varies fast, flip flop output may glitch. Digital circuit glitches are hard to identify and fix.

Types of D Flip Flop

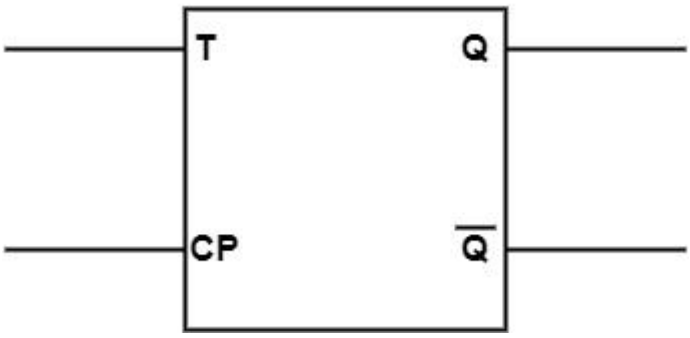
- D Latch.
- Edge Triggered D Flip Flop.

Application of D Flip Flop

D flip flop is having numerous number of application in digital system is described as follows:

- **Memory:** D flip flop is used to create memory circuit for holding the data.
- **Registers:** D flip flop is used to create register, which can hold data in digital system. By using the D flip flop the designer can built any size of register as per the requirement.
- **Counters:** D flip flops are used to create the counters which counts the number of event occurred in the digital system.
- **Synchronous System:** D flip flop is having in developing the synchronous system.

T- Flip Flop



1. **Basic Structure**: The T flip-flop has a single input T (toggle) and two outputs, Q and Q' (complementary output). It operates based on the rising or falling edge of a clock signal.
2. **Truth Table**: The behavior of a T flip-flop is defined by its truth table, which outlines the output (Q and Q') for all possible combinations of inputs (T) and the current state (Q).

T	Q (output)	Q' (complementary output)
0	Q	Q'
1	Q' (Toggle)	Q (Toggle)

3. **Operation**:
    - When T is LOW (0), the flip-flop maintains its current state. If Q is currently HIGH, it remains HIGH, and if it's LOW, it remains LOW.
    - When T is HIGH (1), the flip-flop toggles its output Q. If Q is currently HIGH, it switches to LOW, and if it's LOW, it switches to HIGH.

4. **Memory Element**: Like other flip-flops, a T flip-flop can store one bit of memory. However, its unique feature is the ability to toggle its output state with each clock pulse.
5. **Applications**:
    - T flip-flops are commonly used in frequency division circuits and as building blocks for more complex sequential circuits.
    - They are also utilized in counters, frequency dividers, and in applications where toggling between two states is required.
6. **Clock Input (Optional)**: A T flip-flop can have an additional clock input for synchronous operation. The state changes (toggle) occur only when the clock signal transitions.
7. **Implementation**:
    - T flip-flops can be built using other types of flip-flops, such as D flip-flops or JK flip-flops, with additional logic gates to achieve the toggling behavior.
    - They can also be implemented using electronic components like transistors, where the input T controls the state of the flip-flop.