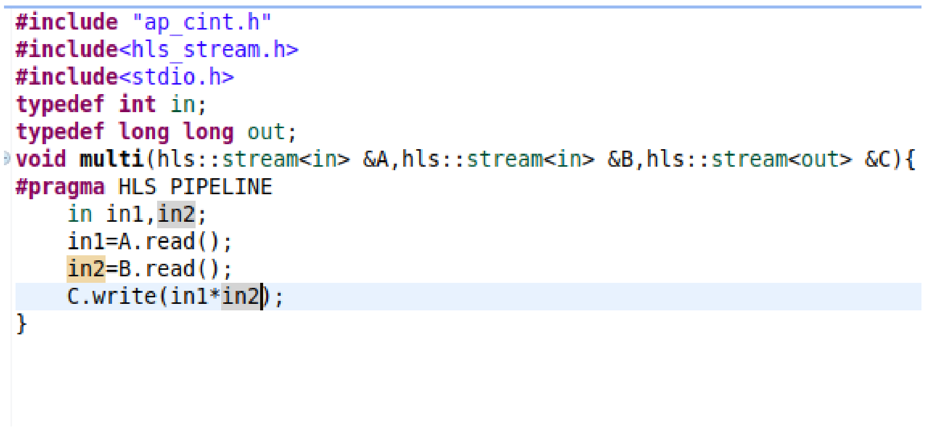
HLS-Assignment 3

March 21, 2023

ramesh randhi
FWC22076

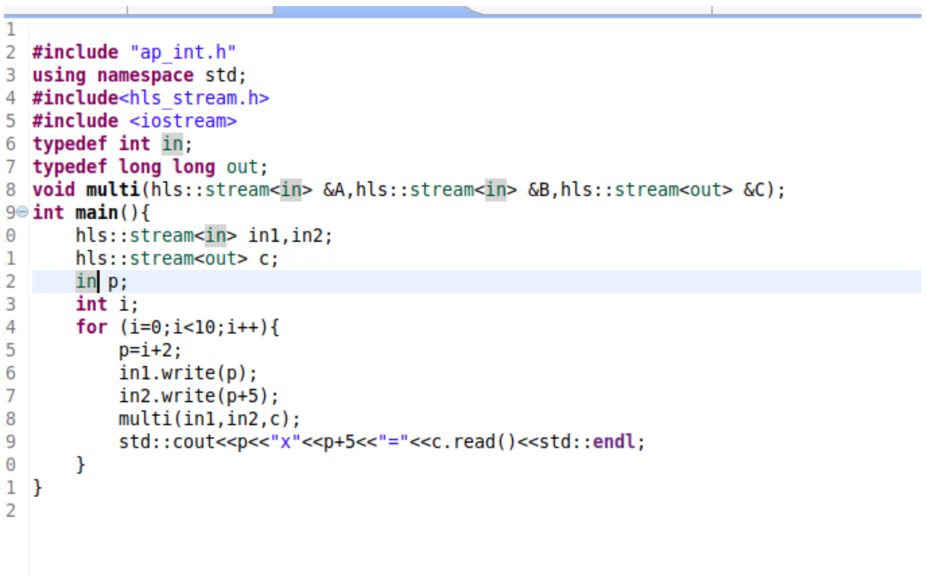
1 Problem Statement

Repeat the experiment in Assignment 2.3 but by configuring the module as pipelined.
Record your observations wrt timing and resource consumption. Explain why you think pipeline affected those numbers.
Include all code, entire synthesis report, simulation output, and C/RTL co simulation output and report.



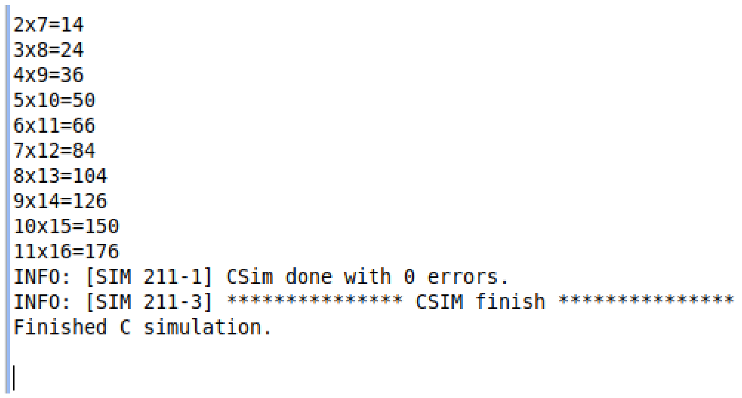
```
#include "ap_cint.h"
#include<hls_stream.h>
#include<stdio.h>
typedef int in;
typedef long long out;
void multi(hls::stream<in> &A,hls::stream<in> &B,hls::stream<out> &C){
#pragma HLS PIPELINE
    in in1,in2;
    in1=A.read();
    in2=B.read();
    C.write(in1*in2);
}
```

Figure 1: cpp file 3.1.1



```
#include "ap_int.h"
using namespace std;
#include<hls_stream.h>
#include <iostream>
typedef int in;
typedef long long out;
void multi(hls::stream<in> &A,hls::stream<in> &B,hls::stream<out> &C);
int main(){
    hls::stream<in> in1,in2;
    hls::stream<out> c;
    in p;
    int i;
    for (i=0;i<10;i++){
        p=i+2;
        in1.write(p);
        in2.write(p+5);
        multi(in1,in2,c);
        std::cout<<p<<"x"<<p+5<<"="<<c.read()<<std::endl;
    }
}
```

Figure 2: testbench file 3.1.2



```
2x7=14
3x8=24
4x9=36
5x10=50
6x11=66
7x12=84
8x13=104
9x14=126
10x15=150
11x16=176
INFO: [SIM 211-1] CSim done with 0 errors.
INFO: [SIM 211-3] *************** CSIM finish ***************
Finished C simulation.
```

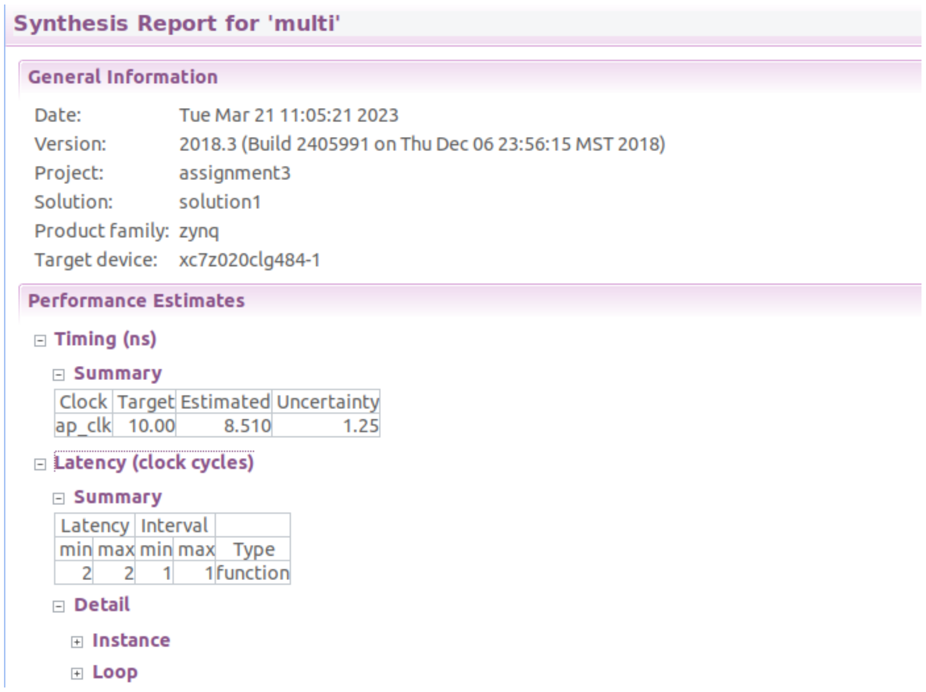
Figure 3: csim file 3.1.3

Pipelining in HLS can improve the throughput of a system by allowing multipl
operations to be executed simultaneously.

It can also reduce the latency of a system by dividing the computation into
stages that can be executed in parallel.

Pipelining can make better use of hardware resources and make timing closure

In the above 2 examples we can observe that usage of LUT will be
decreased by using
the pipeline



Synthesis Report for 'multi'

General Information

Date:	Tue Mar 21 11:05:21 2023
Version:	2018.3 (Build 2405991 on Thu Dec 06 23:56:15 MST 2018)
Project:	assignment3
Solution:	solution1
Product family:	zynq
Target device:	xc7z020clg484-1

Performance Estimates

⊟ Timing (ns)

⊟ Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

⊟ Latency (clock cycles)

⊟ Summary

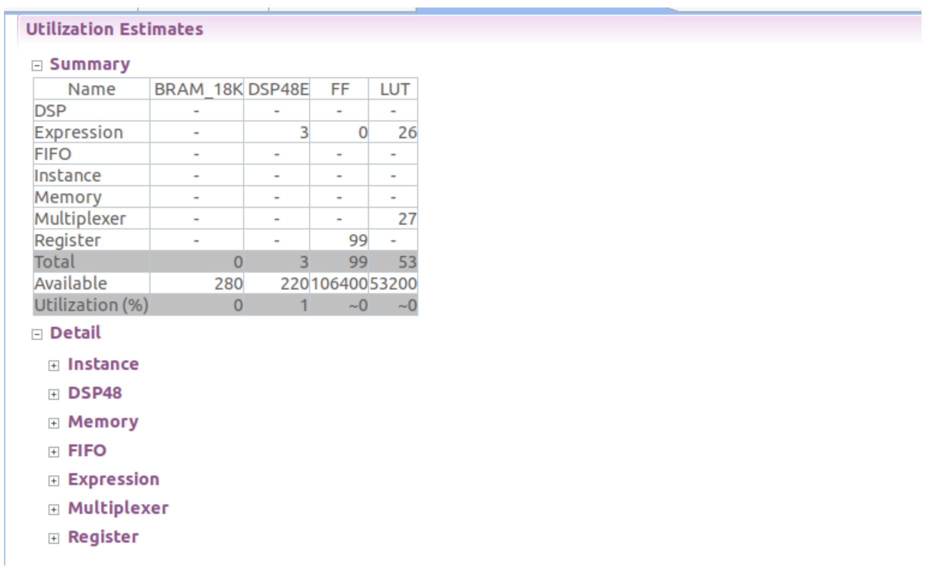
Latency		Interval		
min	max	min	max	Type
2	2	1	1	function

⊟ Detail

⊞ Instance

⊞ Loop

Figure 4: stimulation file 3.1.4.1



Utilization Estimates

⊟ Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	3	0	26
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	27
Register	-	-	99	-
Total	0	3	99	53
Available	280	220	106400	53200
Utilization (%)	0	1	~0	~0

⊟ Detail

⊞ Instance

⊞ DSP48

⊞ Memory

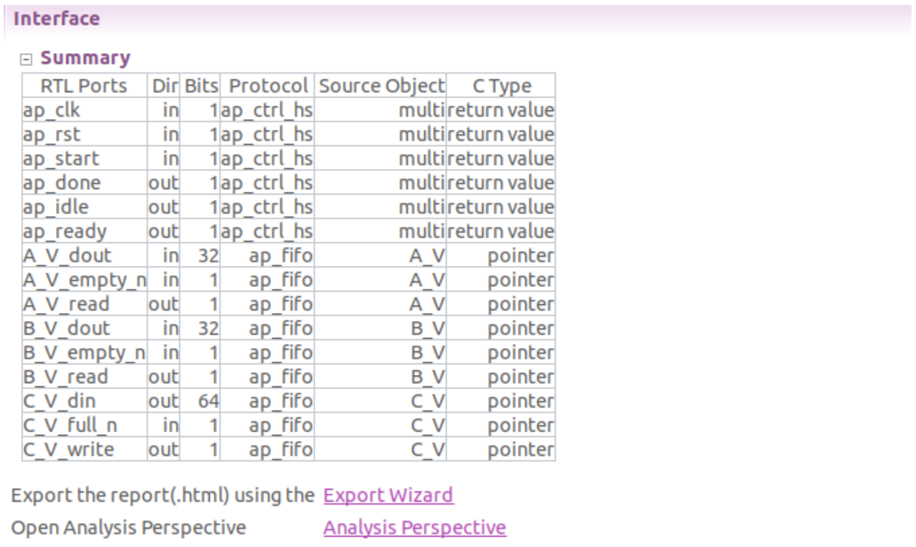
⊞ FIFO

⊞ Expression

⊞ Multiplexer

⊞ Register

Figure 5: synthesis file 3.1.4.2



Interface

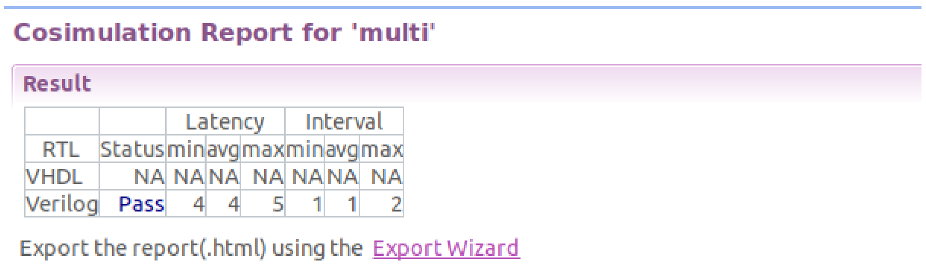
Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	multi	return value
ap_rst	in	1	ap_ctrl_hs	multi	return value
ap_start	in	1	ap_ctrl_hs	multi	return value
ap_done	out	1	ap_ctrl_hs	multi	return value
ap_idle	out	1	ap_ctrl_hs	multi	return value
ap_ready	out	1	ap_ctrl_hs	multi	return value
A_V_dout	in	32	ap_fifo	A_V	pointer
A_V_empty_n	in	1	ap_fifo	A_V	pointer
A_V_read	out	1	ap_fifo	A_V	pointer
B_V_dout	in	32	ap_fifo	B_V	pointer
B_V_empty_n	in	1	ap_fifo	B_V	pointer
B_V_read	out	1	ap_fifo	B_V	pointer
C_V_din	out	64	ap_fifo	C_V	pointer
C_V_full_n	in	1	ap_fifo	C_V	pointer
C_V_write	out	1	ap_fifo	C_V	pointer

Export the report(.html) using the Export Wizard

Open Analysis Perspective Analysis Perspective

Figure 6: synthesis file 3.1.4.3



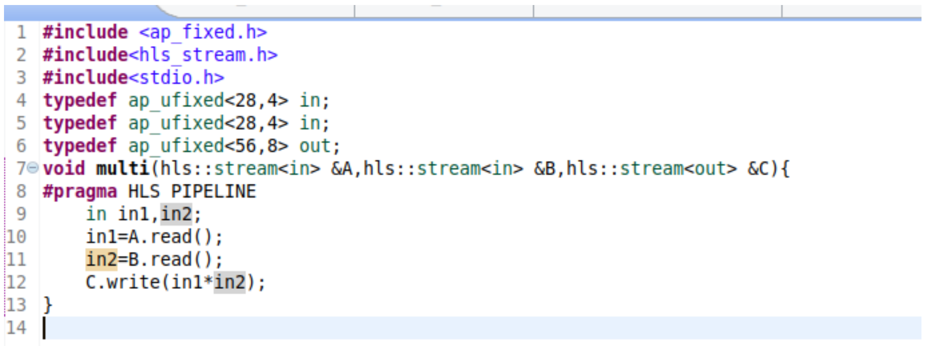
Cosimulation Report for 'multi'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	4	4	5	1	1	2

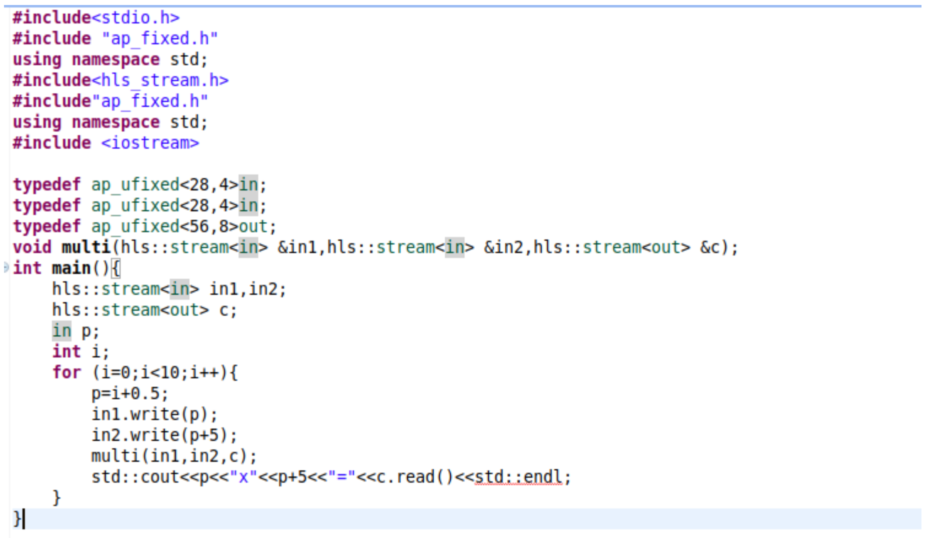
Export the report(.html) using the Export Wizard

Figure 7: co simulation 3.1.5



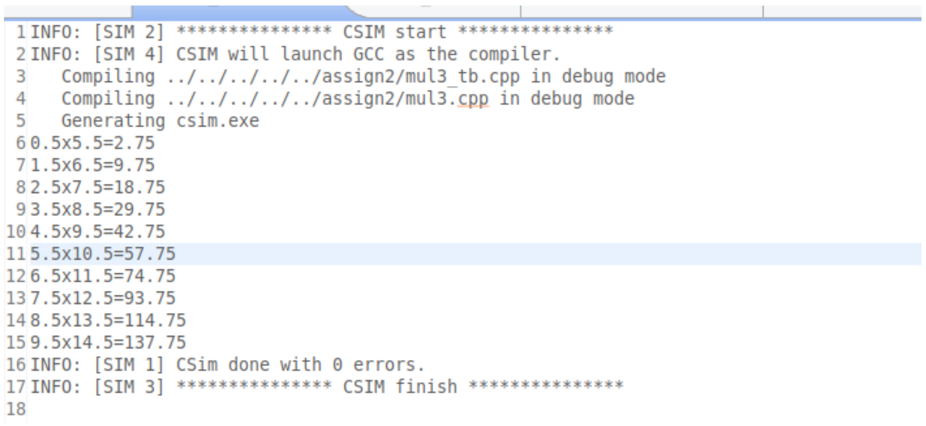
```
#include <ap_fixed.h>
#include<hls_stream.h>
#include<stdio.h>
typedef ap_ufixed<28,4> in;
typedef ap_ufixed<28,4> in;
typedef ap_ufixed<56,8> out;
void multi(hls::stream<in> &A,hls::stream<in> &B,hls::stream<out> &C){
#pragma HLS PIPELINE
    in in1,in2;
    in1=A.read();
    in2=B.read();
    C.write(in1*in2);
}

```

Figure 8: cpp file 3.2.1



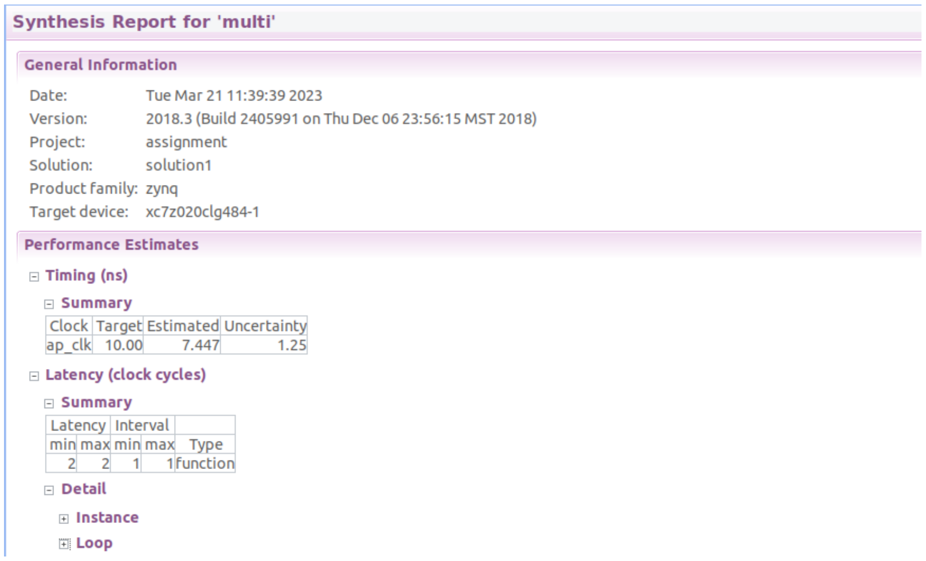
```
#include<stdio.h>
#include "ap_fixed.h"
using namespace std;
#include<hls_stream.h>
#include"ap_fixed.h"
using namespace std;
#include <iostream>

typedef ap_ufixed<28,4>in;
typedef ap_ufixed<28,4>in;
typedef ap_ufixed<56,8>out;
void multi(hls::stream<in> &in1,hls::stream<in> &in2,hls::stream<out> &c);
int main(){
    hls::stream<in> in1,in2;
    hls::stream<out> c;
    in p;
    int i;
    for (i=0;i<10;i++){
        p=i+0.5;
        in1.write(p);
        in2.write(p+5);
        multi(in1,in2,c);
        std::cout<<p<<"x"<<p+5<<"="<<c.read()<<std::endl;
    }
}
```

Figure 9: testbech file 3.2.2



```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../../../assign2/mul3_tb.cpp in debug mode
   Compiling ../../../../../assign2/mul3.cpp in debug mode
   Generating csim.exe
0.5x5.5=2.75
1.5x6.5=9.75
2.5x7.5=18.75
3.5x8.5=29.75
4.5x9.5=42.75
5.5x10.5=57.75
6.5x11.5=74.75
7.5x12.5=93.75
8.5x13.5=114.75
9.5x14.5=137.75
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

Figure 10: csim 3.2.3



Synthesis Report for 'multi'

General Information

Date:	Tue Mar 21 11:39:39 2023
Version:	2018.3 (Build 2405991 on Thu Dec 06 23:56:15 MST 2018)
Project:	assignment
Solution:	solution1
Product family:	zynq
Target device:	xc7z020clg484-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	7.447	1.25

Latency (clock cycles)

Summary

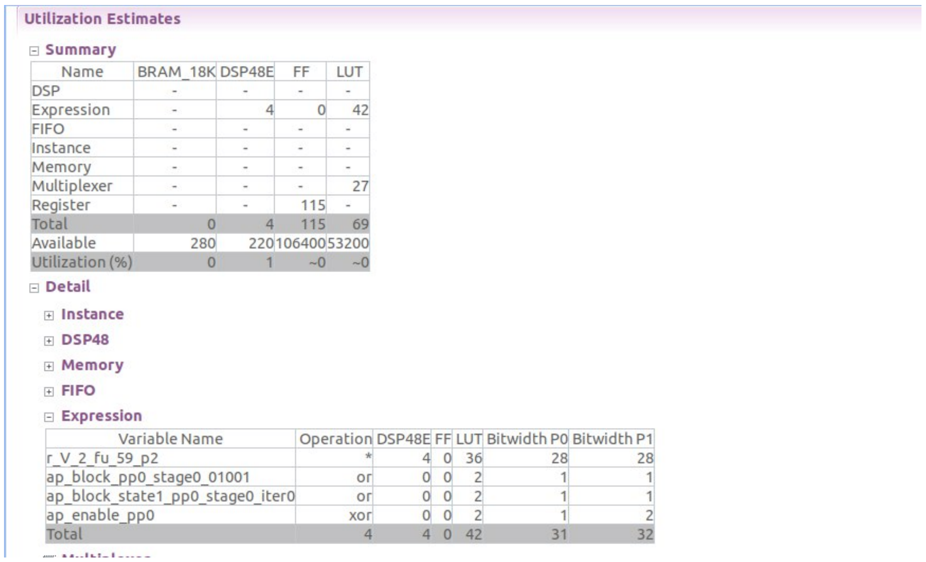
Latency		Interval		
min	max	min	max	Type
2	2	1	1	function

Detail

Instance

Loop

Figure 11: synthesis file 3.2.4.1



Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	4	0	42
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	27
Register	-	-	115	-
Total	0	4	115	69
Available	280	220	106400	53200
Utilization (%)	0	1	~0	~0

Detail

Instance

DSP48

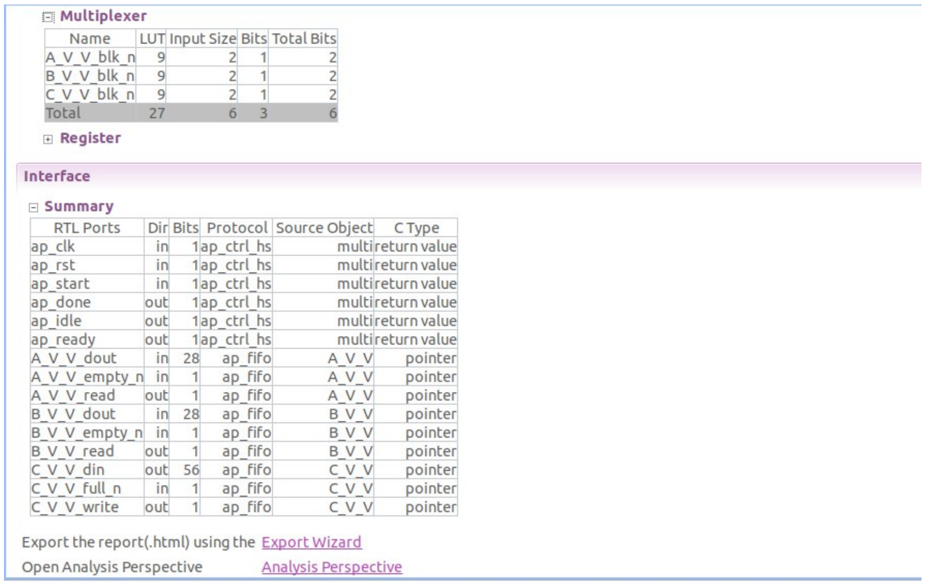
Memory

FIFO

Expression

Variable Name	Operation	DSP48E	FF	LUT	Bitwidth P0	Bitwidth P1
r_V_2_fu_59_p2	*	4	0	36	28	28
ap_block_pp0_stage0_01001	or	0	0	2	1	1
ap_block_state1_pp0_stage0_iter0	or	0	0	2	1	1
ap_enable_pp0	xor	0	0	2	1	2
Total	4	4	0	42	31	32

Figure 12: synthesis file 3.2.4.2



Multiplexer

Name	LUT	Input Size	Bits	Total Bits
A_V_V_blk_n	9	2	1	2
B_V_V_blk_n	9	2	1	2
C_V_V_blk_n	9	2	1	2
Total	27	6	3	6

Register

Interface

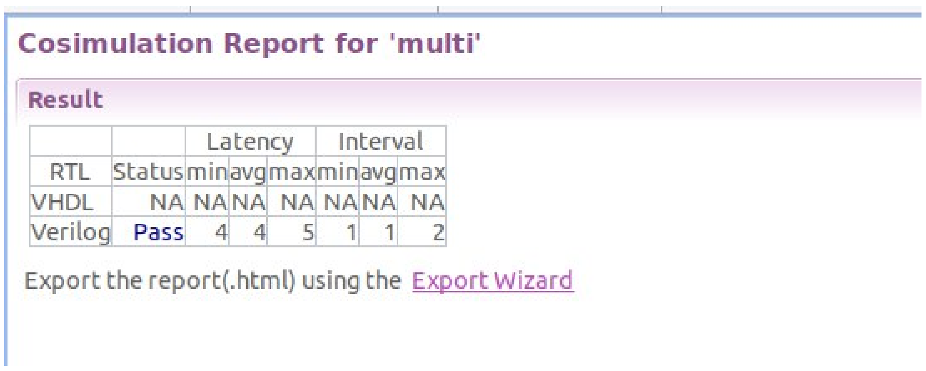
Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	multi	return value
ap_rst	in	1	ap_ctrl_hs	multi	return value
ap_start	in	1	ap_ctrl_hs	multi	return value
ap_done	out	1	ap_ctrl_hs	multi	return value
ap_idle	out	1	ap_ctrl_hs	multi	return value
ap_ready	out	1	ap_ctrl_hs	multi	return value
A_V_V_dout	in	28	ap_fifo	A_V_V	pointer
A_V_V_empty_n	in	1	ap_fifo	A_V_V	pointer
A_V_V_read	out	1	ap_fifo	A_V_V	pointer
B_V_V_dout	in	28	ap_fifo	B_V_V	pointer
B_V_V_empty_n	in	1	ap_fifo	B_V_V	pointer
B_V_V_read	out	1	ap_fifo	B_V_V	pointer
C_V_V_din	out	56	ap_fifo	C_V_V	pointer
C_V_V_full_n	in	1	ap_fifo	C_V_V	pointer
C_V_V_write	out	1	ap_fifo	C_V_V	pointer

Export the report(.html) using the Export Wizard

Open Analysis Perspective Analysis Perspective

Figure 13: synthesis file 3.2.4.3

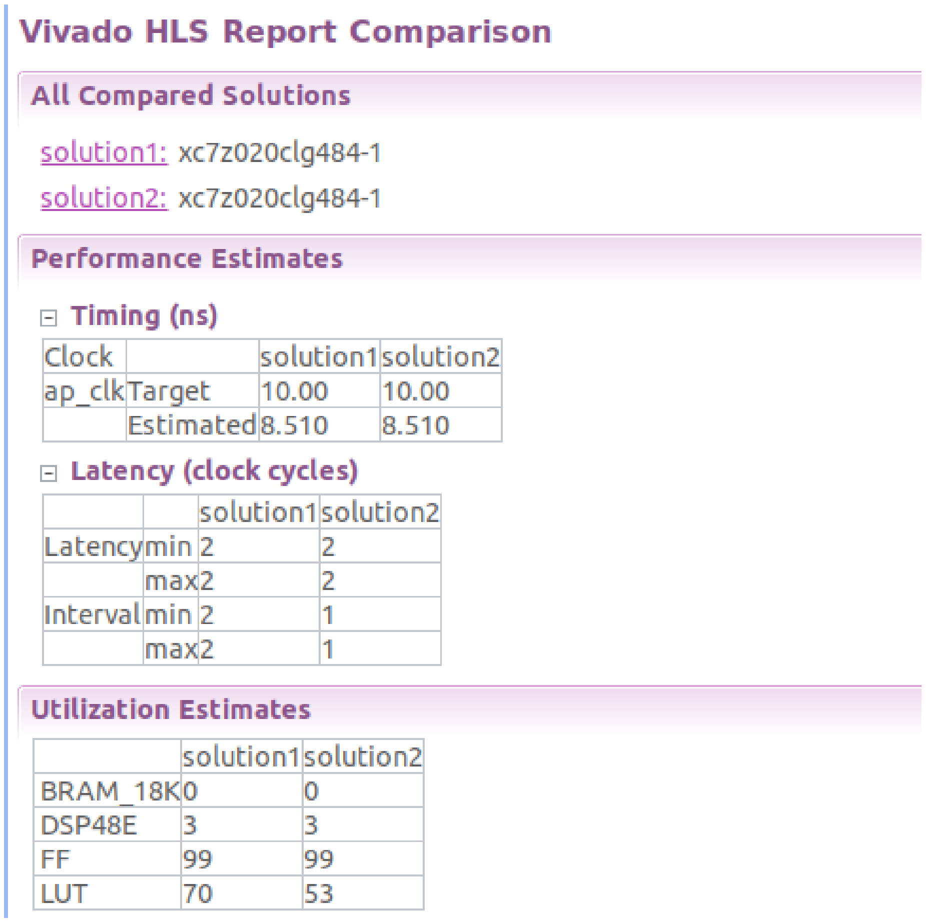

Cosimulation Report for 'multi'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	4	4	5	1	1	2

Export the report(.html) using the Export Wizard

Figure 14: co simulation 3.2.5


Vivado HLS Report Comparison

All Compared Solutions

solution1: xc7z020clg484-1

solution2: xc7z020clg484-1

Performance Estimates

Timing (ns)

Clock		solution1	solution2
ap_clk	Target	10.00	10.00
	Estimated	8.510	8.510

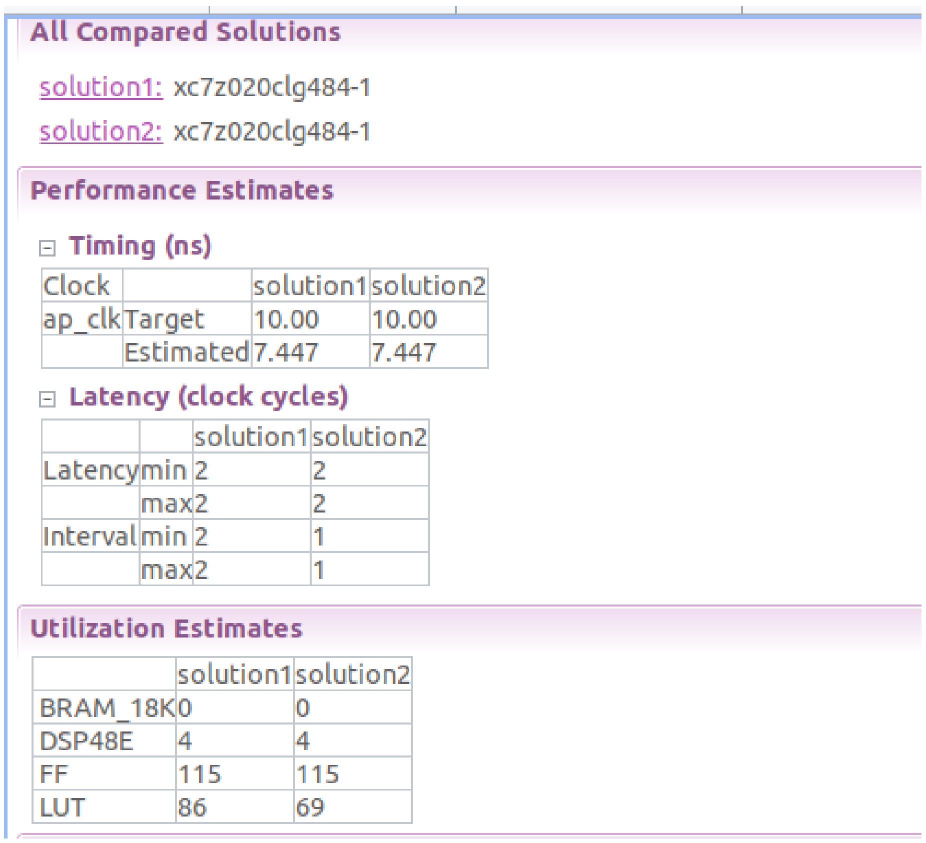
Latency (clock cycles)

		solution1	solution2
Latency	min	2	2
	max	2	2
Interval	min	2	1
	max	2	1

Utilization Estimates

	solution1	solution2
BRAM_18K	0	0
DSP48E	3	3
FF	99	99
LUT	70	53

Figure 15: comparasion results 3.1



All Compared Solutions

solution1: xc7z020clg484-1

solution2: xc7z020clg484-1

Performance Estimates

Timing (ns)

Clock		solution1	solution2
ap_clk	Target	10.00	10.00
	Estimated	7.447	7.447

Latency (clock cycles)

		solution1	solution2
Latency	min	2	2
	max	2	2
Interval	min	2	1
	max	2	1

Utilization Estimates

	solution1	solution2
BRAM_18K	0	0
DSP48E	4	4
FF	115	115
LUT	86	69

Figure 16: comparasion results 3.2