Mapping PCB Library with schematic:

There are the component list is shown that each and every element (component we have tomap with pCB library)

For that select one component then click add.

Then we have to give name or we can give it by simply browsing by Browse option.

- Then circle OK and OK, Then we can able to see

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  - Then it will open one windows there give Valldake changes' option. Then check whether are are green and Tick mark or not
  - -> Then Encute changes option. It there is any error it will show. After that give close.
  - Then in schematic library it you click on any parameters component (Forex: c1) In properties (right-side) it you click show option at footprint click show option at footprint.
    - -> After mapping we need to check
      - · ERC cheeking
      - Netist Verification
      - · Single pin Report
  - > For ERC Chuking right click on project name and varidate PCB project training.
  - is not assigned to schematic etc.
  - For Nettist virification we need to generate the notist for that File -> export -> Nettist schematic then it will show the folder and press save.
  - The win ask for two options to save 1) project

    and we have to relect RINE neterist in weterst format

    then ok!
- -> open that fice using Notepad by risht- Clicking.

- -> for single pin Report right click on project -> Add new to Project > output job file -> Thus again right click on project and save -) After that we have to add Add new Report in Report > Then secut Report single pignets -> [project] -> Then select any forder structure then sive generate content Import Nettist to PCB: -> right click on project -> Add new to project -> PCB -> Give any name for example (training) by risht wilking > After that Design > Import changes from Training : Pr jpcb (projuename) -> Yes' Then their for emos and varidate changes. until it show no Differences Detected "while we go Deri son -> Eneport changes from (project name) is > Then click OK! Agenda: 1) Board whine 3) Board Clearence
- 3) Drisin and Dimensions
- 4) cutable and Slots
- 5) Mounting-Holes and Fiducials
  - 6) Restriction Areas.

- -> Board outine: We can Define Board shape by Importing
- -> That should be provided by mechanical team,
- > Go to File > Import -> DXF/OWG and open DXF file.
- > one separate windows will open. In that we haveto take care of scale (mon, meliench) mon.
- In source cayer vonce select are layer and mechanical and aleck ok!
- > Board clearence: Go to Design > Ruly > Board outline clearence trishterice on it to New role > Under that open Board outline charence.
- > It consists of Ave Track, SMD pad THIPAD, VEQ, Fill toy, Region Ficht as 0.254 (default)
- > After that we have to set the original
- > Origin can be either the left sottom corner of the board or the left bottom mounting hole
- For setting origin edit -> origin -> set and controll the cursor to place ori sin where ever you want.
- -> manting Hole: Mounting hore is a hole, or slot on a PWB, used either to connect to chasis or for mechanical standoff. l'ike screws or Boite can fin in that has and we should be vary carefult while siving charena to that hole.
- > Because it any component is there nearly to mounting have and screw head thay effect the component.

- -> Fiducials: These are alignment targets on an sout board for the vision system in a pack and place equipment.
  - -> Three global fiducial locations for each side of a. board with sout devices are required.
- corners of the PCB offers the most benefit toy alignment
- -> A tiducial should be lacated no closer than 5 mms
- To aid Picks Place machines during component

## -> Cayer stackup?

-		
-	layer-1	1
	Prepres	-
-	Layer-2	
	Core	
	(ayir 3	
	Pripriz	
	Caycol	
	Core	
	1040-5	
	prepris	
1	· layer6	
=		1000

A pcB layer stackup is a arrangement of copper and insulating layer that make up a pcB. Then layer are arranged in a way to get multiple printed circult boards on the same dwice.

at least three conductive layer.