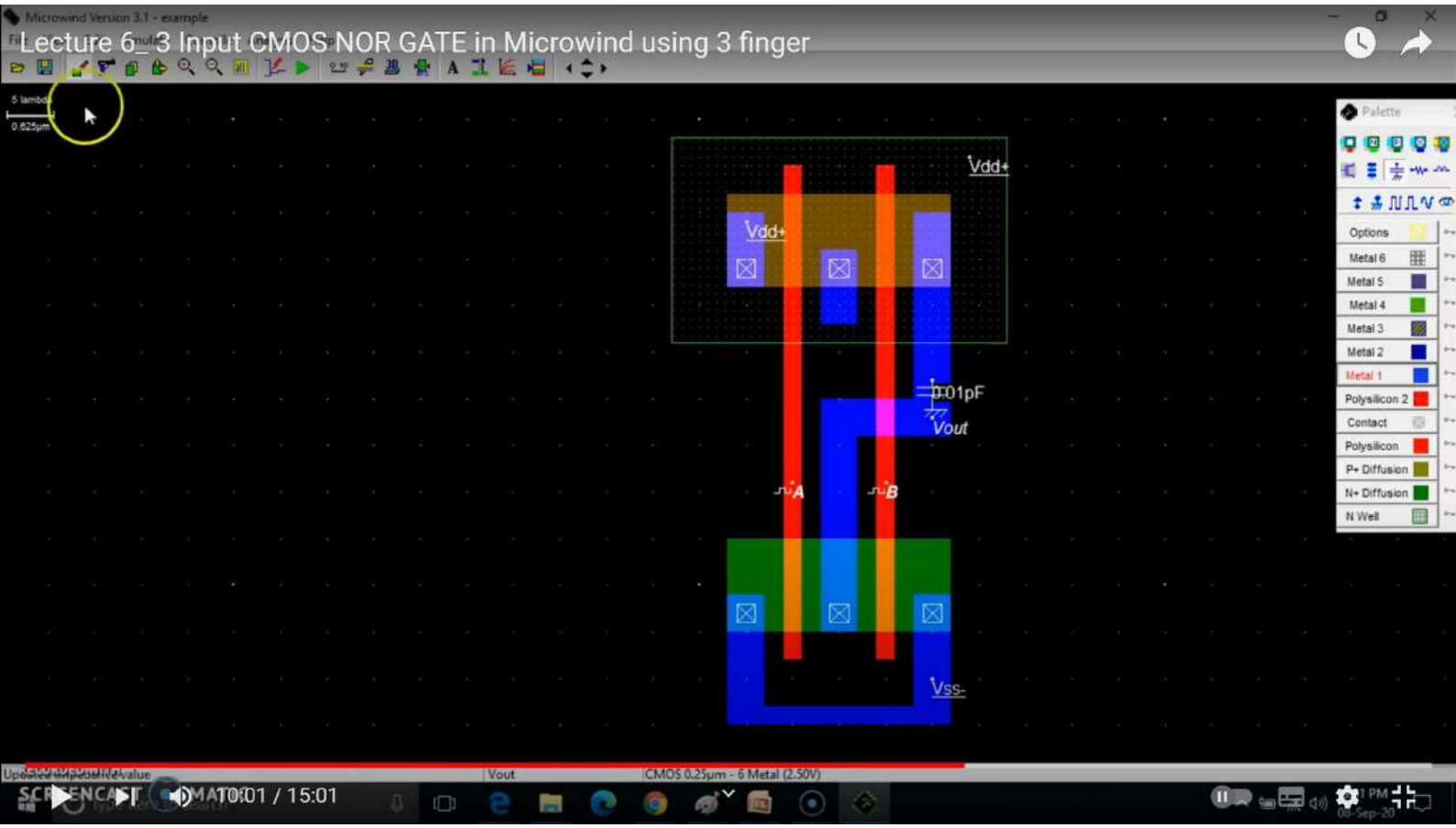
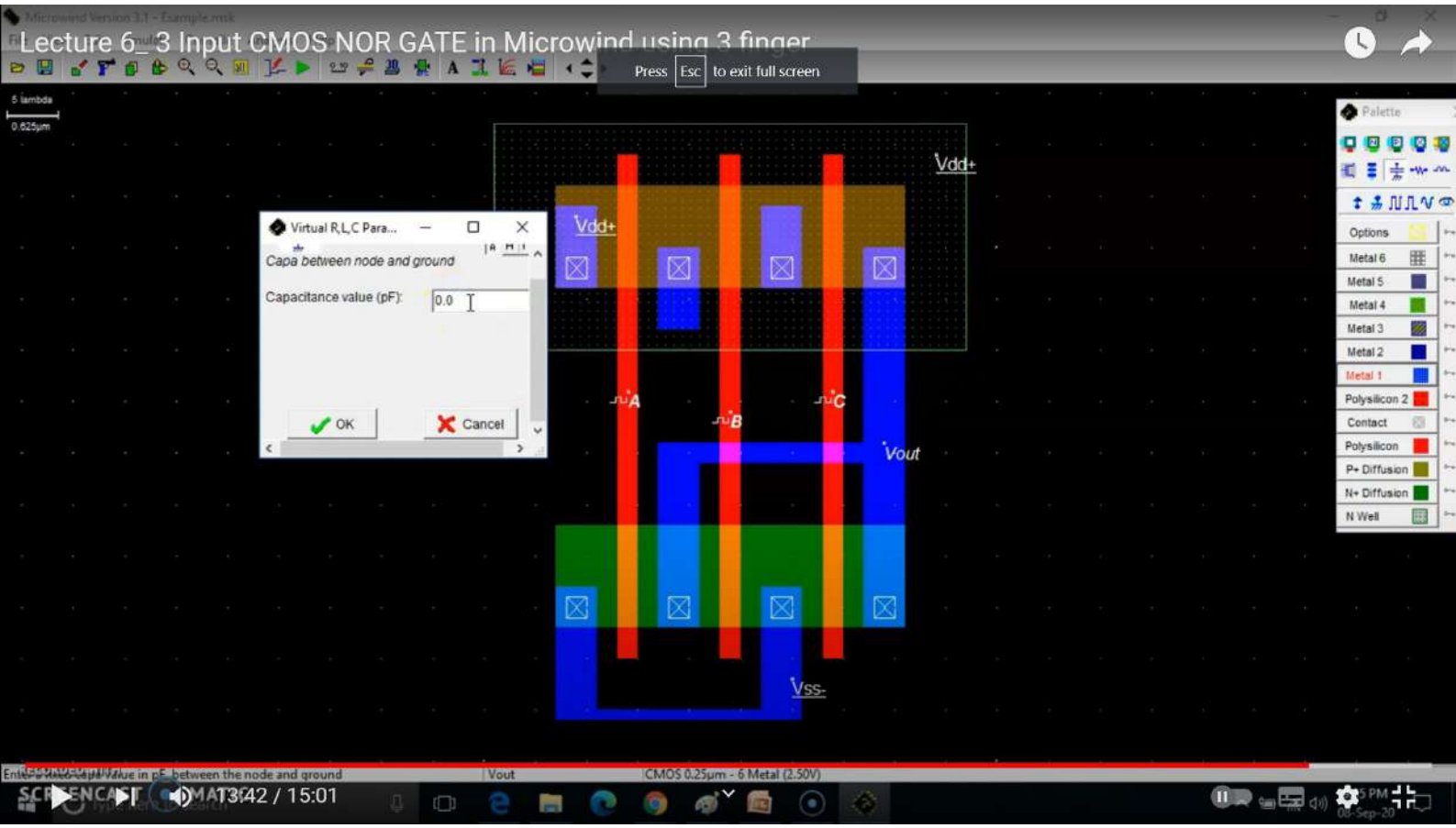
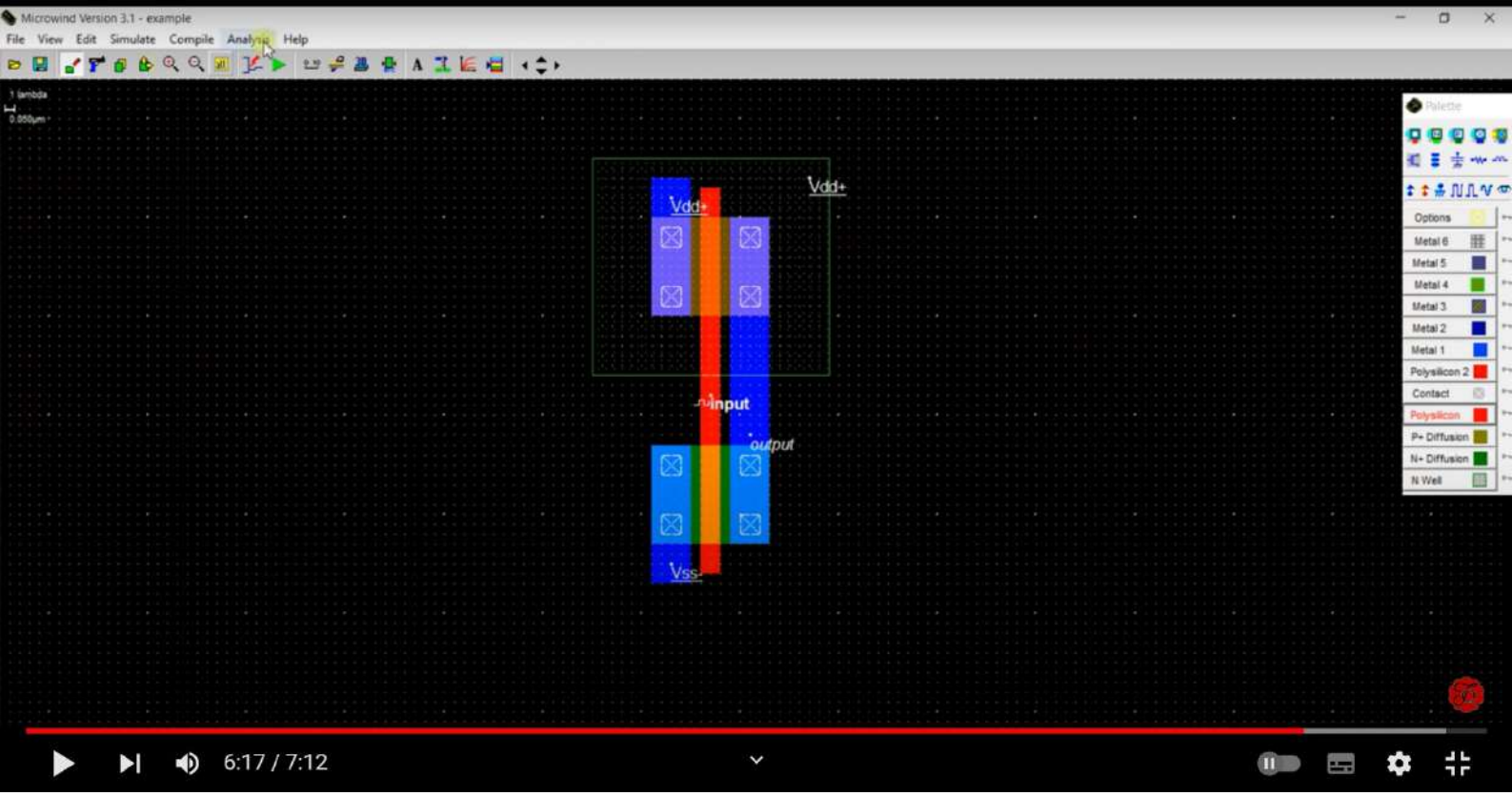
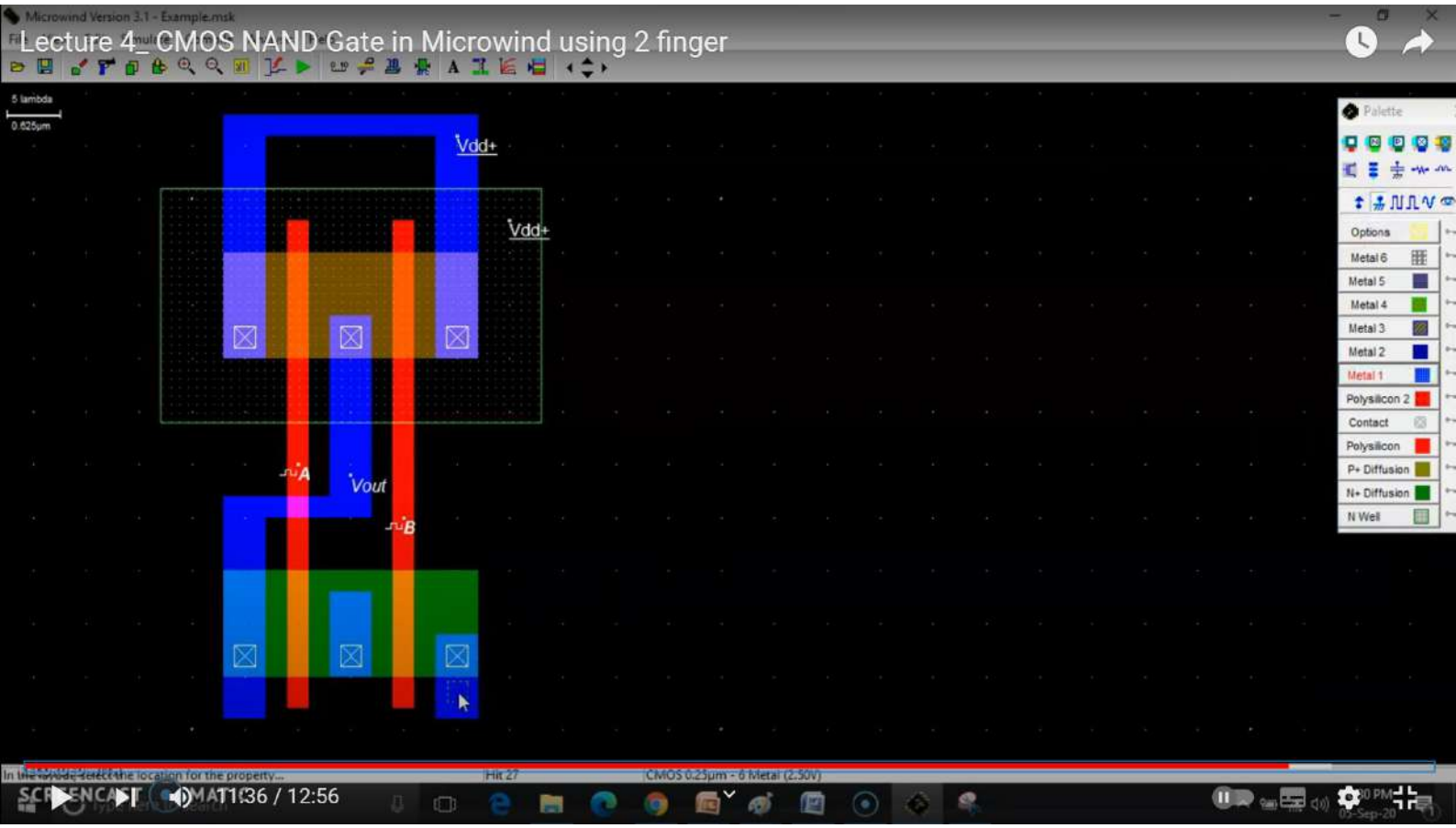

Microwind Version 3.1 - example
Lecture 6_3 Input CMOS NOR GATE in Microwind using 3 finger
Vdd+
Vdd+
0.01pF
Vout
A
B
Vss-
Palette
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
Vout
CMOS 0.25µm - 6 Metal (2.50V)
SCREENCAST-O-MATIC
10:01 / 15:01

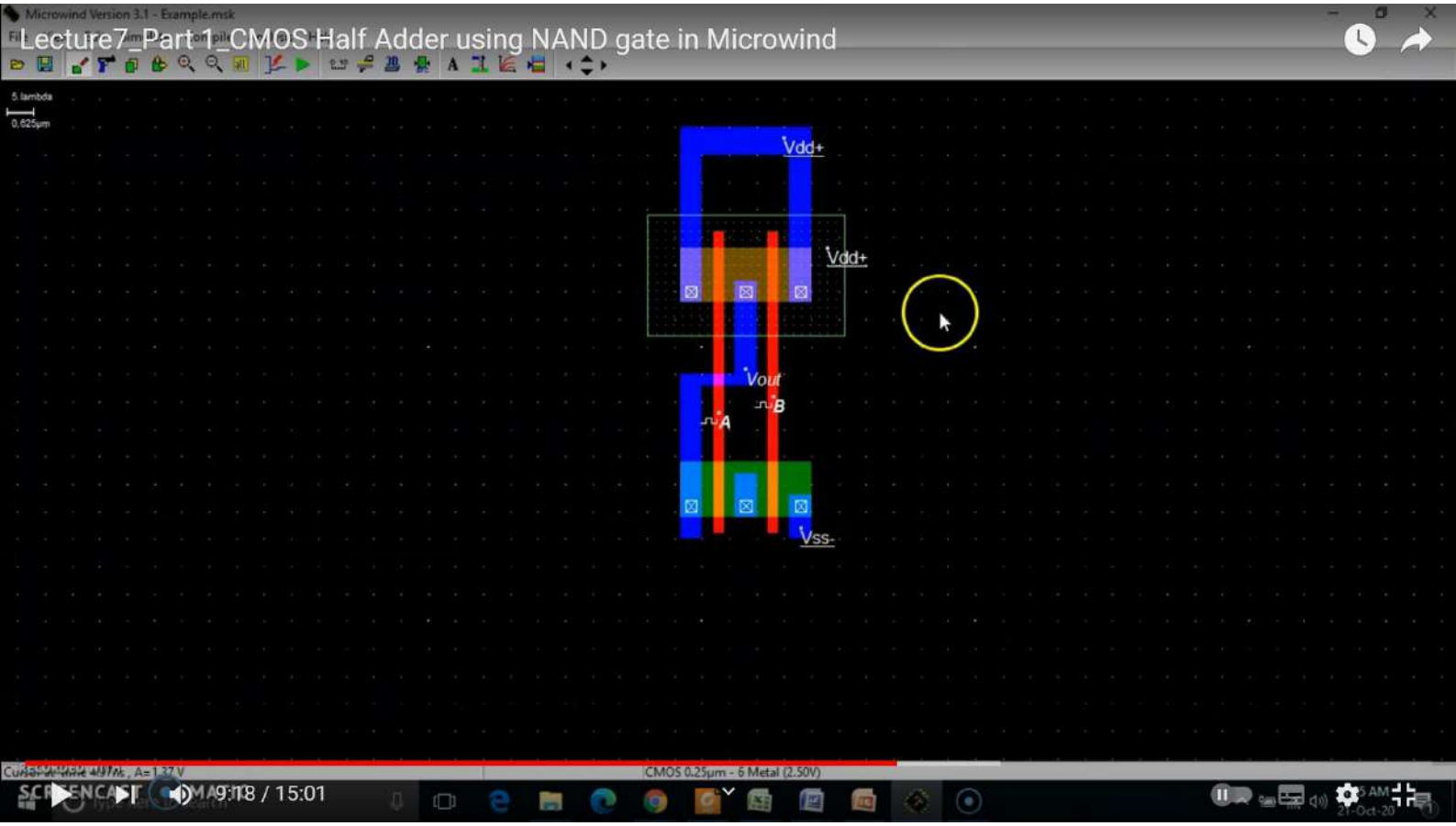

Lecture 6_3 Input CMOS NOR GATE in Microwind using 3 finger
Press Esc to exit full screen
Virtual R,L,C Para...
Capa between node and ground
Capacitance value (pF):
0.0
OK
Cancel
Vdd+
Vdd+
A
B
C
Vout
Vss-
Palette
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
Vout
CMOS 0.25µm - 6 Metal (2.50V)
SCREENCAST MATIC
13:42 / 15:01

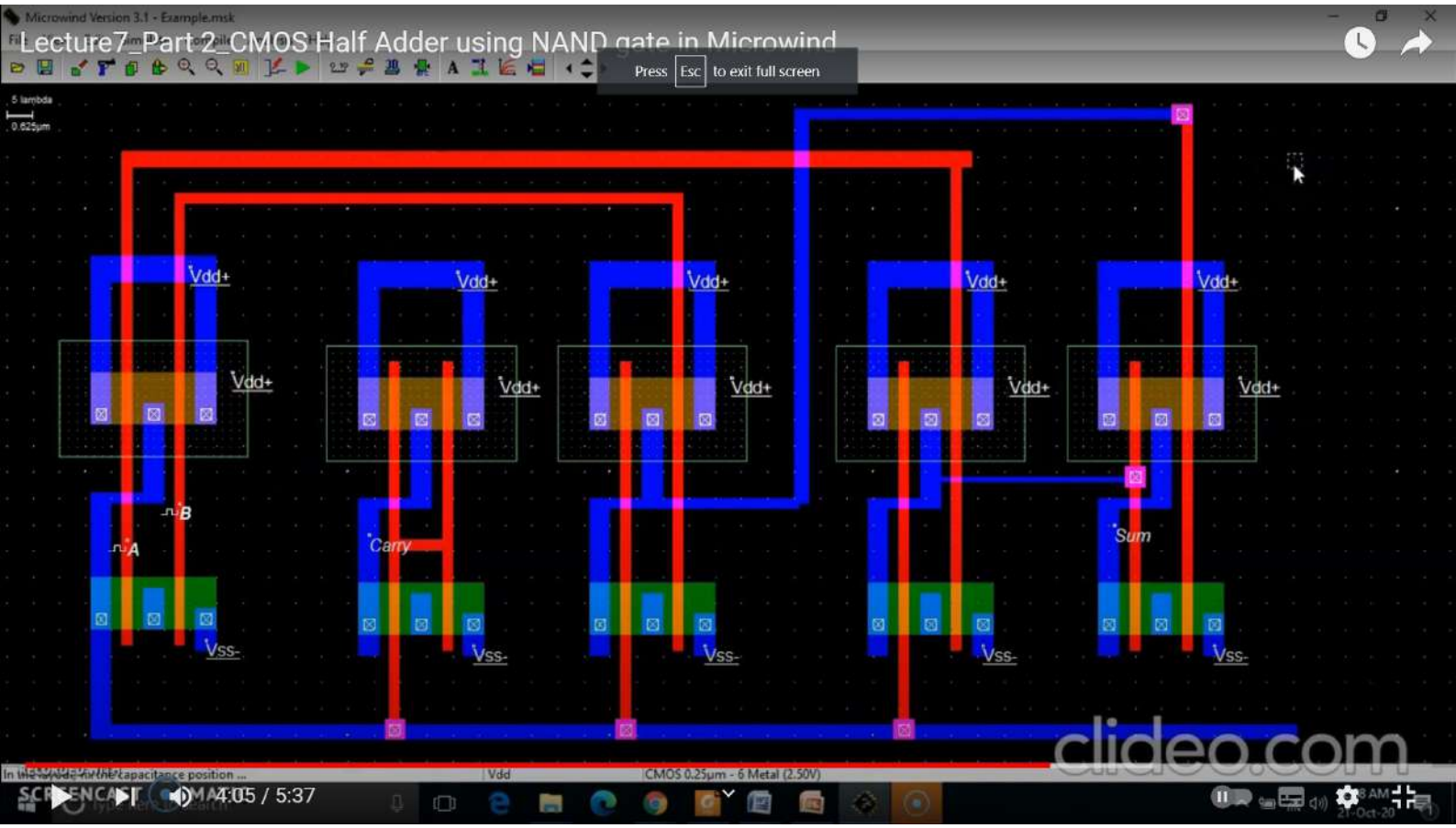
How to make layouts in Microwind software explained with an example of CMOS inverter

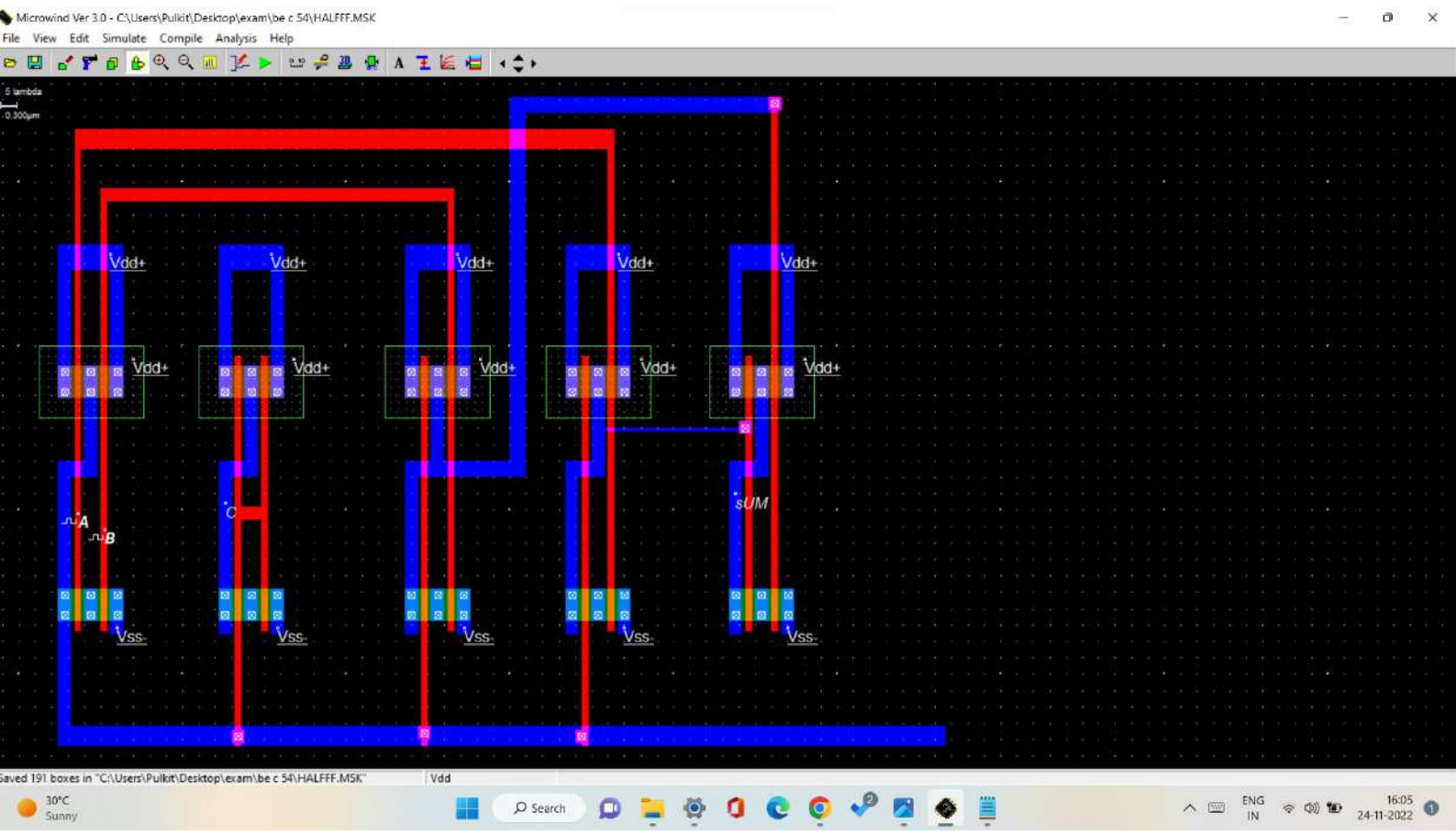


6:17 / 7:12


Microwind Version 3.1 - Example.msk
Lecture 4_ CMOS NAND Gate in Microwind using 2 finger
5 lambda
0.625µm
Vdd+
Vdd+
A
Vout
B
Palette
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
Hit 27
CMOS 0.25µm - 6 Metal (2.50V)
11:36 / 12:56


Lecture7_Part1_CMOS Half Adder using NAND gate in Microwind
Microwind Version 3.1 - Example.msk
5 lambda
0.625µm
Vdd+
Vdd+
Vout
B
A
Vss-
CMOS 0.25µm - 6 Metal (2.50V)
SCREENCAST
9:18 / 15:01


Microwind Version 3.1 - Example.msk
Lecture7_Part2_CMOS Half Adder using NAND gate in Microwind
Press Esc to exit full screen
5 lambda
0.625µm
Vdd+
Vss-
B
A
Carry
Sum
Vdd
CMOS 0.25µm - 6 Metal (2.50V)
clideo.com
SCREENCAST
4:05 / 5:37


Microwind Ver 3.0 - C:\Users\Pulkit\Desktop\exam\be c 54\HALFFF.MSK
File View Edit Simulate Compile Analysis Help
5 lambda
0.300µm
Vdd+
Vss-
A
B
C
SUM
Saved 191 boxes in "C:\Users\Pulkit\Desktop\exam\be c 54\HALFFF.MSK"
Vdd