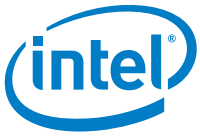


### 6.3.4.2 Data and Address Words — Offset 0x01, 0x02, 0x03...

Each word in the analog configuration section has the same structure: bits 15:8 are the register address and bits 7:0 are the register's data. The analog registers are eight bits wide with an 8-bit address width. After reading the EEPROM word, the register specified in bits 15:8 is loaded with the data from bits 7:0.

## 6.3.5 PCIe General Configuration Module

This section is loaded after a PCIe Reset. It contains general configuration for the PCIe interface (not function specific) and is pointed to by word 0x06 in the EEPROM (full-byte address; must be word aligned).

| Offset | Description |
|---|---|
| 0x00 | Section Length Section 6.3.5.1. |
| 0x01 | PCIe Init Configuration 1 Section 6.3.5.2 |
| 0x02 | PCIe Init Configuration 2 Section 6.3.5.3 |
| 0x03 | PCIe Init Configuration 3 Section 6.3.5.4 |
| 0x04 | PCIe Control 1 Section 6.3.5.5 |
| 0x05 | PCIe Control 2 Section 6.3.5.6 |
| 0x06 | PCIe LAN Power Consumption Section 6.3.5.7 |
| 0x07 | PCIe Control 3 Section 6.3.5.8 |
| 0x08 | PCIe Sub-System ID Section 6.3.5.9 |
| 0x09 | PCIe Sub-System Vendor ID Section 6.3.5.10 |
| 0x0A | PCIe Dummy Device ID Section 6.3.5.11 |
| 0x0B | PCIe Device Revision ID Section 6.3.5.12 |
| 0x0C | IOV Control Word 1 Section 6.3.5.13 |
| 0x0D | IOV Control Word 2 Section 6.3.5.14 |
| 0x0E | Reserved |
| 0x0F | Reserved |
| 0x10 | Reserved |
| 0x11 | Serial Number Ethernet MAC Address Section 6.3.5.15 |

| Offset | Description |
|---|---|
| 0x12 | Serial Number Ethernet MAC Address Section 6.3.5.16 |
| 0x13 | Serial Number Ethernet MAC Address Section 6.3.5.17 |
| 0x14 | PCIe L1 Exit latencies Section 6.3.5.18 |
| 0x15 | Spare Section 6.3.5.19 |

### 6.3.5.1 Section Length — Offset 0x00

The section length word contains the length of the section in words. Note that section length does not include a count for the section length word.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | Section Length | | Section Length in words. | |

### 6.3.5.2 PCIe Init Configuration 1 — Offset 0x01

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15 | Reserved | 0b | Reserved. | |
| 14:12 | L0s acceptable latency | 011b | Loaded to the *Endpoint L0s Acceptable Latency* field in the Device Capabilities register as part of the PCIe Configuration registers at power up. | |
| 11:9 | L0s G2 Sep exit latency | 111b | L0s exit latency G2S. Loaded to *L0s Exit Latency* field in the Link Capabilities register as part of the PCIe Configuration registers in PCIe V2.0 (5GT/s) system with a separate clock setting. | |
| 8:6 | L0s G2 Com exit latency | 100b | L0s exit latency G2C. Loaded to *L0s Exit Latency* field in the Link Capabilities register as part of the PCIe Configuration registers in PCIe V2.0 (5GT/s) system with a common clock setting. | |
| 5:3 | L0s G1 Sep exit latency | 111b | L0s exit latency G1S. Loaded to *L0s Exit Latency* field in the Link Capabilities register as part of the PCIe Configuration registers in PCIe v2.0 (2.5GT/s) system with a separate clock setting. | |
| 2:0 | L0s G1 Com exit latency | 011b | L0s exit latency G1C. Loaded to L0s Exit Latency field in the Link Capabilities register as part of the PCIe Configuration registers in PCIe v2.0 (2.5GT/s) system with a common clock setting. | |

### 6.3.5.3 PCIe Init Configuration 2 — Offset 0x02

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:13 | Reserved | 0x0 | Reserved. | |
| 12 | FLR delay disable | 0b | Disable the FLR value in the *FLR Delay* field in this word. | |
| 11:8 | FLR delay | 0x1 | FLR response time in cycles defines the delay from FLR assertion to its affect. | |
| 7:6 | PCI-E capability version | 10b | PCIe Capability Version.<br>This field must be set to 10b to use extended configuration capability (used for a timeout mechanism). This field is mapped to GCR.PCIe_Capability_Version. | |
| 5 | ECRC generation enable | 1b | Loaded into the *ECRC Generation Capable* bit of the PCIe Configuration registers.<br>At 1b the device is capable of generating ECRC. | |
| 4 | ECRC check enable | 1b | Loaded into the *ECRC Check Capable* bit of the PCIe Configuration registers.<br>At 1b the device is capable of checking ECRC. | |
| 3 | FLR capability enable | 1b | *FLR Capability Enable* bit is loaded to the PCIe Configuration registers via the Device Capabilities register. | |
| 2 | Cache line size | 0b | Cache Line Size<br>0b = 64 bytes.<br>1b = 128 bytes. | |
| 1:0 | Max payload size | 10b | Maximum payload size support for TLPs. Loaded to the PCIe Configuration registers via the Device Capabilities register. | |

### 6.3.5.4 PCIe Init Configuration 3 — Offset 0x03

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:4 | Reserved | 0x0 | Reserved. | |
| 3 | PCIe Down Reset Disable | 0b | Disables a core and reset when the PCIe link goes down. | |
| 2:1 | Act_Stat_PM_Sup | 11b | *Active State Link PM Support* is loaded to the PCIe Configuration registers via the *Link Capabilities* field. | |
| 0 | Slot_Clock_Cfg | 1b | Slot Clock Configuration.<br>When set, the 82599 uses the PCIe reference clock supplied on the connector (for add-in solutions). This bit is loaded to the "PCIe configuration registers" -> "Link Status". | |

### 6.3.5.5 PCIe Control 1 —Offset 0x04

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:5 | Reserved | 0x0 | Reserved. | |
| 4 | DIS Clock Gating in DISABLE | 1b | Disable clock gating when LTSSM is in a disable state. | |
| 3 | DIS Clock Gating in L2 | 1b | Disable clock gating when LTSSM is at L2 state. | |
| 2 | DIS Clock Gating in L1 | 1b | Disable clock gating when LTSSM is at L1 state. | |
| 1 | DIS Clock Gating in G2 | 1b | Disable clock gating in PCIe V2.0 (5GT/s). | |
| 0 | DIS Clock Gating in G1 | 1b | Disable clock gating in PCIe v2.0 (2.5GT/s). | |

### 6.3.5.6 PCIe Control 2 — Offset 0x05

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15 | Completion Timeout Resend | 0b | When set, enables a response to a request once the completion timeout expired.<br>This bit is mapped to GCR.Completion_Timeout_Resend.<br>0b = Do not resend request on completion timeout.<br>1b = Resend request on completion timeout. | |
| 14:4 | Reserved | 0x0 | Reserved. | |
| 3 | LAN Function Select | 0b | When the LAN Function Select field = 0b, LAN 0 is routed to PCI function 0 and LAN 1 is routed to PCI function 1.<br>If the LAN Function Select field = 1b, LAN 0 is routed to PCI function 1 and LAN 1 is routed to PCI function 0.<br>This bit is mapped to FACTPS[30]. | |
| 2 | Dummy Function Enable | 0b | Controls the behavior of function 0 when disabled.<br>0b = Legacy Mode.<br>1b = Dummy Function Mode.<br>See Section 4.4. | |
| 1 | LAN PCI Disable | 0b | LAN PCI Disable. When set to 1b, one LAN port is disabled.<br>The function that is disabled is determined by the *LAN Disable Select* bit. If the disabled function is function 0, it acts as a dummy function or the other LAN function depending on the *Dummy Function Enable* setting. | |
| 0 | LAN Disable Select | 0b | LAN Disable Select<br>0b = LAN 0 is disabled.<br>1b = LAN 1 is disabled. | |

### 6.3.5.7 PCIe LAN Power Consumption — Offset 0x06

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | LAN D0 Power | | The value in this field is reflected in the PCI Power Management Data register of the LAN functions for D0 power consumption and dissipation (Data_Select = 0 or 4).<br>Power is defined in 100 mW units. The power includes also the external logic required for the LAN function. | |
| 7:5 | Function 0 Common Power | | The value in this field is reflected in the PCI Power Management Data register of function 0 when the Data_Select field is set to 8 (common function).<br>The MSBs in the Data register that reflects the power values are padded with zeros. When one port is used this field should be set to 0. | |
| 4:0 | LAN D3 Power | | The value in this field is reflected in the PCI Power Management Data register of the LAN functions for D3 power consumption and dissipation (Data_Select = 3 or 7).<br>Power is defined in 100 mW units. The power includes also the external logic required for the LAN function. The MSBs in the Data register that reflects the power values are padded with zeros. | |

### 6.3.5.8 PCIe Control 3 — Offset 0x07

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15 | Reserved | 0b | Reserved. | |
| 14 | PREFBAR | 0b | Prefetchable bit indication in the memory BARs:<br>0b = BARs are marked as non-prefetchable<br>1b = BARs are marked as prefetchable | |
| 13 | CSR_Size | 0b | The CSR_Size and FLASH_Size fields define the usable Flash size and CSR mapping window size.<br>*Note:* When the CSR_Size and Flash_Size fields in EEPROM are set to 0, Flash Bar in the PCI configuration space is disabled. | |
| 12 | IO_Sup | 1b | I/O Support (affects I/O BAR request).<br>When set to 1b, I/O is supported. When cleared the *I/O Access Enable* bit in the Command register (as part of the Mandatory PCI Configuration) is RO at 0b. | |
| 11 | Reserved | 0b | Reserved. | |
| 10:8 | Flash_Size | 010b | Indicates a Flash size of 64 KB * 2 ^Flash_Size.<br>The Flash_Size impacts the requested memory space for the Flash and expansion ROM BARs in PCIe configuration space.<br>See Table 6-7, Usable Flash_Size below.<br>*Note:* When the CSR_Size and Flash_Size fields in EEPROM are set to 0, Flash Bar in the PCI configuration space is disabled. | |
| 7:2 | Reserved | 0x0 | Reserved | |
| 1 | Load Subsystem IDs | 1b | When set to 1b, indicates that the function is to load its PCIe sub-system ID and sub-system vendor ID from the EEPROM (offset 0x8 and 0x9 in this section). | |

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 0 | Load Device ID | 1b | When set to 1b, indicates that the function is to load its PCI device ID from the EEPROM (offset 0x0A in this section for dummy device ID and offset 2 in PCIe configuration space 0/1 section for active functions). | |

**Table 6-7 Usable Flash_Size**

| Flash_Size | CSR_Size | Resulted CSR + Flash BAR Size | Installed Flash Device | Usable Flash Space |
|---|---|---|---|---|
| 000b | 0 | 128 KByte | No Flash | 0 |
| 000b | 1 | N/A | N/A | Reserved |
| 001b | 0 | 256 KByte | 128 KByte | 128 KByte |
| 001b | 1 | N/A | N/A | Reserved |
| 010b | 0 | 256 KByte | 256 KByte | 256 KByte minus 128 KByte |
| 010b | 1 | 512 KByte | 256 KByte | 256 KByte |
| 011b | 0 | 512 KByte | 512 KByte | 512 KByte minus 128 KByte |
| 011b | 1 | 1 MByte | 512 KByte | 512 KByte |
| 100b | 0 | 1 MByte | 1 MByte | 1 MByte minus 128 KByte |
| 100b | 1 | 2 MByte | 1 MByte | 1 MByte |
| 101b | 0 | 2 MByte | 2 MByte | 2 MByte minus 128 KByte |
| 101b | 1 | 4 MByte | 2 MByte | 2 MByte |
| 110b | 0 | 4 MByte | 4 MByte | 4 MByte minus 128 KByte |
| 110b | 1 | 8 MByte | 4 MByte | 4 MByte |
| 111b | 0 | 8 MByte | 8 MByte | 8 MByte minus 128 KByte |
| 111b | 1 | 16 MByte | 8 MByte | 8 MByte |

### 6.3.5.9 PCIe Sub-System ID — Offset 0x08

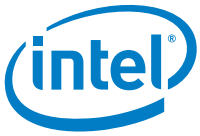
If the load sub-system IDs in offset 0x7 of this section is set, this word is read in to initialize the sub-system ID. The default value is 0x0.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | Sub System ID | 0x0 | | |

### 6.3.5.10 PCIe Sub-System Vendor ID — Offset 0x09

If the load sub-system IDs in offset 0x7 of this section is set, this word is read in to initialize the sub-system vendor ID. The default value is 0x8086.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | Sub System Vendor | 0x8086 | | |



### 6.3.5.11 PCIe Dummy Device ID — Offset 0x0A

If the *Load Device ID* in offset 0x7 of this section is set, this word is read in to initialize the device ID of the dummy device in this function (if enabled). The default value is 0x10A6.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | Sub Device_ID | 0x10A6 | | |

### 6.3.5.12 PCIe Device Revision ID —Offset 0x0B

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | Reserved | 0x0 | Set to 0x0 | |
| 7:0 | DEVREVID | 0x1 | Device Rev ID.<br>The actual device revision ID is the EEPROM value XORed with the hardware value (0x0 for the 82599 A-0 and 0x1 for the 82599 B-0). | |

### 6.3.5.13 IOV Control Word 1 — Offset 0x0C

This word controls the behavior of IOV functionality.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:11 | Reserved | 0x0 | Reserved. | |
| 10:5 | Max VFs | 0x3F | Defines the value of MaxVFs exposed in the IOV structure. Valid values are 0-63. The value exposed, is the value of this field + 1.<br>*Note:* The queue pair of one VF should be assigned to the PF. Therefore, the maximum usable number of VFs is 63. | |
| 4:3 | MSI-X table | 0x2 | Defines the size of the MSI-X table (number of requested MSI-X vectors) — valid values are 0-2. | |
| 2 | 64-Bit Advertisement | 1b | 0b = VF BARs advertise 32 bit size.<br>1b = VF BARs advertise 64 bit size. | |
| 1 | Prefetchable | 0b | 0b = IOV memory BARS (0 and 3) are declared as non-prefetchable.<br>1b = IOV memory BARS (0 and 3) are declared as prefetchable. | |
| 0 | IOV Enabled | 1b | 0b = IOV and ARI capability structures are not exposed as part of the capabilities link list.<br>1b = IOV and ARI capability structures are exposed as part of the capabilities link list. | |

### 6.3.5.14 IOV Control Word 2 — Offset 0x0D

This word defines the device ID for virtual functions.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | VDev ID | 0x10ED | Virtual function device ID. | |

### 6.3.5.15 Serial Number Ethernet MAC Address — Offset 0x11

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | Serial Number Ethernet MAC Address 0, Byte 1 | | Part of the Ethernet MAC address used to generate the PCIe serial number.<br>See Section 9.4.2. | |
| 7:0 | Serial Number Ethernet MAC Address 0, Byte 0 | | Part of the Ethernet MAC address used to generate the PCIe serial number.<br>See Section 9.4.2. | |

### 6.3.5.16 Serial Number Ethernet MAC Address — Offset 0x12

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | Serial Number Ethernet MAC Address 0, Byte 3 | | Part of the Ethernet MAC address used to generate the PCIe serial number.<br>See Section 9.4.2. | |
| 7:0 | Serial Number Ethernet MAC Address 0, Byte 2 | | Part of the Ethernet MAC address used to generate the PCIe serial number.<br>See Section 9.4.2. | |

### 6.3.5.17 Serial Number Ethernet MAC Address — Offset 0x13

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | Serial Number Ethernet MAC Address 0, Byte 5 | | Part of the Ethernet MAC address used to generate the PCIe serial number.<br>See Section 9.4.2 | |
| 7:0 | Serial Number Ethernet MAC Address 0, Byte 4 | | Part of the Ethernet MAC address used to generate the PCIe serial number.<br>See Section 9.4.2. | |

### 6.3.5.18 PCIe L1 Exit latencies — Offset 0x14

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15 | Reserved | 0b | Reserved. | |
| 14:12 | L1_Act_Acc_Latency | 110b | Loaded to the *Endpoint L1 Acceptable Latency* field in the Device Capabilities register as part of the PCIe Configuration registers at power up. | |
| 11:9 | L1 G2 Sep exit latency | 101b | L1 exit latency G2S. Loaded to the Link Capabilities register via the *L1 Exit Latency* field in PCIe V2.0 (5GT/s) systems that have a separate clock setting. | |
| 8:6 | L1 G2 Com exit latency | 011b | L1 exit latency G2C. Loaded to the Link Capabilities register via the *L1 Exit Latency* field in PCIe V2.0 (5GT/s) systems that have a common clock setting. | |
| 5:3 | L1 G1 Sep exit latency | 100b | L1 exit latency G1S. Loaded to the Link Capabilities register via the *L1 Exit Latency* field in PCIe v2.0 (2.5GT/s) systems that have a separate clock setting. | |
| 2:0 | L1 G1 Com exit latency | 010b | L1 exit latency G1C. Loaded to the *L*ink Capabilities register via the *L1 Exit Latency* field in PCIe v2.0 (2.5GT/s) systems that have a common clock setting. | |

### 6.3.5.19 Reserved — Offset 0x15

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:2 | Reserved | 0x1 | Reserved. | |
| 1 | MSIX Memory | 1b | MSIX memory ECC enable. | |
| 0 | CDQ Memory | 1b | CDQ memory ECC enable. | |

## 6.3.6 PCIe Configuration Space 0/1 Modules

Word 0x7 points to the PCIe configuration space defaults of function 0 while word 0x8 points to function 1 defaults. Both sections are loaded after PCIe reset and D3 to D0 transition of the specific function. The structures of both functions are identical as listed in the following table.

| Offset | Description |
|---|---|
| 0x00 | Section LengthSection 6.3.6.1. |
| 0x1 | Control WordSection 6.3.6.2 |
| 0x2 | Device IDSection 6.3.6.3 |
| 0x3 | CDQM Memory Base 0/1 LowSection 6.3.6.4 |
| 0x4 | CDQM Memory Base 0/1 HighSection 6.3.6.5 |
| 0x5 | ReservedSection 6.3.6.6 |

### 6.3.6.1 Section Length — Offset 0x00

The section length word contains the length of the section in words. Note that section length does not include a count for the section length word.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | Section Length | 0x0 | Section length in words. | |

### 6.3.6.2 Control Word — Offset 0x01

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:14 | Reserved | 00b | Reserved. | |
| 13:12 | Interrupt Pin | 0b for LAN0<br>1b for LAN1 | Controls the value advertised in the *Interrupt Pin* field of the PCI configuration header for this device/function.<br>Values of 00b, 01b, 10b and 11b correspond to INTA#, INTB#, INTC# and INTD# respectively. When one port is used this field must be set to 00b (using INTA#) to comply with PCI spec requirements. | |
| 11 | Storage Class | 0b | When set, the class code of this port is set to 0x010000 (SCSI). When cleared, the class code of this port is set to 0x020000 (LAN). | |
| 10 | MSI Mask | 1b | MSI per-vector masking setting.<br>This bit is loaded to the masking bit (bit 8) in the Message Control of the MSI Configuration Capability structure. | |
| 9 | Reserved | 1b | Reserved. | |

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 8 | LAN Boot Disable | 1b | A value of 1b disables the expansion ROM BAR in the PCI configuration space. | |
| 7 | Reserved | 0b | Reserved. | |
| 6:0 | MSI_X_N | 0x3F | This field specifies the number of entries in the MSI-X tables for this function.<br>MSI_X_N is equal to the number of entries minus one. For example, a return value of 0x7 means eight vectors are available. This field is loaded into the PCIe MSI-X capabilities structure. The MSI_X_N must not exceed 0x3F (64 MSI-X vectors). | |

#### 6.3.6.3 Device ID — Offset 0x02 Device ID

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | Device_ID | 0x10D8 | If the *Load Device ID* in offset 0x7 of the PCIe General configuration section is set, this word is loaded to the device ID of the LAN function. | |

#### 6.3.6.4 CDQM Memory Base 0/1 Low — Offset 0x03 [Reserved]

#### 6.3.6.5 CDQM Memory Base 0/1 High — Offset 0x04 [Reserved]

#### 6.3.6.6 EEPROM PCIe Configuration Space 0/1 - Offset 0x05 [Reserved]

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | Reserved | 0x0 | Reserved. | |

## 6.3.7 LAN Core 0/1 Modules

Word 0x9 points to the core configuration defaults of LAN port 0 while word 0xA points to LAN port 1 defaults. The section of each function is loaded at the de-assertion of its core master reset: PCIe reset, D3 to D0 transition, software reset and link reset. The structures of both functions are identical as listed in the following table.

| Offset | High Byte[15:8] | Low Byte[7:0] | Section |
|---|---|---|---|
| 0x0 | Section Length - Section 6.3.7.1. | | |
| 0x1 | Ethernet MAC Address Byte 2 | Ethernet MAC Address Byte 1 | Section 6.3.7.2.1 |
| 0x2 | Ethernet MAC Address Byte 4 | Ethernet MAC Address Byte 3 | Section 6.3.7.2.2 |
| 0x3 | Ethernet MAC Address Byte 6 | Ethernet MAC Address Byte 5 | Section 6.3.7.2.3 |
| 0x4 | LED 1 configuration | LED 0 Configuration | Section 6.3.7.3.1 |
| 0x5 | LED 3 Configuration | LED 2 Configuration | Section 6.3.7.3.2 |
| 0x6 | SDP Control | | Section 6.3.7.4 |
| 0x7 | Filter Control | | Section 6.3.7.5 |

### 6.3.7.1 Section Length — Offset 0x00

The section length word contains the length of the section in words. Note that section length does not include a count for the section length word.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | Section Length | 0x0 | Section length in words. | |

### 6.3.7.2 Ethernet MAC Address Registers

The Ethernet Individual Address (IA) is a 6-byte field that must be unique for each NIC or LOM and must also be unique for each copy of the EEPROM image. The first three bytes are vendor specific. For example, the IA is equal to [00 AA 00] or [00 A0 C9] for Intel products. The value of this field is loaded into the Receive Address register 0 (RAL0/ RAH0).

For the purpose of this datasheet, the numbering convention is as follows:

| Vendor | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| Intel original | 00 | AA | 00 | Variable | Variable | Variable |
| Intel new | 00 | A0 | C9 | Variable | Variable | Variable |

#### 6.3.7.2.1 Ethernet MAC Address Register1 — Offset 0x01

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | Eth_Addr_Byte2 | 0x0 | Ethernet MAC address byte 2. | |
| 7:0 | Eth_Addr_Byte1 | 0x0 | Ethernet MAC address byte 1. | |

#### 6.3.7.2.2 Ethernet MAC Address Register2 — Offset 0x02

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | Eth_Addr_Byte4 | 0x0 | Ethernet MAC address byte 4. | |
| 7:0 | Eth_Addr_Byte3 | 0x0 | Ethernet MAC address byte 3. | |

#### 6.3.7.2.3 Ethernet MAC Address Register3 — Offset 0x03

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | Eth_Addr_Byte6 | 0x0 | Ethernet MAC address byte 6. | |
| 7:0 | Eth_Addr_Byte5 | 0x0 | Ethernet MAC address byte 5. | |

### 6.3.7.3 LED Configuration

The LEDCTL register (Section 8.2.3.1.6) defaults are loaded from two words as listed in the following tables.

#### 6.3.7.3.1 LED Control Lower Word — Offset 0x04

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | LEDCTL1 | 0x0 | LED 1 control. | |
| 7:0 | LEDCTL0 | 0x0 | LED 0 control. | |

#### 6.3.7.3.2 LED control Upper Word — Offset 0x05

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | LEDCTL3 | 0x0 | LED 3 control. | |
| 7:0 | LEDCTL2 | 0x0 | LED 2 control. | |

**Note:** The content of the EEPROM words is similar to the register content.

### 6.3.7.4 SDP Control — Offset 0x06

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15 | SDP1_NATIVE | 0b | Defines the SDP1 operating mode that is mapped to ESDP.SDP1_NATIVE loaded at power up:<br>0b = Operates as generic software controlled IO.<br>1b = Native mode operation (hardware function). | |
| 14:12 | Reserved | 000b | Set to 000b. | |
| 11 | SDPDIR[3] | 0b | SDP3 Pin.<br>Initial direction is mapped to ESDP.SDP3_IODIR loaded at power up. | |
| 10 | SDPDIR[2] | 0b | SDP2 Pin.<br>Initial direction is mapped to ESDP.SDP2_IODIR loaded at power up. | |
| 9 | SDPDIR[1] | 0b | SDP1 Pin.<br>Initial direction is mapped to ESDP.SDP1_IODIR loaded at power up. | |
| 8 | SDPDIR[0] | 0b | SDP0 Pin.<br>Initial direction is mapped to ESDP.SDP0_IODIR loaded at power up. | |
| 7:4 | Reserved | 0x0 | Reserved. | |
| 3 | SDPVAL[3] | 0b | SDP3 Pin.<br>Initial output value is mapped to ESDP.SDP3_DATA loaded at power up. | |
| 2 | SDPVAL[2] | 0b | SDP2 Pin.<br>Initial output value is mapped to ESDP.SDP2_DATA loaded at power up. | |
| 1 | SDPVAL[1] | 0b | SDP1 Pin.<br>Initial output value is mapped to ESDP.SDP1_DATA loaded at power up. | |
| 0 | SDPVAL[0] | 0b | SDP0 Pin.<br>Initial output value is mapped to ESDP.SDP0_DATA loaded at power up. | |

### 6.3.7.5 Filter Control — Offset 0x07

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | Reserved | 0x1 | *Note:* Reserved. | |

## 6.3.8 MAC 0/1 Modules

Word 0xB points to the LAN MAC configuration defaults of function 0 while word 0xC points to function 1 defaults. Both sections are loaded at the de-assertion of their core master reset. The structures of both sections are identical; as listed in the following table.

| Offset | Content | Section |
|---|---|---|
| | Section Length = 0x5 | |
| 0x1 | Link Mode Configuration | Section 6.3.8.2 |
| 0x2 | Swap Configuration | Section 6.3.8.3 |
| 0x3 | Swizzle and Polarity Configuration | Section 6.3.8.4 |
| 0x4 | Auto Negotiation Default Bits | Section 6.3.8.5 |
| 0x5 | AUTOC2 Upper Half | Section 6.3.8.6 |
| 0x6 | SGMIIC Lower Half | Section 6.3.8.7 |
| 0x7 | KR-PCS configurations | Section 6.3.8.8 |

### 6.3.8.1 Section Length — Offset 0x00

The section length word contains the length of the section in words. Note that the section length does not include a count for the section length word.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | Section_length | 0x0 | Section length in words. | |

### 6.3.8.2 Link Mode Configuration – Offset 0x01

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:13 | Link Mode Select | 100b | 000b = 1 Gb/s link (no auto-negotiation).<br>001b = 10 Gb/s parallel link (no auto-negotiation).<br>010b = 1 Gb/s link with clause 37 auto-negotiation enable.<br>011b = 10 Gb/s serial link (no auto-negotiation). Supports SFI without backplane auto-negotiation.<br>100b = KX/KX4/KR backplane auto-negotiation enable. 1 Gb/s (Clause 37) auto-negotiation disable.<br>101b = SGMII 1G/100M link.<br>110b = KX/KX4/KR backplane auto-negotiation enable. 1 Gb/s (Clause 37) auto-negotiation enable.<br>111b = KX/KX4/KR backplane auto-negotiation enable. SGMII 1 Gb/s or 100 Mb/s (in KX) enable. These bits are mapped to AUTOC.LMS | |
| 12 | Restart AN | 0b | Restarts the KX/KX4/KR backplane auto-negotiation process (self-clearing bit).<br>Mapped to AUTOC.Restart_Auto Negotiation. | |
| 11 | RATD | 0b | Restarts backplane auto-negotiation on a transition to Dx.<br>Mapped to AUTOC.RATD and applied to AUTOC.RATD. | |
| 10 | D10GMP | 0b | Disables 10 Gb/s (KX4/KR) on Dx (Dr/D3) without main power.<br>Mapped to AUTOC.D10GMP. | |
| 9 | 1G PMA_PMD | 1b | PMA/PMD used for 1 Gb/s.<br>Mapped to AUTOC.1G_PMA_PMD. | |
| 8:7 | 10G PMA_PMD_ PARALLEL | 01b | PMA/PMD used for 10 Gb/s over four differential pairs for TX and RX each.<br>Mapped to AUTOC.10G_PMA_PMD_PARALLEL. | |
| 6:2 | ANSF | 00001b | AN Selector Field (Debug mode).<br>Mapped to AUTOC.ANSF | |
| 1 | ANACK2 | 0b | *AN Ack2* field.<br>This value is transmitted in the *Achnowledge2* field of the Null Next Page that is transmitted during next page handshake. Mapped to AUTOC.ANACK2 | |
| 0 | Reserved | 0b | Reserved. | |

### 6.3.8.3 SWAP Configuration — Offset 0x02

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:14 | Swap_Rx_Lane_0 | 00b | Determines which core lane is mapped to MAC Rx lane 0.<br>00b = Core Rx lane 0 to MAC Rx lane 0.<br>01b = Core Rx lane 1 to MAC Rx lane 0.<br>10b = Core Rx lane 2 to MAC Rx lane 0.<br>11b = Core Rx lane 3 to MAC Rx lane 0.<br>Mapped to SERDESC.swap_rx_lane_0. | |
| 13:12 | Swap_Rx_Lane_1 | 01b | Determines which core lane is mapped to MAC Rx lane 1.<br>Mapped to SERDESC.swap_rx_lane_1. | |
| 11:10 | Swap_Rx_Lane_2 | 10b | Determines which core lane is mapped to MAC Rx lane 2.<br>Mapped to SERDESC.swap_rx_lane_2. | |
| 9:8 | Swap_Rx_Lane_3 | 11b | Determines which core lane is mapped to MAC Rx lane 3.<br>Mapped to SERDESC.swap_rx_lane_3. | |
| 7:6 | Swap_Tx_Lane_0 | 00b | Determines the core destination Tx lane for MAC Tx lane 0.<br>00b = MAC tx lane 0 to Core Tx lane 0.<br>01b = MAC tx lane 0 to Core Tx lane 1.<br>10b = MAC tx lane 0 to Core Tx lane 2.<br>11b = MAC tx lane 0 to Core Tx lane 3.<br>Mapped to SERDESC.swap_tx_lane_0. | |
| 5:4 | Swap_Tx_Lane_1 | 01b | Determines the core destination Tx lane for MAC Tx lane 1.<br>Mapped to SERDESC.swap_tx_lane_1. | |
| 3:2 | Swap_Tx_Lane_2 | 10b | Determines the core destination Tx lane for MAC Tx lane 2.<br>Mapped to SERDESC.swap_tx_lane_2. | |
| 1:0 | Swap_Tx_Lane_3 | 11b | Determines the core destination Tx lane for MAC Tx lane 3.<br>Mapped to SERDESC.swap_tx_lane_3. | |

### 6.3.8.4 Swizzle and Polarity Configuration — Offset 3

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:12 | Swizzle_Rx | 0x0 | Swizzle_Rx[0] — Swizzles the bits of MAC Rx lane 0.<br>Swizzle_Rx[1] — Swizzles the bits of MAC Rx lane 1.<br>Swizzle_Rx[2] — Swizzles the bits of MAC Rx lane 2.<br>Swizzle_Rx[3] — Swizzles the bits of MAC Rx lane 3.<br>Swizzles the bits if set to 1b.<br>Mapped to SERDESC.Swizzle_Rx_lanes. | |
| 11:8 | Swizzle_Tx | 0x0 | Swizzle_Tx[0] — Swizzles the bits of MAC Tx lane 0.<br>Swizzle_Tx[1] — Swizzles the bits of MAC Tx lane 1.<br>Swizzle_Tx[2] — Swizzles the bits of MAC Tx lane 2.<br>Swizzle_Tx[3] — Swizzles the bits of MAC Tx lane 3.<br>Swizzles the bits if set to 1b.<br>Mapped to SERDESC.Swizzle_Tx_lanes. | |

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 7:4 | Polarity_Rx | 0x0 | Polarity_Rx[0] — Changes the bit polarity of MAC Rx lane 0<br>Polarity_Rx[1] — Changes the bit polarity of MAC Rx lane 1<br>Polarity_Rx[2] — Changes the bit polarity of MAC Rx lane 2<br>Polarity_Rx[3] — Changes the bit polarity of MAC Rx lane 3<br>Changes bit polarity if set to 1b.<br>Mapped to SERDESC.Rx_lanes_polarity. | |
| 3:0 | Polarity_Tx | 0x0 | Polarity_Tx[0] — Changes the bit polarity of MAC Tx lane 0.<br>Polarity_Tx[1] — Changes the bit polarity of MAC Tx lane 1.<br>Polarity_Tx[2] — Changes the bit polarity of MAC Tx lane 2.<br>Polarity_Tx[3] — Changes the bit polarity of MAC Tx lane 3.<br>Changes bit polarity if set to 1b.<br>Mapped to SERDESC.Tx_lanes_polarity. | |

### 6.3.8.5 Auto Negotiation Defaults — Offset 4

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:14 | KX Support | 1b | The value of these EEPROM settings are shown in bits A0:A1 of the *Technology Ability* field of the backplane auto-negotiation word while A2 field is configured in the KR_support bit:<br>00b = A0 = 0 A1 = 0. KX not supported. KX4 not supported. Value is illegal if KR is also not supported (AUTOC.KR_support = 0b).<br>01b = A0 = 1 A1 = 0. KX supported. KX4 not supported.<br>10b = A0 = 0 A1 = 1. KX not supported. KX4 supported.<br>11b = A0 = 1 A1 = 1. KX supported. KX4 supported.<br>Mapped to AUTOC.KX_support. | |
| 13:12 | Pause Bits | 0b | The value of these bits is loaded to bits D11:D10 of the link code word (pause data). Bit 12 is loaded to D11.<br>Mapped to AUTOC.PB. | |
| 11 | RF | 0b | This bit is loaded to the RF bit in the backplane auto-negotiation word.<br>Mapped to AUTOC.RF. | |
| 10:9 | AN Parallel Detect Timer | 00b | Configures the parallel detect counters.<br>00b = 1 ms.<br>01b = 2 ms.<br>10b = 5 ms.<br>11b = 8 ms.<br>Mapped to AUTOC.ANPDT. | |
| 8 | AN RX Loose Mode | 0b | Enables less restricted functionality (allow 9/11 bit symbols).<br>0b = Disables loose mode.<br>1b = Enables loose mode.<br>Mapped to AUTOC.ANRXLM. | |
| 7 | AN RX Drift Mode | 1b | Enables the drift caused by PPM in the RX data.<br>0b = Disables drift mode.<br>1b = Enables drift mode.<br>Mapped to AUTOC.ANRXDM. | |

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 6:3 | AN RX Align Threshold | 0011b | Sets the threshold to determine that the alignment is stable.<br>Sets how many stable symbols to find before declaring the AN_RX.<br>10b = Symbol stable.<br>Mapped to AUTOC.ANRXAT. | |
| 2 | FEC Ability | 1b | FEC Ability. Configures the F0 bit in the backplane auto-negotiation base link code word.<br>Should be set to 1b only if KR ability is set to 1b (AUTOC.KR = 1b).<br>0b = FEC not supported.<br>1b = FEC supported.<br>Mapped to AUTOC.FECA. | |
| 1 | FEC Requested | 0b | FEC requested.<br>Configures the F1 bit in the backplane auto-negotiation base link code word. Should be set to 1b only if KR ability is set to 1b (AUTOC.KR = 1b).<br>0b = FEC not requested from link partner.<br>1b = FEC requested from link partner.<br>Mapped to AUTOC.FECR. | |
| 0 | KR Support | 1b | Configures the A2 bit of the *Technology Ability Field* in the backplane auto-negotiation word while the A0:A1 field is configured according to the KX_support field (bits 31:30):<br>0b = KR not supported. Value is illegal if KX and KX4 are also not supported (AUTOC.KX_support = 00b).<br>1b = KR supported.<br>Mapped to AUTOC.KR_Support. | |

## 6.3.8.6 AUTOC2 Upper Half – Offset 5

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15 | Force FEC Enable | 0b | Force FEC Enable.<br>Enables FEC without dependency on the auto-negotiation resolution. Debug mode only. Mapped to AUTOC2.FORCE_FEC. | |
| 14 | Parallel Detect Disable | 0b | Disables the parallel detect part in the KX/KX4/KR backplane auto-negotiation process.<br>Mapped to AUTOC2.PDD. | |
| 13 | ANIGNRRXRF | 1b | AN Ignore Received RF Field.<br>Mapped to SGMIIC.ANIGNRRXRF | |
| 12 | Reserved | 0b | Reserved | |
| 11:8 | Reserved | 0x0 | Reserved | |
| 7 | Latch High 10G Aligned Indication | 0b | Override any de-skew alignment failures in the 10 Gb/s link (by latching high).<br>Mapped to AUTOC2.LH1GAI. | |
| 6 | Reserved | 0b | Reserved. | |

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 5 | AN 1G TIMEOUT EN | 1b | Auto Negotiation1 Gb/s Timeout Enable.<br>Mapped to PCS1GLCTL.AN 1G TIMEOUT EN | |
| 4 | Reserved | 0b | Reserved | |
| 3 | MAC DFT Override Comma Align | 0b | Override Internal Comma-Align Control.<br>Mapped to MDFTC2. MACDOCA. | |
| 2 | DDPT | 0b | Loaded to the *Disable DME Pages Transmit* bit in the AUTOC2 register. | |
| 1:0 | 10G PMA/PMD serial operation | 00b | PMA/PMD used for 10 Gb/s serial link.<br>Mapped to AUTOC2.10G_PMA_PMD_Serial. | |

### 6.3.8.7 SGMIIC Lower Half — Offset 6

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15 | ANSLNKTMR | 0b | AN SGMII Link-Timer.<br>Mapped to SGMIIC.ANSLNKTMR. | |
| 14 | ANSTRIG | 0b | AN SGMII Trigger.<br>Mapped to SGMIIC.ANSTRIG. | |
| 13 | ANSBYP | 0b | AN SGMII Bypass.<br>Mapped to SGMIIC.ANSBYP. | |
| 12 | ANSFLU100 | 0b | AN SGMII Force Link Up 100 Mb/s.<br>Mapped to SGMIIC.ANSFLU100. | |
| 11:8 | STXRASMP | 0x0 | Shift TX Rate-Adapt Sampling.<br>Mapped to SGMIIC.STXRASMP. | |
| 7:4 | SRXRARSMP | 0x0 | Shift RX Rate-Adapt Replicated Data Sampling.<br>Mapped to SGMIIC.SRXRARSMP. | |
| 3:0 | SRXRASSMP | 0x0 | Shift RX Rate-Adapt Single Data Sampling.<br>Mapped to SGMIIC.SRXRASSMP. | |

### 6.3.8.8 KR-PCS configurations — Offset 7

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15 | IE3_MODE | 1b | IEEE sync mode (debug mode).<br>Mapped to KRPCSFC.IE3_MODE. | |
| 14:11 | Reserved | 0x0 | Reserved. | |
| 10 | BYP_FEC_SIG_DET | 0b | Bypass FEC signal detect (Debug mode).<br>Mapped to KRPCSFC. BYP_FEC_SIG_DET. | |

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 9:0 | Reserved | 0x0 | Reserved. | |

## 6.3.9 CSR 0/1 Auto Configuration Modules

Word 0xD points to the CSR auto configuration of function 0 while word 0xE points to function 1. Both sections are loaded at the de-assertion of their core master reset.

The structures of both sections are identical; the structure is listed in the following table.

| Offset | High Byte[15:8] | Low Byte[7:0] | Section |
|---|---|---|---|
| 0x0 | Section Length = 3*n | | |
| 0x1 | CSR Address | | Section 6.3.9.2 |
| 0x2 | Data LSB | | Section 6.3.9.3 |
| 0x3 | Data MSB | | Section 6.3.9.4 |
| | … | | |
| 3*n — 2 | CSR Address | | Section 6.3.9.2 |
| 3*n — 1 | Data LSB | | Section 6.3.9.3 |
| 3*n | Data MSB | | Section 6.3.9.4 |

**Note:** The 82599 blocks any write to the Analog Configuration registers through these sections.

### 6.3.9.1 Section Length — Offset 0x0

The section length word contains the length of the section in words. Note that section length does not include a count for the section length word.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | Section_length | 0x0 | Section length in words. | |

### 6.3.9.2 CSR Address — Offset 0x1, 0x4, 0x7...

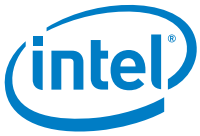
| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | CSR_ADDR | 0x0 | CSR address. | |

### 6.3.9.3 CSR Data LSB — Offset 0x2, 0x5, 0x8...

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | CSR_Data_LSB | 0x0 | CSR data LSB. | |

### 6.3.9.4 CSR Data MSB — Offset 0x3, 0x6, 0x9...

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:0 | CSR_Data_MSB | 0x0 | CSR data MSB. | |



# 6.4 Firmware Module

The following table lists the EEPROM global offsets used by the 82599 firmware.

| Global MNG Word Offset | Description |
|---|---|
| 0x0 | Test Configuration Pointer - Section 6.4.1 |
| 0x1 | Reserved |
| 0x2 | LESM Module Pointer - Appendix B |
| 0x3 | Common Firmware Parameters - Section 6.4.2 |
| 0x4 | Pass Through Patch Configuration Pointer (Patch structure identical to the Loader Patch) - Section 6.4.2 |
| 0x5 | Pass Through LAN 0 Configuration Pointer - Section 6.4.3 |
| 0x6 | SideBand Configuration Pointer - Section 6.4.4 |
| 0x7 | Flexible TCO Filter Configuration Pointer - Section 6.4.5 |
| 0x8 | Pass Through LAN 1 Configuration Pointer - Section 6.4.3 |
| 0x9 | NC-SI Microcode Download Pointer - Section 6.4.6 |
| 0xA | NC-SI Configuration Pointer - Section 6.4.7 |

## 6.4.1 Test Configuration Module

### 6.4.1.1 Section Header — Offset 0x0

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | Block CRC | | | |
| 7:0 | Block Length | | Block length in words | |

### 6.4.1.2 SMBus Address — Offset 0x1

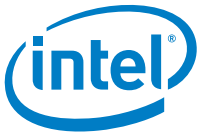
| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:9 | Reserved | | | |
| 8 | SMBus Interface Number | | | |
| 7:0 | SMBus Slave Address | | | |

### 6.4.1.3 Loopback Test Configuration — Offset 0x2

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:2 | Reserved | | | |
| 1 | Loopback Test Use SDP Output | | | |
| 0 | Loopback Test Enable | | | |

## 6.4.2 Common Firmware Parameters — (Global MNG Offset 0x3)

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15 | Reserved | 0b | Reserved, should be set to 0b. | |
| 14 | Redirection Sideband Interface | | 0b = SMBus.<br>1b = NC-SI. | |
| 13:11 | Reserved | 000b | Reserved. | |
| 10:8 | Manageability Mode | | 0x0 = None.<br>0x1 = Reserved.<br>0x2 = Pass Through (PT) mode.<br>0x3 = Reserved.<br>0x4:0x7 = Reserved. | |
| 7 | Port1 Manageability Capable | | 0b = Not capable<br>1b = Bits 3 is applicable to port 1. | |
| 6 | Port0 Manageability Capable | | 0b = Not capable<br>1b = Bits 3 is applicable to port 0. | |
| 5 | LAN1 Force TCO Reset Disable | 0b | 0b = Enable Force TCO reset on LAN1.<br>1b = Disable Force TCO reset on LAN1. | |
| 4 | LAN0 Force TCO Reset Disable | 0b | 0b = Enable Force TCO reset on LAN0.<br>1b = Disable Force TCO reset on LAN0. | |
| 3 | Pass Through Capable | | 0b = Disable.<br>1b = Enable. | |
| 2:0 | Reserved | 000b | Reserved. | |



## 6.4.3 Pass Through LAN 0/1 Configuration Modules

The following sections describe pointers and structures dedicated to pass-through mode for LAN 0 and LAN 1. LAN 0 structure is pointed by the *Firmware Module* pointer at offset 0x5. LAN 1 structure is pointed by the *Firmware Module* pointer at offset 0x8.

### 6.4.3.1 Section Header — Offset 0x0

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | Block CRC8 | | | |
| 7:0 | Block Length | | Block length in words. | |

### 6.4.3.2 LAN 0/1 IPv4 Address 0 (LSB) MIPAF0 — Offset 0x01

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | | | LAN 0/1 IPv4 Address 0, Byte 1. | |
| 7:0 | | | LAN 0/1 IPv4 Address 0, Byte 0. | |

### 6.4.3.3 LAN 0/1 IPv4 Address 0 (MSB) (MIPAF0) — Offset 0x02

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | | | LAN 0/1 IPv4 Address 0, Byte 3. | |
| 7:0 | | | LAN 0/1 IPv4 Address 0, Byte 2. | |

### 6.4.3.4 LAN 0/1 IPv4 Address 1 MIPAF1 — Offset 0x03:0x04

Same structure as LAN0 IPv4 Address 0.

### 6.4.3.5 LAN 0/1 IPv4 Address 2 MIPAF2 — Offset 0x05:0x06

Same structure as LAN0 IPv4 Address 0.

### 6.4.3.6 LAN 0/1 IPv4 Address 3 MIPAF3 — Offset 0x07:0x08

Same structure as LAN0 IPv4 Address 0.

### 6.4.3.7 LAN 0/1 Ethernet MAC Address 0 (LSB) MMAL0 — Offset 0x09

This word is loaded by Firmware to the 16 LS bits of the MMAL[0] register.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | | | LAN 0/1 Ethernet MAC Address 0, Byte 1. | |
| 7:0 | | | LAN 0/1 Ethernet MAC Address 0, Byte 0. | |

### 6.4.3.8 LAN 0/1 Ethernet MAC Address 0 (Mid) MMAL0 — Offset 0x0A

This word is loaded by Firmware to the 16 MS bits of the MMAL[0] register.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | | | LAN 0/1 Ethernet MAC Address 0, Byte 3. | |
| 7:0 | | | LAN 0/1 Ethernet MAC Address 0, Byte 2. | |

### 6.4.3.9 LAN 0/1 Ethernet MAC Address 0 (MSB) MMAH0 — Offset 0x0B

This word is loaded by Firmware to the MMAH[0] register.

| Bits | Name | Default | Description | Reserved |
|---|---|---|---|---|
| 15:8 | | | LAN 0/1 Ethernet MAC Address 0, Byte 5. | |
| 7:0 | | | LAN 0/1 Ethernet MAC Address 0, Byte 4. | |