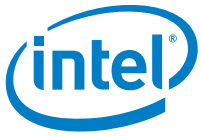


8.2.3.20.14 FC Filter RW Control — FCFLTRW (0x05110; WO)

Field	Bit(s)	Init Val	Description
FCoESEL	8:0	0x0	FCoE context Select. This field defines the FCoE Rx context index (equals the OX_ID for that context).
Reserve	12:9	0x0	Reserved.
Re-Validate	13	0b	Fast re-validation of the filter context. Setting this bit together with the *WE* bit in this register validates the selected filter context. Hardware sets the *Valid* bit and clears the *First* bit (described in the FCFLT register) while keeping all other filter parameters intact.
WE	14	0b	Write Enable. When this bit is set, the content of the FCFLT register is programmed to the filter of index FCoESEL. This bit should never be set together with the *RE* bit in this register.
RE	15	0b	Read Enable. When this bit is set, the internal filter context of index FCoESEL is fetched to the FCFLT register. This bit should never be set together with the *WE* bit in this register.
Reserve	31:16	0x0	Reserved.

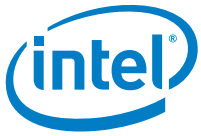
8.2.3.21 Flow Director Registers

Global settings registers.

8.2.3.21.1 Flow Director Filters Control Register — FDIRCTRL (0x0EE00; RW)

Note: This register should be configured ONLY as part of the flow director initialization flow or clearing the flow director table. Programming of this register with non-zero value PBALLOC initializes the flow director table.

Field	Bit(s)	Init Val	Description
PBALLOC	1:0	00b	Memory allocation for the flow director filters. 00b = No memory allocation — Flow Director Filters are disabled 01b = 64 KB (8 K minus 2 signature filters or 2 K minus 2 perfect match filters). 10b = 128 KB (16 K minus 2 signature filters or 4 K minus 2 perfect match filters). 11b = 256 KB (32 K minus 2 signature filters or 8 K minus 2 perfect match filters).
Reserved	2	0b	Reserved.
INIT-Done	3	0b	Flow director initialization completion indication (read only status). Indicates that hardware initialized the flow director table according to the PBALLOC setting. Software must not access any other flow director filters registers before the *INIT-Done* bit is set. When flow director filters are enabled (PBALLOC > 0), software must wait for the *INIT-Done* indication before Rx is enabled.
Perfect-Match	4	0b	Flow director filters mode of operation. When set to 1b, hardware supports perfect match filters according to PBALLOC. When cleared to 0b, hardware supports signature filters according to PBALLOC.
Report-Status	5	0b	Report flow director filter's status in the *RSS* field of the Rx descriptor for packets that matches a flow director filter. Enabling the flow director filter's status, the RXCSUM.PCSD bit should be set as well (disabling the fragment checksum). *Note:* The *Flow Director Filter Status* and *Error* bits in the *Extended Status* and *Error* fields in the Rx descriptor are always enabled.
Reserved	6	0b	Reserved.
Report-Status always	7	0b	Report flow director status in the *RSS* field of the Rx descriptor on any packet that can be candidates for the flow director filters. This bit can be set to 1b only when both the RXCSUM.PCSD bit and the *Report-Status* bit in this register are set.
Drop-Queue	14:8	0x0	Absolute Rx queue index used for the dropped packets. Software can set this queue to an empty one by setting RDLEN[n] to 0x0.
Reserved	15	0b	Reserved.
Flex-Offset	20:16	0x0	Offset within the first 64 bytes of the packet of a flexible 2-byte tuple. The offset is defined in word units counted from the first byte of the destination Ethernet MAC address.
Reserved	23:21	0x0	Reserved.



Field	Bit(s)	Init Val	Description
Max-Length	27:24	0x0	Maximum linked list length. This field defines the maximum recommended linked list associated to any hash value (defined in units of two filters). Packets that match filters that exceed the *Max-Length* are reported with an active *Length* bit in the *Extended Error* field. In addition, drop filters that exceed the *Max-Length* are posted to the Rx queue defined in the filter context rather than the *Drop-Queue* defined in this register. *Note:* Software should set this field to a value that indicates exceptional long buckets. Supporting 32 K filters with good hash scheme key, it is expected that a value of 0xA can be a good choice.
Full-Thresh	31:28	0x0	Full threshold is a recommended minimum number of flows that should remain unused (defined in units of 16 filters). When software exceeds this threshold (too low number of unused flows), hardware generates the flow director full interrupt. Software should avoid additional programming following this interrupt. *Note:* When the flow director filters are used completely, hardware discards silently further filters programming.

8.2.3.21.2 Flow Director Filters Lookup Table HASH Key — FDIRHKEY (0x0EE68; RW)

Field	Bit(s)	Init Val	Description
Key	31:0	0x80000001	Programmable hash lookup table key.

8.2.3.21.3 Flow Director Filters Signature Hash Key — FDIRSKEY (0x0EE6C; RW)

Field	Bit(s)	Init Val	Description
Key	31:0	0x80800101	Programmable Signature Key.

8.2.3.21.4 Flow Director Filters DIPv4 Mask — FDIRDIP4M (0x0EE3C; RW)

Field	Bit(s)	Init Val	Description
IPM	31:0	0x0	Mask Destination IPv4 Address. Each cleared bit means that the associated bit of the destination IPv4 address is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the destination IPv4 address is ignored (masked out). The LS bit of this register matches the first byte on the wire.

8.2.3.21.5 Flow Director Filters Source IPv4 Mask — FDIRSIP4M (0x0EE40; RW)

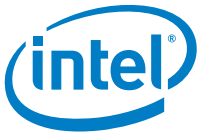
Field	Bit(s)	Init Val	Description
IPM	31:0	0x0	Mask Source IPv4 Address. Each cleared bit means that the associated bit of the source IPv4 address is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the source IPv4 address is ignored (masked out). The LS bit of this register matches the first byte on the wire.

8.2.3.21.6 Flow Director Filters TCP Mask — FDIRTCPM (0x0EE44; RW)

Field	Bit(s)	Init Val	Description
SPortM	15:0	0x0	Mask TCP Source Port. Each cleared bit means that the associated bit of the TCP source port is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the TCP source port is ignored (masked out). *Note:* This register is swizzle as follows: bit 0 in the mask affects bit 15 of the source port as defined in FDIRPORT.Source. bit 1 in the mask affects bit 14 in FDIRPORT.Source and so on while bit 15 in the mask affects bit 0 in FDIRPORT.Source.
DPortM	31:16	0x0	Mask TCP Destination Port. Each cleared bit means that the associated bit of the TCP destination port is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the TCP destination port is ignored (masked out). *Note:* This register is swizzle the same as the FDIRTCPM.SPortM.

8.2.3.21.7 Flow Director Filters UDP Mask — FDIRUDPM (0x0EE48; RW)

Field	Bit(s)	Init Val	Description
SPortM	15:0	0x0	Mask UDP Source Port. Each cleared bit means that the associated bit of the UDP source port is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the UDP source port is ignored (masked out). *Note:* This register is swizzle the same as the FDIRTCPM.SPortM.
DPortM	31:16	0x0	Mask UDP Destination Port. Each cleared bit means that the associated bit of the UDP destination port is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the UDP destination port is ignored (masked out). *Note:* This register is swizzle the same as the FDIRTCPM.SPortM.



8.2.3.21.8 Flow Director Filters IPv6 Mask — FDIRIP6M (0x0EE74; RW)

Field	Bit(s)	Init Val	Description
SIPM	15:0	0x0	Mask Source IPv6 address. Each cleared bit means that the associated byte of the source IPv6 address is meaningful for the filtering functionality. Each bit set to 1b means that the associated byte of the source IPv6 address is ignored (masked out). The LS bit of this register matches the first byte on the wire.
DIPM	31:16	0x0	Mask Destination IPv6 address. Each cleared bit means that the associated byte of the destination IPv6 address is meaningful for the filtering functionality. Each bit set to 1b means that the associated byte of the destination IPv6 address is ignored (masked out). The entire field is meaningful only for the hash function and the signature-based filters. The *DIPv6* bit in the FDIRM register is meaningful for perfect match filters. The LS bit of this register matches the first byte on the wire.

8.2.3.21.9 Flow Director Filters Other Mask — FDIRM (0x0EE70; RW)

Field	Bit(s)	Init Val	Description
VLANID	0	0b	Mask VLAN ID tag. When cleared the 12 bits of the VLAN ID tag are meaningful for the filtering functionality.
VLANP	1	0b	Mask VLAN Priority tag. When cleared the 3 bits of the VLAN Priority are meaningful for the filtering functionality.
POOL	2	0b	Mask Pool. When cleared the target pool number is meaningful for the filtering functionality.
L4P	3	0b	Mask L4 Protocol. When cleared the UDP/TCP/SCTP protocol type is meaningful for the filtering functionality. *Note:* For the flow director filtering aspects, SCTP is treated as if it is TCP.
FLEX	4	0b	Mask Flexible Tuple. When cleared the 2 bytes of the flexible tuple are meaningful for the filtering functionality.
DIPv6	5	0b	Mask Destination IPv6. When cleared the compare against the IP6AT filter is meaningful for IPv6 packets.
Reserved	31:6	0x0	Reserved.

Global Status / Statistics Registers

8.2.3.21.10 Flow Director Filters Free — FDIRFREE (0x0EE38; RW)

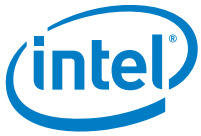
Field	Bit(s)	Init Val	Description
FREE	15:0	0x8000	Number of free (non programmed) filters in the flow director Filters logic.
Reserved	30:16	0x0	Reserved.
Reserved	31	0b	Reserved.

8.2.3.21.11 Flow Director Filters Length — FDIRLEN (0x0EE4C; RC)

Field	Bit(s)	Init Val	Description
MAXLEN	5:0	0x0	Longest linked list of filters in the table. This field records the length of the longest linked list that is updated since the last time this register was read by software. The longest bucket reported by this field includes MAXLEN + 1 filters.
Reserved	7:6	00b	Reserved.
Bucket Length	13:8	0x0	The length of the linked list indicated by a query command. This field is valid following a query command completion.
Reserved	15:14	00b	Reserved.
Reserved	30:16	0x0	Reserved.
Reserved	31	0b	Reserved.

8.2.3.21.12 Flow Director Filters Usage Statistics — FDIRUSTAT (0x0EE50; RW/RC)

Field	Bit(s)	Init Val	Description
ADD	15:0	0x0	Number of added filters. This field counts the number of added filters to the flow director filters logic. The counter is stacked at 0xFFFF and cleared on read.
REMOVE	31:16	0x0	Number of removed filters. This field counts the number of removed filters to the flow director filters logic. The counter is stacked at 0xFFFF and cleared on read.



8.2.3.21.13 Flow Director Filters Failed Usage Statistics — FDIRFSTAT (0x0EE54; RW/RC)

Field	Bit(s)	Init Val	Description
FADD	7:0	0x0	Number of filters addition events that do not change the number of free (non programmed) filters in the flow director filters logic (FDIRFREE.FREE). These events can be either filters update, filters collision, or tentative of filter additions when there is no sufficient space remaining in the filter table. The counter is stacked at 0xFF and cleared on read.
FREMOVE	15:8	0x0	Number of failed removed filters. The counter is stacked at 0xFF and cleared on read.
Reserved	31:16	0x0	Reserved.

8.2.3.21.14 Flow Director Filters Match Statistics — FDIRMATCH (0x0EE58; RC)

Field	Bit(s)	Init Val	Description
PCNT	31:0	0x0	Number of packets that matched any flow director filter. The counter is stacked at 0xFF…F and cleared on read. *Note:* This counter can include packets that match the L2 filters or 5 tuple filters or Syn filters even if they are enabled for queue assignment.

8.2.3.21.15 Flow Director Filters Miss Match Statistics — FDIRMISS (0x0EE5C; RC)

Field	Bit(s)	Init Val	Description
PCNT	31:0	0x0	Number of packets that missed matched any flow director filter. The counter is stacked at 0xFF…F and cleared on read.

Flow Programming Registers

8.2.3.21.16 Flow Director Filters Source IPv6 — FDIRSIPv6[n] (0x0EE0C + 4*n, n=0…2; RW)

Field	Bit(s)	Init Val	Description
IP6SA	31:0	0x0	Three MS DWords of the source IPv6 address. While the LS byte of FDIRSIPv6[0] is first on the wire. The FDIRIPSA contains the LS Dword of the IP6 address while its MS byte is last on the wire.

8.2.3.21.17 Flow Director Filters IP SA — FDIRIPSA (0x0EE18; RW)

Field	Bit(s)	Init Val	Description
IP4SA	31:0	0x0	Source IPv4 address or LS Dword of the Source IPv6 address. While the field is defined in big endian (LS byte is first on the wire).

8.2.3.21.18 Flow Director Filters IP DA — FDIRIPDA (0x0EE1C; RW)

Field	Bit(s)	Init Val	Description
IP4DA	31:0	0x0	Destination IPv4 address. While the field is defined in big endian (LS byte is first on the wire).

8.2.3.21.19 Flow Director Filters Port — FDIRPORT (0x0EE20; RW)

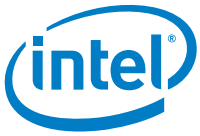
Field	Bit(s)	Init Val	Description
Source	15:0	0x0	Source Port number while the field is defined in Little Endian (MS byte is first on the wire). *Note:* For SCTP filter the Source and Destination port numbers must be set to zero (while the HW does not check it).
Destination	31:16	0x0	Destination Port number while the field is defined in Little Endian (MS byte is first on the wire). *Note:* For SCTP filter the Source and Destination port numbers must be set to zero (while the HW does not check it).

8.2.3.21.20 Flow Director Filters VLAN and FLEX Bytes — FDIRVLAN (0x0EE24; RW)

Field	Bit(s)	Init Val	Description
Vlan	15:0	0x0	Vlan Tag while the field is defined in Little Endian (MS byte is first on the wire). The CFI bit must be set to Zero while it is not checked by hardware.
Flex	31:16	0x0	Flexible tuple data as defined by the *Flex-Offset* field in the FDIRCTRL register while the field is defined in big endian (LS byte is first on the wire).

8.2.3.21.21 Flow Director Filters Hash Signature — FDIRHASH (0x0EE28; RW)

Field	Bit(s)	Init Val	Description
Hash	14:0	0x0	Bucket hash value that identifies a filter's linked list.
Bucket Valid	15	0b	The *Valid* bit is set by hardware each time there is at least one filter assigned to this hash.



Field	Bit(s)	Init Val	Description
Signature / SW-Index	30:16	0x0	Flow director filter signature for signature filters and software-index for perfect match filters.
Reserved	31	0b	Reserved.

8.2.3.21.22 Flow Director Filters Command Register — FDIRCMD (0x0EE2C; RW)

Field	Bit(s)	Init Val	Description
CMD	1:0	00b	Flow Director Filter Programming Command. 00b = No Action 01b = Add Flow 10b = Remove Flow 11b = Query Command Following a command completion hardware clears the *CMD* field. In a query command, all other parameters are valid when the *CMD* field is zero.
Filter Valid	2	0b	Valid filter is found by the query command. This bit is set by the 82599 following a query command completion.
Filter-Update	3	0b	Filter Update Command. This bit is relevant only for Add Flow command and must be set to zero in any other commands. When cleared, the filter parameters do not override existing ones if exist while setting only the collision bit. When set to 1b the new filter parameters override existing ones if exist keeping the collision bit as is.
IPv6DMatch	4	0b	IP Destination match to IP6AT filter. This bit is meaningful only for perfect match IPv6 filters. Otherwise it should be cleared by software at programming time. When set to 1b the destination IPv6 address should match the IP6AT. When cleared, the destination IPv6 address should not match the IP6AT. This field can never match local VM to VM traffic.
L4TYPE	6:5	0b	L4 Packet Type. Defines the packet as one of the following L4 types: 00b = Reserved 01b = UDP 10b = TCP 11b = SCTP *Note:* Encoding of the L4TYPE for the flow director filters is defined differently than the protocol type encoding in the FTQF registers for the 128 x 5 tuple filters.
IPV6	7	0b	IPv6 packet type when set to 1b and IPv4 packet type at 0b. *Note:* The IP type is checked always even if the filters do not check for IP address match.
CLEARHT	8	0b	Clear Internal Flow Director Head and Tail Registers. This bit is set only as part of Flow Director init. During nominal Operation it must be kept at 0b.

Field	Bit(s)	Init Val	Description
Drop	9	0b	Packet drop action: Receive packets that match a filter with active Drop bit and do not exceed the maximum recommended linked list length defined in FDIRCTRL.Max-Length field are posted to the global queue defined by FDIRCTRL.Drop-Queue. Receive packets that match a filter with active Drop bit and exceeds the maximum recommended linked list length defined in FDIRCTRL.Max-Length field are posted to the queue defined by RX-Queue field in this register. The receive descriptor of such packets is reported with active FDIRErr(0) flag indicating that the Max-Length was exceeded. The Drop Flag is useful only for perfect match filters and it should be cleared by software for Signature filters. When the Drop bit is set, the Queue-EN flag must be set and Rx-Queue in this register must be valid as well. Otherwise, the result is unexpected.
INT	10	0b	Matched packet generates a LLI.
Last	11	0b	Last filter indication in the linked list. At flow programming, software should set the last bit to 1b. Hardware can modify this bit when adding or removing flows from the same linked list.
Collision	12	0b	Collision Indication. This field is set to 1b when software programs the same multiple times. In signature based filtering, it is set when software programs a filter with the same hash and signature multiple times. It should be cleared by software when it adds a flow. It can also be set by hardware when two flows collide with the same hash and signature. During reception, this bit is reported on the Rx descriptor of packets that match the filter. See bit 7 for description of the query- type.
Reserved	14:13	00b	Reserved.
Queue-EN	15	0b	Enable routing matched packet to the queue defined by the Rx-Queue. *Note:* Packets redirection to the FDIRCTRL.Drop-Queue is not gated by the Queue-EN bit.
Rx-Queue	22:16	0x0	Rx Queue Index. This field defines the absolute Rx queue index in all modes of operation (regardless of DCB and VT enablement).
Reserved	23	0b	Reserved.
Pool	29:24	0x0	Pool number is meaningful when VT mode is enabled. When both VT is not enabled, this field must be set by software to 0x0.
Reserved	31:30	0x0	Reserved.

8.2.3.22 MAC Registers

8.2.3.22.1 PCS_1G Global Config Register 1 — PCS1GCFIG (0x04200; RW)

Field	Bit(s)	Init Val	Description
Reserved	29:0	0x8	Reserved.
PCS_isolate	30	0b	PCS Isolate. Setting this bit isolates the 1 GbE PCS logic from the MAC's data path. PCS control codes are still sent and received.
Reserved	31	1b	Reserved.

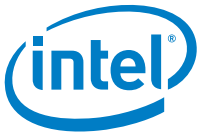
8.2.3.22.2 PCG_1G link Control Register — PCS1GLCTL (0x04208; RW)

Field	Bit(s)	Init Val	Description
FLV	0	0	Forced Link 1 GbE Value. This bit denotes the link condition when *Force Link* is set. 0b = Forced link down. 1b = Forced 1 GbE link up.
Reserved	4:1	0x7	Reserved.
FORCE 1G LINK	5	0	Force 1 GbE Link. If this bit is set then the internal LINK_OK variable is forced to *Forced Link Value*, bit 0 of this register. Else LINK_OK is decided by internal AN/SYNC state machines. This bit is only valid when the link mode is 1 GbE mode.
LINK LATCH LOW	6	0	Link Latch Low Enable. If this bit is set then *Link OK* going LOW; negedge) is latched until a CPU read happens. Once a CPU read happens *Link OK* is continuously updated until *Link OK* again goes LOW (negedge is seen).
Reserved	17:7	0	Reserved.
AN 1G TIMEOUT EN	18	1b	Auto Negotiation 1 GbE Timeout Enable. This bit enables the 1 GbE auto- negotiation timeout feature. During 1 GbE auto-negotiation, if the link partner doesn't respond with auto-negotiation pages but continues to send good idle symbols then linkup is assumed. (This enables a link-up condition when a link partner is not auto-negotiation capable and does not affect otherwise).
Reserved	19	0b	Reserved.
Reserved	20	0b	Reserved, must be set to 0b.
Reserved	24:21	0x0	Reserved.

Field	Bit(s)	Init Val	Description
LINK OK FIX EN	25	1b	Link OK Fix En. Control for enabling/disabling LinkOK-SyncOK fix. This bit should be set to 1b for nominal operation.
Reserved	31:26	0x0	Reserved.

8.2.3.22.3 PCS_1G Link Status Register — PCS1GLSTA (0x0420C; RO)

Field	Bit(s)	Init Val	Description
Reserved	3:0	1110b	Reserved.
SYNC OK 1G	4	0b	Sync OK 1 GbE. This bit indicates the current value of SYN OK from the 1G PCS Sync state machine,
Reserved	15:5	0x0	Reserved.
AN 1G COMPLETE	16	0b	Auto Negotiation1 GbE Complete. This bit indicates that the 1 GbE auto-negotiation process completed.
AN PAGE RECEIVED	17	0b	Auto-Negotiation Page Received. This bit indicates that a link partner's page was received during auto-negotiation process. Clear on read.
AN 1G TIMEDOUT	18	0b	Auto Negotiation1 GbE Timed Out. This bit indicates 1 GbE auto-negotiation process was timed out. Valid after *AN 1G Complete* bit is set.
AN REMOTE FAULT	19	0b	Auto Negotiation Remote Fault. This bit indicates that a 1 GbE auto-negotiation page was received with remote fault indication during 1 GbE auto-negotiation process. Clear on read.
AN ERROR (RW)	20	0b	Auto Negotiation Error. This bit indicates that an auto-negotiation error condition was detected in 1 GbE auto-negotiation mode. Valid after the *AN 1G Complete* bit is set. Auto-negotiation error conditions: Both nodes not full duplex or remote fault indicated or received. Software can also force an auto-negotiation error condition by writing to this bit (or can clear an existing auto-negotiation error condition). Cleared at the start of auto-negotiation.
Reserved	31:21	0x0	Reserved.



8.2.3.22.4 PCS_1 Gb/s Auto Negotiation Advanced Register — PCS1GANA (0x04218; RW)

Field	Bit(s)	Init Val	Description
Reserved	4:0	0x0	Reserved.
FDC	5	1b	FD: Full-Duplex. Setting this bit means the local device is capable of full-duplex operation. This bit should be set to 1b for normal operation.
Reserved	6	0b	Reserved.
ASM	8:7	11b	ASM_DIR/PAUSE: Local PAUSE Capabilities. The local device's PAUSE capability is encoded in this field. 00b = No PAUSE. 01b = Symmetric PAUSE. 10b = Asymmetric PAUSE toward link partner. 11b = Both symmetric and asymmetric PAUSE toward local device.
Reserved	11:9	0x0	Reserved.
RFLT	13:12	00b	Remote Fault. The local device's remote fault condition is encoded in this field. Local device can indicate a fault by setting a non-zero remote fault encoding and re-negotiating. 00b = No error, link good. 01b = Link failure. 10b = Offline. 11b = Auto-negotiation error.
Reserved	14	0b	Reserved.
NEXTP	15	0b	NEXTP: Next Page Capable. The local device asserts this bit to request next page transmission. Clear this bit when local device has no subsequent next pages.
Reserved	31:16	0x0	Reserved.

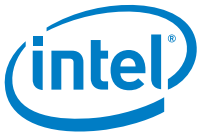
8.2.3.22.5 PCS_1GAN LP Ability Register — PCS1GANLP (0x0421C; RO)

Field	Bit(s)	Init Val	Description
Reserved	4:0	0x0	Reserved.
LPFD	5	0b	LP Full-Duplex (SerDes). When 1b, link partner is capable of full-duplex operation. When 0b, link partner is incapable of full-duplex mode.
LPHD	6	0b	LP Half-Duplex (SerDes). When 1b, link partner is capable of half-duplex operation. When 0b, link partner is incapable of half-duplex mode.

Field	Bit(s)	Init Val	Description
LPASM	8:7	00b	LPASMDR/LPPAUSE(SERDES). The link partner's PAUSE capability is encoded in this field. 00b = No PAUSE. 01b = Symmetric PAUSE. 10b = Asymmetric PAUSE toward link partner. 11b = Both symmetric and asymmetric PAUSE toward local device.
Reserved	11:9	0x0	Reserved.
PRF	13:12	00b	LP Remote Fault (SerDes)[13:12]. The link partner's remote fault condition is encoded in this field. 00b = No error, link good. 10b = Link failure. 01b = Offline. 11b = Auto-negotiation error.
ACK	14	0b	Acknowledge (SerDes). The link partner has acknowledged page reception.
LPNEXTP	15	0b	LP Next Page Capable (SerDes). The link partner asserts this bit to indicate its ability to accept next pages.
Reserved	31:16	0x0	Reserved.

8.2.3.22.6 PCS_1G Auto Negotiation Next Page Transmit Register — PCS1GANNP (0x04220; RW)

Field	Bit(s)	Init Val	Description
CODE	10:0	0x0	Message/Unformatted Code Field. The message field is an 11-bit wide field that encodes 2048 possible messages. Unformatted code field is an 11-bit wide field, which can contain an arbitrary value.
TOGGLE	11	0b	Toggle. This bit is used to ensure synchronization with the link partner during a next page exchange. This bit always takes the opposite value of the *Toggle* bit in the previously exchanged link code word. The initial value of the *Toggle* bit in the first next page transmitted is the inverse of bit 11 in the base link code word and, therefore, can assume a value of 0b or 1b. The Toggle bit must be set as follows: 0b Previous value of the transmitted Link Code Word equaled 1b. 1b Previous value of the transmitted Link Code Word equaled 0b.
ACK2	12	0b	Acknowledge2. Acknowledge is used to indicate that a device has successfully received its link partner’s link code word.
PGTYPE	13	0b	Message/ Unformatted Page. This bit is used to differentiate a message page from an unformatted page. The encodings are: 0b = Unformatted page. 1b = Message page.
Reserved	14	0b	Reserved.



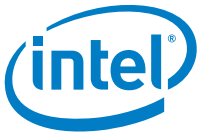
Field	Bit(s)	Init Val	Description
NXTPG	15	0b	Next Page. This bit is used to indicate whether or not this is the last next page to be transmitted. The encodings are: 0b = Last page. 1b = Additional next pages follow.
Reserved	31:16	0x0	Reserved.

8.2.3.22.7 PCS_1G Auto Negotiation LP's Next Page Register — PCS1GANLPNP (0x04224; RO)

Field	Bit(s)	Init Val	Description
CODE	10:0	0x0	Message/Unformatted Code Field. The message field is an 11-bit wide field that encodes 2048 possible messages. Unformatted code field is an 11-bit wide field, which can contain an arbitrary value.
TOGGLE	11	0bb	Toggle. This bit is used to ensure synchronization with the link partner during a next page exchange. This bit always takes the opposite value of the *Toggle* bit in the previously exchanged link code word. The initial value of the *Toggle* bit in the first next page transmitted is the inverse of bit 11 in the base link code word and, therefore, can assume a value of 0b or 1b. The Toggle bit must be set as follows: 0b = Previous value of the transmitted link code word equalled 1b. 1b = Previous value of the transmitted link code word equalled 0b.
ACK2	12	0	Acknowledge2. Acknowledge is used to indicate that a device has successfully received its link partner's link code word.
MSGPG	13	0bb	Message Page. This bit is used to differentiate a message page from an unformatted page. The encodings are: 0b = Unformatted page. 1b = Message page.
ACK	14	0	Acknowledge. The link partner has acknowledge next page reception.
NXTPG	15	0b	Next Page. This bit is used to indicate whether or not this is the last next page to be transmitted. The encodings are: 0b = Last page. 1b = Additional next pages follow.
Reserved	31:16	0x0	Reserved.

8.2.3.22.8 MAC Core Control 0 Register — HLREG0 (0x04240; RW)

Field	Bit(s)	Init Val	Description
TXCRCEN	0	1b	Tx CRC Enable. Enables a CRC to be appended by hardware to a Tx packet if requested by user. 0b = No CRC appended, packets always passed unchanged. 1b = Enable CRC by hardware (default).
Reserved	1	1b	Reserved.
RXCRCSTRP	1	1	Rx CRC STRIP. Causes the CRC to be stripped by HW from all packets The RDRXCTL.CRCStrip must be set the same as this bit. 0b = No CRC Strip by HW. 1b = Strip CRC by HW (Default).
JUMBOEN	2	0b	Jumbo Frame Enable. Enables frames up to the size specified in Reg MAXFRS (31:16). 0b = Disable jumbo frames (default). 1b = Enable jumbo frames.
Reserved	9:3	0x1	Reserved. Must be set to 0x1.
TXPADEN	10	1b	Tx Pad Frame Enable. Pad short Tx frames to 64 bytes if requested by user. 0b = Transmit short frames with no padding. 1b = Pad frames (default).
Reserved	14:11	0101b	Reserved.
LPBK	15	0b	LOOPBACK. Turn On Loopback Where Transmit Data Is Sent Back Through Receiver. 0b = Loopback disabled (Default). 1b = Loopback enabled.
MDCSPD	16	1b	MDC SPEED. High or Low Speed MDC Clock Frequency To PCS, XGXS, WIS, etc. **MDCSPD / Freq at 10 GbE / Freq at 1 GbEs / Freq at 100 Mb/s** 0b / 2.4 MHz / 240 KHz / 240 KHz 1b / 24 MHz / 2.4 MHz / 240 KHz *Note:* 1b = default.
CONTMDC	17	0b	Continuous MDC. Turn Off MDC Between MDIO Packets 0b = MDC Off Between Packets (default) 1b = Continuous MDC
Reserved	19:18	00b	Reserved.
PREPEND	23:20	0x0	Prepend Value. Number of 32-bit words starting after the preamble and SFD, to exclude from the CRC generator and checker (default – 0x0).
Reserved	24	0b	Reserved.
Reserved	26:25	00b	Reserved.



Field	Bit(s)	Init Val	Description
RXLNGTHERREN	27	1b	Rx Length Error Reporting. 0b = Disable reporting of all rx_length_err events. 1b = Enable reporting of rx_length_err events if length field < 0x0600.
RXPADSTRIPEN	28	0b	Rx Padding Strip Enable. 0b = Do not strip padding from Rx packets with length field < 64 (default). 1b = Strip padding from Rx packets with length field < 64 (debug only). *Note:* This functionality should be used as debug mode only. If Rx pad stripping is enabled, then the Rx CRC stripping needs to be enabled as well.
Reserved	31:29	0x0	Reserved.

8.2.3.22.9 MAC Core Status 1 Register- HLREG1 (0x04244; RO)

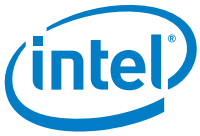
Field	Bit(s)	Init Val	Description
Reserved	3:0	0001b	Reserved.
Reserved	4	0b	Reserved.
RXERRSYM	5	0b	Rx Error Symbol. Error Symbol During Rx Packet (Latch High, Clear On Read). 0b = No error symbol (default). 1b = Error symbol received.
RXILLSYM	6	0b	Rx Illegal Symbol. Illegal Symbol During Rx Packet (Latch High, Clear On Read). 0b = No illegal symbol received (default). 1b = Illegal symbol received.
RXIDLERR	7	0b	Rx Idle Error. Non Idle Symbol During Idle Period (Latch High, Clear On Read). 0b = No idle errors received (default). 1b = Idle error received.
RXLCLFLT	8	0b	Rx Local Fault. Fault reported from PMD, PMA, or PCS (Latch High, Clear On Read). 0b = No local fault (default). 1b = Local fault is or was active.
RXRMTFLT	9	0b	Rx Remote Fault. Link Partner Reported Remote Fault (Latch High, Clear On Read). 0b = No remote fault (default). 1b = Remote fault is or was active.
Reserved	31:10	0x0	Reserved.

8.2.3.22.10 Pause and Pace Register — PAP (0x04248; RW)

Field	Bit(s)	Init Val	Description
Reserved	15:0	0xFFFF	Reserved.
PACE	19:16	0x0	0000b = 10 GbE (LAN) 0001b = 1 GbE 0010b = 2 GbE 0011b = 3 GbE 0100b = 4 GbE 0101b = 5 GbE 0110b = 6 GbE 0111b = 7 GbE 1000b = 8 GbE 1001b = 9 GbE 1111b = 9.294196 GbE (WAN) All other values are reserved.
Reserved	31:20	0x0	Reserved

8.2.3.22.11 MDI Single Command and Address — MSCA (0x0425C; RW)

Field	Bit(s)	Init Val	Description
MDIADD	15:0	0x0000	MDI Address. Address used for new protocol MDI accesses (default – 0x0000).
DEVADD	20:16	0x0	DeviceType/Register Address. Five bits representing either device type if STCODE = 00b or register address if STCODE = 01b.
PHYADD	25:21	0x0b	PHY Address. The address of the external device.
OPCODE	27:26	00	OP Code. Two bits identifying operation to be performed (default – 00b). 00b = Address cycle (new protocol only). 01b = Write operation. 10b = Read increment address (new protocol only) or read operation (old protocol only). 11b = Read operation (new protocol only).
STCODE	29:28	01b	ST Code. Two Bits Identifying Start Of Frame And Old Or New Protocol (Default – 01). 00b = New protocol. 01b = Old protocol. 1Xb = Illegal.



Field	Bit(s)	Init Val	Description
MDICMD	30	0b	MDI Command. Perform the MDIO Operation in this register, cleared when done. 0b = MDI Ready, operation complete (default). 1b = Perform operation, operation in progress.
Reserved	31	0b	Reserved.

8.2.3.22.12 MDI Single Read and Write Data — MSRWD (0x04260; RW)

Field	Bit(s)	Init Val	Description
MDIWRDATA	15:0	0x0	MDI Write Data. Write data For MDI writes to the external device.
MDIRDDATA	31:16	0x0	MDI Read Data. Read data from the external device (RO).

8.2.3.22.13 Max Frame Size — MAXFRS (0x04268; RW)

Field	Bit(s)	Init Val	Description
Reserved	15:0	0x0	Reserved.
MFS	31:16	0x5EE	This field defines the maximum frame size in bytes units from Ethernet MAC addresses up to inclusive the CRC. Frames received that are larger than this value are dropped. This field is meaningful when jumbo frames are enabled (HLREG0.JUMBOEN = 1b). When jumbo frames are not enabled the 82599 uses a hardwired value of 1518 for this field. The MFS does not include the 4 bytes of the VLAN header. Packets with VLAN header can be as large as MFS + 4. When double VLAN is enabled, the device adds 8 to the MFS for any packets. This value has no effect on transmit frames; it is the responsibility of software to limit the size of transmit frames.

8.2.3.22.14 XGXS Status 1 — PCSS1 (0x4288; RO)

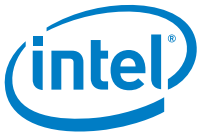
Field	Bit(s)	Init Val	Description
Reserved	1:0	00b	Reserved.
PCS Receive Link Status	2	0b	0b = PCS receive link down.The receive link status remains cleared until it is read (latching low). 1b = PCS receive link up. For 10BASE-X ->lanes de-skewed.
Reserved	6:3	0x0	Reserved.
Local Fault	7	1b	0b = No LF detected on receive path. 1b = LF detected on transmit or receive path. The *LF* bit is set to one when either of the local fault bits located in PCS Status 2 register are set to a 1b.
Reserved	31:8	0x0	Reserved.

8.2.3.22.15 XGXS Status 2 — PCSS2 (0x0428C; RO)

Field	Bit(s)	Init Val	Description
10GBASE-R Capable	0	0b	0b = PCS is not able to support 10GBASE-R port type. 1b = PCS is able to support 10GBASE-R port type.
10GBASE-X capable	1	1b	0b = PCS is not able to support 10GBASE-X port type. 1b = PCS is able to support 10GBASE-X port type.
10GBASE-W capable	2	0b	0b = PCS is not able to support 10GBASE-W port type. 1b = PCS is able to support 10GBASE-W port type.
Reserved	9:3	0x0	Reserved.
Receive local fault	10	1b	0b = No local fault condition on the receive path (latch high) 1b = Local fault condition on the receive path.
Transmit local fault	11	0b	0b = No local fault condition on the transmit path (latch high) 1b = Local fault condition on the transmit path.
Reserved	13:12	00b	Reserved.
Device present	15:14	10b	00b = No device responding at this address. 01b = No device responding at this address. 10b = Device responding at this address. 11b = No device responding at this address.
Reserved	31:16	0x0	Reserved.

8.2.3.22.16 10GBASE-X PCS Status — XPCSS (0x04290; RO)

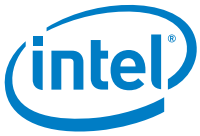
Field	Bit(s)	Init Val	Description
Lane 0 sync	0	0b	0b = Lane 0 is not synchronized. 1b = Lane 0 is synchronized.
Lane 1 sync	1	0b	0b = Lane 1 is not synchronized. 1b = Lane 1 is synchronized.
Lane 2 sync	2	0b	0b = Lane 2 is not synchronized. 1b = Lane 2 is synchronized.
Lane 3 sync	3	0b	0b = Lane 3 is not synchronized. 1b = Lane 3 is synchronized.
Reserved	11: 4	0b	Ignore when read.
10GBASE-X lane alignment status	12	0b	0b = 10GBASE-X PCS receive lanes not aligned. 1b = 10GBASE-X PCS receive lanes aligned (align_status – good).
Reserved	15:13	0x0	Reserved, ignore when read.



Field	Bit(s)	Init Val	Description
De-skew error	16	0b	0b = Indicates no de-skew error was detected (latch high). 1b = Indicates a de-skew error was detected.
Align column count 4	17	0b	0b = Indicates the align column count is less than four (latch high). 1b = Indicates the align column count has reached four.
Lane 0 invalid code	18	0b	0b = Indicates no invalid code was detected (latch high). 1b = Indicates an invalid code was detected for that lane.
Lane 1 invalid code	19	0b	0b = Indicates no invalid code was detected (latch high). 1b = Indicates an invalid code was detected for that lane.
Lane 2 invalid code	20	0b	0b = Indicates no invalid code was detected (latch high). 1b = Indicates an invalid code was detected for that lane.
Lane 3 invalid code	21	0b	0b = Indicates no invalid code was detected (latch high). 1b = Indicates an invalid code was detected for that lane.
Lane 0 comma count4	22	0b	0b = Indicates the comma count for that lane is less than four (latch high). 1b = Indicates the comma count for that lane has reached four.
Lane 1 comma count 4	23	0b	0b = Indicates the comma count for that lane is less than four (latch high). 1b = Indicates the comma count for that lane has reached four.
Lane 2 comma count 4	24	0b	0b = Indicates the comma count for that lane is less than four (latch high). 1b = Indicates the comma count for that lane has reached four.
Lane 3 comma count 4	25	0b	0b = Indicates the comma count for that lane is less than four (latch high). 1b = Indicates the comma count for that lane has reached four.
Lane 0 Signal Detect	26	0b	0b = Indicates noise, no signal is detected. 1b = Indicates a signal is detected.
Lane 1 Signal Detect	27	0b	0b = Indicates noise, no signal is detected. 1b = Indicates a signal is detected.
Lane 2 Signal Detect	28	0b	0b = Indicates noise, no signal is detected. 1b = Indicates a signal is detected.
Lane 3 Signal Detect	29	0b	0b = Indicates noise, no signal is detected. 1b = Indicates a signal is detected.
Reserved	31:30	0b	Reserved.

8.2.3.22.17 SerDes Interface Control Register — SERDESC (0x04298; RW)

Field	Bit(s)	Init Val	Description
Tx_lanes_polarity	3:0	0*	Bit 3 = Changes bits polarity of MAC Tx lane 3. Bit 2 = Changes bits polarity of MAC Tx lane 2. Bit 1 = Changes bits polarity of MAC Tx lane 1. Bit 0 = Changes bits polarity of MAC Tx lane 0. Changes bits polarity if set to 1b.
Rx_lanes_polarity	7:4	0*	Bit 7 = Changes bits polarity of MAC Rx lane 3. Bit 6 = Changes bits polarity of MAC Rx lane 2. Bit 5 = Changes bits polarity of MAC Rx lane 1. Bit 4 = Changes bits polarity of MAC Rx lane 0. Changes bits polarity if set to 1b.
swizzle_tx_lanes	11:8	0*	Bit 11 = Swizzles bits of MAC Tx lane 3. Bit 10 = Swizzles bits of MAC Tx lane 2. Bit 9 = Swizzles bits of MAC Tx lane 1. Bit 8 = Swizzles bits of MAC Tx lane 0. Swizzles bits if set to 1b. These bits are for debug only – software should not change the default EEPROM value.
swizzle_rx_lanes	15:12	0*	Bit 15 = Swizzles bits of MAC Rx lane 3. Bit 14 = Swizzles bits of MAC Rx lane 2. Bit 13 = Swizzles bits of MAC Rx lane 1. Bit 12 = Swizzles bits of MAC Rx lane 0. Swizzles bits if set to 1b. These bits are for debug only – software should not change the default EEPROM value.
swap_tx_lane_3	17:16	11b*	Determines Core destination Tx lane for MAC Tx lane 3.
swap_tx_lane_2	19:18	10b*	Determines Core destination Tx lane for MAC Tx lane 2.
swap_tx_lane_1	21:20	01b*	Determines Core destination Tx lane for MAC Tx lane 1.
swap_tx_lane_0	23:22	00b*	Determines Core destination Tx lane for MAC tx lane 0. 00b = MAC Tx lane 0 to Core Tx lane 0. 01b = MAC Tx lane 0 to Core Tx lane 1. 10b = MAC Tx lane 0 to Core Tx lane 2. 11b = MAC Tx lane 0 to Core Tx lane 3.
swap_rx_lane_3	25:24	11b*	Determines which Core lane is mapped to MAC Rx lane 3.
swap_rx_lane_2	27:26	10b*	Determines which Core lane is mapped to MAC Rx lane 2.



Field	Bit(s)	Init Val	Description
swap_rx_lane_1	29:28	01b*	Determines which Core lane is mapped to MAC Rx lane 1.
swap_rx_lane_0	31:30	00b*	Determines which Core lane is mapped to MAC Rx lane 0. 00b = Core Rx lane 0 to MAC Rx lane 0. 01b = Core Rx lane 1 to MAC Rx lane 0. 10b = Core Rx lane 2 to MAC Rx lane 0. 11b = Core Rx lane 3 to MAC Rx lane 0.

* Also programmable via EEPROM.

8.2.3.22.18 FIFO Status/CNTL Report Register — MACS (0x0429C; RW)

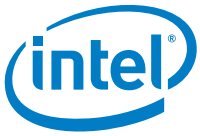
This register reports FIFO status in xgmii_mux.

Field	Bit(s)	Init Val	Description
XGXS SYNC Fix Disable	0	0b	Use shift-fsm control for the XGXS sync process. 0b = Normal functionality (default). 1b = Use shift-fsm control, disable fix (debug only).
XGMII-GMII Tx END Fix Disable	1	0b	Disable tx_end on link-down. 0b = Normal functionality, link down causes tx_end (default). 1b = Disable tx_end on link-down (debug only).
XGXS Deskew Fix Disable	2	0b	Disable align on invalid fix. 0b = Normal functionality (default). 1b = Disable align on invalid fix (debug only).
Nonce Match Disable	3	0b	Disable nonce match. 0b = Normal functionality (default). 1b = Disable nonce match (debug only).
Reserved	15:4	0x0	Reserved. On a write access to this field the SW should maintain the value of this field.
Config fault length	23:16	0x1F	Sets the length in clock cycles of LF stream.
Config FIFO threshold	27:24	0x6	Determines threshold for asynchronous FIFO (generation of data_available signal is determined by cfg_fifo_th[3:0]).
tx FIFO underrun	28	0b	Indicates FIFO under run in xgmii_mux_tx_fifo.
tx FIFO overrun	29	0b	Indicates FIFO overrun in xgmii_mux_tx_fifo.
rx FIFO underrun	30	0b	Indicates FIFO under run in xgmii_mux_rx_fifo.
rx FIFO overrun	31	0b	Indicates FIFO overrun in xgmii_mux_rx_fifo.

8.2.3.22.19 Auto Negotiation Control Register — AUTOC (0x042A0; RW)

Note: The 82599 Device Firmware may access AUTOC register in parallel to software driver and a synchronization between them is needed. For more information see Section 10.5.4.

Field	Bit(s)	Init Val	Description
FLU	0	0b	Force Link Up. 0b = Normal mode. 1b = MAC forced to link_up. Link is active in the speed configured in AUTOC.LMS. This setting forces the auto-negotiation arbitration state machine to AN_GOOD and sets the link_up indication regardless of the XGXS/ PCS_1G status.
ANACK2	1	0b*	Auto-Negotiation Ack2 field. This value is transmitted in the *Achnowledge2* field of the null next page that is transmitted during a next page handshake.
ANSF	6:2	00001b*	Auto-Negotiation Selector Field. This value will be used as the Selector Field in the Link Control Word during Clause 73 Backplane Auto–Negotiation process. (Default value set according to 802.3ap-2007).
10G_PMA_PMD_PARALLEL	8:7	01b*	Define 10 GbE PMA/PMD over four differential pairs (Tx and Rx each). 00b = XAUI PMA/PMD. 01 = KX4 PMA/PMD. 10 = CX4 PMA/PMD. 11 = Reserved.
1G_PMA_PMD	9	1b*	PMA/PMD used for 1 GbE. 0b = SFI PMA/PMD (the AUTOC.LMS should be set to 000b). 1b = KX or BX PMA/PMD.
D10GMP	10	0b*	Disables 10 GbE Parallel Detect on Dx (Dr/D3) without main–power. 0b = No specific action. 1b = Disables 10 GbE Parallel Detect when main power is removed. This bit is valid only if RATD is set. *Note:* If MNG_VETO bit is set, any low-power link mode changes will be hold off.
RATD	11	0b*	Restarts auto-negotiation on transition to Dx. This bit enables the functionality to restart KX/KX4/KR backplane auto-negotiation on transition to Dx (Dr/D3), targeting an 1GbE link. 0b = Does not restart auto-negotiation when the 82599 moves to the Dx state. 1b = Restarts auto-negotiation to reach a low–power link mode (1 GbE link) when the 82599 transitions to the Dx state. Only 1GbE will be advertised by auto-negotiation. In this case, if a partner doesn't have 1GbE capabilities, a link will not be established. 10GbE can still be achieved by Parallel Detect of a XAUI partner if D10GMP bit is clear. *Note:* If MNG_VETO bit is set, any low-power link mode changes will be hold off.



Field	Bit(s)	Init Val	Description
Restart_AN	12	0b*	Applies new link settings and restarts relative auto-negotiation process (self–clearing bit). 0b = No action needed. 1b = Applies new link settings and restarts auto-negotiation. *Note:* This bit must be set to make any new link settings affective as indicated in Section 3.7.4.2.
LMS	15:13	100b*	Link Mode Select. Selects the active link mode: 000b = 1 GbE link (no backplane auto-negotiation). 001b = 10 GbE parallel link (KX4 – no backplane auto-negotiation). 010b = 1 GbE link with clause 37 auto-negotiation enable (BX interface). 011b = 10 GbE serial link (SFI – no backplane auto-negotiation). 100b = KX/KX4/KR backplane auto-negotiation enable. 1 GbE (Clause 37) auto-negotiation disabled. 101b = SGMII 100M/1 GbE link. 110b = KX/KX4/KR backplane auto-negotiation enable. 1 GbE (Clause 37) auto-negotiation enable. 111b = KX/KX4/KR auto-negotiation enable. SGMII 100 Mb/s and 1GbE (in KX) enable.
KR_support	16	1b*	Configures the *A2* bit of the *Technology Ability Field* in the auto-negotiation word while *A0:A1* fields are configured in the KX_support field (bits 31:30): 0b = KR not supported. Value is Illegal if KX and KX4 are also not supported (AUTOC.KX_support – 00b). 1b = KR supported. *Note:* This bit is not relevant to the parallel detect process.
FECR	17	0b*	FEC Requested. Configures the *F1* bit in the backplane auto-negotiation base link code word. Should be set to 1b only if KR ability is set to 1b (AUTOC.KR = 1b). 0b = FEC not requested from link partner. 1b = FEC requested from link partner.
FECA	18	1b*	FEC Ability. Configures the *F0* bit in the backplane auto-negotiation base link code word. Should be set to 1b only if KR ability is set to 1b (AUTOC.KR = 1b). 0b = FEC not supported. 1b = FEC supported.
ANRXAT	22:19	0011b*	Backplane Auto-Negotiation Rx Align Threshold. Sets threshold to determine alignment is stable.
ANRXDM	23	1b*	Auto-Negotiation Rx Drift Mode. Enables following the drift caused by PPM in the Rx data. 0b = Disables drift mode. 1b = Enables drift mode.
ANRXLM	24	1b*	Auto-Negotiation Rx Loose Mode. Enables less restricted functionality (allow 9/11 bit symbols). 0b = Disables loose mode. 1b = Enables loose mode.

Field	Bit(s)	Init Val	Description
ANPDT	26:25	00b*	Auto-Negotiation Parallel Detect Timer. Configures the parallel detect counters. 00b = 1 ms 01b = 2 ms 10b = 5 ms 11b = 8 ms
RF	27	0b*	This bit is loaded to the RF of the auto-negotiation word.
PB	29:28	00b*	Pause Bits. The value of these bits is loaded to bits D11–D10 of the Link code word (pause data). Bit 29 is loaded to D11.
KX_support	31:30	11b*	Configures the A0:A1 bits of the *Technology Ability Field* of the backplane auto-negotiation word while A2 field is configured in the KR_support bit (bit 16): 00b= A0 – 0; A1 – 0. KX not supported. KX4 not supported. Value is Illegal if KR is also not supported (AUTOC.KR_support – 0b). 01b = A0 – 1; A1 – 0. KX supported. KX4 not supported. 10b = A0 – 0; A1 – 1. KX not supported. KX4 supported. 11b = A0 – 1; A1 – 1. KX supported. KX4 supported.

* Also programmable via EEPROM.

8.2.3.22.20 Link Status Register — LINKS (0x042A4; RO)

Field	Bit(s)	Init Val	Description
KX_SIG_DET	0	0b	Signal Detect of 1 GbE and 100 Mb/s. 0b = A signal is not present (Fail). 1b = A signal is present (OK).
FEC_SIG_DET	1	0b	Signal detect of FEC 0b = FEC reports signal not detected (failed). 1b = FEC reports signal detected (good).
FEC_BLOCK_LOCK	2	0b	10 GbE serial PCS FEC block lock. 0b = No FEC block lock. 1b = FEC reached block lock.
KR_HI_BERR	3	0b	10GbE serial KR_PCS high error rate (greater than 10^{-4}). 0b = Low BERR. 1b = High BERR.
KR_PCS_BLOCK_LOCK	4	0b	10 GbE serial PCS block lock. 0b = No KR_PCS block lock. 1b = KR_PCS reached block lock.
KX/KX4/KR Backplane AN Next Page received	5	0b	KX/KX4/KR AN Next Page Received. A new link partner next page was received during the backplane auto-negotiation process. Latch high, clear on read.