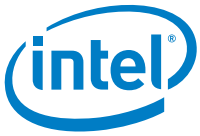
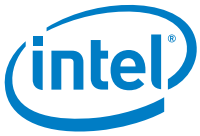


Field	Bit(s)	Init Val	Description
KX/KX4/KR Backplane AN Page received	6	0b	KX/KX4/KR Backplane Auto Negotiation Page Received. A new link partner page was received during the auto-negotiation process. Latch high, clear on read.
Link Status	7	0b	0b = Link is currently down or link was down since last time read. 1b = Link is Up and there was no link down from last time read. Self cleared upon read if the link is low and set if the link is up.
KX4_SIG_DET	11:8		Signal Detect of 10 GbE Parallel (KX4, CX4 or XAUI). Bit[11, 10, 9, 8] shows lane <3,2,1,0> status, respectively. For each bit: 0b = A signal is not present (failed). 1b = A signal is present (good).
KR_SIG_DET	12		Signal Detect of 10 GbE serial (KR or SFI). 0b = Signal not detected (failed). 1b = Signal detected (good).
10G lane sync_status	16:13		10G Parallel lane sync status. bit[16,15,14,13] show lane <3,2,1,0> status accordingly. per each bit: 0b = sync_status is FAILED (not synchronized to code-group). 1b = sync_status is OK (synchronized to code-group).
10G Align Status	17		10 GbE align_status. 0b = Align_status failed (deskew process not complete). 1b = Align_status good (all lanes are synchronized and aligned).
1G Sync Status	18		1G sync_status. 0b = Sync_status failed (not synchronized to code-group). 1b = Sync_status is good (synchronized to code-group).
KX/KX4/KR Backplane AN Receiver Idle	19		KX/KX4/KR Backplane Auto Negotiation Rx Idle. 0b = Receiver good. 1b = Receiver is in idle-waiting to align and sync on DME.
1G AN enabled (clause 37 AN)	20		PCS_1 GbE auto-negotiation is enabled (clause 37).
1G link Enabled PCS_1G	21		1 GbE PCS enabled for 1 GbE and SGMII operation.
10G link Enabled (XGXS)	22		XGXS Enabled for 10 GbE operation.
FEC_EN	23		Status of forward–error–correction in 10 GbE serial link (KR operating mode). 0b = FEC disabled. 1b = FEC enabled.
10G_SER_EN	24		Status of 10 GbE serial PCS (KR PCS) for KR or SFI operation. 0b = KR PCS disabled. 1b = KR PCS enabled.
SGMII_EN	25		Status of SGMII operation. 0b = SGMII disabled. 1b = SGMII enabled.

Field	Bit(s)	Init Val	Description
MLINK_MODE	27:26		MAC link mode status. 00b = 1 GbE 01b = 10 GbE parallel 10b = 10 GbE serial 11b = Auto-negotiation
LINK_SPEED	29:28		MAC link speed status. 00b = Reserved 01b = 100 Mb/s 10b = 1 GbE 11b = 10 GbE
Link Up	30	0b	link up 0b = Link is down. 1b = Link is up.
KX/KX4/KR Backplane AN Completed	31	0b	Indicates KX/KX4/KR backplane auto-negotiation has completed successfully.

8.2.3.22.21 Link Status Register 2 — LINKS2 (0x04324; RO)

Field	Bit(s)	Init Val	Description
MAC Rx Link Mode	1:0	00b	MAC link mode in the Core Rx path. 00b = 1 GbE 01b = 10 GbE parallel 10b = 10GbE serial 11b = Auto-negotiation
Reserved	2	0b	Reserved.
MAC Tx Link Mode	4:3	00b	MAC link mode in the Core Tx path. 00b = 1 GbE 01b = 10 GbE parallel 10b = 10GbE serial 11b = Auto-negotiation
Reserved	5	0b	Reserved.
Link-Partner AN	6	0b	Link Partner KX/KX4/KR Backplane Auto-Negotiation Ability. 0b = Link partner is not KX/KX4/KR backplane auto-negotiation capable. 1b = Link partner is KX/KX4/KR backplane auto-negotiation capable.
Reserved	31:7	0x0	Reserved.



8.2.3.22.22 Auto Negotiation Control 2 Register — AUTOC2 (0x042A8; RW)

Field	Bit(s)	Init Val	Description
Reserved	15:0	0b	Reserved.
10G_PMA_PMD_Serial	17:16	00b*	PMAPMD used for 10 GbE serial link operation: 00b = KR 01b = Reserved 10b = SFI 11b = Reserved
DDPT	18	0*	Disable DME Pages Transmit. Setting this bit disables the DME pages transmitting while the device in auto–negotiation mode (it transmits 0bs instead).
Reserved	27:19	0b	Reserved
FASM	28	0b	Force the auto-negotiation arbitration state machine to idle 0b = No Force (normal operation). 1b = Force state and keep constant forced state
Reserved	29	0b	Reserved.
PDD	30	0b*	Disable the parallel detect part in the KX/KX4/KR backplane auto-negotiation. When set to 1b the auto-negotiation process avoids any parallel detect activity, and relies only on the DME pages received and transmitted. 0b = Enable the parallel detect (normal operation). 1b = Disable the parallel detect (debug only).
Reserved	31	0b	Reserved.

* Loaded from the AUTOC2 word in the MAC EEPROM section

8.2.3.22.23 Auto Negotiation Link Partner Link Control Word 1 Register — ANLP1 (0x042B0; RO)

Field	Bit(s)	Init Val	Description
LP AN page D low	15:0	0x0	LP auto-negotiation advertisement page fields D[15:0]. [15] = NP [14] = Acknowledge [13] = RF [12] = Reserved [11:10] = Pause [9:5] = Echoed Nonce field [4:0] = Selector field
ANAS	19:16	0x0	Auto-Negotiation state machine status. If zero, it indicates that state machine is in idle state.
Reserved	31:20	0x0	Reserved.

To ensure that software has the ability to read the same Link Partner Link Control Word (located across two registers), once ANLP1 is read, ANLP2 is locked until the ANLP2 register is read. ANLP2 does not hold valid data before ANLP1 is read.

8.2.3.22.24 Auto Negotiation Link Partner Link Control Word 2 Register — ANLP2 (0x042B4; RO)

Field	Bit(s)	Init Val	Description
LP Transmitted Nonce Field	4:0	0x0	LP auto-negotiation advertisement page fields T[4:0].
LP Technology Ability Field Low	15:5	0x0	LP auto-negotiation advertisement page fields A[10:0].
LP Technology Ability Field High	31:16	0x0	LP auto-negotiation advertisement page fields A[26:11].

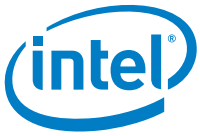
To ensure that software has the ability to read the same Link Partner Link Control Word (located across two registers), once ANLP1 is read, ANLP2 is locked until the ANLP2 register is read. ANLP2 does not hold valid data before ANLP1 is read.

8.2.3.22.25 MAC Manageability Control Register — MMNGC (0x042D0; Host-RO/MNG-RW)

Field	Bit(s)	Init Val	Description
MNG_VETO	0	0b	MNG_VETO (default 0b). Access read/write by manageability, read only to the host. 0b = No specific constraints on link from manageability. 1b = Hold off any low-power link mode changes. This is done to avoid link loss and interrupting manageability activity.
Reserved	31:1	0x0	Reserved.

8.2.3.22.26 Auto Negotiation Link Partner Next Page 1 Register — ANLPNP1 (0x042D4; RO)

Field	Bit(s)	Init Val	Description
LP AN Next Page Low	31:0	0x0	LP Auto-Negotiation Next Page Fields D[31:0]. [31:16] = Unformatted Code [15] = NP [14] = Acknowledge [13] = MP [12] = Acknowledge2 [11] = Toggle [10:0] = Message/Unformatted Code



To ensure that software has the ability to read the same Link Partner Link Control Word (located across two registers), once ANLP1 is read, ANLP2 is locked until the ANLP2 register is read. ANLP2 does not hold valid data before ANLP1 is read.

8.2.3.22.27 Auto Negotiation Link Partner Next Page 2 Register — ANLPNP2 (0x042D8; RO)

Field	Bit(s)	Init Val	Description
LP AN Next Page high	15:0	0x0	LP AN Next Page Fields D[47:32]. [15:0] = Unformatted Code.
Reserved	31:16	0x0	Reserved.

To ensure that software has the ability to read the same Link Partner Link Control Word (located across two registers), once ANLPNP1 is read, ANLPNP2 is locked until the ANLPNP2 register is read. ANLPNP2 does not hold valid data before ANLPNP1 is read.

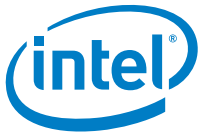
8.2.3.22.28 KR PCS and FEC Control Register — KRPCSFC (0x042EO; RW)

Field	Bit(s)	Init Val	Description
Reserved	10:0	0x0	Reserved. Bits should be written as 0x0 and ignored on read.
Reserved	15:11	0x0	Reserved.
FEC_ENABLE_ERR	16	1b	FEC Enable Error Indication to KR-PCS. 0b = Disabled. 1b = The FEC decoder indicates error to the KR-PCS by means of setting both sync bits to the value 11 in the 1st, 9th, 17th, 25th, and 32nd of the 32 decoded 64b/66b blocks from the corresponding erred FEC block.
Reserved	17	0b	Reserved.
FEC_N_CNT	19:18	00b	Good Parity Block Count. Indicates the number of good parity blocks required for block lock. 00b = 4 good blocks 01b = 2 good blocks 10b = 5 good blocks 11b = 7 good blocks
FEC_M_CNT	21:20	00b	Bad Parity Block Count. Indicates the number of bad parity blocks required for loss of block lock. 00b = 8 errors 01b = 4 errors 10b = 12 errors 11b =-15 errors
FEC_LOOSE_MODE	22	0b	Enables FEC Loose Mode 0b = All errors counted. 1b = Correctable errors are not counted.

Field	Bit(s)	Init Val	Description
FEC_RX_SWAP	23	0b	FEC Rx Bit Order Swap. Swaps the bit order of the FEC_RX inputs. Swaps both *din* and sync_in bit order.
FEC_TX_SWAP	24	0b	FEC Tx Bit Order Swap. Swaps the bit order of the FEC_TX inputs. Swaps both *din* and *sync_in* bit order.
Reserved	25	0b	Reserved.
SLIPASS	26	0b	Loss of Sync (frame_align) Idle Pass-Through Select. 0b = LF passed to XGMII output when loss of sync. 1b = Decoder output data passed to XGMII output when loss of sync.
SSYNC	27	0b	Rx Block Lock Override. Once block lock sync has been acquired on the Rx input, Rx input remains in block lock sync regardless of Rx input data.
Reserved	28	0b	Reserved.
Reserved	31:29	0x0	Reserved.

8.2.3.22.29 KR PCS Status Register — KRPCSS (0x042E4; RO)

Field	Bit(s)	Init Val	Description
Reserved	2:0	0x0	Reserved. Write 0 ignore read.
ERRCNT_BLK	10:3	0x0	Rx Decoder Error Counter. This counter does not rollover and holds its value until it is read if it reaches its maximum value. This count is cleared when this register is read.
BERBAD_CNTR	16:11	0x0	BER Bad Counter (count cleared on register read) Field indicates number of times BER_BAD state was entered.
RX_FIFO_ERR_LH	17	0b	Elastic Buffer Error (latched high, clear on read). 0b = No Rx elastic buffer overflow or underflow condition since last read. 1b = Indicates that Rx elastic buffer overflow or underflow condition occurred since last read.
RX_LF_DET	18	0b	RX_LF Detect (latched high, clear on read). 0b = No local fault message was detected in the Rx path since last read. 1b = Indicates that the local fault message was detected in the Rx path since last read.
RX_FRM_ALIGN_ERR	19	0b	Frame Align Error (latched high, clear on read). 0b = No hi_ber or miss of frame_lock occurred since last read. 1b = Indicates that the hi_ber or miss of frame_lock occurred since last time the register was read.
BLKLCK	20	0b	Rx Block Lock Status bit (latched low, set on read). 0b = Link lost block lock since last register read. 1b = Indicates that the link has remained in the block lock state since the last read of this register.



Field	Bit(s)	Init Val	Description
HBER_STS	21	0b	Rx High Bit Error Rate Status bit (latched high, clear on read). 0b = Link has not been in high BER state since previous read. 1b = Indicates that the link has been in the high BER state since the last time the register was read.
RX_LF_DET	22	0b	RX_LF Detect (latched high, clear on read). 0b = No local fault message was detected in the Rx path. 1b = Indicates that the local fault message was detected in the Rx path.
LNK_STS	23	0b	Rx Link Status (latched low, set on read). 0b = Indicates that the link has been lost since the last time the bit was read. 1b = No loss of link since last time bit was read.
RX_UNDERFLOW	24	0b	Rx Underflow Status (latched high, clear on read). 0b = No underflow condition in rx_fifo. 1b = Indicates that the rx_fifo has reached the underflow condition and data might have been lost/corrupted.
RX_OVERFLOW	25	0b	Rx Overflow Status (latched high, clear on read). 0b = No overflow condition in rx_fifo. 1b = Indicates that the rx_fifo has reached the overflow condition and data might have been lost or corrupted.
RX_FIFO_ERR	26	0b	Rx Elastic Buffer Error 0b = No elastic buffer error. 1b = Indicates that Rx elastic buffer is currently in the overflow or underflow condition. This bit is not latched and is asserted only when the FIFO is in the overflow or underflow condition.
RX_DATA_VALID	27	1b	Data Valid Status (latched low, set on read). This bit indicates that the rx_fifo has not experienced an overflow or underflow since the last time this register was read.
TX_UNDERFLOW	28	0b	Tx Underflow Status (latched high, clear on read). This bit indicates that the tx_fifo has reached the underflow condition and data might have been lost/corrupted.
TX_OVERFLOW	29	0b	Tx Overflow Status (latched high, clear on read). This bit indicates that the tx_fifo has reached the overflow condition and data might have been lost/corrupted.
TX_FIFO_ERR	30	0b	Unlatched FIFO Error Status. This bit indicates that the tx_fifo has reached the overflow or underflow condition and data might have been lost / corrupted. This bit is not latched and is only asserted while the FIFO is in the overflow or underflow condition.
TX_DATA_VALID	31	1b	Data Valid Status (latched low, set on read). 0b = tx_fifo has experienced an overflow or underflow since the last time this register was read. 1b = tx_fifo has not experienced an overflow or underflow since the last time this register was read.

8.2.3.22.30 FEC Status 1 Register — FECS1 (0x042E8; RC)

Field	Bit(s)	Init Val	Description
FEC_CR_OUT	31:0	0x0	FEC Correctable Error Counter. The FECS1 counts the correctable FEC data blocks, detected and corrected by the FEC Rx logic.

8.2.3.22.31 FEC Status 2 Register — FECS2 (0x042EC; RC)

Field	Bit(s)	Init Val	Description
FEC_UNCR_OUT	31:0	0x0	FEC Uncorrectable Error Counter. The FECS2 counts the bad uncorrectable FEC data blocks, detected by the FEC Rx logic.

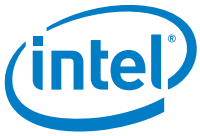
8.2.3.22.32 Core Analog Configuration Register — CoreCTL (0x014F00; RW)

Field	Bit(s)	Init Val	Description
Data	7:0	0x0	Data to Core Analog Registers. Data is ignored when bit 16 is set.
Address	15:8	0x0	Address to Core Analog Registers.
Latch address	16	0b	0b = Normal write operation. 1b = Latch this address for the next read transaction. Data is ignored and is not written on this transaction.
Reserved	31:17	0x0	Reserved.

Reading the Core registers must be done in two steps:

1. Send a Write command with bit 16 set, and the desired reading offset in the *Address* field (bits [15:8]).
2. Send a Read command to CoreCTL. The returned data is from the indirect address in the Core register space, which was provided in step (1).

To configure (write) registers in the Core block, the driver should write the proper address to CoreCTL.Address and data written to CoreCTL.Data.



8.2.3.22.33 Core Common Configuration Register — SMADARCTL (0x014F10; RW)

Field	Bit(s)	Init Val	Description
Data	7:0	0b	Data to Core Analog Registers. Data is ignored when bit 16 is set.
Address	15:8	0x0	Address to Core Analog Registers.
Latch address	16	0b	0b = Normal write operation. 1b = Latch this address for the next read transaction. Data is ignored and is not written on this transaction.
Reserved	31:17	0x0	Reserved.

Reading the Smadar registers must be done in two steps:

1. Send a Write command with bit 16 set, and the desired reading offset in the *Address* field (bits [15:8]).
2. Send a Read command to SMADARCTL. The returned data is from the indirect address in the Core register space, which was provided in step (1).

To configure (write) registers in the Smadar block, the driver should write the proper address to SMADARCTL.Address and data written to SMADARCTL.Data.

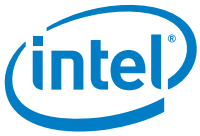
8.2.3.22.34 MAC Flow Control Register — MFLCN (0x04294; RW)

Field	Bit(s)	Init Val	Description
PMCF	0	0b	Pass MAC Control Frames. Filter out unrecognizable pause (flow control opcode doesn't match) and other control frames. 0b = Filter unrecognizable pause frames. 1b = Pass/forward unrecognizable pause frames.
DPF	1	0b	Discard Pause Frame When set to 0b, pause frames are sent to the host. Setting this bit to 1b causes pause frames to be discarded only when *RFCE* or *RPFCE* are set to 1b. If both *RFCE* and *RPFCE* are set to 0b, this bit has no effect on incoming pause frames.
RPFCE	2	0b	Receive Priority Flow Control Enable**.** Indicates that the 82599 responds to receiving PFC packets. If auto-negotiation is enabled, this bit should be set by software to the negotiated flow control value. *Note:* PFC should be enabled in DCB mode only. *Note:* Receive PFC and receive link flow control are mutually exclusive and programmers should not configure both of them to be enabled at the same time. *Note:* This bit should not be set if bit 3 is set.

Field	Bit(s)	Init Val	Description
RFCE	3	0b	Receive Flow Control Enable Indicates that the 82599 responds to the reception of link flow control packets. If auto-negotiation is enabled, this bit should be set by software to the negotiated flow control value. *Note:* This bit should not be set if bit 2 is set.
Reserved	31:4	0x0	Reserved.

8.2.3.22.35 SGMII Control Register — SGMIIC (0x04314; RW)

Field	Bit(s)	Init Val	Description
SRXRASSMP	3:0	0x0	Shift Rx Rate-Adapt Single Data Sampling. This value determines the sampling point of the sampled received data in the fast domain by the fast clock relative to the slow clock.
SRXRARSMP	7:4	0x0	Shift Rx Rate-Adapt Replicated Data Sampling. This value determines the sampling point of the received replicated data in the fast domain by the fast clock.
STXRASMP	11:8	0x0	Shift Tx Rate-Adapt Sampling. This value determines the sampling point of the transmitted data in the slow domain by the fast clock.
ANSFLU100	12	0b	AN SGMII Force Link Up 100 Mb/s. 0b = Normal mode. 1b = PGS_1G forced to 100 Mb/s link. This setting forces the PCS_1G Link_Ok indication and forced the 100 Mb/s speed indication toward the auto-negotiation ARB state machine regardless of the PCS_1G status.
ANSBYP	13	0b	AN SGMII Bypass. I f this bit is set, the IDLE detect state is bypassed during auto-negotiation (Clause 37) in SGMII mode. This reduces the acknowledge time in SGMII mode.
ANSTRIG	14	0b	AN SGMII Trigger. If this bit is set, auto-negotiation (Clause 37) is not automatically triggered in SGMII mode even if SYNC fails. Auto-negotiation is triggered only in response to PHY messages or by a manual setting like changing auto-negotiation *Enable*/*Restart* bits.
ANSLNKTMR	15	0b	AN SGMII Link-Timer (Configure the SGMII Link Timer). 0b = 1.6 ms 1b = 3.2 ms
Reserved	16	0b	Reserved.
ANIGNRRXRF	17	0b	Auto-Negotiation Ignore Received RF Field. 0b = If the received page contains RF != 00b, don't set link_up indication. 1b = Ignore from the received RF field content.
Reserved	31:18	0x0	Reserved.



8.2.3.23 Statistic Registers

General notes:

- All statistics registers are cleared on read. In addition, they stick at 0xFF...F when the maximum value is reached.
- For the receive statistics it should be noted that a packet is indicated as received if it passes the device filters and is placed into the packet buffer memory. A packet does not have to be DMA'd to host memory in order to be counted as received.
- Due to divergent paths between interrupt-generation and logging of relevant statistics counts, it might be possible to generate an interrupt to the system for a noteworthy event prior to the associated statistics count actually being incremented. This is extremely unlikely due to expected delays associated with the system interrupt-collection and ISR delay, but might be an explanation for interrupt statistics values that do not quite make sense. Hardware guarantees that any event noteworthy of inclusion in a statistics count is reflected in the appropriate count within 1 µs; a small time-delay prior to reading the statistics is required to avoid a potential mismatch between an interrupt and its cause.
- If RSC is enabled, statistics are collected before RSC is applied to the packets.
- If TSO is enabled, statistics are collected after segmentation.
- All byte (octet) counters composed of two registers can be fetched by two consecutive 32-bit accesses while reading the low 32-bit register first or a single 64-bit access.
- All receive statistic counters count the packets and bytes before coalescing by the RSC logic or FCoE DDP logic.
- All receive statistic counters in the filter unit (listed as follows) include also packets that might be dropped by the packet buffer or receive DMA. Same comment is valid for the byte counters associated with these packet counters: PRC64, PRC127, PRC255, PRC511, PRC1023, PRC1522, BPRC, MPRC, GPRC, RXNFGPC, RUC and ROC

8.2.3.23.1 CRC Error Count — CRCERRS (0x04000; RC)

Field	Bit(s)	Init Val	Description
CEC	31:0	0x0	CRC Error Count. Counts the number of receive packets with CRC errors. In order for a packet to be counted in this register, it must be 64 bytes or greater (from <Destination Address> through <CRC>, inclusively) in length. This register counts all packets received, regardless of L2 filtering and receive enablement.

8.2.3.23.2 Illegal Byte Error Count — ILLERRC (0x04004; RC)

Field	Bit(s)	Init Val	Description
IBEC	31:0	0x0	Illegal Byte Error Count. Counts the number of receive packets with illegal bytes errors (such as there is an illegal symbol in the packet). This registers counts all packets received, regardless of L2 filtering and receive enablement.

8.2.3.23.3 Error Byte Packet Count — ERRBC (0x04008; RC)

Field	Bit(s)	Init Val	Description
EBC	31:0	0x0	Error Byte Count. Counts the number of receive packets with error bytes (such as there is an error symbol in the packet). This registers counts all packets received, regardless of L2 filtering and receive enablement.

8.2.3.23.4 Rx Missed Packets Count — RXMPC[n] (0x03FA0 + 4*n, n=0...7; RC) DBU-Rx

Note: This is a RO register only.

8.2.3.23.5 MAC Local Fault Count — MLFC (0x04034; RC)

Field	Bit(s)	Init Val	Description
MLFC	31:0	0x0	Number of faults in the local MAC. This register is valid only when the link speed is 10 Gb/s.

8.2.3.23.6 MAC Remote Fault Count — MRFC (0x04038; RC)

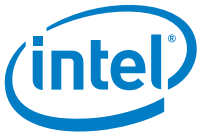
Field	Bit(s)	Init Val	Description
MRFC	31:0	0x0	Number of faults in the remote MAC. This register is valid only when the link speed is 10 Gb/s.

8.2.3.23.7 Receive Length Error Count — RLEC (0x04040; RC)

Field	Bit(s)	Init Val	Description
RLEC	31:0	0x0	Number of packets with receive length errors. A length error occurs if an incoming packet length field in the MAC header doesn't match the packet length. To enable the receive length error count, the HLREG.RXLNGTHERREN bit needs to be set to 1b. This registers counts all packets received, regardless of L2 filtering and receive enablement.

8.2.3.23.8 Switch Security Violation Packet Count — SSVPC (0x08780; RC)

Field	Bit(s)	Init Val	Description
SSVPC	31:0	0x0	Switch Security Violation Packet Count. This register counts Tx packets dropped due to switch security violations such as SA or VLAN anti-spoof filtering or a packet that has (inner) VLAN that contradicts with PFVMVIR register definitions. Valid only in VMDq or IOV mode.



8.2.3.23.9 Link XON Transmitted Count — LXONTXC (0x03F60; RC)

Note: This is a RO register only.

8.2.3.23.10 Link XON Received Count — LXONRXCNT (0x041A4; RC)

Note: This counter is similar to LXONRXC in the 82598 that was in address 0x0CF60.

Field	Bit(s)	Init Val	Description
XONRXC	15:0	0	Number of XON packets received. Sticks to 0xFFFF. XON packets can use the global address, or the station address. This register counts any XON packet whether it is a legacy XON or a priority XON. Each XON packet is counted once even if it is designated to a few priorities. If a priority FC packet contains both XOFF and XON, only the LXOFFRXCNT counter is incremented.
Reserved	31:16	0	Reserved.

8.2.3.23.11 Link XOFF Transmitted Count — LXOFFTXC (0x03F68; RC)

Note: This is a RO register only.

8.2.3.23.12 Link XOFF Received Count — LXOFFRXCNT (0x041A8; RC)

Note: This counter is similar to LXOFFRXC in the 82598 that was in address 0x0CF68.

Field	Bit(s)	Init Val	Description
XOFFRXC	15:0	0x0	Number of XOFF packets received. Sticks to 0xFFFF. XOFF packets can use the global address or the station address. This register counts any XOFF packet whether it is a legacy XOFF or a priority XOFF. Each XOFF packet is counted once even if it is designated to a few priorities. If a priority FC packet contains both XOFF and XON, only this counter is incremented.
Reserved	31:16	0x0	Reserved.

8.2.3.23.13 Priority XON Transmitted Count — PXONTXC[n] (0x03F00 + 4*n, n=0...7; RC)

Note: This is a RO register only.

8.2.3.23.14 Priority XON Received Count — PXONRXCNT[n] (0x04140 + 4*n, n=0...7; RC)

Note: These counters are similar to PXONRXC[n] in the 82598 that were in address 0x0CF00 + 4*n, n=0...7.

Field	Bit(s)	Init Val	Description
XONRXC	15:0	0x0	Number of XON packets received per UP. Sticks to 0xFFFF.
Reserved	31:16	0x0	Reserved.

8.2.3.23.15 Priority XOFF Transmitted Count — PXOFFTXCNT[n] (0x03F20 + 4*n, n=0...7; RC)

Note: This is a RO register only.

8.2.3.23.16 Priority XOFF Received Count — PXOFFRXCNT[n] (0x04160 + 4*n, n=0...7; RC)

Note: These counters are similar to PXOFFRXC[n] in the 82598 that were in address 0x0CF20 + 4*n, n=0...7.

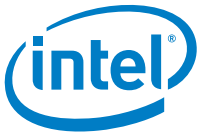
Field	Bit(s)	Init Val	Description
XOFFRXC	15:0	0x0	Number of XOFF packets received per UP. Sticks to 0xFFFF.
Reserved	31:16	0x0	Reserved.

8.2.3.23.17 Priority XON to XOFF Count — PXON2OFFCNT[n] (0x03240 + 4*n, n=0...7; RC)

Note: This is a RO register only.

8.2.3.23.18 Packets Received [64 Bytes] Count — PRC64 (0x0405C; RW)

Field	Bit(s)	Init Val	Description
PRC64	31:0	0x0	Number of good packets received that are 64 bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets.



8.2.3.23.19 Packets Received [65–127 Bytes] Count — PRC127 (0x04060; RW)

Field	Bit(s)	Init Val	Description
PRC127	31:0	0x0	Number of packets received that are 65-127 bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets.

8.2.3.23.20 Packets Received [128–255 Bytes] Count — PRC255 (0x04064; RW)

Field	Bit(s)	Init Val	Description
PRC255	31:0	0x0	Number of packets received that are 128-255 bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets.

8.2.3.23.21 Packets Received [256–511 Bytes] Count — PRC511 (0x04068; RW)

Field	Bit(s)	Init Val	Description
PRC511	31:0	0x0	Number of packets received that are 256-511 bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets.

8.2.3.23.22 Packets Received [512–1023 Bytes] Count — PRC1023 (0x0406C; RW)

Field	Bit(s)	Init Val	Description
PRC1023	31:0	0x0	Number of packets received that are 512-1023 bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets.

8.2.3.23.23 Packets Received [1024 to Max Bytes] Count — PRC1522 (0x04070; RW)

Field	Bit(s)	Init Val	Description
PRC1522	31:0	0x0	Number of packets received that are 1024-max bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets. The maximum is dependent on the current receiver configuration and the type of packet being received. If a packet is counted in receive oversized count, it is not counted in this register (see Section 8.2.3.23.52). Due to changes in the standard for maximum frame size for VLAN tagged frames in 802.3, this device accepts packets that have a maximum length of 1522 bytes. The RMON statistics associated with this range has been extended to count 1522 byte long packets.

8.2.3.23.24 Broadcast Packets Received Count — BPRC (0x04078; RO)

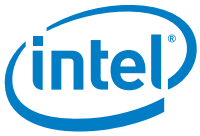
Field	Bit(s)	Init Val	Description
BPRC	31:0	0x0	Number of good (non-erred) broadcast packets received. This register does not count received broadcast packets when the broadcast address filter is disabled. The counter counts packets regardless on receive enablement.

8.2.3.23.25 Multicast Packets Received Count — MPRC (0x0407C; RO)

Field	Bit(s)	Init Val	Description
MPRC	31:0	0x0	Number of good (non-erred) multicast packets received that pass L2 filtering (excluding broadcast packets). This register does not count received flow control packets. This registers counts packets regardless on receive enablement.

8.2.3.23.26 Good Packets Received Count — GPRC (0x04074; RO)

Field	Bit(s)	Init Val	Description
GPRC	31:0	0x0	Number of good (non-erred) Rx packets (from the network) that pass L2 filtering and has a legal length as defined by *LongPacketEnable*. This registers counts packets regardless on receive enablement.



8.2.3.23.27 Good Octets Received Count Low — GORCL (0x04088; RC)

Field	Bit(s)	Init Val	Description
CNT_L	31:0	0x0	Lower 32 bits of the good octets received counter. The GORCL and GORCH registers make up a logical 36-bit octet counter of the packets counted by GPRC. This register includes bytes received in a packet from the <Destination Address> field through the <CRC> field, inclusively.

8.2.3.23.28 Good Octets Received Count High — GORCH (0x0408C; RC)

Field	Bit(s)	Init Val	Description
CNT_H	3:0	0x0	Higher four bits of the good octets received counter.
Reserved	31:4	0x0	Reserved

8.2.3.23.29 Good Rx Non-Filtered Packet Counter — RXNFGPC (0x041B0; RC)

Field	Bit(s)	Init Val	Description
GPC	31:0	0x0	Number of good (non-erred with legal length) Rx packets (from the network) regardless of packet filtering and receive enablement.

8.2.3.23.30 Good Rx Non-Filter Byte Counter Low — RXNFGBCL (0x041B4; RC)

Field	Bit(s)	Init Val	Description
BCL	31:0	0x0	Low 32 bits of the 36-bit byte counter of good (non-erred) Rx packets that match RXNFGPC. The counter counts all bytes from <Destination Address> field through the <CRC> field, inclusively.

8.2.3.23.31 Good Rx Non-Filter Byte Counter High — RXNFGBCH (0x041B8; RC)

Field	Bit(s)	Init Val	Description
BCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated with RXFGBCL.
Reserved	31:4	0x0	Reserved

8.2.3.23.32 DMA Good Rx Packet Counter — RXDGPC (0x02F50; RC)

Field	Bit(s)	Init Val	Description
GPC	31:0	0x0	Number of good (non-erred) Rx packets from the network posted to the host memory. In case of packet replication (or mirrored), the counter counts each packet only once. The counter counts packets directed to ALL Rx queues or specific Rx queues as defined by the RXDSTATCTRL register.

8.2.3.23.33 DMA Good Rx Byte Counter Low — RXDGBCL (0x02F54; RC)

Field	Bit(s)	Init Val	Description
GBCL	31:0	0x0	Lower 32 bits of the 36-bit byte counter of good (non-erred) Rx packets that match RXDGPC. The counter counts all bytes posted to the host before VLAN strip. Furthermore, bytes of RSC and FCoE are counted before coalescing or DDP.

8.2.3.23.34 DMA Good Rx Byte Counter High — RXDGBCH (0x02F58; RC)

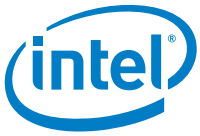
Field	Bit(s)	Init Val	Description
GBCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated with RXDGBCL.
Reserved	31:4	0x0	Reserved.

8.2.3.23.35 DMA Duplicated Good Rx Packet Counter — RXDDPC (0x02F5C; RC)

Field	Bit(s)	Init Val	Description
GPC	31:0	0x0	Number of replicated or mirrored packets that meet the RXDGPC conditions. The sum of RXDDPC and RXDGPC is the total good (non-erred) Rx packets from the network that are posted to the host. *Note:* The counter counts packets directed to ALL Rx queues or specific Rx queues as defined by the RXDSTATCTRL register.

8.2.3.23.36 DMA Duplicated Good Rx Byte Counter Low — RXDDBCL (0x02F60; RC)

Field	Bit(s)	Init Val	Description
GBCL	31:0	0x0	Lower 32 bits of the 36-bit byte counter of good (non-erred) Rx packets that match RXDDPC. The counter counts all bytes posted to the host before VLAN strip. Furthermore, bytes of RSC and FCoE are counted before coalescing or DDP.



8.2.3.23.37 DMA Duplicated Good Rx Byte Counter High — RXDDBCH (0x02F64; RC)

Field	Bit(s)	Init Val	Description
GBCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated with RXDDBCL.
Reserved	31:4	0x0	Reserved.

8.2.3.23.38 DMA Good Rx LPBK Packet Counter — RXLPBKPC (0x02F68; RC)

Field	Bit(s)	Init Val	Description
GPC	31:0	0x0	Number of good (non-erred) Rx packets from a local VM posted to the host memory. In case of packet replication (or mirrored), the counter counts each packet only once. The counter counts packets directed to ALL Rx queues or specific Rx queues as defined by the RXDSTATCTRL register. The counter is not affected by RSC and FCoE DDP since both functions are not supported for LPBK traffic.

8.2.3.23.39 DMA Good Rx LPBK Byte Counter Low — RXLPBKBCL (0x02F6C; RC)

Field	Bit(s)	Init Val	Description
GBCL	31:0	0x0	Lower 32 bits of the 36-bit byte counter of good (non-erred) Rx packets that match RXLPBKPC. The counter counts all bytes posted to the host before VLAN strip. Furthermore, bytes of RSC and FCoE are counted before coalescing or DDP.

8.2.3.23.40 DMA Good Rx LPBK Byte Counter High — RXLPBKBCH (0x02F70; RC)

Field	Bit(s)	Init Val	Description
GBCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated with RXLPBKBCL.
Reserved	31:4	0x0	Reserved.

8.2.3.23.41 DMA Duplicated Good Rx LPBK Packet Counter — RXDLPBKPC (0x02F74; RC)

Field	Bit(s)	Init Val	Description
GPC	31:0	0x0	Number of replicated or mirrored packets that meet the RXLPBKPC conditions. The sum of RXDLPBKPC and RXLPBKPC is the total good (non-erred) Rx packets from a local VM posted to the host. *Note:* The counter counts packets directed to ALL Rx queues or specific Rx queues as defined by the RXDSTATCTRL register.

8.2.3.23.42 DMA Duplicated Good Rx LPBK Byte Counter Low — RXDLPBKBCL (0x02F78; RC)

Field	Bit(s)	Init Val	Description
GBCL	31:0	0x0	Low 32 bits of the 36-bit byte counter of good (non-erred) Rx packets that match RXDLPBKPC. The counter counts all bytes posted to the host before VLAN strip. Furthermore, bytes of RSC and FCoE are counted before coalescing or DDP.

8.2.3.23.43 DMA Duplicated Good Rx LPBK Byte Counter High — RXDLPBKBCH (0x02F7C; RC)

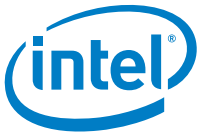
Field	Bit(s)	Init Val	Description
GBCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated with RXDLPBKBCL.
Reserved	31:4	0x0	Reserved.

8.2.3.23.44 Good Packets Transmitted Count — GPTC (0x04080; RC)

Field	Bit(s)	Init Val	Description
GPTC	31:0	0x0	Number of good packets transmitted. This register counts good (non-erred) transmitted packets. A good transmit packet is considered one that is 64 or more bytes (from <Destination Address> through <CRC>, inclusively) in length. The register counts transmitted clear packets, secure packets and FC packets.

8.2.3.23.45 Good Octets Transmitted Count Low — GOTCL (0x04090; RC)

Field	Bit(s)	Init Val	Description
CNT_L	31:0	0x0	Lower 32 bits of the good octets transmitted counter. See complete description in Section 8.2.3.23.46.



8.2.3.23.46 Good Octets Transmitted Count High — GOTCH (0x04094; RC)

Field	Bit(s)	Init Val	Description
CNT_H	3:0	0x0	Higher four bits of the good octets transmitted counter. The GOTCL and GOTCH registers make up a logical 36-bit counter of successfully transmitted octets (in packets counted by GPTC). This register includes transmitted bytes in a packet from the <Destination Address> field through the <CRC> field, inclusively.
Reserved	31:4	0x0	Reserved.

8.2.3.23.47 DMA Good Tx Packet Counter – TXDGPC (0x087A0; RC)

Field	Bit(s)	Init Val	Description
GPTC	31:0	0x0	Number of Tx packets from the host memory. This counter includes packets that are transmitted to the external network as well as packets that are transmitted only to local VMs. The later case can happen only in VT mode when the local switch is enabled. Packets dropped due to anti-spoofing filtering or VLAN tag validation (as described in Section 7.10.3.9.2) are not counted.

8.2.3.23.48 DMA Good Tx Byte Counter Low – TXDGBCL (0x087A4; RC)

Field	Bit(s)	Init Val	Description
BCL	31:0	0x0	Lower 32 bits of the 36-bit byte counter of the Tx packets that match TXDGPC. The counter counts all bytes posted by the host AND the VLAN (if bytes were added by hardware).

8.2.3.23.49 DMA Good Tx Byte Counter High – TXDGBCH (0x087A8; RC)

Field	Bit(s)	Init Val	Description
BCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated to TXDGBCL.
Reserved	31:4	0x0	Reserved.

8.2.3.23.50 Receive Undersize Count — RUC (0x040A4; RC)

Field	Bit(s)	Init Val	Description
RUC	31:0	0x0	Receive Undersize Error. This register counts the number of received frames that are shorter than minimum size (64 bytes from <Destination Address> through <CRC>, inclusively), and had a valid CRC. This register counts packets regardless of L2 filtering and receive enablement.

8.2.3.23.51 Receive Fragment Count — RFC (0x040A8; RC)

Field	Bit(s)	Init Val	Description
RFC	31:0	0x0	Number of receive fragment errors (frame shorted than 64 bytes from <Destination Address> through <CRC>, inclusively) that have bad CRC (this is slightly different from the Receive Undersize Count register). This register counts packets regardless of L2 filtering and receive enablement.

8.2.3.23.52 Receive Oversize Count — ROC (0x040AC; RC)

Field	Bit(s)	Init Val	Description
ROC	31:0	0x0	Receive Oversize Error. This register counts the number of received frames that are longer than maximum size as defined by MAXFRS.MFS (from <Destination Address> through <CRC>, inclusively) and have valid CRC. This register counts packets regardless of L2 filtering and receive enablement.

8.2.3.23.53 Receive Jabber Count — RJC (0x040B0; RC)

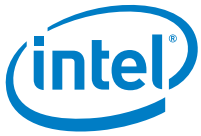
Field	Bit(s)	Init Val	Description
RJC	31:0	0x0	Number of receive jabber errors. This register counts the number of received packets that are greater than maximum size and have bad CRC (this is slightly different from the Receive Oversize Count register). The packets length is counted from <Destination Address> through <CRC>, inclusively. This register counts packets regardless of L2 filtering and receive enablement.

8.2.3.23.54 Management Packets Received Count — MNGPRC (0x040B4; RO)

Field	Bit(s)	Init Val	Description
MNGPRC	31:0	0x0	Number of management packets received. This register counts the total number of packets received that pass the management filters. Management packets include RMCP and ARP packets. Any packets with errors are not counted, except for the packets that are dropped because the management receive FIFO is full are counted.

8.2.3.23.55 Management Packets Dropped Count — MNGPDC (0x040B8; RO)

Field	Bit(s)	Init Val	Description
MPDC	31:0	0	Number of management packets dropped. This register counts the total number of packets received that pass the management filters and then are dropped because the management receive FIFO is full. Management packets include any packet directed to the manageability console (such as RMCP and ARP packets).



8.2.3.23.56 Management Packets Transmitted Count — MNGPTC (0x0CF90; RO)

Note: This is a RO register only.

8.2.3.23.57 Total Octets Received Low — TORL (0x040C0; RC)

Field	Bit(s)	Init Val	Description
CNT_L	31:0	0x0	Lower 32 bits of the total octets received counter. See complete description in Section 8.2.3.23.58.

8.2.3.23.58 Total Octets Received High — TORH (0x040C4; RC)

Field	Bit(s)	Init Val	Description
CNT_H	3:0	0x0	Higher four bits of the total octets received counter. The TORL and TORH registers make up a logical 36-bit counter of the total received octets (in the packets counted by the TPR counter). This register includes bytes received in a packet from the <Destination Address> field through the <CRC> field, inclusively.
Reserved	31:4	0x0	Reserved.

8.2.3.23.59 Total Packets Received — TPR (0x040D0; RC)

Field	Bit(s)	Init Val	Description
TPR	31:0	0x0	Number of all packets received. This register counts the total number of all packets received. All packets received are counted in this register, regardless of their length, whether they are erred, regardless on L2 filtering and receive enablement but excluding flow control packets. TPR can count packets interrupted by link disconnect although they have a CRC error.

8.2.3.23.60 Total Packets Transmitted — TPT (0x040D4; RC)

Field	Bit(s)	Init Val	Description
TPT	31:0	0x0	Number of all packets transmitted. This register counts the total number of all packets transmitted. This register counts all packets, including standard packets, secure packets, FC packets, and manageability packets.

8.2.3.23.61 Packets Transmitted (64 Bytes) Count — PTC64 (0x040D8; RC)

Field	Bit(s)	Init Val	Description
PTC64	31:0	0x0	Number of packets transmitted that are 64 bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, FC packets, and manageability packets.

8.2.3.23.62 Packets Transmitted [65–127 Bytes] Count — PTC127 (0x040DC; RC)

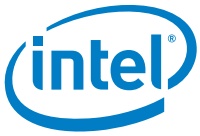
Field	Bit(s)	Init Val	Description
PTC127	31:0	0x0	Number of packets transmitted that are 65-127 bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, and manageability packets.

8.2.3.23.63 Packets Transmitted [128–255 Bytes] Count — PTC255 (0x040E0; RC)

Field	Bit(s)	Init Val	Description
PTC255	31:0	0x0	Number of packets transmitted that are 128-255 bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, and manageability packets.

8.2.3.23.64 Packets Transmitted [256–511 Bytes] Count — PTC511 (0x040E4; RC)

Field	Bit(s)	Init Val	Description
PTC511	31:0	0x0	Number of packets transmitted that are 256-511 bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, and manageability packets.



8.2.3.23.65 Packets Transmitted [512–1023 Bytes] Count — PTC1023 (0x040E8; RC)

Field	Bit(s)	Init Val	Description
PTC1023	31:0	0x0	Number of packets transmitted that are 512-1023 bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, and manageability packets.

8.2.3.23.66 Packets Transmitted [Greater Than 1024 Bytes] Count — PTC1522 (0x040EC; RC)

Field	Bit(s)	Init Val	Description
PTC1522	31:0	0x0	Number of packets transmitted that are 1024 or more bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, and manageability packets. Due to changes in the standard for maximum frame size for VLAN tagged frames in 802.3, this device transmits packets that have a maximum length of 1522 bytes. The RMON statistics associated with this range has been extended to count 1522 byte long packets. This register counts all packets, including standard and secure packets.

8.2.3.23.67 Multicast Packets Transmitted Count — MPTC (0x040F0; RC)

Field	Bit(s)	Init Val	Description
MPTC	31:0	0x0	Number of multicast packets transmitted. This register counts the number of multicast packets transmitted. This register counts all packets, including standard packets, secure packets, FC packets and manageability packets.

8.2.3.23.68 Broadcast Packets Transmitted Count — BPTC (0x040F4; RC)

Field	Bit(s)	Init Val	Description
BPTC	31:0	0x0	Number of broadcast packets transmitted count. This register counts all packets, including standard packets, secure packets, FC packets and manageability packets

8.2.3.23.69 MAC Short Packet Discard Count — MSPDC (0x04010; RC)

Field	Bit(s)	Init Val	Description
MSPDC	31:0	0x0	Number of MAC short packet discard packets received.

8.2.3.23.70 XSUM Error Count — XEC (0x04120; RC)

Field	Bit(s)	Init Val	Description
XEC	31:0	0x0	Number of receive IPv4, TCP, UDP or SCTP XSUM errors.

XSUM errors are not counted when a packet has any MAC error (CRC, length, under-size, over-size, byte error or symbol error).

8.2.3.23.71 Receive Queue Statistic Mapping Registers — RQSMR[n] (0x02300 + 4*n, n=0...31; RW)

These registers define the mapping of the receive queues to the per queue statistics. Several queues can be mapped to a single statistic register. Each statistic register counts the number of packets and bytes of all the queues that are mapped to that statistics. The registers counting Rx queue statistics are: QPRC, QBRC, and QPRDC.

Field	Bit(s)	Init Val	Description
Q_MAP[0]	3:0	0x0	For each register 'n', Q_MAP[0] defines the per queue statistic registers that are mapped to Rx queue '4*n+0'. (see examples that follow).
Reserved	7:4	0x0	Reserved.
Q_MAP[1]	11:8	0x0	For each register 'n', Q_MAP[1] defines the per queue statistic registers that are mapped to Rx queue '4*n+1'. (see examples that follow).
Reserved	15:12	0x0	Reserved.
Q_MAP[2]	19:16	0x0	For each register 'n', Q_MAP[2] defines the per queue statistic registers that are mapped to Rx queue '4*n+2'. (see examples that follow).
Reserved	23:20	0x0	Reserved.
Q_MAP[3]	27:24	0x0	For each register 'n', Q_MAP[3] defines the per queue statistic registers that are mapped to Rx queue '4*n+3'. (see examples that follow).
Reserved	31:28	0x0	Reserved.

For example, setting RQSMR[0].Q_MAP[0] to 3 maps Rx queue 0 to the counters QPRC[3], QBRC[3], and QPRDC[3]. Setting RQSMR[2].Q_MAP[1] to 5 maps Rx queue 9 to the QPRC[5], QBRC[5], and QPRDC[5].