8.2 Device Registers — PF

8.2.1 MSI-X BAR Register Summary PF

See Section 9.3.6.1 for the MSI-X BAR offset in 32-bit and 64-bit BAR options.

Category	BAR 3 Offset	Alias Offset	Abbreviation	Name	RW
MSI-X	0x0000 — (N-1)*0x10	N/A	MSIXTADD	MSIX table entry lower address.	RW
MSI-X	0x0004 — (N-1)*0x10	N/A	MSIXTUADD	MSIX table entry upper address.	RW
MSI-X	0x0008 — (N-1)*0x10	N/A	MSIXTMSG	MSIX table entry message.	RW
MSI-X	0x000C — (N-1)*0x10	N/A	MSIXTVCTRL	MSIX table vector control.	RW
MSI-X	0x2000 — 0x200C	N/A	MSIXPBA	MSI-X Pending bit array.	RO

8.2.2 Registers Summary PF — BAR 0

All of the 82599's non-PCIe configuration registers are listed in the following table. These registers are ordered by grouping and are not necessarily listed in the order that they appear in the address space.

Note: All registers should be accessed as a 32-bit width on reads with an appropriate software mask, if needed. A software read/modify/write mechanism should be invoked for partial writes.

Table 8-2 Register Summary

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
General Control Registers						
0x00000 / 0x00004	CTRL	Device Control Register	Target	RW		543
0x00008	STATUS	Device Status Register	Target	RO		544
0x00018	CTRL_EXT	Extended Device Control Register	Target	RW		544
0x00020	ESDP	Extended SDP Control	Target	RW		545
0x00028	I2CCTL	I2C Control	Target	RW	PERST	549
0x00200	LEDCTL	LED Control	Target	RW		549
0x05078	EXVET	Extended VLAN Ether Type	Target	RW		551

Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
EEPROM/Flash Registers						
0x10010	EEC	EEPROM/Flash Control Register	FLEEP	RW		552
0x10014	EERD	EEPROM Read Register	FLEEP	RW		554
0x1001C	FLA	Flash Access Register	FLEEP	RW		555
0x10114	EEMNGDATA	Manageability EEPROM Read/ Write Data	FLEEP	RW		556
0x10118	FLMNGCTL	Manageability Flash Control Register	FLEEP	RW		557
0x1011C	FLMNGDATA	Manageability Flash Read Data	FLEEP	RW		557
0x01013C	FLOP	Flash Opcode Register	FLEEP	RW		558
0x10200	GRC	General Receive Control	FLEEP	RW		558
Flow Control Registers						
0x0431C / 0x03008	PFCTOP	Priority Flow Control Type Opcode	MAC	RW		559
0x03200+4*n, n=0...3	FCTTVn	Flow Control Transmit Timer Value n	DBU-Rx	RW		559
0x03220+4*n, n=0...7	FCRTL[n]	Flow Control Receive Threshold Low	DBU-Rx	RW		560
0x03260+4*n, n=0...7	FCRTH[n]	Flow Control Receive Threshold High	DBU-Rx	RW		560
0x032A0	FCRTV	Flow Control Refresh Threshold Value	DBU-Rx	RW		561
0x0CE00	TFCS	Transmit Flow Control Status	DBU-Tx	RO		561
0x03D00	FCCFG	Flow Control Configuration	DBU-Rx	RW		561
PCIe Registers						
0x11000	GCR	PCIe Control Register	PCIe	RW		562
0x11010	GSCL_1	PCIe Statistic Control Register #1	PCIe	RW		562
0x11014	GSCL_2	PCIe Statistic Control Registers #2	PCIe	RW		563
0x011030+4*n, n=0...3	GSCL_5_8	PCIe Statistic Control Register #5...#8	PCIe	RW		565

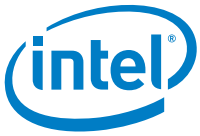


Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x11020+4*n, n=0...3	GSCN_0_3	PCIe Statistic Counter Registers #0...#3	PCIe	RO		565
0x10150	FACTPS	Function Active and Power State to Manageability	FLEEP	RO		565
0x11040	PCIEPHYADR	PCIe PHY Address Register	PCIe	RW		566
0x11044	PCIEPHYDAT	PCIe PHY Data Register	PCIe	RW		567
0x10140	SWSM	Software Semaphore Register	FLEEP	RW		567
0x10148	FWSM	Firmware Semaphore Register	FLEEP	RW		567
0x10160	SW_FW_SYNC	Software–Firmware Synchronization	FLEEP	RW		569
0x11050	GCR_EXT	PCIe Control Extended Register	PCIe	RW		569
0x11064	MREVID	Mirrored Revision ID	PCIe	RO		570
0x110B0	PICAUSE	PCIe Interrupt Cause	PCIe	RO		570
0x110B8	PIENA	PCIe Interrupts Enable	PCIe	RW		571
Interrupt Registers						
0x00800	EICR	Extended Interrupt Cause Register	Interrupt	RW1C		572
0x00808	EICS	Extended Interrupt Cause Set Register	Interrupt	WO		573
0x00880	EIMS	Extended Interrupt Mask Set/ Read Register	Interrupt	RWS		573
0x00888	EIMC	Extended Interrupt Mask Clear Register	Interrupt	WO		574
0x00810	EIAC	Extended Interrupt Auto Clear Register	Interrupt	RW		574
0x00890	EIAM	Extended Interrupt Auto Mask Enable Register	Interrupt	RW		574
0x00A90+4*(n-1), n=1...2	EICS[n]	Extended Interrupt Cause Set Registers	Interrupt	WO		575
0x00AA0+4*(n-1), n=1...2	EIMS[n]	Extended Interrupt Mask Set/ Read Registers	Interrupt	RWS		575
0x00AB0+4*(n-1), n=1...2	EIMC[n]	Extended Interrupt Mask Clear Registers	Interrupt	WO		575
0x00AD0+4*(n-1), n=1...2	EIAM[n]	Extended Interrupt Auto Mask Enable registers	Interrupt	RW		575

Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x00894	EITRSEL	MSI to EITR Select	Interrupt	RW		575
0x00820+4*n, n=0...23 and 0x012300+4*(n-24), n=24...128	EITR[n]	Extended Interrupt Throttle Registers	Interrupt	RW		576
0x0E800+4*n, n=0...127	L34TIMIR[n]	L3 L4 Tuples Immediate Interrupt Rx	DBU-Rx	RW		576
0x0EC90	LLITHRESH	LLI Size Threshold	DBU-Rx	RW		577
0x0EC60 / 0x05AC0	IMIRVP	Immediate Interrupt Rx VLAN Priority Register	DBU-Rx	RW		577
0x00900+4*n, n=0...63	IVAR[n]	Interrupt Vector Allocation	Interrupt	RW		578
0x00A00	IVAR_MISC	Miscellaneous Interrupt Vector Allocation	Interrupt	RW		579
0x00898	GPIE	General Purpose Interrupt Enable	Interrupt	RW		579
MSI-X Table Registers						
0x110C0+4*n, n=0...7 / 0x11068 [n=0]	PBACL[n]	MSI-X PBA Clear	PCIe	RW		581
Receive Registers						
0x05080	FCTRL	Filter Control Register	Rx-Filter	RW		582
0x05088	VLNCTRL	VLAN Control Register	Rx-Filter	RW		583
0x05090	MCSTCTRL	Multicast Control Register	Rx-Filter	RW		583
0x0EA00+4*n, n=0...63 / 0x05480+4*n, n=0…15	PSRTYPE[n]	Packet Split Receive Type Register	DBU-Rx	RW		584
0x05000	RXCSUM	Receive Checksum Control	Rx-Filter	RW		585
0x05008	RFCTL	Receive Filter Control Register	Rx-Filter	RW		586
0x05200+4*n, n=0...127	MTA[n]	Multicast Table Array	Rx-Filter	RW		587
0x0A200+8*n, n=0...127	RAL[n]	Receive Address Low	Rx-Filter	RW		587
0x0A204+8*n, n=0...127	RAH[n]	Receive Address High	Rx-Filter	RW		587
0x0A600+4*n, n=0...255	MPSAR[n]	MAC Pool Select Array	Rx-Filter	RW		588
0x0A000+4*n, n=0...127	VFTA[n]	VLAN Filter Table Array	Rx-Filter	RW		588
0x0EC80 / 0x05818	MRQC	Multiple Receive Queues Command Register	DBU-Rx	RW		589

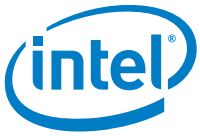


Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x0EC70	RQTC	RSS Queues Per Traffic Class Register	DBU-Rx	RW		590
0x0EB80+4*n, n=0...9 / 0x05C80+4*n, n=0...9	RSSRK[n]	RSS Random Key Register	DBU-Rx	RW		591
0x0EB00+4*n, n=0...31 / 0x05C00+4*n, n=0...31	RETA[n]	Redirection Table	DBU-Rx	RW		591
0x0E000+4*n, n=0...127	SAQF[n]	Source Address Queue Filter	DBU-Rx	RW		592
0x0E200+4*n, n=0...127	DAQF[n]	Destination Address Queue Filter	DBU-Rx	RW		592
0x0E400+4*n, n=0...127	SDPQF[n]	Source Destination Port Queue Filter	DBU-Rx	RW		592
0x0E600+4*n, n=0...127	FTQF[n]	Five Tuple Queue Filter	DBU-Rx	RW		593
0x0EC30	SYNQF	SYN Packet Queue Filter	DBU-Rx	RW		594
0x05128+4*n, n=0...7	ETQF[n]	EType Queue Filter	Rx-Filter	RW		594
0x0EC00+4*n, n=0...7	ETQS[n]	EType Queue Select	DBU-Rx	RW		595
Receive DMA Registers						
0x01000+0x40*n, n=0...63 and 0x0D000+0x40*(n-64), n=64...127	RDBAL[n]	Receive Descriptor Base Address Low	DMA-Rx	RW		596
0x01004+0x40*n, n=0...63 and 0x0D004+0x40*(n-64), n=64...127	RDBAH[n]	Receive Descriptor Base Address High	DMA-Rx	RW		596
0x01008+0x40*n, n=0...63 and 0x0D008+0x40*(n-64), n=64...127	RDLEN[n]	Receive Descriptor Length	DMA-Rx	RW		596
0x01010+0x40*n, n=0...63 and 0x0D010+0x40*(n-64), n=64...127	RDH[n]	Receive Descriptor Head	DMA-Rx	RO		597
0x01018+0x40*n, n=0...63 and 0x0D018+0x40*(n-64), n=64...127	RDT[n]	Receive Descriptor Tail	DMA-Rx	RW		597
0x01028+0x40*n, n=0...63 and 0x0D028+0x40*(n-64), n=64...127	RXDCTL[n]	Receive Descriptor Control	DMA-Rx	RW		597
0x01014+0x40*n, n=0...63 and 0x0D014+0x40*(n-64), n=64...127 / 0x02100+4*n, [n=0...15]	SRRCTL[n]	Split Receive Control Registers	DMA-Rx	RW		598
0x02F00	RDRXCTL	Receive DMA Control Register	DMA-Rx	RW		599

Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x03C00+4*n, n=0...7	RXPBSIZE[n]	Receive Packet Buffer Size	DBU-Rx	RW		600
0x03000	RXCTRL	Receive Control Register	DBU-Rx	RW		600
0x03190	RXMEMWRAP	Rx Packet Buffer Flush Detect	DBU-Rx	RO		600
0x03028	RSCDBU	RSC Data Buffer Control Register	DBU-Rx	RW		602
0x0102C+0x40*n, n=0...63 and 0x0D02C+0x40*(n-64), n=64...127	RSCCTL[n]	RSC Control	DMA-Rx	RW		602
Transmit Registers						
0x08100	DTXMXSZRQ	DMA Tx TCP Max Allow Size Requests	DMA-Tx	RW		603
0x04A80	DMATXCTL	DMA Tx Control	DMA-Tx	RW		603
0x04A88	DTXTCPFLGL	DMA Tx TCP Flags Control Low	DMA-Tx	RW		604
0x04A8C	DTXTCPFLGH	DMA Tx TCP Flags Control High	DMA-Tx	RW		604
0x06000+0x40*n, n=0...127	TDBAL[n]	Transmit Descriptor Base Address Low	DMA-Tx	RW		604
0x06004+0x40*n, n=0...127	TDBAH[n]	Transmit Descriptor Base Address High	DMA-Tx	RW		605
0x06008+0x40*n, n=0...127	TDLEN[n]	Transmit Descriptor Length	DMA-Tx	RW		605
0x06010+0x40*n, n=0...127	TDH[n]	Transmit Descriptor Head	DMA-Tx	RO		605
0x06018+0x40*n, n=0...127	TDT[n]	Transmit Descriptor Tail	DMA-Tx	RW		606
0x06028+0x40*n, n=0...127	TXDCTL[n]	Transmit Descriptor Control	DMA-Tx	RW		606
0x06038+0x40*n, n=0...127	TDWBAL[n]	Tx Descriptor Completion Write Back Address Low	DMA-Tx	RW		607
0x0603C+0x40*n, n=0...127	TDWBAH[n]	Tx Descriptor Completion Write Back Address High	DMA-Tx	RW		608
0x0CC00+0x4*n, n=0...7	TXPBSIZE[n]	Transmit Packet Buffer Size	DBU-Tx	RW		608
0x0CD10	MNGTXMAP	Manageability Transmit TC Mapping	DBU-Tx	RW		608
0x08120	MTQC	Multiple Transmit Queues Command Register	DMA-Tx	RW		609
0x04950 +0x4*n, n=0...7	TXPBTHRESH	Tx Packet Buffer Threshold	DMA-Tx	RW		610

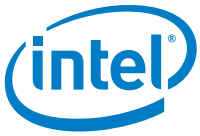


Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
DCB Registers						
0x02430	RTRPCS	DCB Receive Packet plane Control and Status	DMA-Rx	RW		611
0x04900	RTTDCS	DCB Transmit Descriptor Plane Control and Status	DMA-Tx	RW		611
0x0CD00	RTTPCS	DCB Transmit Packet Plane Control and Status	DBU-Tx	RW		617
0x03020	RTRUP2TC	DCB Receive User Priority to Traffic Class	DBU-Rx	RW		613
0x0C800	RTTUP2TC	DCB Transmit User Priority to Traffic Class	DBU-Tx	RW		614
0x02140+4*n, n=0...7	RTRPT4C[n]	DCB Receive Packet Plane T4 Config	DMA-Rx	RW		615
0x082E0+4*n, n=0...3	TXLLQ[n]	Strict Low Latency Tx Queues	DMA-Tx	RW		616
0x02160+4*n, n=0...7	RTRPT4S[n]	DCB Receive Packet plane T4 Status	DMA-Rx	RO		616
0x04910+4*n, n=0...7	RTTDT2C[n]	DCB Transmit Descriptor plane T2 Config	DMA-Tx	RW		616
0x0CD20+4*n, n=0...7	RTTPT2C[n]	DCB Transmit Packet Plane T2 Config	DBU-Tx	RW		617
0x0CD40+4*n, n=0...7	RTTPT2S[n]	DCB Transmit Packet Plane T2 Status	DBU-Tx	RO		617
0x04980	RTTBCNRM	DCB Transmit Rate–Scheduler MMW	DMA-Tx	RW		617
0x04904	RTTDQSEL	DCB Transmit Descriptor Plane Queue Select	DMA-Tx	RW		618
0x04908	RTTDT1C	DCB Transmit Descriptor Plane T1 Config	DMA-Tx	RW		618
0x0490C	RTTDT1S	DCB Transmit Descriptor Plane T1 Status	DMA-Tx	RO		618
0x04984	RTTBCNRC	DCB Transmit Rate-Scheduler Config	DMA-Tx	RW		619
0x04988	RTTBCNRS	DCB Transmit Rate-Scheduler Status	DMA-Tx	RW		619
0x0498C	RTTBCNRD	DCB Transmit Rate Scheduler Rate Drift	DMA-Tx	RW		620

Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
DCA Registers						
0x0100C+0x40*n, n=0...63 and 0x0D00C+0x40*(n-64), n=64...127 / 0x02200+4*n, [n=0...15]	DCA_RXCTRL[n]	Rx DCA Control Register	DMA-Rx	RW		621
0x0600C+0x40*n, n=0...127	DCA_TXCTRL[n]	Tx DCA Control Register	DMA-Tx	RW		622
0x11070	DCA_ID	DCA Requester ID Information Register	PCIe	RO		623
0x11074	DCA_CTRL	DCA Control Register	PCIe	RW		622
Security Registers						
0x08800	SECTXCTRL	Security Tx Control	SEC-Tx	RW		624
0x08804	SECTXSTAT	Security Tx Status	SEC-Tx	RO		625
0x08808	SECTXBUFFAF	Security Tx Buffer Almost Full	SEC-Tx	RW		625
0x08810	SECTXMINIFG	Security Tx Buffer Minimum IFG	SEC-Tx	RW		625
0x08D00	SECRXCTRL	Security Rx Control	SEC-Rx	RW		626
0x08D04	SECRXSTAT	Security Rx Status	SEC-Rx	RO		626
LinkSec Registers						
0x08A00	LSECTXCAP	LinkSec Tx Capabilities Register	SEC-Tx	RW		627
0x08F00	LSECRXCAP	LinkSec Rx Capabilities Register	SEC-Rx	RW		627
0x08A04	LSECTXCTRL	LinkSec Tx Control Register	SEC-Tx	RW		628
0x08F04	LSECRXCTRL	LinkSec Rx Control Register	SEC-Rx	RW		628
0x08A08	LSECTXSCL	LinkSec Tx SCI Low	SEC-Tx	RW		629
0x08A0C	LSECTXSCH	LinkSec Tx SCI High	SEC-Tx	RO		629
0x08A10	LSECTXSA	LinkSec Tx SA	SEC-Tx	RW		630
0x08A14	LSECTXPN0	LinkSec Tx SA PN 0	SEC-Tx	RW		630
0x08A18	LSECTXPN1	LinkSec Tx SA PN 1	SEC-Tx	RW		630
0x08A1C+4*n, n=0...3	LSECTXKEY0[n]	LinkSec Tx Key 0	SEC-Tx	WO		631
0x08A2C+4*n, n=0...3	LSECTXKEY1[n]	LinkSec Tx Key 1	SEC-Tx	WO		631
0x08F08	LSECRXSCL	LinkSec Rx SCI Low	SEC-Rx	RW		631

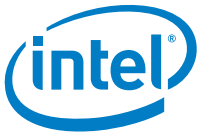


Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x08F0C	LSECRXSCH	LinkSec Rx SCI High	SEC-Rx	RW		632
0x08F10+4*n, n=0...1	LSECRXSA[n]	LinkSec Rx SA	SEC-Rx	RW		632
0x08F18+4*n, n=0...1	LSECRXPN[n]	LinkSec Rx SA PN	SEC-Rx	RW		633
0x08F20+0x10*n+4*m, n=0...1, m=0...3	LSECRXKEY[n,m]	LinkSec Rx Key	SEC-Rx	WO		633
0x08A3C	LSECTXUT	Tx Untagged Packet Counter	SEC-Tx	RO		634
0x08A40	LSECTXPKTE	Encrypted Tx Packets	SEC-Tx	RO		634
0x08A44	LSECTXPKTP	Protected Tx Packets	SEC-Tx	RO		634
0x08A48	LSECTXOCTE	Encrypted Tx Octets	SEC-Tx	RO		634
0x08A4C	LSECTXOCTP	Protected Tx Octets	SEC-Tx	RO		635
0x08F40	LSECRXUT	LinkSec Untagged Rx Packet	SEC-Rx	RO		636
0x08F44	LSECRXOCTE	LinkSec Rx Octets Decrypted	SEC-Rx	RO		636
0x08F48	LSECRXOCTP	LinkSec Rx Octets Validated	SEC-Rx	RO		636
0x08F4C	LSECRXBAD	LinkSec Rx Packet with Bad Tag	SEC-Rx	RO		636
0x08F50	LSECRXNOSCI	LinkSec No SCI	SEC-Rx	RO		637
0x08F54	LSECRXUNSCI	LinkSec Unknown SCI	SEC-Rx	RO		637
0x08F58	LSECRXUC	LinkSec Rx Unchecked Packets	SEC-Rx	RO		638
0x08F5C	LSECRXDELAY	LinkSec Rx Delayed Packets	SEC-Rx	RO		638
0x08F60	LSECRXLATE	LinkSec Rx Late Packets	SEC-Rx	RO		638
0x08F64+4*n, n=0...1	LSECRXOK[n]	LinkSec Rx Packet OK	SEC-Rx	RO		639
0x08F6C+4*n, n=0...1	LSECRXINV[n]	LinkSec Rx Invalid	SEC-Rx	RO		639
0x08F74+4*n, n=0...1	LSECRXNV[n]	LinkSec Rx Not Valid	SEC-Rx	RC		639
0x08F7C	LSECRXUNSA	LinkSec Rx Unused SA	SEC-Rx	RC		639
0x08F80	LSECRXNUSA	LinkSec Rx Not Using SA	SEC-Rx	RC		640
IPsec Registers						
0x08900	IPSTXIDX	IPsec Tx Index	SEC-Tx	RW		641
0x08908+4*n, n=0...3	IPSTXKEY[n]	IPsec Tx Key Registers	SEC-Tx	RW		641

Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x08904	IPSTXSALT	IPsec Tx Salt Register	SEC-Tx	RW		642
0x08E00	IPSRXIDX	IPsec Rx Index	SEC-Rx	RW		642
0x08E04+4*n, n=[0...3]	IPSRXIPADDR	IPsec Rx IP address Register	SEC-Rx	RW		643
0x08E14	IPSRXSPI	IPsec Rx SPI Register	SEC-Rx	RW		643
0x08E18	IPSRXIPIDX	IPsec Rx SPI Register	SEC-Rx	RW		643
0x08E1C+4*n, n=0...3	IPSRXKEY[n]	IPsec Rx Key Register	SEC-Rx	RW		643
0x08E2C	IPSRXSALT	IPsec Rx Salt Register	SEC-Rx	RW		644
0x08E30	IPSRXMOD	IPsec Rx Mode Register	SEC-Rx	RW		644
Timers Registers						
0x0004C	TCPTIMER	TCP Timer	Target	RW		645
FCoE Registers						
0x05100	FCRXCTRL	FC Receive Control	Rx-Filter	RW		647
0x0ED00	FCRECTL	FCoE Redirection Control	DBU-Rx	RW		648
0x0ED10+4*n, n=0...7	FCRETA[n]	FCoE Redirection Table	DBU-Rx	RW		648
0x02410	FCPTRL	FC User Descriptor PTR Low	DMA-Rx	RW		648
0x02414	FCPTRH	FC User Descriptor PTR High	DMA-Rx	RW		649
0x02418	FCBUFF	FC Buffer Control	DMA-Rx	RW		649
0x02420	FCDMARW	FC Receive DMA RW	DMA-Rx	RW		650
0x05108	FCFLT	FC FLT Context	Rx-Filter	RW		650
0x051D8	FCPARAM	FC Offset Parameter	Rx-Filter	RW		650
0x05110	FCFLTRW	FC Filter RW Control	Rx-Filter	WO		651
Flow Director Registers						
Global Settings Registers						
0x0EE00	FDIRCTRL	Flow Director Filters Control Register	DBU-Rx	RW		652
0x0EE68	FDIRHKEY	Flow Director Filters Lookup Table Hash Key	DBU-Rx	RW		653
0x0EE6C	FDIRSKEY	Flow Director Filters Signature Hash Key	DBU-Rx	RW		653

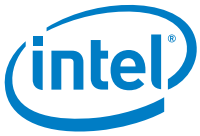


Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x0EE3C	FDIRDIP4M	Flow Director Filters IPv4 Mask	DBU-Rx	RW		653
0x0EE40	FDIRSIP4M	Flow Director Filters Source IPv4 Mask	DBU-Rx	RW		654
0x0EE44	FDIRTCPM	Flow Director Filters TCP Mask	DBU-Rx	RW		654
0x0EE48	FDIRUDPM	Flow Director Filters UDP Mask	DBU-Rx	RW		654
0x0EE74	FDIRIP6M	Flow Director Filters IPv6 Mask	DBU-Rx	RW		655
0x0EE70	FDIRM	Flow Director Filters Other Mask	DBU-Rx	RW		655
Global Status / Statistics Registers						
0x0EE38	FDIRFREE	Flow Director Filters Free	DBU-Rx	RW		656
0x0EE4C	FDIRLEN	Flow Director Filters Length	DBU-Rx	RC		656
0x0EE50	FDIRUSTAT	Flow Director Filters Usage Statistics	DBU-Rx	RW / RC		656
0x0EE54	FDIRFSTAT	Flow Director Filters Failed Usage Statistics	DBU-Rx	RW / RC		657
0x0EE58	FDIRMATCH	Flow Director Filters Match Statistics	DBU-Rx	RC		657
0x0EE5C	FDIRMISS	Flow Director Filters Miss Match Statistics	DBU-Rx	RC		657
Flow Programming Registers						
0x0EE0C+4*n, n=0…2	FDIRSIPv6[n]	Flow Director Filters Source IPv6	DBU-Rx	RW		657
0x0EE18	FDIRIPSA	Flow Director Filters IP SA	DBU-Rx	RW		658
0x0EE1C	FDIRIPDA	Flow Director Filters IP DA	DBU-Rx	RW		658
0x0EE20	FDIRPORT	Flow Director Filters Port	DBU-Rx	RW		658
0x0EE24	FDIRVLAN	Flow Director Filters VLAN and FLEX bytes	DBU-Rx	RW		658
0x0EE28	FDIRHASH	Flow Director Filters Hash Signature	DBU-Rx	RW		658
0x0EE2C	FDIRCMD	Flow Director Filters Command Register	DBU-Rx	RW		659
MAC Registers						
0x04200	PCS1GCFIG	PCS_1G Global Config Register 1	MAC	RW		661
0x04208	PCS1GLCTL	PCG_1G link Control Register	MAC	RW		661

Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x0420C	PCS1GLSTA	PCS_1G Link Status Register	MAC	RO		662
0x04218	PCS1GANA	PCS_1 Gb/s Auto-Negotiation Advanced Register	MAC	RW		663
0x0421C	PCS1GANLP	PCS_1GAN LP Ability Register	MAC	RO		663
0x04220	PCS1GANNP	PCS_1G Auto-Negotiation Next Page Transmit Register	MAC	RW		664
0x04224	PCS1GANLPNP	PCS_1G Auto-Negotiation LP's Next Page Register	MAC	RO		665
0x04240	HLREG0	MAC Core Control 0 Register	MAC	RW		666
0x04244	HLREG1	MAC Core Status 1 Register	MAC	RO		667
0x04248	PAP	Pause and Pace Register	MAC	RW		668
0x0425C	MSCA	MDI Single Command and Address	MAC	RW		668
0x04260	MSRWD	MDI Single Read and Write Data	MAC	RW		669
0x04268	MAXFRS	Max Frame Size	MAC	RW		669
0x4288	PCSS1	XGXS Status 1	MAC	RO		669
0x0428C	PCSS2	XGXS Status 2	MAC	RO		670
0x04290	XPCSS	10GBASE-X PCS Status	MAC	RO		670
0x04298	SERDESC	SerDes Interface Control Register	MAC	RW		672
0x0429C	MACS	FIFO Status/CNTL report Register	MAC	RW		673
0x042A0	AUTOC	Auto-Negotiation Control Register	MAC	RW		674
0x042A4	LINKS	Link Status Register	MAC	RO		676
0x04324	LINKS2	Link Status Register 2	MAC	RO		678
0x042A8	AUTOC2	Auto-Negotiation Control 2 Register	MAC	RW		679
0x042B0	ANLP1	Auto-Negotiation Link Partner Link Control Word 1 Register	MAC	RO		679
0x042B4	ANLP2	Auto-Negotiation Link Partner Link Control Word 2 Register	MAC	RO		680

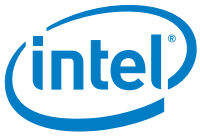


Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x042D0	MMNGC	MAC Manageability Control Register	MAC	RO		680
0x042D4	ANLPNP1	Auto-Negotiation Link Partner Next Page 1 register	MAC	RO		680
0x042D8	ANLPNP2	Auto-Negotiation Link Partner Next Page 2 register	MAC	RO		681
0x042E0	KRPCSFC	KR PCS and FEC Control Register	MAC	RW		681
0x042E4	KRPCSS	KR PCS Status Register	MAC	RO		682
0x042E8	FECS1	FEC Status 1 Register	MAC	RC		684
0x042EC	FECS2	FEC Status 2 Register	MAC	RC		684
0x014F00	CoreCTL	Core Analog Configuration Register	MAC	RW		684
0x014F10	SMADARCTL	Core Common Configuration Register	MAC	RW		685
0x04294	MFLCN	MAC Flow Control Register	MAC	RW		685
0x04314	SGMIIC	SGMII Control Register	MAC	RW		686
Statistic Registers						
0x04000	CRCERRS	CRC Error Count	STAT	RC		687
0x04004	ILLERRC	Illegal Byte Error Count	STAT	RC		687
0x04008	ERRBC	Error Byte Count	STAT	RC		688
0x04034	MLFC	MAC Local Fault Count	STAT	RC		688
0x04038	MRFC	MAC Remote Fault Count	STAT	RC		688
0x04040	RLEC	Receive Length Error Count	STAT	RC		688
0x08780	SSVPC	Switch Security Violation Packet Count	DMA-Tx	RC		688
0x041A4	LXONRXCNT	Link XON Received Count	STAT	RC		689
0x041A8	LXOFFRXCNT	Link XOFF Received Count	STAT	RC		689
0x04140+4*n, n=0...7	PXONRXCNT[n]	Priority XON Received Count	STAT	RC		690
0x04160+4*n, n=0...7	PXOFFRXCNT[n]	Priority XOFF Received Count	STAT	RC		690
0x0405C	PRC64	Packets Received [64 Bytes] Count	STAT	RW		690

Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x04060	PRC127	Packets Received [65–127 Bytes] Count	STAT	RW		691
0x04064	PRC255	Packets Received [128–255 Bytes] Count	STAT	RW		691
0x04068	PRC511	Packets Received [256–511 Bytes] Count	STAT	RW		691
0x0406C	PRC1023	Packets Received [512–1023 Bytes] Count	STAT	RW		691
0x04070	PRC1522	Packets Received [1024 to Max Bytes] Count	STAT	RW		692
0x04078	BPRC	Broadcast Packets Received Count	STAT	RC		692
0x0407C	MPRC	Multicast Packets Received Count	STAT	RC		692
0x04074	GPRC	Good Packets Received Count	STAT	RC		692
0x04088	GORCL	Good Octets Received Count Low	STAT	RC		693
0x0408C	GORCH	Good Octets Received Count High	STAT	RC		693
0x041B0	RXNFGPC	Good Rx Non-Filtered Packet Counter	STAT	RC		693
0x041B4	RXNFGBCL	Good Rx Non-Filter Byte Counter Low	STAT	RC		693
0x041B8	RXNFGBCH	Good Rx Non-Filter Byte Counter High	STAT	RC		693
0x02F50	RXDGPC	DMA Good Rx Packet Counter	DMA-Rx	RC		694
0x02F54	RXDGBCL	DMA Good Rx Byte Counter Low	DMA-Rx	RC		694
0x02F58	RXDGBCH	DMA Good Rx Byte Counter High	DMA-Rx	RC		694
0x02F5C	RXDDPC	DMA Duplicated Good Rx Packet Counter	DMA-Rx	RC		694
0x02F60	RXDDBCL	DMA Duplicated Good Rx Byte Counter Low	DMA-Rx	RC		694
0x02F64	RXDDBCH	DMA Duplicated Good Rx Byte Counter High	DMA-Rx	RC		695
0x02F68	RXLPBKPC	DMA Good Rx LPBK Packet Counter	DMA-Rx	RC		695

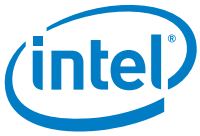


Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x02F6C	RXLPBKBCL	DMA Good Rx LPBK Byte Counter Low	DMA-Rx	RC		695
0x02F70	RXLPBKBCH	DMA Good Rx LPBK Byte Counter High	DMA-Rx	RC		695
0x02F74	RXDLPBKPC	DMA Duplicated Good Rx LPBK Packet Counter	DMA-Rx	RC		696
0x02F78	RXDLPBKBCL	DMA Duplicated Good Rx LPBK Byte Counter Low	DMA-Rx	RC		696
0x02F7C	RXDLPBKBCH	DMA Duplicated Good Rx LPBK Byte Counter High	DMA-Rx	RC		696
0x04080	GPTC	Good Packets Transmitted Count	STAT	RO		696
0x04090	GOTCL	Good Octets Transmitted Count Low	STAT	RC		696
0x04094	GOTCH	Good Octets Transmitted Count High	STAT	RC		697
0x087A0	TXDGPC	DMA Good Tx Packet Counter	DMA-Tx	RC		697
0x087A4	TXDGBCL	DMA Good Tx Byte Counter Low	DMA-Tx	RC		697
0x087A8	TXDGBCH	DMA Good Tx Byte Counter High	DMA-Tx	RC		697
0x040A4	RUC	Receive Undersize Count	STAT	RC		697
0x040A8	RFC	Receive Fragment Count	STAT	RC		698
0x040AC	ROC	Receive Oversize Count	STAT	RC		698
0x040B0	RJC	Receive Jabber Count	STAT	RC		698
0x040B4	MNGPRC	Management Packets Received Count	STAT	RO		698
0x040B8	MNGPDC	Management Packets Dropped Count	STAT	RO		698
0x040C0	TORL	Total Octets Received	STAT	RC		699
0x040C4	TORH	Total Octets Received	STAT	RC		699
0x040D0	TPR	Total Packets Received	STAT	RC		699
0x040D4	TPT	Total Packets Transmitted	STAT	RC		699
0x040D8	PTC64	Packets Transmitted (64 Bytes) Count	STAT	RC		700

Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x040DC	PTC127	Packets Transmitted [65–127 Bytes] Count	STAT	RC		700
0x040E0	PTC255	Packets Transmitted [128–255 Bytes] Count	STAT	RC		700
0x040E4	PTC511	Packets Transmitted [256–511 Bytes] Count	STAT	RC		700
0x040E8	PTC1023	Packets Transmitted [512–1023 Bytes] Count	STAT	RC		701
0x040EC	PTC1522	Packets Transmitted [Greater than 1024 Bytes] Count	STAT	RC		701
0x040F0	MPTC	Multicast Packets Transmitted Count	STAT	RC		701
0x040F4	BPTC	Broadcast Packets Transmitted Count	STAT	RC		701
0x04010	MSPDC	MAC short Packet Discard Count	STAT	RC		702
0x04120	XEC	XSUM Error Count	STAT	RC		702
0x02300+4*n, n=0...31	RQSMR[n]	Receive Queue Statistic Mapping Registers	DMA-Rx	RW		702
0x02F40	RXDSTATCTRL	Rx DMA Statistic Counter Control	DMA-Tx	RW		703
0x08600+4*n, n=0...31 / 0x07300+4*n, n=0…7	TQSM[n]	Transmit Queue Statistic Mapping Registers	DMA-Tx	RW		703
0x01030+0x40*n, n=0...15	QPRC[n]	Queue Packets Received Count	DMA-Rx	RC		704
0x01430+0x40*n, n=0...15	QPRDC[n]	Queue Packets Received Drop Count	DMA-Rx	RC		704
0x1034+0x40*n, n=0...15	QBRC_L[n]	Queue Bytes Received Count Low	DMA-Rx	RC		704
0x1038+0x40*n, n=0...15	QBRC_H[n]	Queue Bytes Received Count High	DMA-Rx	RC		704
0x08680+0x4*n, n=0...15 / 0x06030+0x40*n, n=0...15	QPTC	Queue Packets Transmitted Count	DMA-Tx	RC		704
0x08700+0x8*n, n=0...15	QBTC_L[n]	Queue Bytes Transmitted Count Low	DMA-Tx	RC		705
0x08704+0x8*n, n=0...15	QBTC_H[n]	Queue Bytes Transmitted Count High	DMA-Tx	RC		705
0x05118	FCCRC	FC CRC Error Count	Rx-Filter	RC		705
0x0241C	FCOERPDC	FCoE Rx Packets Dropped Count	DMA-Rx	RC		706

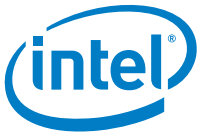


Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x02424	FCLAST	FC Last Error Count	DMA-Rx	RC		706
0x02428	FCOEPRC	FCoE Packets Received Count	DMA-Rx	RC		706
0x0242C	FCOEDWRC	FCOE DWord Received Count	DMA-Rx	RC		706
0x08784	FCOEPTC	FCoE Packets Transmitted Count	DMA-Tx	RC		706
0x08788	FCOEDWTC	FCoE DWord Transmitted Count	DMA-Tx	RC		707
Wake-Up Control Registers						
0x05800	WUC	Wake Up Control Register	Rx-Filter	RW		708
0x05808	WUFC	Wake Up Filter Control Register	Rx-Filter	RW		708
0x5838	IPAV	IP Address Valid	Rx-Filter	RW		709
0x05840+8*n, n = 0...3	IP4AT[n]	IPv4 Address Table	Rx-Filter	RW		710
0x05880+4*n, n = 0...3	IP6AT[n]	IPv6 Address Table	Rx-Filter	RW		710
0x05900	WUPL	Wake Up Packet Length	Rx-Filter	RO		710
0x05A00+4*n, n=0...31	WUPM[n]	Wake Up Packet Memory (128 Bytes)	Rx-Filter	RO		710
0x09000 — 0x093FC, 0x09800 — 0x099FC	FHFT	Flexible Host Filter Table registers	Rx-Filter	RW		710
Management Filters Registers						
0x5010 +4*n, n=0...7	MAVTV[n]	Management VLAN TAG Value	Rx-Filter	RW		712
0x5030+4*n, n=0...7	MFUTP[n]	Management Flex UDP/TCP Ports	Rx-Filter	RW		712
0x05190+4*n, n=0...3	METF[n]	Management Ethernet Type Filters	Rx-Filter	RW		713
0x05820	MANC	Management Control Register	Rx-Filter	RW		713
0x5824	MFVAL	Manageability Filters Valid	Rx-Filter	RW		714
0x5860	MANC2H	Management Control To Host Register	Rx-Filter	RW		714
0x5890+4*n, n=0...7	MDEF[n]	Manageability Decision Filters	Rx-Filter	RW		715
0x05160+4*n, n=0...7	MDEF_EXT[n]	Manageability Decision Filters	Rx-Filter	RW		716
0x58B0+0x10*m+4*n, m=0...3, n=0...3	MIPAF	Manageability IP Address Filter	Rx-Filter	RW		716

Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x5910+8*n, n=0...3	MMAL[n]	Manageability Ethernet MAC Address Low	Rx-Filter	RW		717
0x5914+8*n, n=0...3	MMAH[n]	Manageability Ethernet MAC Address High	Rx-Filter	RW		717
0x09400-0x097FC	FTFT	Flexible TCO Filter Table registers	Rx-Filter	RW		717
0x015F14	LSWFW	LinkSec SW/FW Interface	MNG	RO		718
Time Sync (IEEE 1588) Registers						
0x05188	TSYNCRXCTL	Rx Time Sync Control Register	Rx-Filter	RW		720
0x051E8	RXSTMPL	Rx Timestamp Low	Rx-Filter	RO		720
0x051A4	RXSTMPH	Rx Timestamp High	Rx-Filter	RO		720
0x051A0	RXSATRL	Rx Timestamp Attributes Low	Rx-Filter	RO		721
0x051A8	RXSATRH	Rx Timestamp Attributes High	Rx-Filter	RO		721
0x05120	RXMTRL	Rx Message Type Register Low	Rx-Filter	RW		721
0x08C00	TSYNCTXCTL	Tx Time Sync Control Register	SEC-Tx	RW		721
0x08C04	TXSTMPL	Tx Timestamp Value Low	SEC-Tx	RO		722
0x08C08	TXSTMPH	Tx Timestamp Value High	SEC-Tx	RO		722
0x08C0C	SYSTIML	System Time Register Low	SEC-Tx	RW		722
0x08C10	SYSTIMH	System Time Register High	SEC-Tx	RW		722
0x08C14	TIMINCA	Increment Attributes Register	SEC-Tx	RW		722
0x08C18	TIMADJL	Time Adjustment Offset Register low	SEC-Tx	RW		723
0x08C1C	TIMADJH	Time Adjustment Offset Register High	SEC-Tx	RW		723
0x08C20	TSAUXC	TimeSync Auxiliary Control Register	SEC-Tx	RW		723
0x08C24	TRGTTIML0	Target Time Register 0 Low	SEC-Tx	RW		724
0x08C28	TRGTTIMH0	Target Time Register 0 High	SEC-Tx	RW		724
0x08C2C	TRGTTIML1	Target Time Register 1 Low	SEC-Tx	RW		724
0x08C30	TRGTTIMH1	Target Time Register 1 High	SEC-Tx	RW		724

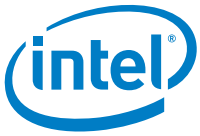


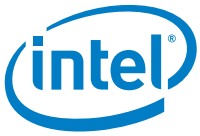
Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x08C3C	AUXSTMPL0	Auxiliary Time Stamp 0 Register low	SEC-Tx	RO		725
0x08C40	AUXSTMPH0	Auxiliary Time Stamp 0 Register high	SEC-Tx	RO		725
0x08C44	AUXSTMPL1	Auxiliary Time Stamp 1 Register low	SEC-Tx	RO		725
0x08C48	AUXSTMPH1	Auxiliary Time Stamp 1 Register high	SEC-Tx	RO		725
Virtualization PF Registers						
0x051B0	PFVTCTL	PF Virtual Control Register	Rx-Filter	RW		726
0x04B00+4*n, n=0...63	PFMailbox[n]	PF Mailbox	Target	RW		726
0x00710+4*n, n=0...3	PFMBICR[n]	PF Mailbox Interrupt Causes Register	Target	RW1C		727
0x00720+4*n, n=0...1	PFMBIMR[n]	PF Mailbox Interrupt Mask Register	Target	RW		727
0x00600, 0x001C0	PFVFLRE[n]	PF VFLR Events Indication	Target	RO		727
0x00700+4*n, n=0...1	PFVFLREC[n]	PF VFLR Events Clear	Target	W1C		728
0x051E0+4*n, n=0...1	PFVFRE[n]	PF VF Receive Enable		RW		728
0x08110+4*n, n=0...1	PFVFTE[n]	PF VF Transmit Enable	DMA-Tx	RW		728
0x02F04	PFQDE	PF Queue Drop Enable Register	DMA-Rx	RW		728
0x05180+4 *n, n=0...1	PFVMTXSW[n]	PF VM Tx Switch Loopback Enable	Rx-Filter	RW		729
0x08200+4*n, n=0...7	PFVFSPOOF[n]	PF VF Anti Spoof Control	DMA-Tx	RW		729
0x08220	PFDTXGSWC	PF DMA Tx General Switch Control	DMA-Tx	RW		729
0x08000+4*n, n=0...63	PFVMVIR[n]	PF VM VLAN Insert Register	DMA-Tx	RW		730
0x0F000+4*n, n=0...63	PFVML2FLT[n]	PF VM L2 Control Register	Rx-Filter	RW		730
0x0F100+4*n, n=0...63	PFVLVF[n]	PF VM VLAN Pool Filter	Rx-Filter	RW		730
0x0F200+4*n, n=0...127	PFVLVFB[n]	PF VM VLAN Pool Filter Bitmap	Rx-Filter	RW		731
0x0F400+4*n, n=0...127	PFUTA[n]	PF Unicast Table Array	Rx-Filter	RW		731
0x0F600+4*n, n= 0...3	PFMRCTL[n]	PF Mirror Rule Control	Rx-Filter	RW		732

Table 8-2 Register Summary (Continued)

Offset / Alias Offset	Abbreviation	Name	Block	RW	Reset Source	Page
0x0F610+4*n, n= 0...7	PFMRVLAN[n]	PF Mirror Rule VLAN	Rx-Filter	RW		732
0x0F630+4*n, n= 0...7	PFMRVM[n]	PF Mirror Rule Pool	Rx-Filter	RW		732

Note: (*) The MAC Manageability Control Register is read only to the host and read/write to manageability.



8.2.3 Detailed Register Descriptions — PF

8.2.3.1 General Control Registers

8.2.3.1.1 Device Control Register — CTRL (0x00000 / 0x00004; RW)

CTRL is also mapped to address 0x00004 to maintain compatibility with previous devices.

Field	Bit(s)	Init Val	Description
Reserved	1:0	0b	Reserved. Write as 0b for future compatibility.
PCIe Master Disable	2	0b	When set, the 82599 blocks new master requests, including manageability requests, by using this function. Once no master requests are pending by using this function, the *PCIe Master Enable Status* bit is cleared.
LRST	3	0b	Link Reset. This bit performs a reset of the MAC, PCS, and auto negotiation functions and the entire Intel® 82599 10 GbE Controller (software reset) resulting in a state nearly approximating the state following a power-up reset or internal PCIe reset, except for the system PCI configuration. Normally 0b, writing 1b initiates the reset. This bit is self-clearing. Also referred to as MAC reset.
Reserved	25:4	0b	Reserved.
RST	26	0b	Device Reset. This bit performs a complete reset of the 82599, resulting in a state nearly approximating the state following a power-up reset or internal PCIe reset, except for the system PCI configuration. Normally 0b, writing 1b initiates the reset. This bit is self-clearing. Also referred to as a software reset or global reset.
Reserved	31:27	0x0	Reserved.

LRST and RST can be used to globally reset the entire Intel® 82599 10 GbE Controller. This register is provided primarily as a last-ditch software mechanism to recover from an indeterminate or suspected hung hardware state. Most registers (receive, transmit, interrupt, statistics, etc.) and state machines are set to their power-on reset values, approximating the state following a power-on or PCI reset. However, PCIe Configuration registers are not reset, thereby leaving the 82599 mapped into system memory space and accessible by a software device driver.

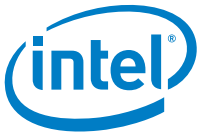
To ensure that a global device reset has fully completed and that the 82599 responds to subsequent accesses, programmers must wait approximately 1 ms after setting before attempting to check if the bit has cleared or to access (read or write) any other device register.

8.2.3.1.2 Device Status Register — STATUS (0x00008; RO)

Field	Bit(s)	Init Val	Description
Reserved	1:0	0b	Reserved.
LAN ID	3:2	0b	LAN ID. Provides software a mechanism to determine the device LAN identifier for this MAC. Read as: [0,0] LAN 0, [0,1] LAN 1.
Reserved	6:4	0b	Reserved.
LinkUp	7	0b	Linkup Status Indication. This bit is Read/Write, and is useful for IOV mode. The PF software driver sets it according to Links register and PHY state. It is reflected in the VFSTATUS register indicating linkup to the VF drivers.
Reserved	9:8	0b	Reserved.
Num VFs	17:10	0x0	The *Num VFs* field reflects the value of the Num VFs in the IOV capability structure *Note:* Bit 17 is always 0b.
IOV Active	18	0b	The *IO Active* bit, reflects the value of the *VF Enable (VFE)* bit in the IOV Control/ Status register.
PCIe Master Enable Status	19	1b	This is a status bit of the appropriate CTRL.PCIe *Master Disable* bit. 0b = Associated LAN function does not issue any master request and all previously issued requests are complete. 1b = Associated LAN function can issue master requests.
Reserved	31:20	0b	Reserved. Reads as 0b.

8.2.3.1.3 Extended Device Control Register — CTRL_EXT (0x00018; RW)

Field	Bit(s)	Init Val	Description
Reserved	13:0	0x0	Reserved.
PFRSTD (SC)	14	0b	PF Reset Done. When set, the RSTI bit in all the VFMailbox registers are cleared and the RSTD bit in all the VFMailbox regs is set.
Reserved	15	0b	Reserved.
NS_DIS	16	0b	No Snoop Disable. When set to 1b, the 82599 does not set the no snoop attribute in any PCIe packet, independent of PCIe configuration and the setting of individual no snoop enable bits. When set to 0b, behavior of no snoop is determined by PCIe configuration and the setting of individual no snoop enable bits. *Note:* If legacy descriptors are used, this bit should be set to 1b. This bit must be set during Rx flow initialization for proper device operation.



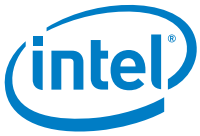
Field	Bit(s)	Init Val	Description
RO_DIS	17	0b	Relaxed Ordering Disable. When set to 1b, the device does not request any relaxed ordering transactions. When this bit is cleared and the *Enable Relaxed Ordering* bit in the Device Control register is set, the device requests relaxed ordering transactions per queues as configured in the DCA_RXCTRL[n] and DCA_TXCTRL[n] registers.
Reserved	25:18	0b	Reserved.
Extended VLAN	26	0b	Extended VLAN. When set, all incoming Rx packets are expected to have at least one VLAN with the Ether type as defined in EXVET register. The packets can have an inner-VLAN that should be used for all filtering purposes. All Tx packets are expected to have at least one VLAN added to them by the host. In the case of an additional VLAN request (VLE), the inner-VLAN is added by the hardware after the outer-VLAN is added by the host. This bit should only be reset by a PCIe reset and should only be changed while Tx and Rx processes are stopped. The exception to this rule are MAC control packets such as flow control, 802.1x, LACP, etc. that never carry a VLAN tag of any type.
Reserved	27	0b	Reserved.
DRV_LOAD	28	0b	Driver loaded and the corresponding network interface is enabled. This bit should be set by the software device driver after it was loaded and cleared when it unloads or at PCIe soft reset. The Manageability Controller (MC) loads this bit as an indication that the driver successfully loaded to it.
Reserved	31:29	0b	Reserved.

8.2.3.1.4 Extended SDP Control — ESDP (0x00020; RW)

This register is initialized only at LAN Power Good preserving the SDP states across software and PCIe resets. Some specific I/O pins are initialized in other resets in native mode as expected for the specific behavior and described explicitly as follows.

Field	Bit(s)	Init Val	Description
SDP0_DATA	0	0b[1]	SDP0 Data Value. Used to read (write) a value of the software-controlled I/O pin SDP0. If SDP0 is configured as an output (SDP0_IODIR = 1b), this bit controls the value driven on the pin. If SDP0 is configured as an input, all reads return the current value of the pin.
SDP1_DATA	1	0b[1]	SDP1 Data Value. Used to read (write) a value of the software-controlled I/O pin SDP1. If SDP1 is configured as an output (SDP1_IODIR = 1b), this bit controls the value driven on the pin. If SDP1 is configured as an input, all reads return the current value of the pin.
SDP2_DATA	2	0b[1]	SDP2 Data Value. Used to read (write) a value of software-controlled I/O pin SDP2. If SDP2 is configured as an output (SDP2_IODIR = 1b), this bit controls the value driven on the pin. If SDP2 is configured as an input, all reads return the current value of the pin.

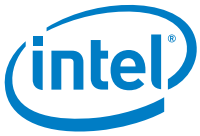
Field	Bit(s)	Init Val	Description
SDP3_DATA	3	0b[1]	SDP3 Data Value. Used to read (write) a value of the software-controlled I/O pin SDP3. If SDP3 is configured as an output (SDP3_IODIR = 1b), this bit controls the value driven on the pin. If SDP3 is configured as an input, all reads return the current value of the pin.
SDP4_DATA[2]	4	0b	SDP4 Data Value. Used to read (write) a value of the software-controlled I/O pin SDP4. If SDP4 is configured as an output (SDP4_IODIR = 1b), this bit controls the value driven on the pin. If SDP4 is configured as an input, all reads return the current value of the pin.
SDP5_DATA	5	0b	SDP5 Data Value. Used to read (write) a value of the software-controlled I/O pin SDP5. If SDP5 is configured as an output (SDP5_IODIR = 1b), this bit controls the value driven on the pin. If SDP5 is configured as an input, all reads return the current value of the pin.
SDP6_DATA	6	0b	SDP6 Data Value. Used to read (write) a value of the software-controlled I/O pin SDP6. If SDP6 is configured as an output (SDP6_IODIR = 1b), this bit controls the value driven on the pin. If SDP6 is configured as an input, all reads return the current value of the pin.
SDP7_DATA	7	0b	SDP7 Data Value. Used to read (write) a value of the software-controlled I/O pin SDP7. If SDP7 is configured as an output (SDP7_IODIR = 1b), this bit controls the value driven on the pin. If SDP7 is configured as an input, all reads return the current value of the pin.
SDP0_IODIR	8	0b[1]	SDP0 Pin Directionality. Controls whether or not software-controlled pin SDP0 is configured as an input or output. 0b = Input 1b = Output
SDP1_IODIR	9	0b[1]	SDP1 Pin Directionality. Controls whether or not software-controlled pin SDP1 is configured as an input or output. 0b = Input 1b = Output
SDP2_IODIR	10	0b[1]	SDP2 Pin Directionality. Controls whether or not software-controlled pin SDP2 is configured as an input or output. 0b = Input 1b = Output
SDP3_IODIR	11	0b[1]	SDP3 Pin Directionality. Controls whether or not software-controlled pin SDP3 is configured as an input or output. 0b = Input 1b = Output
SDP4_IODIR[2]	12	0b	SDP4 Pin Directionality. Controls whether or not software-controlled pin SDP4 is configured as an input or output. 0b = Input 1b = Output



Field	Bit(s)	Init Val	Description
SDP5_IODIR	13	0b	SDP5 Pin Directionality. Controls whether or not software-controlled pin SDP5 is configured as an input or output. 0b = Input 1b = Output
SDP6_IODIR	14	0b	SDP6 Pin Directionality. Controls whether or not software-controlled pin SDP6 is configured as an input or output. 0b = Input 1b = Output
SDP7_IODIR	15	0b	SDP7 Pin Directionality. Controls whether or not software-controlled pin SDP7 is configured as an input or output. 0b = Input 1b = Output
SDP0_NATIVE	16	0b	SDP0 Operating Mode. 0b = Generic software controlled I/O by SDP0_DATA and SDP0_IODIR. 1b = Reserved.
SDP1_NATIVE	17	0b[1]	SDP1 Operating Mode. 0b = Generic software controlled I/O by SDP1_DATA and SDP1_IODIR. 1b = Native mode operation (connected to hardware function). In this mode, the SDP1_IODIR must be set to 1b.
SDP2_NATIVE	18	0b	SDP2 operating mode. 0b = Generic software controlled IO by SDP2_DATA and SDP2_IODIR. 1b = Native mode operation (Connected to hardware function). In this mode pin functions as defined by the SDP2_TSync_TT1 bit
SDP3_NATIVE	19	0b	SDP3 Operating Mode. 0b = Generic software controlled I/O by SDP3_DATA and SDP3_IODIR. 1b = Native mode operation (connected to hardware function). In this mode pin functions as defined by the SDP3_TSync_TT0 bit.
SDP4_NATIVE[2]	20	0b	SDP4 Operating Mode. 0b = Generic software controlled I/O by SDP4_DATA and SDP4_IODIR. 1b = Native mode operation (connected to hardware function). Drives optical module reset according to functionality defined by the SDP4_Function bit.
SDP5_NATIVE	21	0b	SDP5 Operating Mode. 0b = Generic software controlled I/O by SDP5_DATA and SDP5_IODIR. 1b = Native mode operation (connected to hardware function). Drives optical module transmit disable according to functionality defined by the SDP5_Function bit.
SDP6_NATIVE	22	0b	SDP6 Operating Mode. 0b = Generic software controlled I/O by SDP6_DATA and SDP6_IODIR. 1b = Native mode operation (connected to hardware function). In this mode, pin functions as defined by the SDP6_TSync_TT1 bit.
SDP7_NATIVE	23	0b	SDP7 Operating Mode. 0b = Generic software controlled I/O by SDP7_DATA and SDP7_IODIR. 1b = Native mode operation (connected to hardware function). In this mode, pin functions as defined by the SDP7_TSync_TT0 bit.
Reserved	25:24	0	Reserved.

Field	Bit(s)	Init Val	Description
SDP2_TSync_TT1	26	0b	SDP2 Native Mode Functionality (SDP2_NATIVE = 1). 0b = TS0 functionality. Samples IEEE 1588 time stamp into Auxiliary Time Stamp 0 register on level change of SDP2 signal (For TS0 functionality, SDP2_IODIR should be configured as input). 1b = TT1 functionality. Asserts SDP2 to 1 when IEEE 1588 time stamp equals Target Time register 1 (For TT1 functionality, SDP2_IODIR should be configured as output).
SDP3_TSync_TT0	27	0b	SDP3 Native Mode Functionality (SDP3_NATIVE = 1). 0b = TS1 functionality. Samples IEEE 1588 time stamp into Auxiliary Time Stamp 1 register on level change of SDP3 signal (For TS1 functionality, SDP3_IODIR should be configured as input). 1b = TT0 functionality. Asserts SDP3 to 1b when IEEE 1588 time stamp equals Target Time register 0 (For TT0 functionality, SDP3_IODIR should be configured as output).
SDP4_Function[2]	28	0b	SDP4 Native Mode Functionality (SDP4_NATIVE = 1). 0b = Pin functionality is driven by software (SDP4_data bit) except when the MAC is reset or when entering D3 power state when management functionality is disabled. In the previous case SDP4 pin moves to tri-state (by resetting SDP4_IODIR bit) and optical module is reset by placing an appropriate external pull-up or pull-down resistor on the SDP4 pin. 1b = SDP4 pin is driven high when the MAC is reset or powered down (D3 state). SDP4_IODIR should be configured as output for this functionality.
SDP5_Function	29	0b	SDP5 Native Mode Functionality (SDP5_NATIVE = 1). 0b = Pin functionality is driven by software (SDP5_data bit) except when the MAC is reset or when entering D3 power state when management functionality is disabled. In the previous case, SDP5 pin moves to tri-state (by resetting SDP5_IODIR bit) and optical module transmission is disabled by placing an appropriate external pull-up or pull-down resistor on the SDP5 pin. 1b = SDP5 pin is driven high when the MAC is reset or powered down (D3 state). SDP5_IODIR should be configured as output for this functionality.
SDP6_TSync_TT1	30	0b	SDP6 Native Mode Functionality (SDP6_NATIVE = 1). 0b = CLK0 functionality. Drives a reference clock with the frequency defined in the Frequency Out 0 Control register (For CLK0 functionality, SDP6_IODIR should be configured as output). 1b = TT1 functionality. Asserts SDP6 to 1b when IEEE 1588 time stamp equals Target Time register 1 (For TT1 functionality, SDP6_IODIR should be configured as output).
SDP7_TSync_TT0	31	0b	SDP7 Native Mode Functionality (SDP7_NATIVE = 1). 0b = CLK1 functionality. Drives a reference clock with the frequency defined in the Frequency Out 1 Control register (for CLK1 functionality, SDP7_IODIR should be configured as output). 1b = TT0 functionality. Asserts SDP7 to 1b when IEEE 1588 time stamp equals Target Time register 1 (For TT0 functionality, SDP7_IODIR should be configured as output).

1. Initial value can be configured using the EEPROM.
2. SDP4 in port 0 is a dedicated input pin for Security enablement. See Section 4.6.12.



8.2.3.1.5 I2C Control — I2CCTL (0x00028; RW)

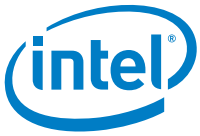
Field	Bit(s)	Init Val	Description
I2C_CLK_IN	0	0b	I2C_CLK In Value. Provides the value of I2C_CLK (input from external PAD). This bit is RO.
I2C_CLK_OUT	1	1b	I2C_CLK Out Value. Used to drive the value of I2C_CLK (output to PAD).
I2C_DATA_IN	2	0b	I2C_DATA In Value. Provides the value of I2C_DATA (input from external PAD). This bit is RO.
I2C_DATA_OUT	3	1b	I2C_DATA Out Value. Used to drive the value of I2C_DATA (output to PAD).
Reserved	31:4	0x0	Reserved.

8.2.3.1.6 LED Control — LEDCTL (0x00200; RW)

Field	Bit(s)	Init Val	Description
LED0_MODE	3:0	0x0[1]	LED0 Mode. This field specifies the control source for the LED0 output. An initial value of 0000b selects the LINK_UP indication.
Reserved	4	0b[1]	Reserved.
GLOBAL_BLINK_MODE	5	0b[1]	GLOBAL Blink Mode. This field specifies the blink mode of all LEDs. 0b = Blink at 200 ms on and 200 ms off. 1b = Blink at 83 ms on and 83 ms off.
LED0_IVRT	6	0b[1]	LED0 Invert. This field specifies the polarity/inversion of the LED source prior to output or blink control. By default the output drives the cathode of the LED so when the LED output is 0b the LED is on. 0b = LED output is active low. 1b = LED output is active high.
LED0_BLINK	7	0b[1]	LED0 Blink. This field specifies whether or not to apply blink logic to the (inverted) LED control source prior to the LED output. 0b = Do not blink LED output. 1b = Blink LED output.
LED1_MODE	11:8	0x1[1]	LED1 Mode. This field specifies the control source for the LED1 output. An initial value of 0001b selects the 10 Gb/s link indication.
Reserved	13:12	0b[1]	Reserved.

Field	Bit(s)	Init Val	Description
LED1_IVRT	14	0b[1]	LED1 Invert. This field specifies the polarity/inversion of the LED source prior to output or blink control. By default the output drives the cathode of the LED so when the LED output is 0b the LED is on. 0b = LED output is active low. 1b = LED output is active high.
LED1_BLINK	15	1b[1]	LED1 Blink. This field specifies whether or not to apply blink logic to the (inverted) LED control source prior to the LED output. 0b = Do not blink LED output. 1b = Blink LED output.
LED2_MODE	19:16	0x4[1]	LED2 Mode. This field specifies the control source for the LED0 output. An initial value of 0100 selects LINK/ACTIVITY indication.
Reserved	21:20	0[1]	Reserved
LED2_IVRT	22	0[1]	LED2 Invert. This field specifies the polarity/inversion of the LED source prior to output or blink control. By default the output drives the cathode of the LED so when the LED output is 0b the LED is on. 0b = LED output is active low. 1b = LED output is active high.
LED2_BLINK	23	0[1]	LED2 Blink. This field specifies whether or not to apply blink logic to the (inverted) LED control source prior to the LED output. 0b = Do not blink LED output. 1b = Blink LED output.
LED3_MODE	27:24	0x5[1]	LED3 Mode. This field specifies the control source for the LED0 output. An initial value of 0101b selects the 1 Gb/s link indication.
Reserved	29:28	0b[1]	Reserved.
LED3_IVRT	30	0b[1]	LED3 Invert. This field specifies the polarity/inversion of the LED source prior to output or blink control. By default the output drives the cathode of the LED so when the LED output is 0b the LED is on. 0b = LED output is active low. 1b = LED output is active high.
LED3_BLINK	31	0b[1]	LED3 Blink. This field specifies whether or not to apply blink logic to the (inverted) LED control source prior to the LED output. 0b = Do not blink LED output. 1b = Blink LED output.

1. These bits are read from the EEPROM.



The following mapping is used to specify the LED control source (MODE) for each LED output:

MODE	Selected Mode	Source Indication
0000b	LINK_UP	Asserted or blinking according to the LEDx_BLINK setting when any speed link is established and maintained.
0001b	LINK_10G	Asserted or blinking according to the LEDx_BLINK setting when a 10 Gb/s link is established and maintained.
0010b	MAC_ACTIVITY	Active when link is established and packets are being transmitted or received. In this mode, the LEDx_BLINK must be set.
0011b	FILTER_ACTIVITY	Active when link is established and packets are being transmitted or received that passed MAC filtering. In this mode, the LEDx_BLINK must be set.
0100b	LINK/ACTIVITY	Asserted steady when link is established and there is no transmit or receive activity. Blinking when there is link and receive or Transmit activity.
0101b	LINK_1G	Asserted or blinking according to the LEDx_BLINK setting when a 1 Gb/s link is established and maintained.
0110	LINK_100	Asserted or blinking according to the LEDx_BLINK setting when a 100 Mb/s link is established and maintained.
0111b:1101b	Reserved	Reserved.
1110b	LED_ON	Always asserted or blinking according to the LEDx_BLINK setting.
1111b	LED_OFF	Always de-asserted.

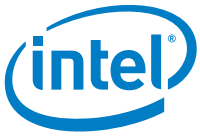
8.2.3.1.7 Extended VLAN Ether Type — EXVET (0x05078; RW)

Field	Bit(s)	Init Val	Description
Reserved	15:0	0x0	Reserved.
VET EXT	31:16	0x8100	Outer-VLAN Ether Type (VLAN Tag Protocol Identifier - TPID). *Note:* This field appears in little endian (MS byte first on the wire).

8.2.3.2 EEPROM/Flash Registers

8.2.3.2.1 EEPROM/Flash Control Register — EEC (0x10010; RW)

Field	Bit(s)	Init Val	Description
EE_SK	0	0b	Clock input to the EEPROM. When EE_GNT is set to 1b, the EE_SK output signal is mapped to this bit and provides the serial clock input to the EEPROM. Software clocks the EEPROM via toggling this bit with successive writes.
EE_CS	1	0b	Chip select input to the EEPROM. When EE_GNT is set to 1b, the EE_CS output signal is mapped to the chip select of the EEPROM device. Software enables the EEPROM by writing a 0b to this bit.
EE_DI	2	0b	Data input to the EEPROM. When EE_GNT is set to 1b, the EE_DI output signal is mapped directly to this bit. Software provides data input to the EEPROM via writes to this bit.
EE_DO (RO field)	3	X	Data output bit from the EEPROM. The EE_DO input signal is mapped directly to this bit in the register and contains the EEPROM data output. This bit is read-only from a software perspective; writes to this bit have no effect.
FWE	5:4	01b	Flash Write Enable Control. These two bits control whether or not writes to the Flash are allowed. 00b = Flash erase (along with bit 31 in the FLA register). 01b = Flash writes disabled. 10b = Flash writes enabled. 11b = Not allowed.
EE_REQ	6	0b	Request EEPROM Access. Software must write a 1b to this bit to get direct EEPROM access. It has access when EE_GNT is set to 1b. When software completes the access, it must then write a 0b.
EE_GNT (RO field)	7	0b	Grant EEPROM Access. When this bit is set to 1b, software can access the EEPROM using the EE_SK, EE_CS, EE_DI, and EE_DO bits.
EE_PRES (RO field)	8	(see desc.)	EEPROM Present. Setting this bit to 1b indicates that an EEPROM is present and has the correct signature field. This bit is read-only.
Auto_RD (RO field)	9	0b	EEPROM Auto-Read Done. When set to 1b, this bit indicates that the auto-read by hardware from the EEPROM is done. This bit is also set when the EEPROM is not present or when its signature field is not valid.
Reserved	10	1b	Reserved.
EE_Size (RO field)	14:11	0010b[1]	EEPROM Size. This field defines the size of the EEPROM (see Table 8-3).



Field	Bit(s)	Init Val	Description
PCI _ANA_done (RO field)	15	0b	PCIe Analog Done. When set to 1b, indicates that the PCIe analog section read from EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid.
PCI _Core_done (RO field)	16	0b	PCIe Core Done. When set to 1b, indicates that the Core analog section read from EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid. *Note:* This bit returns the relevant done indication for the function that reads the register.
PCI _genarl_done (RO field)	17	0b	PCIe General Done. When set to 1b, indicates that the PCIe general section read from the EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid.
PCI_FUNC_DONE (RO field)	18	0b	PCIe Function Done. When set to 1b, indicates that the PCIe function section read from EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid. *Note:* This bit returns the relevant done indication for the function that reads the register.
CORE_DONE (RO field)	19	0b	Core Done. When set to 1b, indicates that the Core analog section read from the EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid. *Note:* This bit returns the relevant done indication for the function that reads the register.
CORE_CSR_DONE (RO field)	20	0b	Core CSR Done. When set to 1b, indicates that the Core CSR section read from the EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid. *Note:* This bit returns the relevant done indication for the function that reads the register.
MAC_DONE (RO field)	21	0b	MAC Done. When set to 1b, indicates that the MAC section read from the EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid. *Note:* This bit returns the relevant done indication for the function that reads the register.
Reserved	31:22	0x0	Reserved. Reads as 0b.

1. These bits are read from the EEPROM.

Table 8-3 EEPROM Sizes (Bits 14:11)

Field Value	EEPROM Size	EEPROM Address Size
0100b	16 Kb	2 bytes
0101b	32 Kb	2 bytes
0110b	64 Kb	2 bytes
0111b	128 Kb	2 bytes
1000b	256 Kb	2 bytes
1001b:1111b	Reserved	Reserved

This register provides software-direct access to the EEPROM. Software can control the EEPROM by successive writes to this register. Data and address information is clocked into the EEPROM by software toggling the EESK bit (2) of this register. Data output from the EEPROM is latched into bit 3 of this register via the internal 62.5 MHz clock and can be accessed by software via reads of this register.

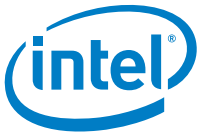
Note: Attempts to write to the Flash device when writes are disabled (FWE = 01b) should not be attempted. Behavior after such an operation is undefined, and might result in component and/or system hangs.

8.2.3.2.2 EEPROM Read Register — EERD (0x10014; RW)

Field	Bit(s)	Init Val	Description
START	0	0b	Start Read. Writing a 1b to this bit causes the EEPROM to read a 16-bit word at the address stored in the EE_ADDR field and then stores the result in the EE_DATA field. This bit is self-clearing.
DONE	1	0b	Read Done. Set this bit to 1b when the EEPROM read completes. Set this bit to 0b when the EEPROM read is in progress. *Note:* Writes by software are ignored.
ADDR	15:2	0x0	Read Address. This field is written by software along with *Start Read* to indicate that the address of the word to read.
DATA	31:16	0x0	Read Data. Data returned from the EEPROM read.

This register is used by software to cause the 82599 to read individual words in the EEPROM. To read a word, software writes the address to the *Read Address* field and simultaneously writes a 1b to the Start Read field. The 82599 reads the word from the EEPROM and places it in the *Read Data* field, setting the *Read Done* field to 1b. Software can poll this register, looking for a 1b in the *Read Done* field and then using the value in the *Read Data* field.

When this register is used to read a word from the EEPROM, that word is not written to any of the 82599's internal registers even if it is normally a hardware-accessed word.



8.2.3.2.3 Flash Access Register — FLA (0x1001C; RW)

Field	Bit(s)	Init Val	Description
FL_SCK	0	0b	Clock input to the Flash. When FL_GNT is set to 1b, the FL_SCK output signal is mapped to this bit and provides the serial clock input to the Flash. Software clocks the Flash via toggling this bit with successive writes.
FL_CE	1	0b	Chip select input to the Flash. When FL_GNT is set to 1b, the FL_CE output signal is mapped to the chip select of the Flash device. Software enables the Flash by writing a 0b to this bit.
FL_SI	2	0b	Data input to the Flash. When FL_GNT is set to 1b, the FL_SI output signal is mapped directly to this bit. Software provides data input to the Flash via writes to this bit.
FL_SO	3	X	Data output bit from the Flash. The FL_SO input signal is mapped directly to this bit in the register and contains the Flash serial data output. This bit is read-only from a software perspective. *Note:* Writes to this bit have no effect.
FL_REQ	4	0b	Request Flash Access. Software must write a 1b to this bit to get direct Flash access. It has access when FL_GNT is set to 1b. When software completes the access, it must then write a 0b.
FL_GNT	5	0b	Grant Flash Access. When this bit is set to 1b, software can access the Flash using the FL_SCK, FL_CE, FL_SI, and FL_SO bits.
Reserved	29:6	0b	Reserved. Reads as 0b.
FL_BUSY	30	0b	Flash Busy. This bit is set to 1b while a write or an erase to the Flash is in progress, While this bit is cleared (reads as 0b), software can access to write a new byte to the Flash. *Note:* This bit is read-only from a software perspective.
FL_ER	31	0b	Flash Erase Command. This command is sent to the Flash only if bits 5:4 of register EEC are also set to 00b. This bit is auto-cleared and reads as 0b.

This register provides software direct access to the Flash. Software can control the Flash by successive writes to this register. Data and address information is clocked into the EEPROM by software toggling FL_SCK in this register. Data output from the Flash is latched into bit 3 of this register via the internal 125 MHz clock and can be accessed by software via reads of this register.

Note: In the 82599, the FLA register is only reset at LAN_PWR_GOOD as opposed to legacy devices at software reset.

8.2.3.2.4 Manageability EEPROM Control Register — EEMNGCTL (0x10110; RW)

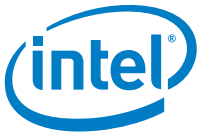
Note: This register can be read/write by manageability firmware and is read-only to host software.

Field	Bit(s)	Init Val	Description
ADDR	14:0	0x0	Address. This field is written by manageability along with *Start* bit and the *Write* bit to indicate which EEPROM address to read or write.
START	15	0b	Start. Writing a 1b to this bit causes the EEPROM to start the read or write operation according to the write bit. This bit is self cleared by hardware.
WRITE	16	0b	Write. This bit signals the EEPROM if the current operation is read or write. 0b = Read. 1b = Write.
EEBUSY	17	0b	EPROM Busy. This bit indicates that the EEPROM is busy processing an EEPROM transaction and should not be accessed.
Reserved	30:18	0x0	Reserved.
DONE	31	1b	Transaction Done. This bit is cleared after the *Start* bit and *Write* bit are set by manageability and is set back again when the EEPROM write or read transaction completes.

8.2.3.2.5 Manageability EEPROM Read/Write Data — EEMNGDATA (0x10114; RW)

Note: This register can be read/write by manageability firmware and is read-only to host software.

Field	Bit(s)	Init Val	Description
WRDATA	15:0	0x0	Write Data. Data to be written to the EEPROM.
RDDATA	31:16	X	Read Data. Data returned from the EEPROM read. *Note:* This field is read only.



8.2.3.2.6 Manageability Flash Control Register — FLMNGCTL (0x10118; RW)

Note: This register can be read/write by manageability firmware and is read-only to host software.

Field	Bit(s)	Init Val	Description
ADDR	23:0	0x0	Address. This field is written by manageability along with CMD and CMDV to indicate which Flash address to read or write.
CMD	25:24	00b	Command. Indicates which command should be executed. Valid only when the *CMDV* bit is set. 00b = Read command. 01b = Write command (single byte). 10b = Sector erase. *Note:* Sector erase is applicable only for Atmel Flashes. 11b = Erase.
CMDV	26	0b	Command Valid. When set, indicates that the manageability firmware issues a new command and is cleared by hardware at the end of the command.
FLBUSY	27	0b	Flash Busy. This bit indicates that the Flash is busy processing a Flash transaction and should not be accessed.
Reserved	29:28	00b	Reserved.
DONE	30	1b	Read Done. This bit is cleared by firmware when it sets the *CMDV* bit. It is set by hardware for each Dword read that completes. This bit is read/clear by hardware enabling the multiple Dword read flow.
WRDONE	31	1b	Global Done. This bit clears after the *CMDV* bit is set by manageability and is set back again after all Flash transactions complete. For example, the Flash device finished reading all the requested read or other accesses (write and erase).

8.2.3.2.7 Manageability Flash Read Data — FLMNGDATA (0x1011C; RW)

Note: This register can be read/write by manageability firmware and is read-only to host software.

Field	Bit(s)	Init Val	Description
DATA	31:0	0x0	Read/Write Data On a read transaction, this register contains the data returned from the Flash read. On write transactions, bits 7:0 are written to the Flash.

8.2.3.2.8 Flash Opcode Register — FLOP (0x01013C; RW)

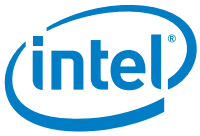
This register enables the host or firmware to define the op-code used in order to erase a sector of the Flash or erase the entire Flash. This register is reset only at power on or during LAN_PWR_GOOD assertion.

Field	Bit(s)	Init Val	Description
SERASE	7:0	0x52	Flash Block Erase Instruction. The op-code for the Flash block erase instruction and is relevant only to Flash access by manageability.
DERASE	15:8	0x62	Flash Device Erase Instruction. The op-code for the Flash erase instruction.
Reserved	31:16	0x0	Reserved.

8.2.3.2.9 General Receive Control — GRC (0x10200; RW)

Field	Bit(s)	Init Val	Description
MNG_EN	0	1b[1]	Manageability Enable. This read-only bit indicates whether or not manageability functionality is enabled.
APME	1	0b[1]	Advance Power Management Enable. If set to 1b, APM wake up is enabled. When APM wake up is enabled and The 82599 receives a matching magic packet, it sets the *PME_Status* bit in the Power Management Control/Status register (PMCSR) and asserts the PE_WAKE_N pin. It is a single read/write bit in a single register, but has two values depending on the function that accesses the register.
Reserved	31:2	0x0	Reserved.

1. Loaded from the EEPROM.



8.2.3.3 Flow Control Registers

8.2.3.3.1 Priority Flow Control Type Opcode — PFCTOP (0x0431C / 0x03008; RW)

This register is also mapped to address 0x0431C to maintain compatibility with the 82598.

Field	Bit(s)	Init Val	Description
FCT	15:0	0x8808	Priority Flow Control EtherType. *Note:* This field appears in little endian (MS byte first on the wire).
FCOP	31:16	0x0101	Priority Flow Control Opcode. *Note:* This field appears in big endian (LS byte first on the wire).

This register contains the *Type* and *Opcode* fields that are matched against a recognized priority flow control packet.

8.2.3.3.2 Flow Control Transmit Timer Value n — FCTTVn (0x03200 + 4*n, n=0...3; RW)

Each 32-bit register (n=0… 3) refers to two timer values (register 0 refers to timer 0 and 1, register 1 refers to timer 2 and 3, etc.).

Field	Bit(s)	Init Val	Description
TTV(2n)	15:0	0x0	Transmit Timer Value 2n. Timer value included in XOFF frames as Timer (2n). The same value shall be set to User Priorities attached to the same TC, as defined in RTTUP2TC register. For legacy 802.3X flow control packets, TTV0 is the only timer that is used.
TTV(2n+1)	31:16	0x0	Transmit Timer Value 2n+1. Timer value included in XOFF frames as Timer 2n+1. The same value shall be set to User Priorities attached to the same TC, as defined in RTTUP2TC register.

The 16-bit value in the *TTV* field is inserted into a transmitted frame (either XOFF frames or any pause frame value in any software transmitted packets). It counts in units of slot time (usually 64 bytes).

Note: The 82599 uses a fixed slot time value of 64 byte times.

8.2.3.3.3 Flow Control Receive Threshold Low — FCRTL[n] (0x03220 + 4*n, n=0...7; RW)

Each 32-bit register (n=0… 7) refers to a different receive packet buffer.

Field	Bit(s)	Init Val	Description
Reserved	4:0	0x0	Reserved.
RTL	18:5	0x0	Receive Threshold Low n. Receive packet buffer n FIFO low water mark for flow control transmission (32 bytes granularity).
Reserved	30:19	0x0	Reserved.
XONE	31	0b	XON Enable n. Per the receive packet buffer XON enable. 0b = Disabled. 1b = Enabled.

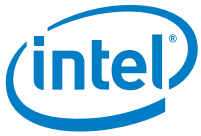
This register contains the receive threshold used to determine when to send an XON packet and counts in units of bytes. The lower four bits must be programmed to 0x0 (16-byte granularity). Software must set XONE to enable the transmission of XON frames. Each time incoming packets cross the receive high threshold (become more full), and then crosses the receive low threshold, with XONE enabled (1b), hardware transmits an XON frame.

8.2.3.3.4 Flow Control Receive Threshold High — FCRTH[n] (0x03260 + 4*n, n=0...7; RW)

Each 32-bit register (n=0…7) refers to a different receive packet buffer.

Field	Bit(s)	Init Val	Description
Reserved	4:0	0x0	Reserved.
RTH	18:5	0x0	Receive Threshold High n. Receive packet buffer n FIFO high water mark for flow control transmission (32 bytes granularity).
Reserved	30:19	0x0	Reserved.
FCEN	31	0b	Transmit flow control enable for packet buffer n.

This register contains the receive threshold used to determine when to send an XOFF packet and counts in units of bytes. This value must be at least eight bytes less than the maximum number of bytes allocated to the receive packet buffer and the lower four bits must be programmed to 0x0 (16-byte granularity). Each time the receive FIFO reaches the fullness indicated by RTH, hardware transmits a pause frame if the transmission of flow control frames is enabled.



8.2.3.3.5 Flow Control Refresh Threshold Value — FCRTV (0x032A0; RW)

Field	Bit(s)	Init Val	Description
FC_refresh_th	15:0	0x0	Flow Control Refresh Threshold. This value is used to calculate the actual refresh period for sending the next pause frame if conditions for a pause state are still valid (buffer fullness above low threshold value). The formula for the refresh period for priority group N is — FCTTV[N/2].TTV[Nmod2] — FCRTV.FC_refresh_th *Note:* The FC_refresh_th must be smaller than TTV of the TC and larger than the max packet size in the TC + FC packet size + link latency and Tx latency and Rx latency in 64 byte units.
Reserved	31:16	0x0	Reserved.

8.2.3.3.6 Transmit Flow Control Status — TFCS (0x0CE00; RO)

Field	Bit(s)	Init Val	Description
TC_XON	7:0	0xFF	Set if flow control is in XON state. If in link flow control mode, only bit 0 should be used. In case of priority flow control mode, each bit represents a TC.
Reserved	31:9	0x0	Reserved.

8.2.3.3.7 Flow Control Configuration — FCCFG (0x03D00; RW)

Field	Bit(s)	Init Val	Description
Reserved	2:0	0x0	Reserved.
TFCE	4:3	0x0	Transmit Flow Control Enable. These bits Indicate that the 82599 transmits flow control packets (XON/XOFF frames) based on receive fullness. If auto-negotiation is enabled, then this bit should be set by software to the negotiated flow control value. 00b = Transmit flow control disabled. 01b = Link flow control enabled. 10b = Priority flow control enabled. 11b = Reserved. *Note:* Priority flow control should be enabled in DCB mode only.
Reserved	31:5	0x0	Reserved.

8.2.3.4 PCIe Registers

8.2.3.4.1 PCIe Control Register — GCR (0x11000; RW)

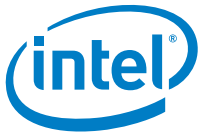
This register is shared for both LAN ports.

Field	Bit (s)	Init Val	Description
Reserved	2:0	100b	Reserved
Reserved	8:3	X	Reserved.
Completion Timeout resend enable	9	1b	When set, enables a resend request after the completion timeout expires. This field is loaded from the *Completion Timeout Resend* bit in the EEPROM (PCIe General Config word 5 bit 15).
Reserved	10	0b	Reserved.
Number of resends	12:11	11b	The number of resends in case of timeout or poisoned.
Reserved	17:13	0x0	Reserved.
PCIe Capability Version	18	1b[1]	Read only field reporting supported PCIe capability version. 0b = Capability version: 0x1. 1b = Capability version: 0x2.
Reserved	20:19	0b	Reserved.
hdr_log inversion	21	0b	If set, the header log in error reporting is written as 31:0 to log1, 63:32 in log2, etc. If not, the header is written as 127:96 in log1, 95:64 in log 2, etc.
Reserved	31:22	0	Reserved.

8.2.3.4.2 PCIe Statistic Control Register #1 — GSCL_1 (0x11010; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
GIO_COUNT_EN_0	0	0b	Enables PCIe statistic counter number 0.
GIO_COUNT_EN_1	1	0b	Enables PCIe statistic counter number 1.
GIO_COUNT_EN_2	2	0b	Enables PCIe statistic counter number 2.
GIO_COUNT_EN_3	3	0b	Enables PCIe statistic counter number 3.



Field	Bit(s)	Init Val	Description
LBC Enable 0	4	0b	When set, statistics counter 0 operates in leaky bucket mode. In this mode there is an internal counter that is incremented by one for each event and is decremented by one each time the LBC timer n (n=0) expires. When the internal counter reaches the value of LBC threshold n (n=0) the internal counter is cleared and the visible associated statistic counter GSCN_0_3[0] is incremented by one. When cleared, Leaky Bucket mode is disabled and the counter is incremented by one for each event.
LBC Enable 1	5	0b	When set, statistics counter 1 operates in leaky bucket mode. See detailed description for LBC Enable 0.
LBC Enable 2	6	0b	When set, statistics counter 2 operates in leaky bucket mode. See detailed description for LBC Enable 0.
LBC Enable 3	7	0b	When set, statistics counter 3 operates in leaky bucket mode. See detailed description for LBC Enable 0.
Reserved	26:8	0x0	Reserved.
GIO_COUNT_TEST	27	0b	Reserved.
GIO_64_BIT_EN	28	0b	Enables two 64-bit counters instead of four 32-bit counters.
GIO_COUNT_RESET	29	0b	Reset indication of PCIe statistic counters.
GIO_COUNT_STOP	30	0b	Stop indication of PCIe statistic counters.
GIO_COUNT_START	31	0b	Start indication of PCIe statistic counters.

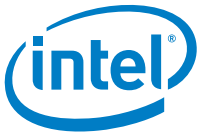
8.2.3.4.3 PCIe Statistic Control Registers #2- GSCL_2 (0x11014; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
GIO_EVENT_NUM_0	7:0	0x0	Event number that counter 0 counts (GSCN_0).
GIO_EVENT_NUM_1	15:8	0x0	Event number that counter 1 counts (GSCN_1).
GIO_EVENT_NUM_2	23:16	0x0	Event number that counter 2 counts (GSCN_2).
GIO_EVENT_NUM_3	31:24	0x0	Event number that counter 3 counts (GSCN_3).

Table 8-4 PCIe Statistic Events Encoding

Transaction layer Events	Event Mapping (Hex)	Description
Bad TLP from LL	00	For each cycle, the counter increases by one, if a bad TLP is received (bad CRC, error reported by AL, misplaced special character, reset in thI of received tlp).
Requests that reached timeout	10	Number of requests that reached time out.
NACK DLLP received	20	For each cycle, the counter increases by one, if a message was transmitted.
Replay happened in retry buffer	21	Occurs when a replay happened due to timeout (not asserted when replay initiated due to NACK.
Receive error	22	Set when one of the following occurs: 1. Decoder error occurred during training in the PHY. It is reported only when training ends. 2. Decoder error occurred during link-up or until the end of the current packet (in case the link failed). This error is masked when entering/ exiting Electrical Idle (EI).
Replay roll over	23	Occurs when replay was initiated for more than three times (threshold is configurable by the PHY CSRs).
Re-sending packets	24	Occurs when TLP is resent in case of completion timeout.
Surprise link down	25	Occurs when link is unpredictably down (not because of reset or DFT).
LTSSM in L0s in both Rx and Tx	30	Occurs when LTSSM enters L0s state in both Tx & Rx.
LTSSM in L0s in Rx	31	Occurs when LTSSM enters L0s state in Rx.
LTSSM in L0s in Tx	32	Occurs when LTSSM enters L0s state in Tx.
LTSSM in L1 active	33	Occurs when LTSSM enters L1-active state (requested from host side).
LTSSM in L1 software	34	Occurs when LTSSM enters L1-switch (requested from switch side).
LTSSM in recovery	35	Occurs when LTSSM enters recovery state.



8.2.3.4.4 PCIe Statistic Control Register #5...#8 — GSCL_5_8 (0x011030 + 4*n, n=0...3; RW)

Note: These registers are shared for both LAN ports.

These registers control the operation of the leaky bucket counter n. While it is GSCL_5 for n=0. GSCL_6 for n=1, GSCL_7 for n=2 and GSCL_8 for n=3. Note that there are no GSCL_3 and GSCL_4 registers.

Field	Bit(s)	Init Val	Description
LBC threshold n	15:0	0x0	Threshold for the leaky bucket counter n.
LBC timer n	31:16	0x0	Time period between decrementing the value in leaky bucket Counter n. The time period is defined in µS units.

8.2.3.4.5 PCIe Statistic Counter Registers #0...#3 — GSCN_0_3 (0x11020 + 4*n, n=0...3; RO)

Note: This register is shared for both LAN ports.

While it is GSCN_0 for n=0. GSCN_1 for n=1, GSCN_2 for n=2 and GSCN_3 for n=3.

Field	Bit(s)	Init Val	Description
Event Counter	31:0	0x0	Event counter as defined in GSCL_2.GIO_EVENT_NUM fields. These registers are stuck at their maximum value of 0xFF...F and cleared on read.

8.2.3.4.6 Function Active and Power State to Manageability — FACTPS (0x10150; RO)

Register for use by the device firmware for configuration.

Field	Bit(s)	Init Val	Description
Func0 Power State	1:0	00b	Power state indication of function 0. 00b = DR 01b = D0u 10b = D0a 11b = D3
LAN0 Valid	2	0b	LAN 0 Enable. When this bit is set to 0b, it indicates that the LAN 0 function is disabled. When the function is enabled, the bit is set to 1b. This bit is reflected if the function is disabled through the external pad.
Func0 Aux_En	3	0b	Function 0 *Auxiliary (AUX) Power PM Enable* bit shadow from the configuration space.
Reserved	5:4	00b	Reserved.

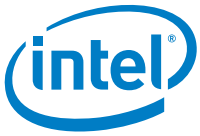
Field	Bit(s)	Init Val	Description
Func1 Power State	7:6	00b	Power state indication of function 1. 00b = DR 01b = D0u 10b = D0a 11b = D3
LAN1 Valid	8	0b	LAN 1 Enable. When this bit is set to 0b, it indicates that the LAN 1 function is disabled. When the function is enabled, the bit is set to 1b. This bit is reflected if the function is disabled through the external pad.
Func1 Aux_En	9	0b	Function 1 *Auxiliary (AUX) Power PM Enable* bit shadow from the configuration space.
Reserved	28:10	0x0	Reserved.
MNGCG	29	0b	Manageability Clock Gated. When set, indicates that the manageability clock is gated.
LAN Function Sel	30	0b[1]	When both LAN ports are enabled and *LAN Function Sel* equals 0b, LAN 0 is routed to PCI function 0 and LAN 1 is routed to PCI function 1. If *LAN Function Sel* equals 1b, LAN 0 is routed to PCI function 1 and LAN 1 is routed to PCI function 0. This bit is loaded from the *LAN Function Select* bit in the PCIe Control 2 EEPROM word at offset 0x05.
PM State changed	31	0b	Indication that one or more of the functions power states had changed. This bit is also a signal to the manageability unit to create an interrupt. This bit is cleared on read, and is not set for at least eight cycles after it was cleared.

1. Loaded from the EEPROM.

8.2.3.4.7 PCIe Analog Configuration Register — PCIEPHYADR (0x11040; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
Address	11:0	0x0	The indirect access' address.
Reserved	24:12	0x0	Reserved
Byte Enable	28:25	0x0	The indirect access' byte enable (4-bit).
Read enable	29	0b	The indirect access is read transaction.
Write enable	30	0b	The indirect access is write transaction.
Done indication	31	0b	Acknowledge for the indirect access to the CSR.



8.2.3.4.8 PCIe PHY Data Register — PCIEPHYDAT (0x11044; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
Data	31:0	0x0	The data to write in the indirect access or the returned data of the indirect read.

8.2.3.4.9 Software Semaphore Register — SWSM (0x10140; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
SMBI	0	0b	Semaphore Bit. This bit is set by hardware, when this register is read by the device driver (one of two PCI functions) and cleared when the host driver writes 0b to it. The first time this register is read, the value is 0b. In the next read the value is 1b (hardware mechanism). The value remains 1b until the device driver clears it. This bit can be used as a semaphore between the two device's drivers. This bit is cleared on PCIe reset.
SWESMBI	1	0b	Software Semaphore bit. This bit is set by the device driver (read only to the firmware) before accessing the SW_FW_SYNC register. This bit can be read as 1b only if the FWSM.FWSMBI bit is cleared. The device driver should clear this bit after accessing the SW_FW_SYNC register as described in Section 10.5.4. Hardware clears this bit on PCIe reset.
RSV	31:2	0x0	Reserved.

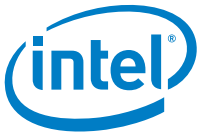
8.2.3.4.10 Firmware Semaphore Register — FWSM (0x10148; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
FWSMBI	0	0b	Firmware Semaphore. Firmware should set this bit to 1b before accessing the SW_FW_SYNC register. This bit can be read as 1b only if the SWSM.SMBI is cleared. Firmware should set it back to 0b after modifying the SW_FW_SYNC register as described in Section 10.5.4.
FW_mode	3:1	000b	Firmware Mode. Indicates the firmware mode as follows: 0x0 = None (manageability off). 0x1 = Reserved. 0x2 = PT mode. 0x3 = Reserved. 0x4 = Host interface enable only. Else = Reserved.
Reserved	5:4	00b	Reserved.

Field	Bit(s)	Init Val	Description
EEP_reload_ ind	6	0b	EEPROM Reloaded Indication. Set to 1b after firmware re-loads the EEPROM. Cleared by firmware once the *Clear Bit* host command is received from host software.
Reserved	14:7	0x0	Reserved.
FW_Val_bit	15	0b	Firmware Valid Bit. Hardware clears this bit in reset de-assertion so software can know firmware mode (bits 1-5) is invalid. firmware should set this bit to 1b when it is ready (end of boot sequence).
Reset_cnt	18:16	000b	Reset Counter. Firmware increments this counter after every reset.
Ext_err_ind	24:19	0x0	External Error Indication. Firmware uses this register to store the reason that the firmware has reset / clock gated (such as EEPROM, Flash, patch corruption, etc.). Possible values: 0x00 = No error. 0x01 = Invalid EEPROM checksum. 0x02 = Unlocked secured EEPROM. 0x03 = Clock off host command. 0x04 = Invalid Flash checksum. 0x05 = C0 checksum failed. 0x06 = C1 checksum failed. 0x07 = C2 checksum failed. 0x08 = C3 checksum failed. 0x09 = TLB table exceeded. 0x0A = DMA load failed. 0x0B = Bad hardware version in patch load. 0x0C = Flash device not supported in the 82599. 0x0D = Unspecified error. 0x3F = Reserved (maximum error value).
PCIe_config_ err_ind	25	0b	PCIe Configuration Error Indication. Set to 1b by firmware when it fails to configure PCIe interface. Cleared by firmware upon successful configuration of PCIe interface.
PHY_SERDES0_config_ err_ind	26	0b	PHY/SERDES0 Configuration Error Indication. Set to 1b by firmware when it fails to configure PHY/SERDES of LAN0. Cleared by firmware upon successful configuration of PHY/SERDES of LAN0.
PHY_SERDES1_config_ err_ind	27	0b	PHY/SERDES1 Configuration Error Indication. Set to 1b by firmware when it fails to configure PHY/SERDES of LAN1. Cleared by firmware upon successful configuration of PHY/SERDES of LAN1.
Reserved	31:28	0000b	Reserved.

Notes: This register should be written only by the manageability firmware. The device driver should only read this register.



The firmware ignores the EEPROM semaphore in operating system hung states.

Bits 15:0 are cleared on firmware reset.

8.2.3.4.11 Software–Firmware Synchronization — SW_FW_SYNC (0x10160; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
SMBITS	9:0	0x0	Semaphore Bits. Each bit represents a different software semaphore agreed between software and firmware as listed. Bits 4:0 are owned by software while bits 9:5 are owned by firmware. *Note:* Hardware does not lock access to these bits. Bit 0 = SW_EEP_SM - at 1b, EEPROM access is owned by software. Bit 1 = SW_PHY_SM0 - at 1b, PHY 0 access is owned by software. Bit 2 = SW_PHY_SM1 - at 1b, PHY 1 access is owned by software. Bit 3 = SW_MAC_CSR_SM - at 1b, Software owns access to shared CSRs. Bit 4 = SW_FLASH_SM - Software Flash semaphore. Bit 5 = FW_EEP_SM - at 1b, EEPROM access is owned by firmware. Bit 6 = FW_PHY_SM0 - at 1b, PHY 0 access is owned by firmware. Bit 7 = FW_PHY_SM1 - at 1b, PHY 1 access is owned by firmware. Bit 8 = FW_MAC_CSR_SM - at 1b, firmware owns access to shared CSRs. Bit 9 = FW_FLASH_SM - at 1b, firmware owns access to the Flash. *Note:* Currently the FW does not access the FLASH.
Reserved	30:10	0x0	Reserved for future use.
Reserved	31	0b	Reserved.

See Section 10.5.4 for more details on software and firmware synchronization.

8.2.3.4.12 PCIe Control Extended Register — GCR_EXT (0x11050; RW)

Field	Bit(s)	Init Val	Description
VT_Mode	1:0	00b	VT mode of operation defines the allocation of physical registers to the VFs. Software must set this field the same as GPIE.VT_Mode. 00b = No VT - Reserved for the case that STSTUS.IOV Ena is not set. 01b = VT16 - Resources are allocated to 16 VFs. 10b = VT32 - Resources are allocated to 32 VFs. 11b = VT64 - Resources are allocated to 64 VFs.
Reserved	3:2	00b	Reserved.

Field	Bit(s)	Init Val	Description
APBACD	4	0b	Auto PBA Clear Disable. When set to 1b, Software can clear the PBA only by direct write to clear access to the *PBA* bit. When set to 0b, any active PBA entry is cleared on the falling edge of the appropriate interrupt request to the PCIe block. The appropriate interrupt request is cleared when software sets the associated interrupt mask bit in the EIMS (re-enabling the interrupt) or by direct write to clear to the PBA.
Reserved	29:5	0x0	Reserved.
Buffers Clear Func	30	0	Initiate a cleaning flow for the buffers in the transaction layer for both the read & write flows. *Note:* Should be only used during Master disable flow. See Section 5.2.5.3.2, Master Disable.
Reserved	31	0	Reserved.

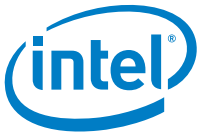
8.2.3.4.13 Mirrored Revision ID- MREVID (0x11064; RO)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
EEPROM_RevID	7:0	0x0	Mirroring of rev ID loaded from EEPROM.
DEFAULT_RevID	15:8	0x0	Mirroring of default rev ID, before EEPROM load (0x0 for the 82599 A0).
Reserved	31:16	0x0	Reserved.

8.2.3.4.14 PCIe Interrupt Cause — PICAUSE (0x110B0; RW1/C)

Field	Bit(s)	Init Val	Description
CA	0	0b	PCI completion abort exception.
UA	1	0b	Unsupported I/O address exception.
BE	2	0b	Wrong byte-enable exception in the FUNC unit.
TO	3	0b	PCI timeout exception in the FUNC unit.
BMEF	4	0b	Asserted when bus master enable of the PF or one of the VFs is de-asserted.
Reserved	31:5	0x0	Reserved



8.2.3.4.15 PCIe Interrupt Enable — PIENA (0x110B8; RW)

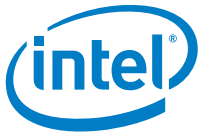
Field	Bit(s)	Init Val	Description
CA	0	0b	When set to 1b, the PCI completion abort interrupt is enabled.
UA	1	0b	When set to 1b, the unsupported I/O address interrupt is enabled.
BE	2	0b	When set to 1b, the wrong byte-enable interrupt is enabled.
TO	3	0b	When set to 1b, the PCI timeout interrupt is enabled.
BMEF	4	0b	When set to 1b, the bus master enable interrupt is enabled.
Reserved	31:5	0x0	Reserved

8.2.3.5 Interrupt Registers

8.2.3.5.1 Extended Interrupt Cause Register- EICR (0x00800; RW1C)

The EICR register is RW1C and can be optionally cleared on a read depending on the ODC flag setting in the GPIE register.

Field	Bit(s)	Init Val	Description
RTxQ	15:0	0x0	Receive/Transmit Queue Interrupts. One bit per queue or a bundle of queues, activated on receive/transmit events. The mapping of the queue to the RTxQ bits is done by the IVAR registers.
Flow Director	16	0b	Flow director exception is activated by one of the following events: 1. Filter Removal failed (no matched filter to be removed). 2. The number of remaining free filters in the flexible filter table exceeds (goes below) the FDIRCTRL.Full-Thresh. 3.
Rx Miss	17	0b	Missed packet interrupt is activated for each received packet that overflows the Rx packet buffer (overrun). *Note:* The packet is dropped and also increments the associated RXMPC[n] counter.
PCI Exception	18	0b	The PCI timeout exception is activated by one of the following events while the specific PCI event is reported in the INTRPT_CSR register: 1. I/O completion abort (write to Flash when Flash is write-disabled). 2. Unsupported I/O request (wrong address). 3. Byte-Enable Error. Access to a client that does not support partial byte-enable access (all but Flash, MSI-X and PCIe target). 4. Timeout occurred in the FUNC block.
MailBox	19	0b	VF to PF MailBox Interrupt. Cause by a VF write access to the PF mailbox.
LSC	20	0b	Link Status Change. This bit is set each time the link status changes (either from up to down, or from down to up).
LinkSec	21	0b	Indicates that the Tx LinkSec packet counter reached the threshold requiring key exchange.
MNG	22	0b	Manageability Event Detected. Indicates that a manageability event happened. When the device is at power down mode, the MC might generate a PME for the same events that would cause an interrupt when the device is at the D0 state.
Reserved	23	0b	Reserved.
GPI_SDP0	24	0b	General Purpose Interrupt on SDP0. If GPI interrupt detection is enabled on this pin (via GPIE), this interrupt cause is set when the SDP0 is sampled high.
GPI_SDP1	25	0b	General Purpose Interrupt on SDP1. If GPI interrupt detection is enabled on this pin (via GPIE), this interrupt cause is set when the SDP1 is sampled high.



Field	Bit(s)	Init Val	Description
GPI_SDP2	26	0b	General Purpose Interrupt on SDP2. If GPI interrupt detection is enabled on this pin (via GPIE), this interrupt cause is set when the SDP2 is sampled high.
GPI_SDP3	27	0b	General Purpose Interrupt on SDP3. If GPI interrupt detection is enabled on this pin (via GPIE), this interrupt cause is set when the SDP3 is sampled high.
ECC	28	0b	Unrecoverable ECC Error. This bit is set when an unrecoverable error is detected in one of the device memories. Software should issue a software reset following this error.
Reserved	29	0b	Reserved.
TCP Timer	30	0b	TCP Timer Expired. This bit is set when the timer expires.
Other Cause Interrupt	31	0b	Activated when any bit (29:20) in the Extended Interrupt Cause Register (EICR) is set and its relevant mask bit in the EIMS is enabled.

8.2.3.5.2 Extended Interrupt Cause Set Register- EICS (0x00808; WO)

Field	Bit(s)	Init Val	Description
Interrupt Cause Set	30:0	0x0	Setting any bit in this field, sets its corresponding bit in the EICR register and generates an interrupt if enabled by the EIMS register.
Reserved	31	0b	Reserved.

8.2.3.5.3 Extended Interrupt Mask Set/Read Register- EIMS (0x00880; RWS)

Field	Bit(s)	Init Val	Description
Interrupt Enable	30:0	0x0	Each bit set to 1b enables its corresponding interrupt in the EICR. Writing 1b to any bit sets it. Writing 0b has no impact. Reading this register provides a map of those interrupts that are enabled.
Reserved	31	0b	Reserved.

8.2.3.5.4 Extended Interrupt Mask Clear Register- EIMC (0x00888; WO)

Field	Bit(s)	Init Val	Description
Interrupt Mask	30:0	0x0	Writing a 1b to any bit clears its corresponding bit in the EIMS register disabling the corresponding interrupt in the EICR register. Writing 0b has no impact. Reading this register provides no meaningful data.
Reserved	31	0b	Reserved.

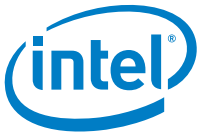
8.2.3.5.5 Extended Interrupt Auto Clear Register — EIAC (0x00810; RW)

Field	Bit(s)	Init Val	Description
RTxQ Auto Clear	15:0	0x0	At 1b, each bit enables auto clear of the corresponding RTxQ bits in the EICR register following interrupt assertion. At 0b, the corresponding bits in the EICR register are not auto cleared.
Reserved	29:16	0x0	Reserved.
TCP Timer Auto Clear	30	0b	At 1b, this bit enables auto clear of the TCP timer interrupt cause in the EICR register following interrupt assertion. At 0b auto clear is not enabled.
Reserved	31	0b	Reserved.

Note: Bits 29:20 should never set auto clear since they share the same MSI-X vector.

8.2.3.5.6 Extended Interrupt Auto Mask Enable Register — EIAM (0x00890; RW)

Field	Bit(s)	Init Val	Description
Auto Mask	30:0	0x0	At 1b, each bit enables auto set and clear of its corresponding bits in the EIMS register. In MSI-X mode, if any of the Auto Mask enable bits is set, the GPIE.EIAME bit must be set as well.
Reserved	31	0b	Reserved.



8.2.3.5.7 Extended Interrupt Cause Set Registers — EICS[n] (0x00A90 + 4*(n-1), n=1...2; WO)

Field	Bit(s)	Init Val	Description
Interrupt Cause Set	31:0	0x0	Setting any bit in these registers sets its corresponding bit in the EICR[n] register and generates an interrupt if enabled by EIMS[n] register. Reading this register provides no meaningful data.

8.2.3.5.8 Extended Interrupt Mask Set/Read Registers — EIMS[n] (0x00AA0 + 4*(n-1), n=1...2; RWS)

Field	Bit(s)	Init Val	Description
Interrupt Enable	31:0	0	Each bit set at 1b enables its corresponding interrupt in the EICR[n] register. Writing 1b to any bit sets it. Writing 0b has no impact. Reading this register provides a map of those interrupts that are enabled. Bits 15:0 of EIMS1 are mirrored in EIMS bits 15:0.

8.2.3.5.9 Extended Interrupt Mask Clear Registers — EIMC[n] (0x00AB0 + 4*(n-1), n=1...2; WO)

Field	Bit(s)	Init Val	Description
Interrupt Mask	31:0	0x0	Writing a 1b to any bit clears its corresponding bit in the EIMS[n] register disabling the corresponding interrupt in the EICR[n] register. Writing 0b has no impact. Reading this register provides no meaningful data.

8.2.3.5.10 Extended Interrupt Auto Mask Enable registers — EIAM[n] (0x00AD0 + 4*(n-1), n=1...2; RW)

Field	Bit(s)	Init Val	Description
Auto Mask	31:0	0x0	At 1b, each bit enables auto set and clear of its corresponding bits in the EIMS[n] register. Bits 15:0 of EIAM1 are mirrored in EIAM bits 15:0. In MSI-X mode, if any of the Auto Mask enable bits is set, the GPIE.EIAME bit must be set as well.

8.2.3.5.11 MSIX to EITR Select — EITRSEL (0x00894; RW)

Field	Bit(s)	Init Val	Description
VFSelect	31:0	0x0	Each bit 'n' in this register selects the VF index (32+'n') or PF interrupt source for the EITR registers (VF 0-31 are not multiplexed as described in Section 7.3.4.3.3). At 0b, it selects the PF and at 1b it selects the VF.

8.2.3.5.12 Extended Interrupt Throttle Registers — EITR[n] (0x00820 + 4*n, n=0...23 and 0x012300 + 4*(n-24), n=24...128; RW)

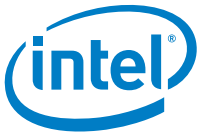
Mapping of the EITR registers to the MSI-X vectors is described in Section 7.3.4.3.3.

Field	Bit(s)	Init Val	Description
Reserved	2:0	000b	Reserved.
ITR Interval	11:3	0x0	Minimum inter-interrupt interval specified in 2 µs units at 1 Gb/2 and 10 Gb/s link. At 100 Mb/s link, the interval is specified in 20 µs units. At 0x0 interrupt throttling is disabled while any "event" causes an immediate interrupt.
Reserved	14:12	000b	Reserved.
LLI Moderation	15	0b	When set, LLI moderation is enabled. Otherwise, any LLI packet generates an immediate interrupt. LLI moderation might be set only if interrupt throttling is enabled by the *ITR Interval* field in this register and LLI moderation is enabled by the *LL Interval* field in the GPIE register.
LLI Credit	20:16	0x0	Reflects the current credits for associated interrupt. When CNT_WDIS is not set on a write cycle, this field must be set to 0x0.
ITR Counter	27:21	0x0	This field represents the seven MS bits (out of nine bits) of the ITR counter. It is a down counter that is loaded with an ITR interval value each time the associated interrupt is asserted. When the ITR counter reaches zero it stops counting and triggers an interrupt. On a write cycle, software must set this field to 0 if CNT_WDIS in this register is cleared (write enable to the ITR counter).
Reserved	30:28	000b	Reserved.
CNT_WDIS	31	0b	Write disable to the LLI credit and ITR counter. When set, the LLI credit and ITR counter are not overwritten by the write access. When cleared, software must set the LLI credit and ITR counter to zero, which enables an immediate interrupt on packet reception. This bit is write only. Always read as 0b.

8.2.3.5.13 L3 L4 Tuples Immediate Interrupt Rx — L34TIMIR[n] (0x0E800 + 4*n, n=0...127; RW)

This register must be initialized by software.

Field	Bit(s)	Init Val	Description
Reserved	11:0	X	Reserved.
Size_BP	12	X	Size Bypass. 0b = Size check is performed. 1b = Size check is bypassed.



Field	Bit(s)	Init Val	Description
Reserved	19:13	X	Reserved. Must be set to 1000000b on any programmed filter.
Low Latency Interrupt	20	X	Enables issuing a LLI when the following conditions are met: • The 5-tuple filter associated with this register matches. • If enabled by the Size_BP bit, the packet length is smaller than the length defined by LLITHRESH.SizeThresh.
Rx Queue	27:21	X	Identifies the Rx queue associated with this 5-tuple filter.
Reserved	31:28	X	Reserved.

8.2.3.5.14 LLI Size Threshold — LLITHRESH (0x0EC90; RW)

Field	Bit(s)	Init Val	Description
SizeThresh	11:0	0x000	Size Threshold. A packet with length below this threshold that matches one of the 5-tuple filters with an active *Low Latency Interrupt* flag in the L34TIMIR[n] registers might trigger an LLI.
Reserved	25:12	0x0	Reserved.
Reserved	31:26	000101b	Reserved.

8.2.3.5.15 Immediate Interrupt Rx VLAN Priority Register- IMIRVP (0x0EC60 / 0x05AC0; RW)

IMIRVP is also mapped to address 0x05AC0 to maintain compatibility with the 82598.

Field	Bit(s)	Init Val	Description
Vlan_Pri	2:0	000b	VLAN Priority. This field includes the VLAN priority threshold. When Vlan_pri_en is set to 1b, then an incoming packet with VLAN tag with a priority equal or higher to VlanPri must trigger a LLI, regardless of the ITR moderation.
Vlan_pri_en	3	0	VLAN Priority Enable. When 1b, an incoming packet with VLAN tag with a priority equal or higher to Vlan_Pri must trigger a LLI, regardless of the ITR moderation. When 0b, the interrupt is moderated by ITR.
Reserved	31:4		Reserved.

8.2.3.5.16 Interrupt Vector Allocation Registers — IVAR[n] (0x00900 + 4*n, n=0...63; RW)

These registers map interrupt causes into EICR entries (legacy/MSI modes) or into MSI-X vectors (MSI-X modes). See Section 7.3.4 for mapping and use of these registers.

Transmit and receive queues mapping to IVAR registers is shown in Figure 8-1:

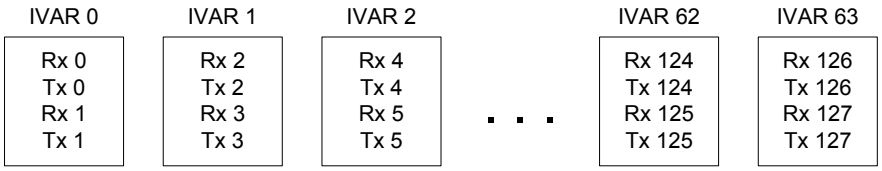
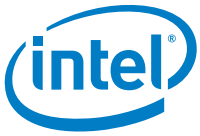


Figure 8-1 Transmit and Receive Queues Mapping to IVAR Registers

Fields of the IVAR registers are described in Table 8-5.

Table 8-5 Fields of IVAR Register

Field	Bit(s)	Init Val	Description
INT_Alloc[0]	5:0	X	The interrupt allocation for Rx queue (‘2xN’ for IVAR register ‘N’).
Reserved	6	0b	Reserved.
INT_Alloc_val[0]	7	0b	Interrupt allocation valid indication for INT_Alloc[0].
INT_Alloc[1]	13:8	X	The interrupt allocation for Tx queue (‘2xN’ for IVAR register ‘N’).
Reserved	14	0b	Reserved.
INT_Alloc_val[1]	15	0b	Interrupt allocation valid indication for INT_Alloc[1].
INT_Alloc[2]	21:16	X	The interrupt allocation for Rx queue (‘2xN’+1 for IVAR register ‘N’).
Reserved	22	0b	Reserved.
INT_Alloc_val[2]	23	0b	Interrupt allocation valid indication for INT_Alloc[2].
INT_Alloc[3]	29:24	X	The interrupt allocation for Tx queue (‘2xN’+1 for IVAR register ‘N’).
Reserved	30	0b	Reserved.
INT_Alloc_val[3]	31	0b	Interrupt allocation valid indication for INT_Alloc[3].



8.2.3.5.17 Miscellaneous Interrupt Vector Allocation — IVAR_MISC (0x00A00; RW)

These register maps interrupt causes into MSI-X vectors (MSI-X modes). See Section 7.3.4 for mapping and use of these registers.

Field	Bit(s)	Init Val	Description
INT_Alloc[0]	6:0	X	Defines the MSI-X vector assigned to the TCP timer interrupt cause.
INT_Alloc_val[0]	7	0b	Valid bit for INT_Alloc[0].
INT_Alloc[1]	14:8	X	Defines the MSI-X vector assigned to the other interrupt cause.
INT_Alloc_val[1]	15	1b	Valid bit for INT_Alloc[1].
Reserved	31:16	0b	Reserved.

Note: The INT_ALLOC_VAL[1] bit default value is one — to enable legacy driver functionality.

8.2.3.5.18 General Purpose Interrupt Enable — GPIE (0x00898; RW)

Field	Bit(s)	Init Val	Description
SDP0_GPIEN	0	0b	General Purpose Interrupt Detection Enable for SDP0. If software-controllable I/O pin SDP0 is configured as an input, this bit (when 1b) enables use for GPI interrupt detection.
SDP1_GPIEN	1	0b	General Purpose Interrupt Detection Enable for SDP1. If software-controllable I/O pin SDP1 is configured as an input, this bit (when 1b) enables use for GPI interrupt detection.
SDP2_GPIEN	2	0b	General Purpose Interrupt Detection Enable for SDP2. If software-controllable I/O pin SDP2 is configured as an input, this bit (when 1b) enables use for GPI interrupt detection.
SDP3_GPIEN	3	0b	General Purpose Interrupt Detection Enable for SDP3. If software-controllable I/O pin SDP3 is configured as an input, this bit (when 1b) enables use for GPI interrupt detection.
Multiple_MSIX	4	0b	MSI-X Mode. Selects between MSI-X interrupts and other interrupt modes. 0b = Legacy and MSI mode (non-MSI-X mode). 1b = MSI-X mode.
OCD	5	0b	Other Clear Disable. 0b = The entire EICR is cleared on read. 1b = Indicates that only bits 29:16 of the EICR register are cleared on read.
EIMEN	6	0b	EICS Immediate Interrupt Enable. When set, setting this bit in the EICS register causes a LLI. If not set, the EICS interrupt waits for EITR expiration.

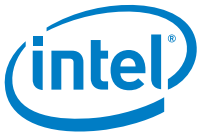
Field	Bit(s)	Init Val	Description
LL Interval	10:7	0x0	Low latency Credits Increment Rate. The interval is specified in 4 µs increments at 1 Gb/s and 10 Gb/s link. It is defined as 40 µs at 100 Mb/s link. A value of 0x0 disables moderation of LLI for all interrupt vectors. When LLI is disabled by the *LL Interval* bit, the *LLI Moderation* bit in all EITR registers must not be set.
RSC Delay	13:11	000b	Delay from RSC completion triggered by ITR and interrupt assertion. The delay = (RSC Delay + 1) x 4 µs = 4, 8, 12... 32 µs.
VT_Mode	15:14	00b	Specify the number of active VFs. Software must set this field the same as GCR_Ext.VT_Mode. 00b = Non-IOV mode. 10b = 32 VF mode. 01b = 16 VF mode. 11b = 64 VF mode.
Reserved	29:16	0x0	Reserved.
EIAME	30	0b	Extended Interrupt Auto Mask Enable. When set, the EIMS register can be auto-cleared (depending on EIAM setting) upon interrupt assertion. In any case, the EIMS register can be auto-cleared (depending on EIAM setting) following a write-to-clear (or read) to the EICR register. Software may set the EIAME only in MSI-X mode.
PBA_support	31	0b	PBA Support. When set, setting one of the extended interrupts masks via EIMS causes the *PBA* bit of the associated MSI-X vector to be cleared. Otherwise, the 82599 behaves in a way supporting legacy INT-x interrupts. *Note:* Should be cleared when working in INT-x or MSI mode and set in MSI-X mode.

The 82599 allows for up to four externally controlled interrupts. The lower four software-definable pins, SDP[3:0], can be mapped for use as GPI interrupt bits. These mappings are enabled by the SDPx_GPIEN bits only when these signals are also configured as inputs via SDPx_IODIR. When configured to function as external interrupt pins, a GPI interrupt is generated when the corresponding pin is sampled in an active-high state.

The bit mappings are listed in Table 8-6 for clarity.

Table 8-6 GPI-to-SDP Bit Mappings

SDP (pin to be used as GPI)	ESDP Field Settings		Resulting EICR Bit (GPI)
	Directionality	Enable as GPI interrupt	
3	SDP3_IODIR	SDP3_GPIEN	27
2	SDP2_IODIR	SDP2_GPIEN	26
1	SDP1_IODIR	SDP1_GPIEN	25
0	SDP0_IODIR	SDP0_GPIEN	24



8.2.3.6 MSI-X Table Registers

MSI-X capability is described in section Section 9.3.8. The MSI-X table is described in Section 9.3.8.2 and the Pending Bit Array (PBA) is described in Section 9.3.8.3. These registers are located in the MSI-X BAR.

8.2.3.6.1 MSI-X PBA Clear — PBACL[n] (0x110C0 + 4*n, n=0...7 / 0x11068 [n=0]; RW)

PBACL[0] is also mapped to address 0x11068 to maintain compatibility with the 82598.

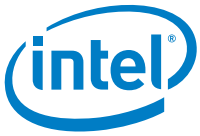
Field	Bit(s)	Init Val	Description
PENBITCLR	31:0	0x0	MSI-X Pending Bits Clear. Writing 1b to any bit clears it's content; writing 0b has no effect. Reading this register returns the MSIPBA.PENBIT value.

8.2.3.7 Receive Registers

8.2.3.7.1 Filter Control Register — FCTRL (0x05080; RW)

Field	Bit(s)	Init Val	Description
Reserved	0	0b	Reserved.
SBP	1	0b	Store Bad Packets. 0b = Do not store. 1b = Store. *Note:* CRC errors before the SFD are ignored. Any packet must have a valid SFD (RX_DV with no RX_ER in the XGMII/GMII i/f) in order to be recognized by the device (even bad packets). *Note:* Packets with errors are not routed to manageability even if this bit is set. *Note:* Erroneous packets can be routed to the default queue rather than the originally intended queue. *Note:* In packets shorter than 64 bytes, the checksum errors can be hidden while MAC errors are reported. *Note:* A packet with a valid error (caused by byte error or illegal error) might have data contamination in the last eight bytes when stored in the host memory if the *Store Bad Packet* bit is set.
Reserved	7:2	0x0	Reserved.
MPE	8	0b	Multicast Promiscuous Enable. 0b = Disabled. 1b = Enabled. When set, all received multicast and broadcast packets pass L2 filtering and can be directed to manageability or the host by a one of the decision filters.
UPE	9	0b	Unicast Promiscuous Enable. 0b = Disabled. 1b = Enabled.
BAM	10	0b	Broadcast Accept Mode. 0b = Ignore broadcast packets to host. 1b = Accept broadcast packets to host.
Reserved	31:11	0x0	Reserved.

Note: Before receive filters are updated/modified the RXCTRL.RXEN bit should be set to 0b. After the proper filters have been set the RXCTRL.RXEN bit can be set to 1b to re-enable the receiver.



8.2.3.7.2 VLAN Control Register — VLNCTRL (0x05088; RW)

Field	Bit(s)	Init Val	Description
VET	15:0	0x8100	VLAN Ether Type (the VLAN Tag Protocol Identifier — TPID). This register contains the type field hardware matches against to recognize an 802.1Q (VLAN) Ethernet packet. For proper operation, software must not change the default setting of this field (802.3ac standard defines it as 0x8100). This field must be set to the same value as the VT field in the DMATXCTL register. *Note:* This field appears in little endian order (the upper byte is first on the wire (VLNCTRL.VET[15:8]).
Reserved	27:16		Reserved.
CFI	28	0b	Canonical Form Indicator Bit Value. If CFIEN is set to 1b, then 802.1q packets with CFI equal to this field are accepted; otherwise, the 802.1q packet is discarded.
CFIEN	29	0b	Canonical Form Indicator Enable. 0b = Disabled (CFI bit not compared to decide packet acceptance). 1b = Enabled (CFI from packet must match next CFI field to accept 802.1q packet).
VFE	30	0b	VLAN Filter Enable. 0b = Disabled (filter table does not decide packet acceptance). 1b = Enabled (filter table decides packet acceptance for 802.1q packets).
Reserved	31	0b	Reserved.

8.2.3.7.3 Multicast Control Register — MCSTCTRL (0x05090; RW)

Field	Bit(s)	Init Val	Description
MO	1:0	00b	Multicast Offset. This determines which bits of the incoming multicast address are used in looking up the bit vector. 00b = [47:36]. 01b = [46:35]. 10b = [45:34]. 11b = [43:32].
MFE	2	0b	Multicast Filter Enable. 0b = The multicast table array filter (MTA[n]) is disabled. 1b = The multicast table array (MTA[n]) is enabled.
Reserved	31:3	0x0	Reserved.

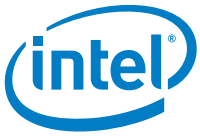
8.2.3.7.4 Packet Split Receive Type Register — PSRTYPE[n] (0x0EA00 + 4*n, n=0...63 / 0x05480 + 4*n, n=0...15; RW)

Registers 0...15 are also mapped to 0x05480 to maintain compatibility with the 82598.

Note:

- This register must be initialized by software.
- Packets are split according to the lowest-indexed entry that applies to the packet and that is enabled. For example, if bits 4 and 8 are set, then an IPv4 packet that is not TCP is split after the IPv4 header.
- This bit mask table enables or disables each type of header to be split. A value of 1b enables an entry.
- In virtualization mode, a separate PSRTYPE register is provided per pool up to the number of pools enabled. In non-virtualization mode, only PSRTYPE[0] is used.
- PSR_type4 should be set to enable RSC, regardless header split mode.

Field	Bit(s)	Init Val	Description
PSR_type0	0	x	Reserved.
PSR_type1	1	x	Split received NFS packets after NFS header.
PSR_type2	2	x	Reserved.
PSR_type3	3	x	Reserved.
PSR_type4	4	x	Split received TCP packets after TCP header.
PSR_type5	5	x	Split received UDP packets after UDP header.
PSR_type6	6	x	Reserved.
PSR_type7	7	x	Reserved.
PSR_type8	8	x	Split received IPv4 packets after IPv4 header.
PSR_type9	9	x	Split received IPv6 packets after IPv6 header.
PSR_type10	10	x	Reserved.
PSR_type11	11	x	Reserved.
PSR_type12	12	x	Split received L2 packets after L2 header.
PSR_type13	13	x	Reserved.
PSR_type14	14	x	Reserved.
PSR_type15	15	x	Reserved.
PSR_type16	16	x	Reserved.



Field	Bit(s)	Init Val	Description
PSR_type17	17	x	Reserved.
PSR_type18	18	x	Reserved.
Reserved	28:19	x	Reserved.
RQPL	31:29	x	Defines the number of bits to use for RSS redirection of packets dedicated to this pool. Valid values are zero, 0001b and 0010b. The default value should be 0010b, meaning that up to 4 queues can be enabled for this pool. A value of 0001b means that up to 2 queues can be enabled for this pool. A value of zero means that all the traffic of the pool is sent to queue 0 of the pool. This field is used only if MRQC.MRQE equals 1010b or 1011b.

8.2.3.7.5 Receive Checksum Control — RXCSUM (0x05000; RW)

Field	Bit(s)	Init Val	Description
Reserved	11:0	0x0	Reserved.
IPPCSE	12	0b	IP Payload Checksum Enable.
PCSD	13	0b	RSS/Fragment Checksum Status Selection. When set to 1b, the extended descriptor write back has the *RSS* field. When set to 0b, it contains the fragment checksum.
Reserved	31:14	0x0	Reserved.

The Receive Checksum Control register controls the receive checksum offloading features of the 82599. The 82599 supports the offloading of three receive checksum calculations: the fragment checksum, the IP header checksum, and the TCP/UDP checksum.

PCSD: The Fragment Checksum and IP Identification fields are mutually exclusive with the RSS hash. Only one of the two options is reported in the Rx descriptor. The RXCSUM.PCSD affect is shown in Table 8-7.

Table 8-7 Checksum Enable/Disable

RXCSUM.PCSD	0b (Checksum Enable)	1b (Checksum Disable)
	Fragment checksum and IP identification are reported in the Rx descriptor.	RSS hash value is reported in the Rx descriptor.

IPPCSE: IPPCSE controls the fragment checksum calculation. As previously noted, the fragment checksum shares the same location as the *RSS* field. The fragment checksum is reported in the receive descriptor when the RXCSUM.PCSD bit is cleared.

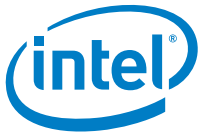
If RXCSUM.IPPCSE is cleared (the default value), the checksum calculation is not done and the value that is reported in the Rx fragment checksum field is 0b.

If RXCSUM.IPPCSE is set, the fragment checksum is aimed to accelerate checksum calculation of fragmented UDP packets. See Section 7.1.13 for a detailed explanation.

This register should only be initialized (written) when the receiver is not enabled (for example, only write this register when RXCTRL.RXEN = 0b).

8.2.3.7.6 Receive Filter Control Register — RFCTL (0x05008; RW)

Field	Bit(s)	Init Val	Description
Reserved	5:0	0x0	Reserved.
RSC_DIS	5	0	RSC Disable. When set, disable RSC for the port by the Rx filter unit. The default value is 0b (RSC feature is enabled).
NFSW_DIS	6	0b	NFS Write disable. Disable filtering of NFS write request headers.
NFSR_DIS	7	0b	NFS Read disable. Disable filtering of NFS read reply headers.
NFS_VER	9:8	00b	NFS version recognized by the hardware. 00b = NFS version 2 01b = NFS version 3 10b = NFS version 4 11b = Reserved for future use
IPv6_dis	10	0b	IPv6 Disable. Disable IPv6 packet filtering Internal use only – should not be set to 1b.
Reserved	11	0b	Reserved, always set to 0b.
Reserved	13:12	00b	Reserved.
IPFRSP_DIS	14	0b	IP Fragment Split Disable When this bit is set the header of IP fragmented packets are not set. Internal use only. Should not be set to 1b.
Reserved	15	0b	Reserved.
Reserved	17:16	00b	Reserved.
Reserved	31:18	0x0	Reserved. Should be written with 0x0 to ensure future compatibility.



8.2.3.7.7 Multicast Table Array — MTA[n] (0x05200 + 4*n, n=0...127; RW)

This table should be initialized by software before transmit and receive are enabled.

Field	Bit(s)	Init Val	Description
Bit Vector	31:0	X	Word wide bit vector specifying 32 bits in the multicast address filter table. The 82599 provides multicast filtering for 4096 multicast addresses by providing single-bit entry per multicast address. Those 4096 address locations are organized in the Multicast Table Array (MTA); 128 registers of 32 bits for each one. Only 12 bits out of the 48-bit destination address are considered as a multicast address. Those 12 bits can be selected by the *MO* field of MCSTCTRL register. The 7 MS bits of the Ethernet MAC address (out of the 12 bits) selects the register index while the 5 LS bits (out of the 12 bits) selects the bit within a register.

8.2.3.7.8 Receive Address Low — RAL[n] (0x0A200 + 8*n, n=0...127; RW)

While "n" is the exact unicast/multicast address entry and it is equals to 0,1,...127.

Field	Bit(s)	Init Val	Description
RAL	31:0	X	Receive Address Low. The lower 32 bits of the 48-bit Ethernet MAC address. *Note:* Field is defined in big endian (LS byte of RAL is first on the wire).

These registers contain the lower bits of the 48-bit Ethernet MAC address. All 32 bits are valid.

If the EEPROM is present, the first register (RAL0) is loaded from the EEPROM.

8.2.3.7.9 Receive Address High — RAH[n] (0x0A204 + 8*n, n=0...127; RW)

While "n" is the exact unicast/multicast address entry and it is equals to 0,1,...127.

Field	Bit(s)	Init Val	Description
RAH	15:0	X	Receive Address High. The upper 16 bits of the 48 bit Ethernet MAC Address. *Note:* Field is defined in Big Endian (MS byte of RAH is Last on the wire).
Reserved	21:16	0x0	Reserved.

Field	Bit(s)	Init Val	Description
Reserved	30:22	0x0	Reserved. Reads as 0. Ignored on write.
AV	31	X (see desc.)	Address Valid. All receive addresses are not initialized by hardware and software should initialize them before receive is enabled. If the EEPROM is present, Receive Address[0] is loaded from the EEPROM and its *Address Valid* field is set to 1b after a software, PCI reset or EEPROM read.

These registers contain the upper bits of the 48-bit Ethernet MAC address. The complete address is {RAH, RAL}. AV determines whether this address is compared against the incoming packet. AV is cleared by a master reset.

Note: The first Receive Address register (RAR0) is also used for exact match pause frame checking (DA matches the first register). RAR0 should always be used to store the individual Ethernet MAC address of the adapter.

After reset, if the EEPROM is present, the first register (Receive Address Register 0) is loaded from the *IA* field in the EEPROM, its *Address Select* field is 00b, and its *Address Valid* field is 1b. If no EEPROM is present, the *Address Valid* field is 0b. The *Address Valid* field for all of the other registers are 0b.

8.2.3.7.10 MAC Pool Select Array — MPSAR[n] (0x0A600 + 4*n, n=0...255; RW)

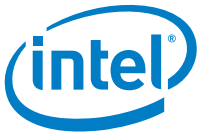
Software should initialize these registers before transmit and receive are enabled.

Field	Bit(s)	Init Val	Description
POOL_ENA	31:0	X	Pool Enable Bit Array. Each couple of registers ‘2*n’ and ‘2*n+1’ are associated with Ethernet MAC address filter ‘n’ as defined by RAL[n] and RAH[n]. Each bit when set, enables packet reception with the associated pools as follows: Bit ‘i’ in register ‘2*n’ is associated with POOL ‘i’. Bit ‘i’ in register ‘2*n+1’ is associated with POOL ‘32+i’.

8.2.3.7.11 VLAN Filter Table Array — VFTA[n] (0x0A000 + 4*n, n=0...127; RW)

This table should be initialized by software before transmit and receive are enabled.

Field	Bit(s)	Init Val	Description
VLAN_FLT	31:0	X	VLAN Filter. Each bit ‘i’ in register ‘n’ affects packets with VLAN tags equal to 32*n+i. 128 VLAN Filter registers compose a table of 4096 bits that cover all possible VLAN tags. Each bit when set, enables packets with the associated VLAN tags to pass. Each bit when cleared, blocks packets with this VLAN tag.



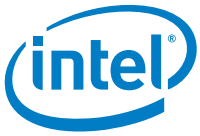
8.2.3.7.12 Multiple Receive Queues Command Register- MRQC (0x0EC80 / 0x05818; RW)

MRQC is also mapped to address 0x05818 to maintain compatibility with the 82598.

Field	Bit(s)	Init Val	Description
MRQE	3:0	0x0	Multiple Receive Queues Enable. Defines the allocation of the Rx queues per RSS, virtualization and DCB. 0000b = RSS disabled. 0001b = RSS only — Single set of RSS 16 queues. 0010b = DCB enabled and RSS disabled — 8 TCs, each allocated 1 queue. 0011b = DCB enabled and RSS disabled — 4 TCs, each allocated 1 queue. 0100b = DCB and RSS — 8 TCs, each allocated 16 RSS queues. 0101b = DCB and RSS — 4 TCs, each allocated 16 RSS queues. 0110b = Reserved 0111b = Reserved 1000b = Virtualization only — 64 pools, no RSS, each pool allocated 2 queues. 1001b = Reserved 1010b = Virtualization and RSS — 32 pools, each allocated 4 RSS queues. 1011b = Virtualization and RSS — 64 pools, each allocated 2 RSS queues. 1100b = Virtualization and DCB — 16 pools, each allocated 8 TCs. 1101b = Virtualization and DCB — 32 pools, each allocated 4 TCs. 1110b = Reserved 1111b = Reserved
Reserved	14:4	0x0	Reserved.
Reserved	15	0x0	Reserved.
RSS Field Enable	31:16	0x0	Each bit, when set, enables a specific field selection to be used by the hash function. Several bits can be set at the same time. Bit[16] = Enable TcpIPv4 hash function. Bit[17] = Enable IPv4 hash function. Bit[19:18] = Reserved Bit[20] = Enable IPv6 hash function. Bit[21] = Enable TcpIPv6 hash function. Bit[22] = Enable UdpIPV4. Bit[23] = Enable UdpIPV6. Bits[31:24] = Reserved *Note:* On Tunnel packets IPv4-IPv6 only the IPv4 header can be used for the RSS filtering.

8.2.3.7.13 RSS Queues Per Traffic Class Register — RQTC (0x0EC70; RW)

Field	Bit(s)	Init Val	Description
RQTC0	2:0	0x4	Defines the number of bits to use for RSS redirection of packets dedicated to Traffic Class (TC) 0. A value of zero means that all the traffic of TC0 is sent to queue 0 of the TC. This field is used only if MRQC.MRQE equals 0100b or 0101b.
Reserved	3	0b	Reserved.
RQTC1	6:4	0x4	Defines the number of bits to use for RSS redirection of packets dedicated to TC 1. A value of zero means that all the traffic of TC1 is sent to queue 0 of the TC. This field is used only if MRQC.MRQE equals 0100b or 0101b.
Reserved	7	0b	Reserved.
RQTC2	10:8	0x4	Defines the number of bits to use for RSS redirection of packets dedicated to TC 2. A value of zero means that all the traffic of TC2 is sent to queue 0 of the TC. This field is used only if MRQC.MRQE equals 0100b or 0101b.
Reserved	11	0b	Reserved.
RQTC3	14:12	0x4	Defines the number of bits to use for RSS redirection of packets dedicated to TC 3. A value of zero means that all the traffic of TC3 is sent to queue 0 of the TC. This field is used only if MRQC.MRQE equals 0100b or 0101b.
Reserved	15	0b	Reserved.
RQTC4	18:16	0x4	Defines the number of bits to use for RSS redirection of packets dedicated to TC 4. A value of zero means that all the traffic of TC4 is sent to queue 0 of the TC. This field is used only if MRQC.MRQE equals 0100b or 0101b.
Reserved	19	0b	Reserved.
RQTC5	22:20	0x4	Defines the number of bits to use for RSS redirection of packets dedicated to TC 5. A value of zero means that all the traffic of TC5 is sent to queue 0 of the TC. This field is used only if MRQC.MRQE equals 0100b or 0101b.
Reserved	23	0b	Reserved.
RQTC6	26:24	0x4	Defines the number of bits to use for RSS redirection of packets dedicated to TC 6. A value of zero means that all the traffic of TC6 is sent to queue 0 of the TC. This field is used only if MRQC.MRQE equals 0100b or 0101b.
Reserved	27	0b	Reserved.
RQTC7	30:28	0x4	Defines the number of bits to use for RSS redirection of packets dedicated to TC 7. A value of zero means that all the traffic of TC7 is sent to queue 0 of the TC. This field is used only if MRQC.MRQE equals 0100b or 0101b.
Reserved	31	0b	Reserved.



8.2.3.7.14 RSS Random Key Register — RSSRK (0x0EB80 + 4*n, n=0...9 / 0x05C80 + 4*n, n=0...9; RW)

RSSRK is also mapped to addresses 0x05C80-0x05CA4 to maintain compatibility with the 82598. The RSS Random Key is 40 bytes wide (see RSS hash in Section 7.1.2.8.1).

Field	Bit(s)	Init Val	Description
K0	7:0	0x0	RSS Key Byte '4*n+0' of the RSS random key, for each register 'n'.
K1	15:8	0x0	RSS Key Byte '4*n+1' of the RSS random key, for each register 'n'.
K2	23:16	0x0	RSS Key Byte '4*n+2' of the RSS random key, for each register 'n'.
K3	31:24	0x0	RSS Key Byte '4*n+3' of the RSS random key, for each register 'n'.

8.2.3.7.15 Redirection Table — RETA[n] (0x0EB00 + 4*n, n=0...31 / 0x05C00 + 4*n, n=0...31; RW)

RETA is also mapped to addresses 0x05C00-0x05C7C to maintain compatibility with the 82598. The redirection table has 128-entries in 32 registers.

Field	Bit(s)	Init Val	Description
Entry0	3:0	X	Entry0 defines the RSS output index for hash value '4*n+0'. While 'n' is the register index, equals to 0...31.
Reserved	7:4	0x0	Reserved.
Entry1	11:8	X	Entry1 defines the RSS output index for hash value '4*n+1'. While 'n' is the register index, equals to 0...31.
Reserved	15:12	0x0	Reserved.
Entry2	19:16	X	Entry2 defines the RSS output index for hash value '4*n+2'. While 'n' is the register index, equals to 0...31.
Reserved	23:20	0x0	Reserved.
Entry3	27:24	X	Entry3 defines the RSS output index for hash value '4*n+3'. While 'n' is the register index, equals to 0...31.
Reserved	31:28	0x0	Reserved.

The contents of the redirection table are not defined following reset of the Memory Configuration registers. System software must initialize the table prior to enabling multiple receive queues. It can also update the redirection table during run time. Such updates of the table are not synchronized with the arrival time of received packets. Therefore, it is not guaranteed that a table update takes effect on a specific packet boundary.

8.2.3.7.16 Source Address Queue Filter — SAQF[n] (0x0E000 + 4*n, n=0...127; RW)

This register must be initialized by software

Field	Bit(s)	Init Val	Description
Source Address	31:0	X	IP Source Address. Part of the 5-tuple queue filters. *Note:* Field is defined in big endian (LS byte is first on the wire).

8.2.3.7.17 Destination Address Queue Filter — DAQF[n] (0x0E200 + 4*n, n=0...127; RW)

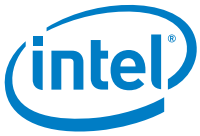
This register must be initialized by software.

Field	Bit(s)	Init Val	Description
Destination Address	31:0	X	IP Destination Address. Part of the 5-tuple queue filters. *Note:* Field is defined in big endian (LS byte is first on the wire).

8.2.3.7.18 Source Destination Port Queue Filter — SDPQF[n] (0x0E400 + 4*n, n=0...127; RW)

This register must be initialized by software.

Field	Bit(s)	Init Val	Description
Source Port	15:0	X	TCP/UDP Source Port. Part of the 5-tuple queue filters. *Note:* Field is defined in Big Endian (LS byte is first on the wire).
Destination Port	31:16	X	TCP/UDP Destination Port. Part of the 5-tuple queue filters.



8.2.3.7.19 Five tuple Queue Filter — FTQF[n] (0x0E600 + 4*n, n=0...127; RW)

Field	Bit(s)	Init Val	Description
Protocol	1:0	X	IP L4 protocol, part of the 5-tuple queue filters. 00b = TCP. 01b = UDP. 10b = SCTP. 11b = Other. *Note:* Encoding of the protocol type for the 128 x 5-tuple filters is defined differently than the L4TYPE encoding for the flow director filters.
Priority	4:2	X	Priority value in case more than one 5-tuple filter matches. 000b = Reserved 001b = Lowest priority. ... 111b = Highest priority.
Reserved	7:5	X	Reserved.
Pool	13:8	X	The pool Index of the pool associated with this filter.
Reserved	24:14	X	Reserved for extension of the *Pool* field.
Mask	29:25	X	Mask bits for the 5-tuple fields (1b = don't compare). The corresponding field participates in the match if the following bit is cleared: Bit 25 = Mask source address comparison. Bit 26 = Mask destination address comparison. Bit 27 = Mask source port comparison. Bit 28 = Mask destination port comparison. Bit 29 = Mask protocol comparison.
Pool Mask	30	X	Mask bit for the *Pool* field. When set to 1b, the *Pool* field is not compared as part of the 5-tuple filter. Software can clear (activate) the *Pool Mask* bit only when operating in IOV mode.
Queue Enable	31	X	When set, enables filtering of Rx packets by the 5-tuple defined in this filter to the queue indicated in register L34TIMIR. *Note:* There are 128 different 5-tuple filter configuration registers sets, with indexes [0] to [127]. The mapping to a specific Rx queue is done by the Rx Queue field in the L34TIMIR register, and not by the index of the register set.

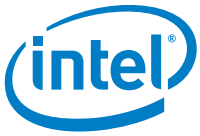
8.2.3.7.20 SYN Packet Queue Filter — SYNQF (0x0EC30; RW)

Field	Bit(s)	Init Val	Description
Queue Enable	0	0b	When set, enables routing of Rx packets to the queue indicated in this register.
Rx Queue	7:1	0x0	Identifies an Rx queue associated with SYN packets.
Reserved	9:8	00b	Reserved for extension of the *Rx Queue* field.
Reserved	30:10	0x0	Reserved.
SYNQFP	31	0b	Defines the priority between SYNQF and 5-tuples filter. 0b = 5-tuple filter priority 1b = SYN filter priority.

8.2.3.7.21 EType Queue Filter — ETQF[n] (0x05128 + 4*n, n=0...7; RW)

See Section 7.1.2.3 for more details on the use of this register.

Field	Bit(s)	Init Val	Description
EType	15:0	0x0	Identifies the protocol running on top of IEEE 802. Used to route Rx packets containing this EtherType to a specific Rx queue. *Note:* Field is defined in little endian (MS byte is first on the wire).
UP	18:16	0x0	User Priority. A 802.1Q UP value to be compared against the *User Priority* field in the Rx packet. Enabled by the *UP Enable* bit.
UP Enable	19	0b	User Priority Enable. Enables comparison of the *User Priority* field in the received packet.
Pool	25:20	0x0	In virtualization modes, determines the target pool for the packet.
Pool Enable	26	0b	In virtualization modes, enables the *Pool* field.
FCoE	27	0b	When set, packets that match this filter are identified as FCoE packets.
Reserved	28	0b	Reserved.
Reserved	29	0b	Reserved.
1588 time stamp	30	0b	When set, packets with this EType are time stamped according to the IEEE 1588 specification.
Filter Enable	31	0b	0b = The filter is disabled for any functionality. 1b = The filter is enabled. Exact actions are determined by separate bits.



8.2.3.7.22 EType Queue Select — ETQS[n] (0x0EC00 + 4*n, n=0...7; RW)

See Section 7.1.2.3 for more details on the use of this register.

Field	Bit(s)	Init Val	Description
Reserved	15:0	0x0	Reserved.
Rx Queue	22:16	0x0	Identifies the Rx queue associated with this EType.
Reserved	24:23	0x0	Reserved for future extension of the *Rx Queue* field.
Reserved	28:25	0x0	Reserved.
Low Latency Interrupt	29	0b	When set, packets that match this filter generate a LLI.
Reserved	30	0x0	Reserved.
Queue Enable	31	0b	When set, enables filtering of Rx packets by the EType defined in this register to the queue indicated in this register.

8.2.3.7.23 Rx Filter ECC Err Insertion 0 — RXFECCERR0 (0x051B8; RW)

Field	Bit(s)	Init Val	Description
Reserved	8:0	0x1FF	Reserved.
ECCFLT_EN	9	0b	Filter ECC Error indication Enablement. When set to 1b, enables the ECC-INT + the RXF-blocking during ECC-ERR in one of the Rx filter memories. At 0b, the ECC logic can still function overcoming only single errors while dual or multiple errors can be ignored silently.
Reserved	31:10	0x0	Reserved.

8.2.3.8 Receive DMA Registers

8.2.3.8.1 Receive Descriptor Base Address Low — RDBAL[n] (0x01000 + 0x40*n, n=0...63 and 0x0D000 + 0x40*(n-64), n=64...127; RW)

Field	Bit(s)	Init Val	Description
0	6:0	0x0	Ignored on writes. Returns 0x0 on reads.
RDBAL	31:7	X	Receive Descriptor Base Address Low.

This register contains the lower bits of the 64-bit descriptor base address. The lower 7 bits are always ignored. The receive descriptor base address must point to a 128 byte-aligned block of data.

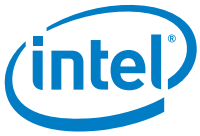
8.2.3.8.2 Receive Descriptor Base Address High — RDBAH[n] (0x01004 + 0x40*n, n=0...63 and 0x0D004 + 0x40*(n-64), n=64...127; RW)

Field	Bit(s)	Init Val	Description
RDBAH	31:0	X	Receive Descriptor Base Address [63:32].

This register contains the upper 32 bits of the 64-bit descriptor base address.

8.2.3.8.3 Receive Descriptor Length — RDLEN[n] (0x01008 + 0x40*n, n=0...63 and 0x0D008 + 0x40*(n-64), n=64...127; RW)

Field	Bit(s)	Init Val	Description
LEN	19:0	0x0	Descriptor Ring Length. This register sets the number of bytes allocated for descriptors in the circular descriptor buffer. It must be 128-byte aligned (7 LS bit must be set to zero). *Note:* Validated lengths up to 128 K (8 K descriptors).
Reserved	31:20	0x0	Reads as 0x0. Should be written to 0x0 for future compatibility.



8.2.3.8.4 Receive Descriptor Head — RDH[n] (0x01010 + 0x40*n, n=0...63 and 0x0D010 + 0x40*(n-64), n=64...127; RO)

Field	Bit(s)	Init Val	Description
RDH	15:0	0x0	Receive Descriptor Head. This register holds the head pointer for the receive descriptor buffer in descriptor units (16-byte datum). The RDH is controlled by hardware.
Reserved	31:16	0x0	Reserved. Should be written with 0x0.

8.2.3.8.5 Receive Descriptor Tail — RDT[n] (0x01018 + 0x40*n, n=0...63 and 0x0D018 + 0x40*(n-64), n=64...127; RW)

Field	Bit(s)	Init Val	Description
RDT	15:0	0x0	Receive Descriptor Tail.
Reserved	31:16	0x0	Reads as 0x0. Should be written to 0x0 for future compatibility.

This register contains the tail pointer for the receive descriptor buffer. The register points to a 16-byte datum. Software writes the tail register to add receive descriptors to the hardware free list for the ring.

Note: The tail pointer should be set to one descriptor beyond the last empty descriptor in host descriptor ring.

8.2.3.8.6 Receive Descriptor Control — RXDCTL[n] (0x01028 + 0x40*n, n=0...63 and 0x0D028 + 0x40*(n-64), n=64...127; RW)

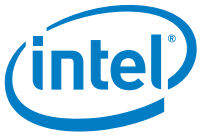
Field	Bit(s)	Init Val	Description
Reserved	13:0	0x0	Reserved.
Reserved	14	0b	Reserved (softwaremight read and write in order to maintain backward compatibility.)
Reserved	15	0b	Reserved.
Reserved	22:16	0x0	Reserved (software might read and write in order to maintain backward compatibility).
Reserved	24:23	00b	Reserved.
ENABLE	25	0b	Receive Queue Enable. When set, the *ENABLE* bit enables the operation of the specific receive queue. Upon read it gets the actual status of the queue (internal indication that the queue is actually enabled/disabled).

Field	Bit(s)	Init Val	Description
Reserved	26	0b	Reserved (software can read and write in order to maintain backward compatibility).
Reserved	29:27	0x0	Reserved.
VME	30	0b	VLAN Mode Enable. 0b = Do not strip VLAN tag. 1b = Strip VLAN tag from received 802.1Q packets destined to this queue.
Reserved	31	0b	Reserved.

8.2.3.8.7 Split Receive Control Registers — SRRCTL[n] (0x01014 + 0x40*n, n=0...63 and 0x0D014 + 0x40*(n-64), n=64...127 / 0x02100 + 4*n, [n=0...15]; RW)

SRRCTL[0...15] are also mapped to address 0x02100... to maintain compatibility with the 82598.

Field	Bit(s)	Init Val	Description
BSIZEPACKET	4:0	0x2	Receive Buffer Size for Packet Buffer. The value is in 1 KB resolution. Value can be from 1 KB to 16 KB. Default buffer size is 2 KB. This field should not be set to 0x0. This field should be greater or equal to 0x2 in queues where RSC is enabled.
Rsv	7:5	000b	Reserved. Should be written with 000b to ensure future compatibility.
BSIZEHEADER	13:8	0x4	Receive Buffer Size for Header Buffer. The value is in 64 bytes resolution. Value can be from 64 bytes to 1024 bytes. *Note:* The maximum supported header size is limited to 1023. Default buffer size is 256 bytes. This field must be greater than zero if the value of DESCTYPE is greater or equal to two. Values above 1024 bytes are reserved for internal use only.
Reserved	21:14	0x0	Reserved.
RDMTS	24:22	000b	Receive Descriptor Minimum Threshold Size. A LLI associated with this queue is asserted each time the number of free descriptors is decreased to RDMTS * 64 (this event is considered as Rx ring buffer almost empty).
DESCTYPE	27:25	000b	Define the descriptor type in Rx: 000b = Legacy. 001b = Advanced descriptor one buffer. 010b = Advanced descriptor header splitting. 011b = Reserved. 100b = Reserved. 101b = Advanced descriptor header splitting always use header buffer. 110b = Reserved. 111b = Reserved.



Field	Bit(s)	Init Val	Description
Drop_En	28	0b	Drop Enabled. If set to 1b, packets received to the queue when no descriptors are available to store them are dropped.
Rsv	31:29	000b	Reserved. Should be written with 000b to ensure future compatibility.

Note: BSIZEHEADER must be bigger than zero if DESCTYPE is equal to 010b, 011b, 100b or 101b.

8.2.3.8.8 Receive DMA Control Register — RDRXCTL (0x02F00; RW)

Field	Bit(s)	Init Val	Description
CRCStrip	1	0	Rx CRC Strip indication to the Rx DMA unit. This bit must be set the same as HLREG0.RXCRCSTRP. 0b = No CRC Strip by HW (Default). 1b = Strip CRC by HW.
Reserved	2	0	Reserved.
DMAIDONE	3	0b	DMA Init Done. When read as 1b, indicates that the DMA initialization cycle is done (RO).
Reserved	16:4	0x0880	Reserved.
RSCFRSTSIZE	21:17	0x8	Defines a minimum packet size (after VLAN stripping, if applicable) for a packet with a payload that can open a new RSC (in units of 16 byte.). See RSCDBU.RSCACKDIS for packets without payload. *Note:* RSCFRSTSIZE is reserved for internal use. Software should set this field to 0x0.
Reserved	24:22	000b	Reserved.
RSCACKC	25	0b	RSC Coalescing on ACK Change. When set, an active RSC completes when the *ACK* bit in the Rx packet is different than the *ACK* bit in the RSC context. When cleared, an active RSC completes only when the *ACK* bit in the Rx packet is cleared while the *ACK* bit in the RSC context is set. *Note:* RSCACKC is reserved for internal use. Software should set this bit to 1b.
FCOE_WRFIX	26	0b	FCoE Write Exchange Fix. When set, DDP context of FC write exchange is closed following a reception of a last packet in a sequence with an active *Sequence Initiative* bit in the F_CTL field. When cleared, the DDP context is not closed. *Note:* FCOE_WRFIX is reserved for internal use. Software should set this bit to 1b.
Reserved	31:27	0	Reserved.

8.2.3.8.9 Receive Packet Buffer Size — RXPBSIZE[n] (0x03C00 + 4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
Reserved	9:0	0x0	Reserved.
SIZE	19:10	0x200	Receive Packet Buffer Size for traffic class 'n' while 'n' is the register index. The size is defined in KB units and the default size of PB[0] is 512 KB. The default size of PB[1-7] is also 512 KB but it is meaningless in non-DCB mode. When DCB mode is enabled the size of PB[1-7] must be set to meaningful values. The total meaningful allocated PB sizes plus the size allocated to the flow director filters should be less or equal to 512 KB. Possible PB allocation in DCB mode for 8 x TCs is 0x40 (64 KB) for all PBs. Other possible setting of 4 x TCs is 0x80 (128 KB) for all PB[0-3] and 0x0 for PB[4-7]. See Section 3.7.7.3.5 for other optional settings with/without the flow director filters *Note:* In any setting the RXPBSIZE[0] must always be enabled (greater than zero).
Reserved	31:20	0x0	Reserved.

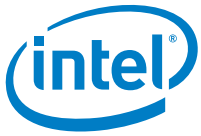
8.2.3.8.10 Receive Control Register — RXCTRL (0x03000; RW)

Field	Bit(s)	Init Val	Description
RXEN	0	0b	Receive Enable. When set to 0b, filter inputs to the packet buffer are ignored.
Reserved	31:1	0x0	Reserved

8.2.3.8.11 Rx Packet Buffer Flush Detect — RXMEMWRAP (0x03190; RO)

This register is used by software as part of a queue disable procedure (described in Section 4.6.7.1)

Field	Bit(s)	Init Val	Description
TC0Wrap	2:0	000b	Packet Buffer 0 Wrap Around Counter. A 3-bit counter that increments on each full cycle through the buffer. Once reaching 111b, the counter warps around to 000b on the next count.
TC0Empty	3	1b	Packet Buffer 0 Empty 0b = Packet buffer is not empty. 1b = Packet buffer is empty.
TC1Wrap	6:4	000b	Packet Buffer 1 Wrap Around Counter. A 3-bit counter that increments on each full cycle through the buffer. Once reaching 111b, the counter warps around to 000b on the next count.
TC1Empty	7	1b	Packet Buffer 1 Empty 0b = Packet buffer is not empty. 1b = Packet buffer is empty.



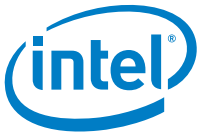
Field	Bit(s)	Init Val	Description
TC2Wrap	10:8	000b	Packet Buffer 2 Wrap Around Counter. A 3-bit counter that increments on each full cycle through the buffer. Once reaching 111b, the counter warps around to 000b on the next count.
TC2Empty	11	1b	Packet Buffer 2 Empty 0b = Packet buffer is not empty. 1b = Packet buffer is empty.
TC3Wrap	14:12	000b	Packet Buffer 3 Wrap Around Counter. A 3-bit counter that increments on each full cycle through the buffer. Once reaching 111b, the counter warps around to 000b on the next count.
TC3Empty	15	1b	Packet Buffer 3 Empty 0b = Packet buffer is not empty. 1b = Packet buffer is empty.
TC4Wrap	18:16	000b	Packet Buffer 4 Wrap Around Counter. A 3-bit counter that increments on each full cycle through the buffer. Once reaching 111b, the counter warps around to 000b on the next count.
TC4Empty	19	1b	Packet Buffer 4 Empty 0b = Packet buffer is not empty. 1b = Packet buffer is empty.
TC5Wrap	22:20	000b	Packet Buffer 5 Wrap Around Counter. A 3-bit counter that increments on each full cycle through the buffer. Once reaching 111b, the counter warps around to 000b on the next count.
TC5Empty	23	1b	Packet Buffer 5 Empty 0b = Packet buffer is not empty. 1b = Packet buffer is empty.
TC6Wrap	26:24	000b	Packet Buffer 6 Wrap Around Counter. A 3-bit counter that increments on each full cycle through the buffer. Once reaching 111b, the counter warps around to 000b on the next count.
TC6Empty	27	1b	Packet Buffer 6 Empty 0b = Packet buffer is not empty. 1b = Packet buffer is empty.
TC7Wrap	30:28	000b	Packet Buffer 7 Wrap Around Counter. A 3-bit counter that increments on each full cycle through the buffer. Once reaching 111b, the counter warps around to 000b on the next count.
TC7Empty	31	1b	Packet Buffer 7 Empty 0b = Packet buffer is not empty. 1b = Packet buffer is empty.

8.2.3.8.12 RSC Data Buffer Control Register — RSCDBU (0x03028; RW)

Field	Bit(s)	Init Val	Description
Reserved	6:0	0x20	Reserved.
RSCACKDIS	7	0b	Disable RSC for ACK Packets. disables the coalescing of TCP packets without TCP payload. This bit should be set if performance problems are found.
Reserved	31:8	0x0	Reserved.

8.2.3.8.13 RSC Control — RSCCTL[n] (0x0102C + 0x40*n, n=0...63 and 0x0D02C + 0x40*(n-64), n=64...127; RW)

Field	Bit(s)	Init Val	Description
RSCEN	0	0b	RSC Enable. When the RSCEN bit is set, RSC is enabled on this queue.
Reserved	1	0b	Reserved
MAXDESC	3:2	00b	Maximum descriptors per Large receive as follow: 00b = Maximum of 1 descriptor per large receive. 01b = Maximum of 4 descriptors per large receive. 10b = Maximum of 8 descriptors per large receive. 11b = Maximum of 16 descriptors per large receive. *Note:* MAXDESC * SRRCTL.BSIZEPKT must not exceed 64 KB minus one, which is the maximum total length in the IP header and must be larger than the expected received MSS.
Reserved	31:4	0x0	Reserved.



8.2.3.9 Transmit Registers

8.2.3.9.1 DMA Tx TCP Max Allow Size Requests — DTXMXSZRQ (0x08100; RW)

This register limits the total number of data bytes that may be in outstanding PCIe requests from the host memory. This allows requests to send low latency packets to be serviced in a timely manner, as this request will be serviced right after the current outstanding requests are completed.

Field	Bit(s)	Init Val	Description
Max_bytes_num_req	11:0	0x10	Max allowed number of bytes requests. The maximum allowed amount of 256 bytes outstanding requests. If the total size request is higher than the amount in the field no arbitration is done and no new packet is requested.
Reserved	31:12	0x0	Reserved.

8.2.3.9.2 DMA Tx Control — DMATXCTL (0x04A80; RW)

Field	Bit(s)	Init Val	Description
TE	0	0b	Transmit Enable. When set, this bit enables the transmit operation of the DMA-Tx.
Reserved	1	0b	Reserved.
Reserved	2	1b	Reserved.
GDV	3	0b	Global Double VLAN Mode. When set, this bit enables the Double VLAN mode.
Reserved	15:4	0x0	Reserved.
VT	31:16	0x8100	VLAN Ether-Type (the VLAN Tag Protocol Identifier — TPID). For proper operation, software must not change the default setting of this field (802.3ac standard defines it as 0x8100). This field must be set to the same value as the VET field in the VLNCTRL register.

8.2.3.9.3 DMA Tx TCP Flags Control Low — DTXTCPFLGL (0x04A88; RW)

This register holds the mask bits for the TCP flags in Tx segmentation (described in Section 7.2.4.7.1 and Section 7.2.4.7.2).

Field	Bit(s)	Init Val	Description
TCP_flg_first_seg	11:0	0xFF6	TCP Flags First Segment. Bits that make AND operation with the TCP flags at TCP header in the first segment.
Reserved	15:12	0x0	Reserved.
TCP_Flg_mid_seg	27:16	0xFF6	TCP Flags Middle Segments. The low bits that make AND operation with the TCP flags at TCP header in the middle segments.
Reserved	31:28	0x0	Reserved.

8.2.3.9.4 DMA Tx TCP Flags Control High- DTXTCPFLGH (0x04A8C; RW)

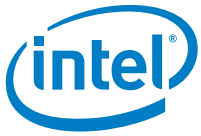
This register holds the mask bits for the TCP flags in Tx segmentation (described in Section 7.2.4.7.3).

Field	Bit(s)	Init Val	Description
TCP_Flg_lst_seg	11:0	0xF7F	TCP Flags Last Segment. Bits that make AND operation with the TCP flags at TCP header in the last segment.
Reserved	31:12	0x0	Reserved.

8.2.3.9.5 Transmit Descriptor Base Address Low — TDBAL[n] (0x06000+0x40*n, n=0...127; RW)

Field	Bit(s)	Init Val	Description
0	6:0	0b	Ignored on writes. Returns 0b on reads.
TDBAL	31:7	X	Transmit Descriptor Base Address Low.

This register contains the lower bits of the 64-bit descriptor base address. The lower seven bits are ignored. The Transmit Descriptor Base Address must point to a 128 byte-aligned block of data.



8.2.3.9.6 Transmit Descriptor Base Address High — TDBAH[n] (0x06004+0x40*n, n=0...127; RW)

Field	Bit(s)	Init Val	Description
TDBAH	31:0	X	Transmit Descriptor Base Address [63:32].

This register contains the upper 32 bits of the 64 bit Descriptor base address.

8.2.3.9.7 Transmit Descriptor Length — TDLEN[n] (0x06008+0x40*n, n=0...127; RW)

Field	Bit(s)	Init Val	Description
LEN	19:0	0x0	Descriptor Ring Length. This register sets the number of bytes allocated for descriptors in the circular descriptor buffer. It must be 128byte-aligned (7 LS bit must be set to zero). *Note:* Validated Lengths up to 128K (8K descriptors).
Reserved	31:20	0x0	Reads as 0x0. Should be written to 0x0.

8.2.3.9.8 Transmit Descriptor Head — TDH[n] (0x06010+0x40*n, n=0...127; RO)

Field	Bit(s)	Init Val	Description
TDH	15:0	0x0	Transmit Descriptor Head.
Reserved	31:16	0x0	Reserved. Should be written with 0x0.

This register contains the head pointer for the transmit descriptor ring. It points to a 16-byte datum. Hardware controls this pointer.

The values in these registers might point to descriptors that are still not in the host memory. As a result, the host cannot rely on these values in order to determine which descriptor to release.

The only time that software should write to this register is after a reset (hardware reset or CTRL.RST) and before enabling the transmit function (TXDCTL.ENABLE). If software were to write to this register while the transmit function was enabled, the on-chip descriptor buffers might be invalidated and the hardware could become confused.

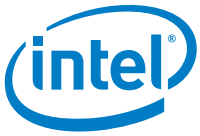
8.2.3.9.9 Transmit Descriptor Tail — TDT[n] (0x06018+0x40*n, n=0...127; RW)

Field	Bit(s)	Init Val	Description
TDT	15:0	0x0	Transmit Descriptor Tail.
Reserved	31:16	0x0	Reads as 0x0. Should be written to 0x0for future compatibility.

This register contains the tail pointer for the transmit descriptor ring. It points to a 16-byte datum. Software writes the tail pointer to add more descriptors to the transmit ready queue. Hardware attempts to transmit all packets referenced by descriptors between head and tail.

8.2.3.9.10 Transmit Descriptor Control — TXDCTL[n] (0x06028+0x40*n, n=0...127; RW)

Field	Bit(s)	Init Val	Description
PTHRESH	6:0	0x0	Pre-Fetch Threshold Controls when a prefetch of descriptors is considered. This threshold refers to the number of valid, unprocessed transmit descriptors the 82599 has in its on-chip buffer. If this number drops below PTHRESH, the algorithm considers pre-fetching descriptors from host memory. However, this fetch does not happen unless there are at least HTHRESH valid descriptors in host memory to fetch. *Note:* HTHRESH should be given a non-zero value each time PTHRESH is used.
Rsv	7	0x0	Reserved.
HTHRESH	14:8	0x0	Host Threshold.
Rsv	15	0x0	Reserved.
WTHRESH	22:16	0x0	Write-Back Threshold. Controls the write-back of processed transmit descriptors. This threshold refers to the number of transmit descriptors in the on-chip buffer that are ready to be written back to host memory. In the absence of external events (explicit flushes), the write-back occurs only after at least WTHRESH descriptors are available for write-back. *Note:* Since the default value for write-back threshold is 0b, descriptors are normally written back as soon as they are processed. WTHRESH must be written to a non-zero value to take advantage of the write-back bursting capabilities of the 82599. *Note:* When WTHRESH is set to a non-zero value, the software driver should not set the RS bit in the Tx descriptors. When WTHRESH is set to zero the software device driver should set the RS bit in the Tx descriptors with the EOP bit set and at least once in the 40 descriptors. *Note:* When Head write-back is enabled (TDWBAL[n].Head_WB_En = 1b), the WTHRESH must be set to zero.
Reserved	24:23	0x0	Reserved.



Field	Bit(s)	Init Val	Description
ENABLE	25	0b	Transmit Queue Enable. When set, this bit enables the operation of a specific transmit queue: Default value for all queues is 0b. Setting this bit initializes all the internal registers of a specific queue. Until then, the state of the queue is kept and can be used for debug purposes. When disabling a queue, this bit is cleared only after all activity at the queue stopped. *Note:* This bit is set only when the queue is enabled. Upon read – get the actual status of the queue (internal indication that the queue is actually enabled/disabled) *Note:* When setting the global Tx enable DMATXCTL.TE the ENABLE bit of Tx queue zero is enabled as well.
SWFLSH	26	0b	Transmit Software Flush. This bit enables software to trigger descriptor write-back flushing, independently of other conditions. This bit is self cleared by hardware.
Reserved	27	0b	Reserved.
Reserved	28	0b	Reserved.
Reserved	29	0b	Reserved.
Reserved	31:30	0x0	Reserved.

This register controls the fetching and write-back of transmit descriptors. The three threshold values are used to determine when descriptors is read from and written to host memory.

Note: When WTHRESH = 0b only descriptors with the *RS* bit set are written back.

For PTHRESH and HTHRESH recommended setting please refer to Section 7.2.3.4.

8.2.3.9.11 Tx Descriptor Completion Write Back Address Low — TDWBAL[n] (0x06038+0x40*n, n=0...127; RW)

Field	Bit(s)	Init Val	Description
Head_WB_En	0	0b	Head Write-Back Enable. 0b = Head write-back is disabled. 1b = Head write-back is enabled. When head_WB_en is set, the 82599 does not write-back Tx descriptors.
Reserved	1	0	Reserved.
HeadWB_Low	31:2	0x0	Lowest 32 bits of the head write-back memory location (Dword aligned). Last 2 bits of this field are ignored and are always read as 0.0, meaning that the actual address is Qword aligned.

8.2.3.9.12 Tx Descriptor Completion Write Back Address High — TDWBAH[n] (0x0603C+0x40*n, n=0...127; RW)

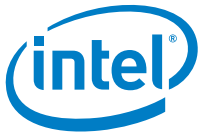
Field	Bit(s)	Init Val	Description
HeadWB_High	31:0	0x0	Highest 32 bits of head write-back memory location (for 64-bit addressing).

8.2.3.9.13 Transmit Packet Buffer Size — TXPBSIZE[n] (0x0CC00 + 0x4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
Reserved	9:0	0x0	Reserved.
SIZE	19:10	0xA0 (160 KB)	Transmit packet buffer size of TCn. At default setting (no DCB) only packet buffer 0 is enabled and TXPBSIZE values for TC 1-7 are meaningless. Other than the default configuration the 82599 supports partitioned configurations when DCB is enabled. Symmetrical 8 TCs partitioning: 0x14 (20KB) for TXPBSIZE[0...7]. Symmetrical 4 TCs partitioning: 0x28 (40KB) for TXPBSIZE[0...3] and 0x0 (0KB) for TXPBSIZE[4...7]. Non-symmetrical partitioning are supported as well. In order to enable wire speed transmission it is recommended to set the transmit packet buffers to: (1) At least 2 times MSS plus PCIe latency (approximate 1 KB) when IPSec AH is not enabled (security block is not enabled or operates in path through mode). (2) At least 3 times MSS plus PCIe latency when IPSec AH is enabled (security block operates in store and forward mode)
Reserved	31:20	0x0	Reserved.

8.2.3.9.14 Manageability Transmit TC Mapping — MNGTXMAP (0x0CD10; RW)

Field	Bit(s)	Init Val	Description
MAP	2:0	0x0	Map value indicates the TC that the transmit manageability traffic is routed to.
Reserved	31:3	0x0	Reserved.



8.2.3.9.15 Multiple Transmit Queues Command Register — MTQC (0x08120; RW)

This register can be modified only as part of the init phase.

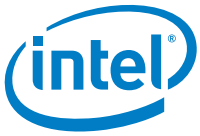
Field	Bit(s)	Init Val	Description
RT_Ena	0	0b	DCB Enabled Mode. See functionality in the following table.
VT_Ena	1	0b	Virtualization Enabled Mode. When set, the 82599 supports either 16, 32, or 64 pools. See functionality in the following table. This bit should be set the same as PFVTCTL.VT_Ena.
NUM_TC_OR_Q	3:2	00b	Number of TCs or Number of Tx Queues per Pools. See functionality in the following table.
Reserved	31:4	0x0	Reserved.

Permitted value and functionality of: RT_Ena; VT_Ena; NUM_TC_OR_Q. For Tx queue assignment in DCB and VT modes refer to Table 7-25 in Section 7.2.1.2.1.

Device Setting			Device Functionality	
RT_Ena	VT_Ena	NUM_TC_OR_Q	Tx Queues	TC & VT
0b	0b	00b	0 — 63	-
<> 0b	<> 0b	00b	Reserved	
0b	0b	<> 00	Reserved	
1b	0b	01b	Reserved	
1b	0b	10b	0 — 127	TC0 — TC3
1b	0b	11b	0 — 127	TC0 — TC7
0b	1b	01b	0 — 127	64 VMs
0b	1b	10b	0 — 127	32 VMs
0b	1b	11b	Reserved	
1b	1b	01b	Reserved	
1b	1b	10b	0 — 127	TC0 — TC3 & 32 VMs
1b	1b	11b	0 — 127	TC0 — TC7 & 16 VMs

8.2.3.9.16 Tx Packet Buffer Threshold — TXPBTHRESH (0x04950 +0x4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
THRESH	9:0	0x96/0x0	Threshold used for checking room place in Tx packet buffer of TCn. Threshold in KB units, when the packet buffer is filled up with payload over that threshold, no more data read request is sent. Default values: 0x96 (150 KB) for TXPBSIZE0. 0x0 (0 KB) for TXPBSIZE1-7. It should be set to: (packet buffer size) — MSS. For instance, if packet buffer size is set to 20 KB in corresponding TXPBSIZE.SIZE, if MSS of 9.5 KB (9728-byte) jumbo frames is supported for TCn, it is set to: 0xA (10 KB).
Reserved	31:10	0x0	Reserved.



8.2.3.10 DCB Registers

DCB registers are owned by the PF in an IOV mode.

8.2.3.10.1 DCB Receive Packet Plane Control and Status — RTRPCS (0x02430; RW)

RTRPCS is equivalent to the 82598's RMCS.

Field	Bit(s)	Init Val	Description
Reserved	0	0b	Reserved.
RRM	1	0b	Receive Recycle Mode defines the recycle mode within a BWG. 0b = No recycle. 1b = Recycle within the BWG. It is the only supported mode when DCB is enabled.
RAC	2	0b	Receive Arbitration Control. 0b = Round Robin (RR). 1b = Weighted Strict Priority (WSP).
Reserved	5:3	0x0	Reserved.
Reserved	15:6	0x0	Reserved.
LRPB	18:16	0x0	Last Received Packet Buffer Status Indication. Indicates the last packet buffer that was used in Rx arbiter.
Reserved	26:19	0x0	Reserved.
Reserved	27	0b	Reserved
Reserved	31:28	0x6	Reserved

8.2.3.10.2 DCB Transmit Descriptor Plane Control and Status — RTTDCS (0x04900; RW) DMA-Tx

RTTDCS was DPMCS mapped to 0x07F40 in the 82598.

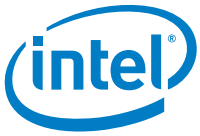
Field	Bit(s)	Init Val	Description
TDPAC	0	0b	TC Transmit Descriptor Plane Arbitration Control. 0b = RR 1b = WSP
VMPAC	1	0b	VM Transmit Descriptor Plane Arbitration Control. 0b = RR 1b = Weighted Round Robin (WRR).
Reserved	3:2	00b	Reserved.

Field	Bit(s)	Init Val	Description
TDRM	4	0b	TC Transmit descriptor plane recycle mode defines the recycle mode within a BWG. 0b = No recycle. 1b = Recycle within the BWG. It is the only supported mode.
Reserved	5	0b	Reserved.
ARBDIS	6	0	DCB Arbiters Disable. When set to 1 this bit pauses the Tx Descriptor plane arbitration state-machine. Therefore, during nominal operation this bit should be set to 0.
Reserved	16:7	0	Reserved.
LTTDESC (RO)	19:17	0x0	Last Transmitted TC (RO). This field indicates the last transmitted TC in XMIT descriptor arbiter DMA.
Reserved	21:20	00b	Reserved.
BDPM	22	1b	Bypass Data_Pipe Monitor. In order to enable bypassing the above limit. In DCB mode, this bit must be cleared.
BPBFSM	23	1b	Bypass Packet Buffer Free Space Monitor. In order to enable bypassing the packet buffer free space monitor (not checking if there is enough free space in the packet buffer before requesting the data). This bit must be cleared in DCB mode or SR-IOV mode.
Reserved	30:24	0x0	Reserved.
SPEED_CHG	31	0b	Link speed has changed. Read and clear flag. Set by hardware to indicate that the link speed has changed. Cleared by software at the end of the link speed change procedure. Refer to Section 4.6.11.2.

8.2.3.10.3 DCB Transmit Packet Plane Control and Status- RTTPCS (0x0CD00; RW)

RTTPCS is mapped to 0x0CD00 for compatibility with the 82598's PDPMCS.

Field	Bit(s)	Init Val	Description
Reserved	4:0	0x0	Reserved
TPPAC	5	0b	Transmit Packet Plane Arbitration Control 0b = RR (with respect to stop markers). 1b = Strict Priority (SP), with respect to stop markers)
Reserved	7:6	00b	Reserved.
TPRM	8	0b	Transmit packet plane recycle mode defines the recycle mode within a BWG. 0b = No recycle. 1b = Recycle within the BWG.



Field	Bit(s)	Init Val	Description
Reserved	21:9	0x0	Reserved.
ARBD	31:22	0x224	ARB_delay. Minimum cycles delay between a packet's arbitration. When RTTPCS.TPPAC is set to 1b the arbitration delay is according to ARBD, otherwise the arbitration delay is 0x0. Should be kept at default in non-DCB mode. In DCB mode, should be set to 0x004.

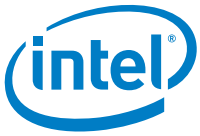
8.2.3.10.4 DCB Receive User Priority to Traffic Class — RTRUP2TC (0x03020; RW)

Field	Bit(s)	Init Val	Description
UP0MAP	2:0	0x0	Receive UP 0 to TC Mapping. When set to n, UP 0 is bound to TC n. Used for two purposes: • Define into which Rx packet buffer incoming traffic carrying 802.1p field set to 0 is routed. • Define according to the filling status of which Rx packet puffer a Priority Flow Control (PFC) frame with the *Timer 0* field and Class Enable Vector bit 0 set is sent.
UP1MAP	5:3	0x0	Receive UP 1 to TC Mapping. When set to n, UP 1 is bound to TC n. Used for two purposes: • Define into which Rx packet buffer incoming traffic carrying 802.1p field set to 1 is routed. • Define according to the filling status of which Rx Packet Buffer a P FC frame with the *Timer 1* field and *Class Enable Vector* bit 1 set is sent.
UP2MAP	8:6	0x0	Receive UP 2 to TC Mapping. When set to n, UP 2 is bound to TC n. Used for two purposes: • Define into which Rx packet buffer incoming traffic carrying 802.1p field set to 2 is routed. • Define according to the filling status of which Rx Packet Buffer a PFC frame with the *Timer 2* field and *Class Enable Vector* bit 2 set is sent.
UP3MAP	11:9	0x0	Receive UP 3 to TC Mapping. When set to n, UP 3 is bound to TC n. Used for two purposes: • Define into which Rx packet buffer incoming traffic carrying 802.1p field set to 3 is routed. • Define according to the filling status of which Rx packet buffer a PFC frame with the *Timer 3* field and *Class Enable Vector* bit 3 set is sent.
UP4MAP	14:12	0x0	Receive UP 4 to TC Mapping. When set to n, UP 4 is bound to TC n. Used for two purposes: • Define into which Rx packet buffer incoming traffic carrying 802.1p field set to 4 is routed. • Define according to the filling status of which Rx packet buffer a PFC frame with the *Timer 4* field and *Class Enable Vector* bit 4 set is sent.

Field	Bit(s)	Init Val	Description
UP5MAP	17:15	0x0	Receive UP 5 to TC Mapping. When set to n, UP 5 is bound to TC n. Used for two purposes: • Define into which Rx packet buffer incoming traffic carrying 802.1p field set to 5 is routed. • Define according to the filling status of which Rx packet buffer a PFC frame with the *Timer 5* field and *Class Enable Vector* bit 5 set is sent.
UP6MAP	20:18	0x0	Receive UP 6 to TC Mapping. When set to n, UP 6 is bound to TC n. Used for two purposes: • Define into which Rx packet buffer incoming traffic carrying 802.1p field set to 6 is routed. • Define according to the filling status of which Rx packet buffer a PFC frame with the *Timer 6* field and *Class Enable Vector* bit 6 set is sent.
UP7MAP	23:21	0x0	Receive UP 7 to TC Mapping. When set to n, UP 7 is bound to TC n. Used for two purposes: • Define into which Rx packet buffer incoming traffic carrying 802.1p field set to 7 is routed. • Define according to the filling status of which Rx packet buffer a PFC frame with the *Timer 7* field and *Class Enable Vector* bit 7 set is sent.
Reserved	31:24	0x0	Reserved.

8.2.3.10.5 DCB Transmit User Priority to Traffic Class — RTTUP2TC (0x0C800; RW)

Field	Bit(s)	Init Val	Description
UP0MAP	2:0	0x0	Transmit UP 0 to TC Mapping. When set to n, UP 0 is bound to TC n. Used when receiving a PFC frame with the *Timer 0* field and *Class Enable Vector* bit 0 set, to determine which TC must be paused.
UP1MAP	5:3	0x0	Transmit UP 1 to TC Mapping. When set to n, UP 1 is bound to TC n. Used when receiving a PFC frame with the *Timer 1* field and *Class Enable Vector* bit 1 set, to determine which TC must be paused.
UP2MAP	8:6	0x0	Transmit UP 2 to TC Mapping. When set to n, UP 2 is bound to TC n. Used when receiving a PFC frame with the *Timer 2* field and *Class Enable Vector* bit 2 set, to determine which TC must be paused.
UP3MAP	11:9	0x0	Transmit UP 3 to TC Mapping. When set to n, UP 3 is bound to TC n. Used when receiving a PFC frame with the *Timer 3* field and *Class Enable Vector* bit 3 set, to determine which TC must be paused.



Field	Bit(s)	Init Val	Description
UP4MAP	14:12	0x0	Transmit UP 4 to TC Mapping. When set to n, UP 4 is bound to TC n. Used when receiving a PFC frame with the *Timer 4* field and *Class Enable Vector* bit 4 set, to determine which traffic class must be paused.
UP5MAP	17:15	0x0	Transmit UP 5 to TC Mapping. When set to n, UP 5 is bound to TC n. Used when receiving a PFC frame with the *Timer 5* field and *Class Enable Vector* bit 5 set, to determine which traffic class must be paused.
UP6MAP	20:18	0x0	Transmit UP 6 to TC Mapping. When set to n, UP 6 is bound to V n. Used when receiving a PFC frame with the *Timer 6* field and *Class Enable Vector* bit 6 set, to determine which traffic class must be paused.
UP7MAP	23:21	0x0	Transmit UP 7 to TC Mapping. When set to n, UP 7 is bound to TC n. Used when receiving a PFC frame with the *Timer 7* field and *Class Enable Vector* bit 7 set, to determine which TC must be paused.
Reserved	31:24	0x0	Reserved.

8.2.3.10.6 DCB Receive Packet Plane T4 Config — RTRPT4C[n] (0x02140 + 4*n, n=0...7; RW)

RTRPT4C is equivalent to the 82598's RT2CR.

Field	Bit(s)	Init Val	Description
CRQ	8:0	0x0	Credit Refill Quantum. Amount of credits to refill in 64-byte granularity. Possible values 0x000:0x1FF (0 to 32,704 bytes).
BWG	11:9	0x0	Bandwidth Group Index. Bandwidth Group (BWG).
MCL	23:12	0x0	Max Credit Limit. Maximum amount of credits for a configured packet buffer in 64-byte granularity. Possible values 0x000:0xFFF (0to 262,080bytes).
Reserved	29:24	0x0	Reserved.
GSP	30	0b	Group Strict Priority. When set to 1b enables strict priority to the appropriate packet buffer over any traffic of other packet buffers within the group.
LSP	31	0b	Link Strict Priority. If set to 1b enables strict priority to the appropriate packet buffer over any traffic of other packet buffers.

8.2.3.10.7 Strict Low Latency Tx Queues — TXLLQ[n] (0x082E0 + 4*n, n=0...3; RW)

Field	Bit(s)	Init Val	Description
Strict Low latency	31:0	0x0	Strict Low Latency Enable. When set, defines the relevant Tx queue as strict low latency. All queues belong to a LSP TC must be set as strict low latency queues. Bit 'm' in register 'n' correspond to Tx queue 32 x 'n' + 'm'.

8.2.3.10.8 DCB Receive Packet Plane T4 Status — RTRPT4S[n] (0x02160 + 4*n, n=0...7; RO)

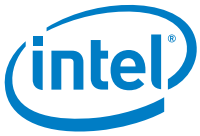
RTRPT4S is equivalent to the 82598's RT2SR.

Field	Bit(s)	Init Val	Description
Reserved	31:0	0x0	Reserved.

8.2.3.10.9 DCB Transmit Descriptor Plane T2 Config - RTTDT2C[n] (0x04910 + 4*n, n=0...7; RW) DMA-Tx

RTTDT2C was TDTQ2TCCR in the 82598 at 0x0602C + 0x40*n, n=0...7.

Field	Bit(s)	Init Val	Description
CRQ	8:0	0x0	Credit Refill Quantum. Amount of credits to refill the TC in 64-byte granularity Possible values 0x000 – 0x1FF (0 – 32,704 bytes)
BWG	11:9	0x0	Bandwidth Group Index. Assignment of this TC to a bandwidth group.
MCL	23:12	0x0	Max Credit Limit. Max amount of credits for a configured TC in 64-byte granularity Possible values 0x000 – 0xFFF (0 – 262,080 bytes)
Reserved	29:24	0x0	Reserved.
GSP	30	0b	Group Strict Priority. When set to 1b enables strict priority to the appropriate TC over any traffic of other TCs within the group.
LSP	31	0b	Link Strict Priority. When set to 1b enables strict priority to the appropriate TC over any traffic of other TCs.



8.2.3.10.10 DCB Transmit Packet Plane T2 Config — RTTPT2C[n] (0x0CD20 + 4*n, n=0...7; RW)

RTTPT2C is mapped to 0x0CD20 + 4*n [n=0...7] for compatibility with the 82598's TDPT2TCCR.

Field	Bit(s)	Init Val	Description
CRQ	8:0	0x0	Credit Refill Quantum. Amount of credits to refill the TC in 64-byte granularity. Possible values 0x000: 0x1FF (0 to 32,704 bytes).
BWG	11:9	0x0	Bandwidth Group. Assignment of this TC to a BWG.
MCL	23:12	0x0	Max Credit Limit. Max amount of credits for a configured TC in 64-byte granularity. Possible values 0x000:0xFFF (0 – 262,080 bytes).
Reserved	29:24	0x0	Reserved.
GSP	30	0b	Group Strict Priority. When set to 1b enables strict priority to the appropriate TC over any traffic of other TCs within the group.
LSP	31	0b	Link Strict Priority. When set to 1b enables strict priority to the appropriate TC over any traffic of other TCs.

8.2.3.10.11 DCB Transmit Packet plane T2 Status — RTTPT2S[n] (0x0CD40 + 4*n, n=0...7; RO)

RTTPT2S is mapped to 0x0CD40 + 4*n [n=0...7] for compatibility with the 82598's TDPT2TCSR.

Field	Bit(s)	Init Val	Description
Reserved	31:0	0x0	Reserved.

8.2.3.10.12 DCB Transmit Rate–Scheduler MMW — RTTBCNRM (0x04980; RW)

Field	Bit(s)	Init Val	Description
MMW_SIZE	10:0	0x0	Maximum memory window size for the rate-scheduler (for all Tx queues). This is the maximum amount of 1 KB units of payload compensation time that can be accumulated for Tx queues attached to TCn. This number must be multiplied by the rate-factor of the Tx queue before performing the MMW saturation check for that queue.
Reserved	31:11	0x0	Reserved.

8.2.3.10.13 DCB Transmit Descriptor Plane Queue Select — RTTDQSEL (0x04904; RW)

Field	Bit(s)	Init Val	Description
TXDQ_IDX	6:0	0x0	Tx Descriptor Queue Index or TX Pool of Queues Index This register is used to set VM and Transmit Scheduler parameters that are configured per Tx queue or per Tx pool of queues via indirect access. It means that prior to read or write access such registers, software has to make sure this field contains the index of the Tx queue or Tx pool of queue to be accessed. When DCB is disabled, VM parameters include a pool of Tx queues. As a result, this field points to the index of the pool (and not a queue index). When DCB is enabled, and/or when programming rate limiters, this field points to a Tx queue index. The registers that are affected by this index are: RTTDT1C, RTTDT1S, RTTBCNRC, RTTBCNRS
Reserved	31:7	0x0	Reserved.

8.2.3.10.14 DCB Transmit Descriptor Plane T1 Config — RTTDT1C (0x04908; RW)

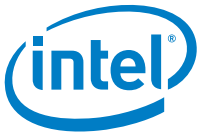
128 internal registers indirectly addressed via RTTDQSEL.TXDQ_IDX. When DCB is disabled, configure the pool index with the credits allocated to the entire pool.

Field	Bit(s)	Init Val	Description
CRQ	13:0	X	Credit Refill Quantum. Amount of credits to refill the VM in 64-byte granularity. Possible values 0x000:0x3FFF (0 to 1,048,512 bytes).
Reserved	31:14	0x0	Reserved.

8.2.3.10.15 DCB Transmit Descriptor Plane T1 Status — RTTDT1S (0x0490C; RO)

128 internal registers indirectly addressed via RTTDQSEL.TXDQ_IDX.

Field	Bit(s)	Init Val	Description
Reserved	31:0	0x0	Reserved.



8.2.3.10.16 DCB Transmit Rate-Scheduler Config — RTTBCNRC (0x04984; RW)

128 internal registers indirectly addressed via RTTDQSEL.TXDQ_IDX.

Field	Bit(s)	Init Val	Description
RF_DEC	13:0	X	Tx rate-scheduler rate factor hexadecimal part, for the Tx queue indexed by TXDQ_IDX field in the RTTDQSEL register. Rate factor bits that come after the hexadecimal point. Meaningful only if the *RS_ENA* bit is set. When RTTBCNRD.DRIFT_ENA is set, this field is periodically modified by hardware as well.
RF_INT	23:14	X	Tx rate-scheduler rate factor integral part, for the Tx queue indexed by TXDQ_IDX field in the RTTDQSEL register Rate factor bits that come before the hexadecimal point. Rate factor is defined as the ratio between the nominal link rate (such as 1 GbE) and the maximum rate allowed to that queue . Minimum allowed bandwidth share for a queue is 0.1% of the link rate. For example, 10 Mb/s for the 82599 operated at 10 GbE, leading to a maximum allowed rate factor of 1000. Meaningful only if the *RS_ENA* bit is set. When RTTBCNRD.DRIFT_ENA is set, this field is periodically modified by hardware as well.
Reserved	30:24	0x0	Reserved.
RS_ENA (SC)	31b	0	Tx rate-scheduler enable, for the Tx queue indexed by TXDQ_IDX field in the RTTDQSEL register When set, the rate programmed in this register is enforced (the queue is rate controlled). At the time it is set, the current timer value is loaded into the time stamp stored for that entry. The bit can be self-cleared internally if the full line rate is recovered via the rate-drift mechanism. When cleared, the rate factor programmed in this register is meaningless, the switch for that queue is always forced to on. The queue is not rate-controlled . Bandwidth group assignment of this TC to a BWG. Each TC must be assigned to a different BWG number, unless the TC is a member of a BWG. No more than two TCs can share the same BWG.

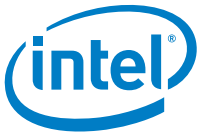
8.2.3.10.17 DCB Transmit Rate-Scheduler Status — RTTBCNRS (0x04988; RW)

128 internal registers indirectly addressed via RTTDQSEL.TXDQ_IDX.

Field	Bit(s)	Init Val	Description
MIFS	31:0		Tx rate-scheduler current Minimum Inter-Frame Spacing (MIFS), for the Tx queue indexed by TXDQ_IDX field in the RTTDQSEL register. When read, it is the current algebraic value of the MIFS interval for the queue, expressed in byte units (31 LS-bits taken), relative to the rate-scheduler. It is obtained by hardware subtracting the current value of the timer associated to that rate-scheduler from the time stamp stored for that queue. A strict positive value means a switch in off state. It is expressed in 2's complement format.

8.2.3.10.18 DCB Transmit BCN Rate Drift — RTTBCNRD (0x0498C; RW)

Field	Bit(s)	Init Val	Description
Reserved	0	0b	Reserved
BCN_CLEAR_ALL	1	0b/SC	Clear all BCN rate-limiters. When set, the 128 RTTBCNRC.RS_ENA bits are cleared — releasing any active BCN rate-limiter. This bit must be set by software each time the link speed has changed. This bit is self cleared by hardware.
DRIFT_FAC	15:2	0b	BCN Rate Drift Factor. Rate drift factor bits that come after the hexadecimal point, while a zero is always assumed before the hexadecimal point (because rate drift factor must be smaller than unity). The rate drift factor ranges from 0.00006 to 0.99994. Rate drift factor is a decreasing factor by which every rate-factor of BCN rate-controlled queues must be multiplied periodically, once every DRIFT_INT µs. Each time the rate-factor of a queue reaches unity, the *RS_ENA* bit in its corresponding RTTBCNRC register is internally cleared. Meaningful only when the *DRIFT_ENA* bit is set.
DRIFT_INT	30:16	0b	BCN Rate Drift Interval Timer. Interval in µs used internally to periodically increase the rate of BCN rate-controlled queues (namely the rate-drift mechanism). Meaningful only when the *DRIFT_ENA* bit is set.
DRIFT_ENA	31	0b	BCN Rate Drift Enable bit. When cleared, the rate-drift mechanism performed by hardware is disabled. It is assumed software handles it. When set, the rate-drift mechanism performed by hardware is enabled. Rate of BCN rate-controlled queues are periodically increased in a multiplicative manner. Relevant only for Tx queues for which the *RX_ENA* bit is set in the RTBCNRC register.



8.2.3.11 DCA Registers

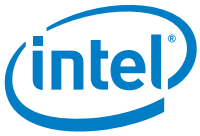
8.2.3.11.1 Rx DCA Control Register — DCA_RXCTRL[n] (0x0100C + 0x40*n, n=0...63 and 0x0D00C + 0x40*(n-64), n=64...127 / 0x02200 + 4*n, [n=0...15]; RW)

DCA_RXCTRL[0...15] are also mapped to address 0x02200... to maintain compatibility with the 82598.

Field	Bit(s)	Init Val	Description
Reserved	4:0	00x	Reserved.
Rx Descriptor DCA EN	5	0b	Descriptor DCA EN. When set, hardware enables DCA for all Rx descriptors written back into memory. When cleared, hardware does not enable DCA for descriptor write-backs.
Rx Header DCA EN	6	0b	Rx Header DCA EN. When set, hardware enables DCA for all received header buffers. When cleared, hardware does not enable DCA for Rx Headers.[1]
Rx Payload DCA EN	7	0b	Payload DCA EN. *Note:* When set, hardware enables DCA for all Ethernet payloads written into memory. When cleared, hardware does not enable DCA for Ethernet payloads. Default cleared.
Reserved	8	0b	Reserved.
RXdescReadROEn	9	1b	Rx Descriptor Read Relax Order Enable
Reserved	10	0b	Reserved.
RXdescWBROen	11	0b (RO)	Rx Descriptor Write Back Relax Order Enable. This bit must be 0b to enable correct functionality of the descriptors write back.
Reserved	12	1b	Reserved. Must be set to 0.
RXdataWriteROEn	13	1b	Rx data Write Relax Order Enable
Reserved	14	0b	Reserved.
RxRepHeaderROEn	15	1b	Rx Split Header Relax Order Enable
Reserved	23:16	0x0	Reserved.
CPUID	31:24	0x0	Physical ID (see complete description in Section 3.1.3.1.2). Legacy DCA capable platforms — The device driver, upon discovery of the physical CPU ID and CPU bus ID, programs the *CPUID* field with the physical CPU and bus ID associated with this Rx queue. DCA 1.0 capable platforms — The device driver programs a value, based on the relevant APIC ID, associated with this Rx queue.

8.2.3.11.2 Tx DCA Control Registers — DCA_TXCTRL[n] (0x0600C + 0x40*n, n=0...127; RW)

Field	Bit(s)	Init Val	Description
Reserved	4:0	0x0	Reserved.
Tx Descriptor DCA EN	5	0b	Descriptor DCA Enable. When set, hardware enables DCA for all Tx descriptors written back into memory. When cleared, hardware does not enable DCA for descriptor write-backs. This bit is cleared as a default and also applies to head write back when enabled.
Reserved	7:6	00b	Reserved.
Reserved	8	0b	Reserved.
TXdescRDROEn	9	1b	Tx Descriptor Read Relax Order Enable.
Reserved	10	0b	Reserved.
TXdescWBROen	11	1b	Relax Order Enable of Tx Descriptor as well as head pointer write back (when set).
Reserved	12	0b	Reserved.
TXDataReadROEn	13	1b	Tx Data Read Relax Order Enable.
Reserved	23:14	0x0	Reserved.
CPUID	31:24	0x0	Physical ID (see complete description in Section 3.1.3.1.2) Legacy DCA capable platforms — the device driver, upon discovery of the physical CPU ID and CPU bus ID, programs the CPUID field with the physical CPU and bus ID associated with this Tx queue. DCA 1.0 capable platforms — the device driver programs a value, based on the relevant APIC ID, associated with this Tx queue.



8.2.3.11.3 DCA Requester ID Information Register — DCA_ID (0x11070; RO)

To ease software implementation, a DCA requester ID field, composed of device ID, bus # and function # is set up in MMIO space for software to program the chipset DCA Requester ID Authentication register.

Field	Bit(s)	Init Val	Description
Function Number	2:0	0x0	Function Number. Function number assigned to the function based on BIOS/OS enumeration.
Device Number	7:3	0x0	Device Number. Device number assigned to the function based on BIOS/OS enumeration.
Bus Number	15:8	0x0	Bus Number. Bus Number assigned to the function based on BIOS/OS enumeration.
Reserved	31:16	0x0	Reserved.

8.2.3.11.4 DCA Control Register — DCA_CTRL (0x11074; RW)

Note: This register is shared by both LAN functions.

Field	Bit(s)	Init Val	Description
DCA_DIS	0	1b	DCA Disable. 0b = DCA tagging is enabled for this device. 1b = DCA tagging is disabled for this device.
DCA_MODE	4:1	0x0	DCA Mode. 0000b = Legacy DCA is supported. The *TAG* field in the TLP header is based on the following coding: bit 0 is DCA enable; bits 3:1 are CPU ID). 0001b = DCA 1.0 is supported. When DCA is disabled for a given message, the *TAG* field is 0000b,0000b. If DCA is enabled, the TAG is set per queue as programmed in the relevant DCA Control register. All other values are undefined.
Reserved	31:5	0x0	Reserved.

8.2.3.12 Security Registers

Security registers are mainly concerned with the internal settings of the AES crypto engine shared by LinkSec and IPsec. They are owned by the PF in an IOV mode.

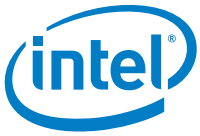
Refer to Section 4.6.12 for the way to modify these registers prior to enabling or disabling a security offload. Note that only one security offload, either LinkSec or IPsec, can be enabled at a time.

Security offload can be disabled via internal security fuses. In this case, the following security related fields are not writable:

- SECTXCTRL.SECTX_DIS is read as 0x1.
- SECRXCTRL.SECRX_DIS is read as 0x1.
- IPSTXIDX.IPS_TX_EN is read as 0x0.
- IPSRXIDX.IPS_RX_EN is read as 0x0.
- LSECTXCTRL bits 1:0 are read as 00b.
- LSECRXCTRL bits 3:2 are read as 00b.

8.2.3.12.1 Security Tx Control — SECTXCTRL (0x08800; RW)

Field	Bit(s)	Init Val	Description
SECTX_DIS	0	1b RW / RO if fused-off	Tx Security Offload Disable Bit. When set, the AES crypto engine used in Tx by LinkSec and IPsec off loads is disabled. This mode must be used to save the 82599's power consumption when no security offload is enabled. When cleared, the AES crypto engine used in Tx by LinkSec or IPsec off load is enabled. Normal operating mode when a security offload is enabled.
TX_DIS	1	0b	Disable Sec Tx Path. When set, no new packet is fetched out from the Tx packet buffers, so that the Tx security block can be internally emptied prior to changing the security mode. SECTXSTAT.SECTX_RDY bit is deasserted until the path is emptied by hardware. When cleared, Tx data path is enabled. Normal operating mode.
STORE_FORWARD	2	0b	Tx Sec Buffer Mode. When set, a complete frame is stored in the internal security Tx buffer prior to being forwarded to the MAC. Operating mode when IPsec offload is enabled (as requested to overwrite ICV field in AH frames). *Note:* It increases the Tx internal latencies (for all TCs). When cleared, Tx sec buffer is operated in pass-through mode. Operating mode when LinkSec is enabled or when no security offload is enabled.
Reserved	31:3	0x0	Reserved.



8.2.3.12.2 Security Tx Status — SECTXSTAT (0x08804; RO)

Field	Bit(s)	Init Val	Description
SECTX_RDY	0	0b	Tx security block ready for mode change. When set, it indicates that the internal data path from the Tx packet buffers to the Tx security block has been emptied, and thus the security mode can be changed by software. When cleared, it indicates that the internal data path from the Tx packet buffers to the Tx security block is not empty, and thus software cannot change the security mode. This bit is polled by software once the SECTXCTRL.TX_DIS bit was set.
SECTX_OFF_DIS	1	0b	Security offload is disabled by fuse or strapping pin.
ECC_TXERR	2	0b	Unrecoverable ECC error in the Tx SA table or SEC Tx FIFO occurred. When set, it indicates that an unrecoverable ECC error occurred when accessing internally the Tx SA table. The ECC interrupt is set as well, until the device is reset by software. When cleared, no ECC error occurred on the Tx SA table from the last time the device has reset.
Reserved	31:3	0x0	Reserved.

8.2.3.12.3 Security Tx Buffer Almost Full — SECTXBUFFAF (0x08808; RW)

Field	Bit(s)	Init Val	Description
FULLTHRESH	9:0	0x250	Tx Security Buffer Almost Full Threshold (relatively to full capacity). The size of the security buffer is 0x274 lines of 16 bytes. In LinkSec offload, the buffer operates in pass-through mode and the recommended threshold is 0x250. It means that the almost full indication is generated very soon while only a fraction of a packet is stored in the buffer. In IPSec mode, the buffer operates in a store and forward mode and the recommended threshold is 0x15. It means that the almost full indication is generated only after the buffer contains at least an entire jumbo packet.
Reserved	31:10	0x0	Reserved.

8.2.3.12.4 Security Tx Buffer Minimum IFG — SECTXMINIFG (0x08810; RW) SEC-Tx

Field	Bit(s)	Init Val	Description
MINSECIFG	3:0	0x1	Minimum IFG between packets. It is the minimum gap between consecutive frames from the DBU-Tx required for the security block. The MINSECIFG is measured in Wake DMA clock units (equal to 6.4 ns in 10 GbE).
Reserved	7:4	0	Reserved.
SECTXDCB	12:8	0x10	This field is used to configure the Security Tx Buffer. • If PFC is enabled, then the *SECTXDCB* field should be set to 0x1F. • If PFC is not enabled, then the default value should be used (0x10).

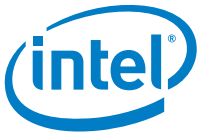
Field	Bit(s)	Init Val	Description
Reserved	31:13	0	Reserved.
Reserved	31:4	0x100	Reserved.

8.2.3.12.5 Security Rx Control — SECRXCTRL (0x08D00; RW)

Field	Bit(s)	Init Val	Description
SECRX_DIS	0	1b RW / RO if fused-off	Rx Security Offload Disable Bit. When set, the AES crypto engine used in Rx by LinkSec and IPsec offloads is disabled. This mode must be used to save the 82599's power consumption when no security offload is enabled. When cleared, the AES crypto engine used in Rx by LinkSec or IPsec offload is enabled. Normal operating mode when a security offload is enabled.
RX_DIS	1	0b	Disable Sec Rx Path. When set, any new packet received from the Rx MAC is filtered out, so that the Rx security block can be internally emptied prior to changing the security mode. SECRXSTAT.SECRX_RDY bit is deasserted until the path is emptied by hardware. When cleared, Rx data path is enabled. Normal operating mode.
Reserved	31:2	0x0	Reserved.

8.2.3.12.6 Security Rx Status — SECRXSTAT (0x08D04; RO)

Field	Bit(s)	Init Val	Description
SECRX_RDY	0	0b	Rx security block ready for mode change. When set, it indicates that the internal data path from the Rx MAC to the Rx security block has been emptied, and thus the security mode can be changed by software. When cleared, it indicates that the internal data path from the Rx MAC to the Rx security block is not empty, and thus software cannot change the security mode. This bit is polled by software once the SECRXCTRL.RX_DIS bit was set.
SECRX_OFF_DIS	1	0b	Security offload is disabled by fuse or strapping pin.
ECC_RXERR	2	0b	Unrecoverable ECC error in an Rx SA table occurred. When set, it indicates that an unrecoverable ECC error occurred when accessing internally one Rx SA table. The ECC interrupt is set as well, until the device is reset by software. When cleared, no ECC error occurred on the Rx SA table from the last time device has reset.
Reserved	31:3	0x0	Reserved.



8.2.3.13 LinkSec Registers

The LinkSec registers are initialized at software reset. When LinkSec is disabled, the LinkSec statistic registers are meaningless and their values are unpredictable.

8.2.3.13.1 LinkSec Tx Capabilities Register — LSECTXCAP (0x08A00; RO)

Field	Bit(s)	Init Val	Description
NCA	2:0	1b	Tx CA-Supported. Number of CA's supported by the device.
NSC	6:3	1b	Tx SC Capable. Number of SC's supported by the device on the transmit data path. The 82599 supports twice the number of SA's as the Tx SC for seamless re-keying, such as 2 SA's.
Reserved	15:7	0x0	Reserved.
LSECTXSUM	23:16	0x0	Tx LSEC Key SUM. A bit wise XOR of the LSECTXKEY 0 bytes and LSECTXKEY 1 bytes. This register can be used by KaY (the programming entity) to validate key programming.
Reserved	31:24	0x0	Reserved.

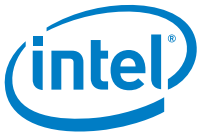
8.2.3.13.2 LinkSec Rx Capabilities Register — LSECRXCAP (0x08F00; RO)

Field	Bit(s)	Init Val	Description
NCA	2:0	1b	Rx CA-supported. Number of CA's supported by the device.
NSC	6:3	1b	Rx SC Capable. Number of SC's supported by the device on the receive data path. The 82599 supports twice the number SA's as the Rx SC for seamless re-keying, such as 2 SA's.
Reserved	15:7	0x0	Reserved.
RXLKM	23:16	0x0	Rx LSEC Key SUM. A byte wise XOR of all bytes of the Rx LinkSec keys 0…1 as defined in registers LSECRXKEY [n, m]. This register can be used by KaY (the programming entity) to validate key programming.
Reserved	31:24	0x0	Reserved.

8.2.3.13.3 LinkSec Tx Control Register — LSECTXCTRL (0x08A04; RW)

Field	Bit(s)	Init Val	Description
LSTXEN	1:0	00b (see Table Note)	Enable Tx LinkSec. Enable Tx LinkSec offloading. 00b = Disable Tx LinkSec (Tx all packets without LinkSec offload). 01b = Add integrity signature. 10b = Encrypt and add integrity signature. 11b = Reserved. When this field equals 00b (LinkSec offload is disabled). The Tx Untagged Packet register is not incremented for transmitted packets when Enable Tx LinkSec equals 00b.
Reserved	2	0b	0b = Reserved.
Reserved	3	0	Reserved.
Reserved	4	00b	Reserved.
AISCI	5	1b	Always Include SCI. This field controls whether SCI is explicitly included in the transmitted SecTag. Since the ES bit in the SecTag is fixed at Zero, the AISCI must always be set to 1b. 0b = False 1b = True
Reserved	6	0b	Reserved.
Reserved	7	0b	Reserved.
PNTRH	31:8	11..1b	PN Exhaustion Threshold. MSB of the threshold over which hardware needs to interrupt KaY to warn Tx SA PN exhaustion and triggers a new SA re-negotiation. Bits 7:0 of the threshold are all 1's.

Note: Bits 1:0 are RW, but they are RO if fused-off and/or if SECTXCTRL.SECTX_DIS is set to 1b, and/or if IPSTXIDX.IPS_TX_EN is set to 1b.



8.2.3.13.4 LinkSec Rx Control register — LSECRXCTRL (0x08F04; RW)

Field	Bit(s)	Init Val	Description
Reserved	1:0	00b	Reserved.
LSRXEN	3:2	00b (see Table Note)	Enable Rx LinkSec. Controls the level of LinkSec packet filtering. 00b = Disable Rx LinkSec (pass all packets to host without LinkSec processing and no LinkSec header strip). 01b = Check (execute LinkSec offload and post frame to host and ME even when it fails LinkSec operation unless failed ICV and C bit was set). 10b = Strict (execute LinkSec offload and post frame to host and ME only if it does not fail LinkSec operation). 11b = Rx LinkSec Drop (drop all packets that include LinkSec header).
Reserved	5:4	00b	Reserved.
PLSH	6	0b	Post LinkSec Header. When set, the device posts the LinkSec header and signature (ICV) to host memory. During normal operation this bit should be cleared.
RP	7	1b	Replay Protect. Enable replay protection.
Reserved	31:8	0x0	Reserved.

Note: Bits 3:2 are RW, but they are RO if fused-off and/or if SECRXCTRL.SECRX_DIS is set to 1b, and/or if IPSRXIDX.IPS_RX_EN is set to 1b.

8.2.3.13.5 LinkSec Tx SCI Low — LSECTXSCL (0x08A08; RW)

Field	Bit(s)	Init Val	Description
SecYL	31:0	0x0	Ethernet MAC Address SecY Low. The 4 LS bytes of the Ethernet MAC address copied to the SCI field in the LinkSec header. *Note:* Field is defined in big endian (LS byte is first on the wire).

8.2.3.13.6 LinkSec Tx SCI High — LSECTXSCH (0x08A0C; RW)

Field	Bit(s)	Init Val	Description
SecYH	15:0	0x0	Ethernet MAC Address SecY High. The 2 MS bytes of the Ethernet MAC address copied to the SCI field in the LinkSec header. *Note:* Field is defined in big endian (LS byte is first on the wire).
PI	31:16	0x0	Port Identifier. Always zero for transmitted packets. This field is RO.

8.2.3.13.7 LinkSec Tx SA — LSECTXSA (0x08A10; RW)

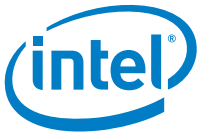
Field	Bit(s)	Init Val	Description
AN0	1:0	0b	AN0 – Association Number 0. This 2-bit field is posted to the AN field in the transmitted LinkSec header when SA 0 is active.
AN1	3:2	0b	AN1 – Association Number 1. This 2-bit field is posted to the AN field in the transmitted LinkSec header when SA 1 is active.
SelSA	4	0b	SA Select (SelSA). This bit selects between SA 0 or SA 1 smoothly, such as on a packet boundary. A value of 0b selects SA 0 and a value of 1b selects SA 1.
ActSA (RO)	5	0b	Active SA (ActSA). This bit indicates the active SA. The ActSA follows the value of the SelSA on a packet boundary. The KaY (the programming entity) can use this indication to retire the old SA.
Reserved	31:6	0x0	Reserved.

8.2.3.13.8 LinkSec Tx SA PN 0 — LSECTXPN0 (0x08A14; RW)

Field	Bit(s)	Init Val	Description
PN	31:0	0x0	PN – Packet Number. This field is posted to the PN field in the transmitted LinkSec header when SA 0 is active. It is initialized by the KaY at SA creation and then increments by 1 for each transmitted packet using this SA. Packets should never be transmitted if the PN repeats itself. In order to protect against such an event hardware generates an LSECPN interrupt to KaY when the PN reaches the exhaustion threshold as defined in the LSECTXCTRL register. There is an additional level of defense against repeating the PN. Hardware never transmits packets after the PN reaches a value of 0xFF...FF. In order to guarantee it, hardware clears the *Enable Tx LinkSec* field in the LSECTXCTRL register to 00b once a packet is transmitted with a PN that equals to 0xFF...F0. *Note:* Field is defined in big endian (LS byte is first on the wire).

8.2.3.13.9 LinkSec Tx SA PN 1 — LSECTXPN1 (0x08A18; RW)

Field	Bit(s)	Init Val	Description
PN	31:0	0x0	PN – Packet Number. This field is posted to the PN field in the transmitted LinkSec header when SA 1 is active. It is initialized by the KaY at SA creation and then increments by 1 for each transmitted packet using this SA. Packets should never be transmitted if the PN repeats itself. In order to protect against such an event hardware generates an LSECPN interrupt to KaY when the PN reaches the exhaustion threshold as defined in the LSECTXCTRL register. There is additional level of defense against repeating the PN. hardware never transmits packets after the PN reaches a value of 0xFF...FF. In order to guarantee it, hardware clears the *Enable Tx LinkSec* field in the LSECTXCTRL register to 00b once a packet is transmitted with a PN that equals to 0xFF...F0. *Note:* Field is defined in big endian (LS byte is first on the wire).



8.2.3.13.10 LinkSec Tx Key 0 — LSECTXKEY0[n] (0x08A1C + 4*n, n=0...3; WO)

Field	Bit(s)	Init Val	Description
LSECK0	31:0	0x0	LSEC Key 0. Transmit LinkSec key of SA 0. n=0 LSEC Key defines bits 31:0 of the Tx LinkSec key. n=1 LSEC Key defines bits 63:32 of the Tx LinkSec key. n=2 LSEC Key defines bits 95:64 of the Tx LinkSec key. n=3 LSEC Key defines bits 127:96 of the Tx LinkSec key. This field is WO for confidentiality protection. For data integrity check, hash value is accessible by the LSECTXSUM field in the LSECCAP register. If for some reason a read request is aimed to this register a value of all zeros are returned.

8.2.3.13.11 LinkSec Tx Key 1 — LSECTXKEY1[n] (0x08A2C + 4*n, n=0...3; WO)

Field	Bit(s)	Init Val	Description
LSECK1	31:0	0x0	LSEC Key 1. Transmit LinkSec key of SA 1. n=0 LSEC Key defines bits 31:0 of the Tx LinkSec key. n=1 LSEC Key defines bits 63:32 of the Tx LinkSec key. n=2 LSEC Key defines bits 95:64 of the Tx LinkSec key. n=3 LSEC Key defines bits 127:96 of the Tx LinkSec key. This field is WO for confidentiality protection. For data integrity check, hash value is accessible by the LSECTXSUM field in the LSECCAP register. If for some reason a read request is aimed to this register a value of all zeros are returned.

8.2.3.13.12 LinkSec Rx SCI Low — LSECRXSCL (0x08F08; RW)

Field	Bit(s)	Init Val	Description
MAL	31:0	0x0	Ethernet MAC Address SecY low. The 4 LS bytes of the Ethernet MAC address in the *SCI* field in the incoming packet that are compared with this field for SCI matching. Comparison result is meaningful only if the *SC* bit in the TCI header is set. *Note:* Field is defined in big endian (LS byte is first on the wire).

8.2.3.13.13 LinkSec Rx SCI High — LSECRXSCH (0x08F0C; RW)

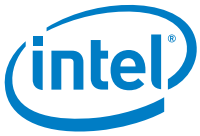
Field	Bit(s)	Init Val	Description
MAH	15:0	0x0	Ethernet MAC Address SecY High. The 2 MS bytes of the Ethernet MAC address in the *SCI* field in the incoming packet that are compared with this field for SCI matching. Comparison result is meaningful only if the *SC* bit in the TCI header is set. *Note:* Field is defined in Big Endian (MS byte is last on the wire).
PI	31:16	0x0	Port Identifier. The port number in the *SCI* field in the incoming packet that is compared with this field for SCI matching. Comparison result is meaningful only if the *SC* bit in the TCI header is set. *Note:* Field is defined in big endian (LS byte is first on the wire).

8.2.3.13.14 LinkSec Rx SA Registers

The registers in this section relate to the LinkSec receive SA context. There are 2 SA(s) in the receive data path defined as SA0 and SA1. The following registers with index n relates to the SA index.

8.2.3.13.15 LinkSec Rx SA — LSECRXSA[n] (0x08F10 + 4*n, n=0...1; RW)

Field	Bit(s)	Init Val	Description
AN	1:0	00b	AN – Association Number. This field is compared with the *AN* field in the *TCI* field in the incoming packet for match.
SAV	2	0b	SA Valid. This bit is set or cleared by the KaY to validate or invalidate the SA.
FRR (RO)	3	0b	Frame Received. This bit is cleared when the *SA Valid* (bit 2) transitions from 0b to 1b, and is set when a frame is received with this SA. When the *Frame Received* bit is set the *Retired* bit of the other SA of the same SC is set. *Note:* A single frame reception with the new SA is sufficient to retire the old SA since it is assumed that the replay window is zero.
Retired (RO)	4	0b	Retired. When this bit is set, the SA is invalid (retired). This bit is cleared when a new SA is configured by the KaY (SA Valid transition to 1b). It is set to 1b when a packet is received with the other SA of the same SC. *Note:* A single frame reception with the new SA is sufficient to retire the old SA since it is assumed that the replay window is zero.
Reserved	31:5	0x0	Reserved.



8.2.3.13.16 LinkSec Rx SA PN — LSECRXPN[n] (0x08F18 + 4*n, n=0...1; RW)

Field	Bit(s)	Init Val	Description
PN	31:0	0x0	PN – Packet Number. Register 'n' holds the *PN* field of the next incoming packet that uses SA 'n', 'n' = 0, 1. The *PN* field in the incoming packet must be greater or equal to the PN register. The PN register is set by KaY at SA creation. It is updated by hardware for each received packet using this SA to be received PN + 1. *Note:* Field is defined in Big Endian (LS byte is first on the wire).

8.2.3.13.17 LinkSec Rx Key — LSECRXKEY[n,m] (0x08F20 + 0x10*n + 4*m, n=0...1, m=0...3; WO)

Field	Bit(s)	Init Val	Description
LSECK	31:0	0x0	LSEC Key. Receive LinkSec key of SA n, while n=0...1. m=0 LSEC Key defines bits 31:0 of the Rx LinkSec key. m=1 LSEC Key defines bits 63:32 of the Rx LinkSec key. m=2 LSEC Key defines bits 95:64 of the Rx LinkSec key. m=3 LSEC Key defines bits 127:96 of the Rx LinkSec key. This field is WO for confidentiality protection. For data integrity check, KaY hash value is accessible by the LSECRXSUM field in the LSECCAP registers. If for some reason a read request is aimed to this register a value of all zeros are returned.

8.2.3.14 LinkSec Tx Port Statistics

These counters are defined by the specification as 64 bits while implementing only 32 bits in hardware. The KaY must implement the 64-bit counter in software by polling regularly the hardware statistic counters. Hardware counters wrap around from 0xFF..F to 0x0 and cleared on read.

Note that 82599 includes a 10 KB FIFO between the security block output and the MAC block. In the case of a pause event, packets stored in this FIFO are dropped for instant response to the pause request. When it is time to resume transmission, the packets are re-transmitted from the transmit packet buffer to the security block. These re-transmitted packets are counted twice in all the relevant security transmit counters.

8.2.3.14.1 Tx Untagged Packet Counter — LSECTXUT (0x08A3C; RW)

Field	Bit(s)	Init Val	Description
UPC	31:0	0x0	Untagged Packet CNT. Increments for each transmitted packet that is transmitted with the ILSec bit cleared in the packet descriptor while *Enable Tx LinkSec* field in the LSECTXCTRL register is either 01b or 10b. The KaY must implement a 64-bit counter. It can do that by reading the LSECTXUT register regularly.

8.2.3.14.2 Encrypted Tx Packets — LSECTXPKTE (0x08A40; RW)

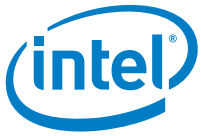
Field	Bit(s)	Init Val	Description
EPC	31:0	0x0	Encrypted Packet CNT. Increments for each transmitted packet through the controlled port with the *E* bit set (such as confidentiality was prescribed for this packet by software/firmware).

8.2.3.14.3 Protected Tx Packets — LSECTXPKTP (0x08A44; RW)

Field	Bit(s)	Init Val	Description
PPC	31:0	0x0	Protected Packet CNT. Increments for each transmitted packet through the controlled port with the *E* bit cleared (such as integrity only was prescribed for this packet by software/firmware).

8.2.3.14.4 Encrypted Tx Octets — LSECTXOCTE (0x08A48; RW)

Field	Bit(s)	Init Val	Description
EOC	31:0	0x0	Encrypted Octet CNT. Increments for each byte of user data through the controlled port with the *E* bit set (such as confidentiality prescribed for this packet by software/firmware).



8.2.3.14.5 Protected Tx Octets — LSECTXOCTP (0x08A4C; RW)

Field	Bit(s)	Init Val	Description
POC	31:0	0x0	Protected Octet CNT. Increments for each byte of user data through the controlled port with the *E* bit cleared such as integrity only was prescribed for this packet by software/firmware).

8.2.3.15 LinkSec Rx Port Statistic Counters

These counters are defined by the specification as 64 bits while implementing only 32 bits in hardware. The KaY must implement the 64-bit counter in software by polling regularly the hardware statistic counters.

8.2.3.15.1 LinkSec Untagged Rx Packet — LSECRXUT (0x08F40; RC)

Field	Bit(s)	Init Val	Description
UPC	31:0	0x0	Untagged Packet CNT. Increments for each packet received having no tag. Also increments for any KaY packets regardless of the LinkSec tag. Increments only when the *Enable Rx LinkSec* field in the LSECRXCTRL register is either 01b or 10b. *Note:* Flow control frames are also counted by this counter.

8.2.3.15.2 LinkSec Rx Octets Decrypted — LSECRXOCTE (0x08F44; RC)

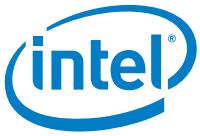
Field	Bit(s)	Init Val	Description
DROC	31:0	0x0	Decrypted Rx Octet CNT. The number of octets of user data recovered from received frames that were both integrity protected and encrypted. This includes the octets from SecTag to ICV not inclusive. These counts are incremented even if the user data recovered failed the integrity check or could not be recovered.

8.2.3.15.3 LinkSec Rx Octets Validated — LSECRXOCTP (0x08F48; RC)

Field	Bit(s)	Init Val	Description
VOC	31:0	0b	Validated Rx Octet CNT. The number of octets of user data recovered from received frames that were integrity protected but not encrypted.This includes the octets from SecTag to ICV not inclusive. These counts are incremented even if the user data recovered failed the integrity check or could not be recovered.

8.2.3.15.4 LinkSec Rx Packet with Bad Tag — LSECRXBAD (0x08F4C; RC)

Field	Bit(s)	Init Val	Description
BRPC	31:0	0b	Bad Rx Packet CNT. Number of packets received having a invalid tag.



8.2.3.15.5 LinkSec Rx Packet No SCI — LSECRXNOSCI (0x08F50; RC)

Field	Bit(s)	Init Val	Description
USRPC	31:0	0b	No SCI Rx Packet CNT. Number of packets received with unrecognizable SCI and dropped due to that condition.

8.2.3.15.6 LinkSec Rx Packet Unknown SCI — LSECRXUNSCI (0x08F54; RC)

Field	Bit(s)	Init Val	Description
USRPC	31:0	0b	Unknown SCI Rx Packet CNT. Number of packets received with an unrecognized SCI but still forwarded to the host.

8.2.3.16 LinkSec Rx SC Statistic Counters

These counters are defined by the specification as 64 bits while implementing only 32 bits in hardware. The KaY must implement the 64-bit counter in software by polling regularly the hardware statistic counters. Hardware counters wrap around from 0xFF..F to 0x0 and cleared on read.

8.2.3.16.1 LinkSec Rx Unchecked Packets — LSECRXUC (0x08F58; RC)

Software/firmware needs to maintain the full-sized register.

Field	Bit(s)	Init Val	Description
URPC	31:0	0x0	Unchecked Rx Packet CNT. Number of packets received with LinkSec encapsulation (SecTag) while Validate Frames is disabled (LSECRXCTRL bits 3:2 equal 00b).

8.2.3.16.2 LinkSec Rx Delayed Packets — LSECRXDELAY (0x08F5C; RC)

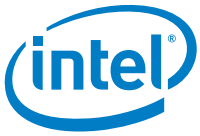
Software/firmware needs to maintain the full-sized register.

Field	Bit(s)	Init Val	Description
DRPC	31:0	0x0	Delayed Rx Packet CNT. Number of packets received and accepted for validation having failed replay protection and Replay Protect is false (LSECRXCTRL bit 7 is 0b).

8.2.3.16.3 LinkSec Rx Late Packets — LSECRXLATE (0x08F60; RC)

Software/firmware needs to maintain the full-sized register.

Field	Bit(s)	Init Val	Description
LRPC	31:0	0x0	Late Rx Packet CNT. Number of packets received and accepted for validation having failed replay-protection and Replay Protect is true (LSECRXCTRL bit 7 is 1b).



8.2.3.17 LinkSec Rx SA Statistic Counters

These counters are defined by the specification as 64 bits while implementing only 32 bits in hardware. The KaY must implement the 64-bit counter in software by polling regularly the hardware statistic counters. Hardware counters wrap around from 0xFF..F to 0x0 and cleared on read.

8.2.3.17.1 LinkSec Rx Packet OK — LSECRXOK[n] (0x08F64 + 4*n, n=0...1; RC)

Field	Bit(s)	Init Val	Description
ORPC	31:0	0x0	OK Rx Packet CNT. Number of packets received that were valid (authenticated) and passed replay protection.

8.2.3.17.2 LinkSec Rx Invalid — LSECRXINV[n] (0x08F6C + 4*n, n=0...1; RC)

Field	Bit(s)	Init Val	Description
ICRPC	31:0	0x0	Invalid Rx Packet CNT. Number of packets received that were not valid (authentication failed) and were forwarded to host.

8.2.3.17.3 LinkSec Rx Not valid count — LSECRXNV[n] (0x08F74 + 4*n, n=0...1; RC)

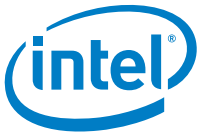
Field	Bit(s)	Init Val	Description
ICRPC	31:0	0x0	Not valid Rx Packet CNT. Number of packets received that were not valid (authentication failed) and were dropped.

8.2.3.17.4 LinkSec Rx Unused SA Count — LSECRXUNSA (0x08F7C; RC)

Field	Bit(s)	Init Val	Description
ISSRPC	31:0	0x0	Invalid SA Rx Packet CNT. Number of packets received that were associated with an SA that is not in use (no match on auto-negotiation or not valid or retired) and were forwarded to host.

8.2.3.17.5 LinkSec Rx Not Using SA Count — LSECRXNUSA (0x08F80; RC)

Field	Bit(s)	Init Val	Description
ISSRPC	31:0	0x0	Invalid SA Rx Packet CNT. Number of packets received that were associated with an SA that is not in use (No match on auto-negotiation or not valid or retired) and were dropped.



8.2.3.18 IPsec Registers

IPsec registers are owned by the PF in an IOV mode.

Unlike LinkSec, there is no added value here to encrypt the SA contents when being read by software because the SA contents is available in clear text from system memory like for any IPsec flow handled in software.

8.2.3.18.1 IPsec Tx Index — IPSTXIDX (0x08900; RW)

Field	Bit(s)	Init Val	Description
IPS_TX_EN	0	0b (see table note)	IPsec Tx offload enable bit. 0b = IPsec offload ability is disabled for the Tx path, regardless of the contents of the Tx SA table. 1b = IPsec offload ability is enabled for the Tx path.
Reserved	2:1	00b	Reserved.
SA_IDX	12:3	0x0	SA index for indirect access into the Tx SA table.
Reserved	29:13	0x0	Reserved.
READ	30	0b SC by HW	Read Command. When set, the contents of the Tx SA table entry pointed by the SA_IDX field is loaded into the IPSTXKEY 0...3 and IPSTXSALT registers. Immediately self cleared by hardware once the entry contents has been loaded into the registers.
WRITE	31	0b SC by HW	Write Command. When set, the contents of the IPSTXKEY 0...3 and IPSTXSALT registers are loaded into the Tx SA table entry pointed to by the SA_IDX field. Immediately self cleared by hardware once the entry contents have been loaded into the memory.

Notes: Write and Read bits must not be set at the same time by software.

IPS_TX_EN is RW, but it is RO if fused-off and/or if SECTXCTRL.SECTX_DIS is set to 1b.

8.2.3.18.2 IPsec Tx Key Registers — IPSTXKEY[n] (0x08908 + 4*n, n=0...3; RW)

Field	Bit(s)	Init Val	Description
AES-128 KEY	31:0	0x0	4 bytes of a 16-byte key that has been read/written from/into the Tx SA entry pointed to by SA_IDX. n=0 Contains the LSB of the key. n=3 Contains the MSB of the key.

8.2.3.18.3 IPsec Tx Salt Register — IPSTXSALT (0x08904; RW)

Field	Bit(s)	Init Val	Description
AES-128 SALT	31:0	0x0	4-byte salt that has been read/written from/into the Tx SA entry pointed to by SA_IDX.

8.2.3.18.4 IPsec Rx Index — IPSRXIDX (0x08E00; RW)

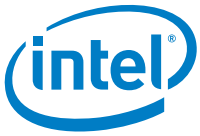
Field	Bit(s)	Init Val	Description
IPS_RX_EN	0	0b (see table note)	IPsec Rx offload enable bit. 0b = IPsec offload ability is disabled for the Rx path, regardless of the contents of Rx SA tables. 1b = IPsec offload ability is enabled for the Rx path.
TABLE	2:1	00b	Table select bits. 00b = No Rx SA table is accessed. 01b = IP address table is accessed. 10b = SPI table is accessed. 11b = Key table is accessed.
TB_IDX	12:3	0x0	Table index bits for indirect access into the Rx SA table selected by the *Table* bits. When accessing the IP address table, only the seven least significant bits of this field are meaningful.
Reserved	29:13	0x0	Reserved.
READ	30	0b SC by HW	Read Command. When set, the contents of the Rx SA table entry as pointed to by the [TABLE, TB_IDX] fields is loaded into the corresponding registers. Immediately self cleared by hardware once the entry contents have been loaded into the corresponding registers. For instance, if this bit is set together with Table=10b and TB_IDX=0x9, then the SPI value stored in entry nine is loaded into the IPSRXSPI 0...3 registers. Rx SA registers related to another Rx SA table (like IPSRXKEY 0...3 registers) must not be read when Table=01b.
WRITE	31	0b SC by HW	Write command. When set, the contents of the registers affected by the Rx SA table pointed to by the *Table* field is loaded into the table entry pointed to by the TB_IDX field. Immediately self cleared by hardware once the entry contents have been loaded into the memory. For instance, if this bit is set together with *Table*=10b and TB_IDX=0x9, then the value written in IPSRXSPI 0...3 registers is loaded into the SPI table entry nine.

Notes:

Write and *Read* bits must not be set at the same time by software.

IPS_RX_EN is RW, but it is RO if fused-off and/or if SECRXCTRL.SECRX_DIS is set to 1b.

Software is not allowed to write/read access registers that belong to different Rx SA tables without writing the IPSRXIDX register in between for setting the *WriteRead* bit. Refer to Rx SA tables access rules described in Section 7.12.9.2.



Software should not make changes in the Rx SA tables while changing the IPSEC_EN bit.

8.2.3.18.5 IPsec Rx IP address Register — IPSRXIPADDR (0x08E04 + 4*n, n=0...3; RW)

These registers are related to the IP Address table.

Field	Bit(s)	Init Val	Description
IPADDR	31:0	0x0	4 bytes of a16-byte destination IP address for the associated Rx SA(s). n=0 Contains the MSB for an IPv6 IP address. n=3 Contains an IPv4 IP address or the LSB for an IPv6 IP address. For an IPv4 address, IPSRXIPADDR 0...2 must be written with zeros. *Note:* Field is defined in big endian (LS byte is first on the wire).

8.2.3.18.6 IPsec Rx SPI Register — IPSRXSPI (0x08E14; RW)

This register is related to the Rx SPI table.

Field	Bit(s)	Init Val	Description
SPI	31:0	0x0	SPI field for the SPI entry. *Note:* Field is defined in big endian (LS byte is first on the wire).

8.2.3.18.7 IPsec Rx SPI Register — IPSRXIPIDX (0x08E18; RW)

This register is related to the Rx SPI table.

Field	Bit(s)	Init Val	Description
IP_IDX	6:0	0x0	IP Index. Index in the IP address table where the destination IP address associated to that SPI entry is found.
Reserved	31:7	0x0	Reserved.

8.2.3.18.8 IPsec Rx Key Register — IPSRXKEY[n] (0x08E1C + 4*n, n=0...3; RW)

These registers are related to the Rx KEY table.

Field	Bit(s)	Init Val	Description
AES-128 KEY	31:0	0x0	4 bytes of a16-byte key of the KEY entry. n=0 Contains the LSB of the key. n=3 Contains the MSB of the key.

8.2.3.18.9 IPsec Rx Salt Register — IPSRXSALT (0x08E2C; RW)

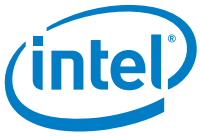
This register is related to the Rx KEY table.

Field	Bit(s)	Init Val	Description
AES-128 SALT	31:0	0x0	4-byte salt associated to the KEY entry.

8.2.3.18.10 IPsec Rx Mode Register — IPSRXMOD (0x08E30; RW)

This register is related to the Rx KEY table.

Field	Bit(s)	Init Val	Description
VALID	0	0b	Valid Bit. 0b = The KEY entry is not valid. 1b = The KEY entry is valid.
Reserved	1	0b	Reserved.
PROTO	2	0b	IPsec Protocol Select. 0b = The KEY entry offloads AH packets. 1b = The KEY entry offloads ESP packets.
DECRYPT	3	0b	Decryption Bit. When set, hardware performs decryption offload for this KEY entry. Meaningful only if the *Proto* bit is set (like ESP mode).
IPv6	4	0b	IPv6 Type. 0b = Only matched IPv4 packets are offloaded for that KEY entry. 1b = Only matched IPv6 packets are offloaded for that KEY entry.
Reserved	31:5	0x0	Reserved.



8.2.3.19 Timers Registers

8.2.3.19.1 TCP Timer — TCPTIMER (0x0004C; RW)

Field	Bit(s)	Init Val	Description
Duration	7:0	0x0	Duration. Duration of the TCP interrupt interval, in ms.
KickStart	8	0b	Counter kick-start. Writing a 1b to this bit kick-starts the counter down-count from the initial value defined in the *Duration* field. Writing 0b has no effect (WS).
TCPCountEn	9	0b	TCP Count Enable. 0b = TCP timer counting is disabled. 1b = TCP timer counting is enabled. Upon enabling, TCP counter must count from its internal state. If the internal state is equal to zero, down-count does not restart until *KickStart* is activated. If the internal state is not 0b, down-count continues from the internal state. This enables a pause of the counting for debug purposes.
TCPCountFinish	10	0b	TCP Count Finish. This bit enables software to trigger a TCP timer interrupt, regardless of the internal state. 0b = No effect (WS). 1b = Triggers an interrupt and resets the internal counter to its initial value. Down-count does not restart until either *KickStart* is activated or *Loop* is set.
Loop	11	0b	TCP Loop. 0b = TCP counter must stop at a zero value, and must not re-start until *KickStart* is activated. 1b = TCP counter must reload duration each time it reaches zero, and must go on down-counting from this point without kick-starting.
Reserved	31:12	0x0	Reserved.

8.2.3.20 FCoE Registers

8.2.3.20.1 Tx FC SOF Flags Register - TSOFF (0x04A98; RW)

Field	Bit(s)	Init Val	Description
SOF0	7:0	0x2D	Start Of Frame 0. Class 2 Start of Frame used in the first packet of FC sequence. Default setting of SOFi2.
SOF1	15:8	0x2E	Start Of Frame 1. Class 3 Start of Frame used in the first packet of FC sequence. Default setting of SOFi3.
SOF2	23:16	0x35	Start Of Frame 2. Class 2 Start of Frame used in all packets but the first one of FC sequence. Default setting of SOFn2.
SOF3	31:24	0x36	Start Of Frame 3. Class 3 Start of Frame used in all packets but the first one of FC sequence. Default setting of SOFn3.

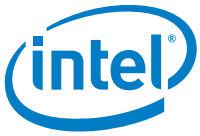
8.2.3.20.2 Tx FC EOF Flags Register - TEOFF (0x04A94; RW)

Field	Bit(s)	Init Val	Description
EOF0	7:0	0x41	End Of Frame 0. By default it is set to EOFn code used in all packets but the last one on a sequence.
EOF1	15:8	0x42	End Of Frame 1. By default it is set to EOFt code used to close a sequence.
EOF2	23:16	0x49	End Of Frame 2. By default it is set to EOFni code.
EOF3	31:24	0x50	End Of Frame 3. By default it is set to EOFa code.

FCoE Rx registers

8.2.3.20.3 Rx FC SOF Flags Register - RSOFF (0x051F8; RW)

Field	Bit(s)	Init Val	Description
SOF0	7:0	0x2D	Start Of Frame 0. Class 2 Start of Frame used in the first packet of FC sequence. Default setting of SOFi2.
SOF1	15:8	0x2E	Start Of Frame 1. Class 3 Start of Frame used in the first packet of FC sequence. Default setting of SOFi3.



Field	Bit(s)	Init Val	Description
SOF2	23:16	0x35	Start Of Frame 2. Class 2 Start of Frame used in all packets but the first one of FC sequence. Default setting of SOFn2.
SOF3	31:24	0x36	Start Of Frame 3. Class 3 Start of Frame used in all packets but the first one of FC sequence. Default setting of SOFn3.

8.2.3.20.4 Rx FC EOF Flags Register - REOFF (0x05158; RW)

Field	Bit(s)	Init Val	Description
EOF0	7:0	0x41	End Of Frame 0. By default it is set to EOFn code used in all packets but the last one on a sequence.
EOF1	15:8	0x42	End Of Frame 1. By default it is set to EOFt code used to close a sequence.
EOF2	23:16	0x49	End Of Frame 2. By default it is set to EOFni code.
EOF3	31:24	0x50	End Of Frame 3. By default it is set to EOFa code.

8.2.3.20.5 FC Receive Control — FCRXCTRL (0x05100; RW)

Field	Bit(s)	Init Val	Description
FCOELLI	0	0b	Low Latency Interrupt by FCoE Frame. When set to 1b any FCP-RSP frame or last data packet in a sequence with the *Sequence Initiative* bit set, generates a Low Latency Interrupt (LLI).
SavBad	1	0	Enable Save Bad Frame. Whenset to 1b, frames with good Ethernet CRC and bad FC CRC are posted to the legacy receive queues. If the *SavBad* bit is set to 0b, such frames are discarded. In both cases frames with bad FC CRC increment the FCCRC statistic counter.
FRSTRDH	2	0	Enable First Read Packet Header. This field impacts received packets that are off-loaded by Large FC receive while their FC payload is posted directly to the user buffers. When set, headers of the first frame that matches an FC DDP context are posted to the legacy receive queues.
LASTSEQH	3	0	Enable Headers of Last Frame in a Sequence. This field impacts received packets that are off-loaded by Large FC receive while their FC payload is posted directly to the user buffers. When set, headers of Last Frame in a Sequence are posted to the legacy receive queues.
ALLH	4	0	Enable All Headers. This field impacts received packets that are off-loaded by Large FC receive while their FC payload is posted directly to the user buffers. When set, headers of any received packet are posted to the legacy receive queues.

Field	Bit(s)	Init Val	Description
FRSTSEQH	5	0	Enable First Sequence Packet Header. This field impacts received packets that are off-loaded by Large FC receive while their FC payload is posted directly to the user buffers. When set, headers of the first frame in any sequence are posted to the legacy receive queues.
ICRC	6	0	Ignore Bad FC CRC. When set, the 82599 ignores bad FC CRC. In this case packets might be processed by the Large FC receive even if they carry bad FC CRC.
FCCRCBO	7	1	FC CRC Byte Ordering. When set to 1b, the FC CRC bytes are treated in Rx as big Endian. Whenset to 0b, the FC CRC are treated as little endian (as Ethernet CRC). This bit should be set to the same value as DMATXCTL.FCCRCBO.
FCOEVER	11:8	0	Supported FCoE Version Number. FCoE frames that carry higher version number than *FCOEVER* are not processed by the FCoE Rx offload logic.
Reserved	31:12	0x0	Reserved.

8.2.3.20.6 FCoE Redirection Control — FCRECTL (0x0ED00; RW)

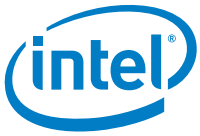
Field	Bit(s)	Init Val	Description
ENA	0	0b	FC Redirection Enable. When cleared, the redirection table is not active. When set to 1b the FC redirection is enabled. *Software Note:* When FC redirection is enabled, the Pool Enable and the Queue Enable bits in the ETQF and ETQS registers must be cleared for FCoE data packets.
Reserved	31:1	0x0	Reserved.

8.2.3.20.7 FCoE Redirection Table — FCRETA[n] (0x0ED10 + 4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
Table Entry	6:0	0x0	Table Entry. Defines the redirection output queue number. Register 'n' is the table entry index 'n' which is the matched value to the 3 LS bits of the FC exchange ID.
Reserved	31:7	0x0	Reserved.

8.2.3.20.8 FC User Descriptor PTR Low — FCPTRL (0x02410; RW)

Field	Bit(s)	Init Val	Description
PTR_LOW	31:0	N/A	User Descriptor PTR Low. Four least significant bytes of the physical pointer to the user descriptor list. The pointer must be 16-byte aligned so the four LS bits are read only as zeros.



8.2.3.20.9 FC User Descriptor PTR High — FCPTRH (0x02414; RW)

Field	Bit(s)	Init Val	Description
PTR_HI	31:0	N/A	User Descriptor PTR High. Four most significant bytes of the physical pointer to the user descriptor list.

8.2.3.20.10 FC Buffer Control — FCBUFF (0x02418; RW)

Field	Bit(s)	Init Val	Description
Valid	0	0b	DMA Context Valid. When set to 1b indicates that the context is valid. If software clears the *Context Valid* bit, software should poll it until it is actually cleared by hardware before unlocking the user buffers.
First	1	0b	DMA First. This bit is a status indication. Software should clear it during FC context programming. The DMA unit sets this bit when it receives a frame that matches the context and marked by the filter unit as first.
Last	2	0b	DMA Last. This bit is a status indication. Software should clear it during FC context programming.Hardware sets this bit when it exhausts the last user buffer.
BUFFSIZE	4:3	00b	Buffer Size. This field defines the user buffer size used in this context as follows: 00b = 4 KB. 10b = 16 KB. 01b = 8 KB. 11b = 64 KB.
Reserved	6:5	00b	Reserved.
WRCONTX	7	0b	Write DDP Context. This bit should be set to 1b for write exchange context aimed for target (responder) usage. This bit should be set to 0b for read exchange context aimed for initiator (originator) usage.
BUFFCNT	15:8	0x0	Buffer Count. Defines the number of the user buffers while 0x0 equals 256. It is programmed by software and updated by hardware during reception.
Offset	31:16	0x0	User Buffer Offset. Byte offset within the user buffer to which the FC data of large FC receive should be posted.

8.2.3.20.11 FC Receive DMA RW — FCDMARW (0x02420; RW)

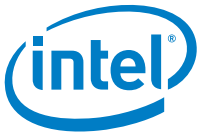
Field	Bit(s)	Init Val	Description
FCoESEL	8:0	0x0	FCoE context Select. This field defines the FCoE Rx context index (equals the OX_ID for that context).
Reserved	12:9	0x0	Reserved.
Reserved	13	0	Reserved.
WE	14	0b	Write Enable. When this bit is set, the content of FCPTRL, FCPTRH and FCBUFF registers are programmed to the FCoE DMA context of index FCoESEL. This bit should never be set together with the *RE* bit in this register.
RE	15	0b	Read Enable. When this bit is set, the internal FCoE DMA context of index FCoESEL is fetched to the FCPTRL, FCPTRH and FCBUFF registers. This bit should never be set together with the *WE* bit in this register.
LASTSIZE	31:16	0x0	Last User Buffer Size. Defines the size in bytes of the last user buffer.

8.2.3.20.12 FC FLT Context — FCFLT (0x05108; RW)

Field	Bit(s)	Init Val	Description
Valid	0	N/A	Filter Context Valid. When set to 1b indicates that the context is valid.
First	1	N/A	Filter First. This bit is a status indication. Software should clear it during FC context programming. The filter unit sets this bit when it receives a first frame that matches the context.
Reserved	7:2	N/A	Reserved.
SEQ_ID	15:8	N/A	Sequence ID. The sequence ID of the last received frame. Initialized to 0x0 by the driver at context programming.
SEQ_CNT	31:16	N/A	Sequence Count. The sequence count of the expected received frame. Initialized to 0x0 by the driver at context programming.

8.2.3.20.13 FC Offset Parameter — FCPARAM (0x051D8; RW)

Field	Bit(s)	Init Val	Description
PARAM	31:0	0x0	FC Parameter. This field contains the expected FC parameter in the next received frame. Initialized to 0x0 by the driver at context programming. *Note:* Field is defined in big endian (LS byte is first on the wire).



8.2.3.20.14 FC Filter RW Control — FCFLTRW (0x05110; WO)

Field	Bit(s)	Init Val	Description
FCoESEL	8:0	0x0	FCoE context Select. This field defines the FCoE Rx context index (equals the OX_ID for that context).
Reserve	12:9	0x0	Reserved.
Re-Validate	13	0b	Fast re-validation of the filter context. Setting this bit together with the *WE* bit in this register validates the selected filter context. Hardware sets the *Valid* bit and clears the *First* bit (described in the FCFLT register) while keeping all other filter parameters intact.
WE	14	0b	Write Enable. When this bit is set, the content of the FCFLT register is programmed to the filter of index FCoESEL. This bit should never be set together with the *RE* bit in this register.
RE	15	0b	Read Enable. When this bit is set, the internal filter context of index FCoESEL is fetched to the FCFLT register. This bit should never be set together with the *WE* bit in this register.
Reserve	31:16	0x0	Reserved.

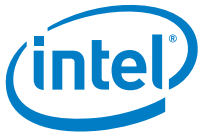
8.2.3.21 Flow Director Registers

Global settings registers.

8.2.3.21.1 Flow Director Filters Control Register — FDIRCTRL (0x0EE00; RW)

Note: This register should be configured ONLY as part of the flow director initialization flow or clearing the flow director table. Programming of this register with non-zero value PBALLOC initializes the flow director table.

Field	Bit(s)	Init Val	Description
PBALLOC	1:0	00b	Memory allocation for the flow director filters. 00b = No memory allocation — Flow Director Filters are disabled 01b = 64 KB (8 K minus 2 signature filters or 2 K minus 2 perfect match filters). 10b = 128 KB (16 K minus 2 signature filters or 4 K minus 2 perfect match filters). 11b = 256 KB (32 K minus 2 signature filters or 8 K minus 2 perfect match filters).
Reserved	2	0b	Reserved.
INIT-Done	3	0b	Flow director initialization completion indication (read only status). Indicates that hardware initialized the flow director table according to the PBALLOC setting. Software must not access any other flow director filters registers before the *INIT-Done* bit is set. When flow director filters are enabled (PBALLOC > 0), software must wait for the *INIT-Done* indication before Rx is enabled.
Perfect-Match	4	0b	Flow director filters mode of operation. When set to 1b, hardware supports perfect match filters according to PBALLOC. When cleared to 0b, hardware supports signature filters according to PBALLOC.
Report-Status	5	0b	Report flow director filter's status in the *RSS* field of the Rx descriptor for packets that matches a flow director filter. Enabling the flow director filter's status, the RXCSUM.PCSD bit should be set as well (disabling the fragment checksum). *Note:* The *Flow Director Filter Status* and *Error* bits in the *Extended Status* and *Error* fields in the Rx descriptor are always enabled.
Reserved	6	0b	Reserved.
Report-Status always	7	0b	Report flow director status in the *RSS* field of the Rx descriptor on any packet that can be candidates for the flow director filters. This bit can be set to 1b only when both the RXCSUM.PCSD bit and the *Report-Status* bit in this register are set.
Drop-Queue	14:8	0x0	Absolute Rx queue index used for the dropped packets. Software can set this queue to an empty one by setting RDLEN[n] to 0x0.
Reserved	15	0b	Reserved.
Flex-Offset	20:16	0x0	Offset within the first 64 bytes of the packet of a flexible 2-byte tuple. The offset is defined in word units counted from the first byte of the destination Ethernet MAC address.
Reserved	23:21	0x0	Reserved.



Field	Bit(s)	Init Val	Description
Max-Length	27:24	0x0	Maximum linked list length. This field defines the maximum recommended linked list associated to any hash value (defined in units of two filters). Packets that match filters that exceed the *Max-Length* are reported with an active *Length* bit in the *Extended Error* field. In addition, drop filters that exceed the *Max-Length* are posted to the Rx queue defined in the filter context rather than the *Drop-Queue* defined in this register. *Note:* Software should set this field to a value that indicates exceptional long buckets. Supporting 32 K filters with good hash scheme key, it is expected that a value of 0xA can be a good choice.
Full-Thresh	31:28	0x0	Full threshold is a recommended minimum number of flows that should remain unused (defined in units of 16 filters). When software exceeds this threshold (too low number of unused flows), hardware generates the flow director full interrupt. Software should avoid additional programming following this interrupt. *Note:* When the flow director filters are used completely, hardware discards silently further filters programming.

8.2.3.21.2 Flow Director Filters Lookup Table HASH Key — FDIRHKEY (0x0EE68; RW)

Field	Bit(s)	Init Val	Description
Key	31:0	0x80000001	Programmable hash lookup table key.

8.2.3.21.3 Flow Director Filters Signature Hash Key — FDIRSKEY (0x0EE6C; RW)

Field	Bit(s)	Init Val	Description
Key	31:0	0x80800101	Programmable Signature Key.

8.2.3.21.4 Flow Director Filters DIPv4 Mask — FDIRDIP4M (0x0EE3C; RW)

Field	Bit(s)	Init Val	Description
IPM	31:0	0x0	Mask Destination IPv4 Address. Each cleared bit means that the associated bit of the destination IPv4 address is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the destination IPv4 address is ignored (masked out). The LS bit of this register matches the first byte on the wire.

8.2.3.21.5 Flow Director Filters Source IPv4 Mask — FDIRSIP4M (0x0EE40; RW)

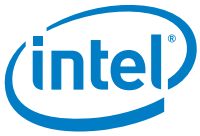
Field	Bit(s)	Init Val	Description
IPM	31:0	0x0	Mask Source IPv4 Address. Each cleared bit means that the associated bit of the source IPv4 address is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the source IPv4 address is ignored (masked out). The LS bit of this register matches the first byte on the wire.

8.2.3.21.6 Flow Director Filters TCP Mask — FDIRTCPM (0x0EE44; RW)

Field	Bit(s)	Init Val	Description
SPortM	15:0	0x0	Mask TCP Source Port. Each cleared bit means that the associated bit of the TCP source port is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the TCP source port is ignored (masked out). *Note:* This register is swizzle as follows: bit 0 in the mask affects bit 15 of the source port as defined in FDIRPORT.Source. bit 1 in the mask affects bit 14 in FDIRPORT.Source and so on while bit 15 in the mask affects bit 0 in FDIRPORT.Source.
DPortM	31:16	0x0	Mask TCP Destination Port. Each cleared bit means that the associated bit of the TCP destination port is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the TCP destination port is ignored (masked out). *Note:* This register is swizzle the same as the FDIRTCPM.SPortM.

8.2.3.21.7 Flow Director Filters UDP Mask — FDIRUDPM (0x0EE48; RW)

Field	Bit(s)	Init Val	Description
SPortM	15:0	0x0	Mask UDP Source Port. Each cleared bit means that the associated bit of the UDP source port is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the UDP source port is ignored (masked out). *Note:* This register is swizzle the same as the FDIRTCPM.SPortM.
DPortM	31:16	0x0	Mask UDP Destination Port. Each cleared bit means that the associated bit of the UDP destination port is meaningful for the filtering functionality. Each bit set to 1b means that the associated bit of the UDP destination port is ignored (masked out). *Note:* This register is swizzle the same as the FDIRTCPM.SPortM.



8.2.3.21.8 Flow Director Filters IPv6 Mask — FDIRIP6M (0x0EE74; RW)

Field	Bit(s)	Init Val	Description
SIPM	15:0	0x0	Mask Source IPv6 address. Each cleared bit means that the associated byte of the source IPv6 address is meaningful for the filtering functionality. Each bit set to 1b means that the associated byte of the source IPv6 address is ignored (masked out). The LS bit of this register matches the first byte on the wire.
DIPM	31:16	0x0	Mask Destination IPv6 address. Each cleared bit means that the associated byte of the destination IPv6 address is meaningful for the filtering functionality. Each bit set to 1b means that the associated byte of the destination IPv6 address is ignored (masked out). The entire field is meaningful only for the hash function and the signature-based filters. The *DIPv6* bit in the FDIRM register is meaningful for perfect match filters. The LS bit of this register matches the first byte on the wire.

8.2.3.21.9 Flow Director Filters Other Mask — FDIRM (0x0EE70; RW)

Field	Bit(s)	Init Val	Description
VLANID	0	0b	Mask VLAN ID tag. When cleared the 12 bits of the VLAN ID tag are meaningful for the filtering functionality.
VLANP	1	0b	Mask VLAN Priority tag. When cleared the 3 bits of the VLAN Priority are meaningful for the filtering functionality.
POOL	2	0b	Mask Pool. When cleared the target pool number is meaningful for the filtering functionality.
L4P	3	0b	Mask L4 Protocol. When cleared the UDP/TCP/SCTP protocol type is meaningful for the filtering functionality. *Note:* For the flow director filtering aspects, SCTP is treated as if it is TCP.
FLEX	4	0b	Mask Flexible Tuple. When cleared the 2 bytes of the flexible tuple are meaningful for the filtering functionality.
DIPv6	5	0b	Mask Destination IPv6. When cleared the compare against the IP6AT filter is meaningful for IPv6 packets.
Reserved	31:6	0x0	Reserved.

Global Status / Statistics Registers

8.2.3.21.10 Flow Director Filters Free — FDIRFREE (0x0EE38; RW)

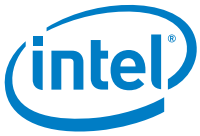
Field	Bit(s)	Init Val	Description
FREE	15:0	0x8000	Number of free (non programmed) filters in the flow director Filters logic.
Reserved	30:16	0x0	Reserved.
Reserved	31	0b	Reserved.

8.2.3.21.11 Flow Director Filters Length — FDIRLEN (0x0EE4C; RC)

Field	Bit(s)	Init Val	Description
MAXLEN	5:0	0x0	Longest linked list of filters in the table. This field records the length of the longest linked list that is updated since the last time this register was read by software. The longest bucket reported by this field includes MAXLEN + 1 filters.
Reserved	7:6	00b	Reserved.
Bucket Length	13:8	0x0	The length of the linked list indicated by a query command. This field is valid following a query command completion.
Reserved	15:14	00b	Reserved.
Reserved	30:16	0x0	Reserved.
Reserved	31	0b	Reserved.

8.2.3.21.12 Flow Director Filters Usage Statistics — FDIRUSTAT (0x0EE50; RW/RC)

Field	Bit(s)	Init Val	Description
ADD	15:0	0x0	Number of added filters. This field counts the number of added filters to the flow director filters logic. The counter is stacked at 0xFFFF and cleared on read.
REMOVE	31:16	0x0	Number of removed filters. This field counts the number of removed filters to the flow director filters logic. The counter is stacked at 0xFFFF and cleared on read.



8.2.3.21.13 Flow Director Filters Failed Usage Statistics — FDIRFSTAT (0x0EE54; RW/RC)

Field	Bit(s)	Init Val	Description
FADD	7:0	0x0	Number of filters addition events that do not change the number of free (non programmed) filters in the flow director filters logic (FDIRFREE.FREE). These events can be either filters update, filters collision, or tentative of filter additions when there is no sufficient space remaining in the filter table. The counter is stacked at 0xFF and cleared on read.
FREMOVE	15:8	0x0	Number of failed removed filters. The counter is stacked at 0xFF and cleared on read.
Reserved	31:16	0x0	Reserved.

8.2.3.21.14 Flow Director Filters Match Statistics — FDIRMATCH (0x0EE58; RC)

Field	Bit(s)	Init Val	Description
PCNT	31:0	0x0	Number of packets that matched any flow director filter. The counter is stacked at 0xFF…F and cleared on read. *Note:* This counter can include packets that match the L2 filters or 5 tuple filters or Syn filters even if they are enabled for queue assignment.

8.2.3.21.15 Flow Director Filters Miss Match Statistics — FDIRMISS (0x0EE5C; RC)

Field	Bit(s)	Init Val	Description
PCNT	31:0	0x0	Number of packets that missed matched any flow director filter. The counter is stacked at 0xFF…F and cleared on read.

Flow Programming Registers

8.2.3.21.16 Flow Director Filters Source IPv6 — FDIRSIPv6[n] (0x0EE0C + 4*n, n=0…2; RW)

Field	Bit(s)	Init Val	Description
IP6SA	31:0	0x0	Three MS DWords of the source IPv6 address. While the LS byte of FDIRSIPv6[0] is first on the wire. The FDIRIPSA contains the LS Dword of the IP6 address while its MS byte is last on the wire.

8.2.3.21.17 Flow Director Filters IP SA — FDIRIPSA (0x0EE18; RW)

Field	Bit(s)	Init Val	Description
IP4SA	31:0	0x0	Source IPv4 address or LS Dword of the Source IPv6 address. While the field is defined in big endian (LS byte is first on the wire).

8.2.3.21.18 Flow Director Filters IP DA — FDIRIPDA (0x0EE1C; RW)

Field	Bit(s)	Init Val	Description
IP4DA	31:0	0x0	Destination IPv4 address. While the field is defined in big endian (LS byte is first on the wire).

8.2.3.21.19 Flow Director Filters Port — FDIRPORT (0x0EE20; RW)

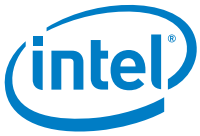
Field	Bit(s)	Init Val	Description
Source	15:0	0x0	Source Port number while the field is defined in Little Endian (MS byte is first on the wire). *Note:* For SCTP filter the Source and Destination port numbers must be set to zero (while the HW does not check it).
Destination	31:16	0x0	Destination Port number while the field is defined in Little Endian (MS byte is first on the wire). *Note:* For SCTP filter the Source and Destination port numbers must be set to zero (while the HW does not check it).

8.2.3.21.20 Flow Director Filters VLAN and FLEX Bytes — FDIRVLAN (0x0EE24; RW)

Field	Bit(s)	Init Val	Description
Vlan	15:0	0x0	Vlan Tag while the field is defined in Little Endian (MS byte is first on the wire). The CFI bit must be set to Zero while it is not checked by hardware.
Flex	31:16	0x0	Flexible tuple data as defined by the *Flex-Offset* field in the FDIRCTRL register while the field is defined in big endian (LS byte is first on the wire).

8.2.3.21.21 Flow Director Filters Hash Signature — FDIRHASH (0x0EE28; RW)

Field	Bit(s)	Init Val	Description
Hash	14:0	0x0	Bucket hash value that identifies a filter's linked list.
Bucket Valid	15	0b	The *Valid* bit is set by hardware each time there is at least one filter assigned to this hash.

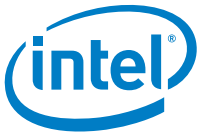


Field	Bit(s)	Init Val	Description
Signature / SW-Index	30:16	0x0	Flow director filter signature for signature filters and software-index for perfect match filters.
Reserved	31	0b	Reserved.

8.2.3.21.22 Flow Director Filters Command Register — FDIRCMD (0x0EE2C; RW)

Field	Bit(s)	Init Val	Description
CMD	1:0	00b	Flow Director Filter Programming Command. 00b = No Action 01b = Add Flow 10b = Remove Flow 11b = Query Command Following a command completion hardware clears the *CMD* field. In a query command, all other parameters are valid when the *CMD* field is zero.
Filter Valid	2	0b	Valid filter is found by the query command. This bit is set by the 82599 following a query command completion.
Filter-Update	3	0b	Filter Update Command. This bit is relevant only for Add Flow command and must be set to zero in any other commands. When cleared, the filter parameters do not override existing ones if exist while setting only the collision bit. When set to 1b the new filter parameters override existing ones if exist keeping the collision bit as is.
IPv6DMatch	4	0b	IP Destination match to IP6AT filter. This bit is meaningful only for perfect match IPv6 filters. Otherwise it should be cleared by software at programming time. When set to 1b the destination IPv6 address should match the IP6AT. When cleared, the destination IPv6 address should not match the IP6AT. This field can never match local VM to VM traffic.
L4TYPE	6:5	0b	L4 Packet Type. Defines the packet as one of the following L4 types: 00b = Reserved 01b = UDP 10b = TCP 11b = SCTP *Note:* Encoding of the L4TYPE for the flow director filters is defined differently than the protocol type encoding in the FTQF registers for the 128 x 5 tuple filters.
IPV6	7	0b	IPv6 packet type when set to 1b and IPv4 packet type at 0b. *Note:* The IP type is checked always even if the filters do not check for IP address match.
CLEARHT	8	0b	Clear Internal Flow Director Head and Tail Registers. This bit is set only as part of Flow Director init. During nominal Operation it must be kept at 0b.

Field	Bit(s)	Init Val	Description
Drop	9	0b	Packet drop action: Receive packets that match a filter with active Drop bit and do not exceed the maximum recommended linked list length defined in FDIRCTRL.Max-Length field are posted to the global queue defined by FDIRCTRL.Drop-Queue. Receive packets that match a filter with active Drop bit and exceeds the maximum recommended linked list length defined in FDIRCTRL.Max-Length field are posted to the queue defined by RX-Queue field in this register. The receive descriptor of such packets is reported with active FDIRErr(0) flag indicating that the Max-Length was exceeded. The Drop Flag is useful only for perfect match filters and it should be cleared by software for Signature filters. When the Drop bit is set, the Queue-EN flag must be set and Rx-Queue in this register must be valid as well. Otherwise, the result is unexpected.
INT	10	0b	Matched packet generates a LLI.
Last	11	0b	Last filter indication in the linked list. At flow programming, software should set the last bit to 1b. Hardware can modify this bit when adding or removing flows from the same linked list.
Collision	12	0b	Collision Indication. This field is set to 1b when software programs the same multiple times. In signature based filtering, it is set when software programs a filter with the same hash and signature multiple times. It should be cleared by software when it adds a flow. It can also be set by hardware when two flows collide with the same hash and signature. During reception, this bit is reported on the Rx descriptor of packets that match the filter. See bit 7 for description of the query- type.
Reserved	14:13	00b	Reserved.
Queue-EN	15	0b	Enable routing matched packet to the queue defined by the Rx-Queue. *Note:* Packets redirection to the FDIRCTRL.Drop-Queue is not gated by the Queue-EN bit.
Rx-Queue	22:16	0x0	Rx Queue Index. This field defines the absolute Rx queue index in all modes of operation (regardless of DCB and VT enablement).
Reserved	23	0b	Reserved.
Pool	29:24	0x0	Pool number is meaningful when VT mode is enabled. When both VT is not enabled, this field must be set by software to 0x0.
Reserved	31:30	0x0	Reserved.



8.2.3.22 MAC Registers

8.2.3.22.1 PCS_1G Global Config Register 1 — PCS1GCFIG (0x04200; RW)

Field	Bit(s)	Init Val	Description
Reserved	29:0	0x8	Reserved.
PCS_isolate	30	0b	PCS Isolate. Setting this bit isolates the 1 GbE PCS logic from the MAC's data path. PCS control codes are still sent and received.
Reserved	31	1b	Reserved.

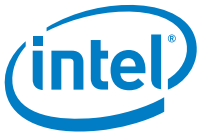
8.2.3.22.2 PCG_1G link Control Register — PCS1GLCTL (0x04208; RW)

Field	Bit(s)	Init Val	Description
FLV	0	0	Forced Link 1 GbE Value. This bit denotes the link condition when *Force Link* is set. 0b = Forced link down. 1b = Forced 1 GbE link up.
Reserved	4:1	0x7	Reserved.
FORCE 1G LINK	5	0	Force 1 GbE Link. If this bit is set then the internal LINK_OK variable is forced to *Forced Link Value*, bit 0 of this register. Else LINK_OK is decided by internal AN/SYNC state machines. This bit is only valid when the link mode is 1 GbE mode.
LINK LATCH LOW	6	0	Link Latch Low Enable. If this bit is set then *Link OK* going LOW; negedge) is latched until a CPU read happens. Once a CPU read happens *Link OK* is continuously updated until *Link OK* again goes LOW (negedge is seen).
Reserved	17:7	0	Reserved.
AN 1G TIMEOUT EN	18	1b	Auto Negotiation 1 GbE Timeout Enable. This bit enables the 1 GbE auto- negotiation timeout feature. During 1 GbE auto-negotiation, if the link partner doesn't respond with auto-negotiation pages but continues to send good idle symbols then linkup is assumed. (This enables a link-up condition when a link partner is not auto-negotiation capable and does not affect otherwise).
Reserved	19	0b	Reserved.
Reserved	20	0b	Reserved, must be set to 0b.
Reserved	24:21	0x0	Reserved.

Field	Bit(s)	Init Val	Description
LINK OK FIX EN	25	1b	Link OK Fix En. Control for enabling/disabling LinkOK-SyncOK fix. This bit should be set to 1b for nominal operation.
Reserved	31:26	0x0	Reserved.

8.2.3.22.3 PCS_1G Link Status Register — PCS1GLSTA (0x0420C; RO)

Field	Bit(s)	Init Val	Description
Reserved	3:0	1110b	Reserved.
SYNC OK 1G	4	0b	Sync OK 1 GbE. This bit indicates the current value of SYN OK from the 1G PCS Sync state machine,
Reserved	15:5	0x0	Reserved.
AN 1G COMPLETE	16	0b	Auto Negotiation1 GbE Complete. This bit indicates that the 1 GbE auto-negotiation process completed.
AN PAGE RECEIVED	17	0b	Auto-Negotiation Page Received. This bit indicates that a link partner's page was received during auto-negotiation process. Clear on read.
AN 1G TIMEDOUT	18	0b	Auto Negotiation1 GbE Timed Out. This bit indicates 1 GbE auto-negotiation process was timed out. Valid after *AN 1G Complete* bit is set.
AN REMOTE FAULT	19	0b	Auto Negotiation Remote Fault. This bit indicates that a 1 GbE auto-negotiation page was received with remote fault indication during 1 GbE auto-negotiation process. Clear on read.
AN ERROR (RW)	20	0b	Auto Negotiation Error. This bit indicates that an auto-negotiation error condition was detected in 1 GbE auto-negotiation mode. Valid after the *AN 1G Complete* bit is set. Auto-negotiation error conditions: Both nodes not full duplex or remote fault indicated or received. Software can also force an auto-negotiation error condition by writing to this bit (or can clear an existing auto-negotiation error condition). Cleared at the start of auto-negotiation.
Reserved	31:21	0x0	Reserved.



8.2.3.22.4 PCS_1 Gb/s Auto Negotiation Advanced Register — PCS1GANA (0x04218; RW)

Field	Bit(s)	Init Val	Description
Reserved	4:0	0x0	Reserved.
FDC	5	1b	FD: Full-Duplex. Setting this bit means the local device is capable of full-duplex operation. This bit should be set to 1b for normal operation.
Reserved	6	0b	Reserved.
ASM	8:7	11b	ASM_DIR/PAUSE: Local PAUSE Capabilities. The local device's PAUSE capability is encoded in this field. 00b = No PAUSE. 01b = Symmetric PAUSE. 10b = Asymmetric PAUSE toward link partner. 11b = Both symmetric and asymmetric PAUSE toward local device.
Reserved	11:9	0x0	Reserved.
RFLT	13:12	00b	Remote Fault. The local device's remote fault condition is encoded in this field. Local device can indicate a fault by setting a non-zero remote fault encoding and re-negotiating. 00b = No error, link good. 01b = Link failure. 10b = Offline. 11b = Auto-negotiation error.
Reserved	14	0b	Reserved.
NEXTP	15	0b	NEXTP: Next Page Capable. The local device asserts this bit to request next page transmission. Clear this bit when local device has no subsequent next pages.
Reserved	31:16	0x0	Reserved.

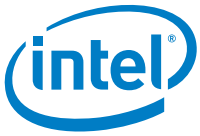
8.2.3.22.5 PCS_1GAN LP Ability Register — PCS1GANLP (0x0421C; RO)

Field	Bit(s)	Init Val	Description
Reserved	4:0	0x0	Reserved.
LPFD	5	0b	LP Full-Duplex (SerDes). When 1b, link partner is capable of full-duplex operation. When 0b, link partner is incapable of full-duplex mode.
LPHD	6	0b	LP Half-Duplex (SerDes). When 1b, link partner is capable of half-duplex operation. When 0b, link partner is incapable of half-duplex mode.

Field	Bit(s)	Init Val	Description
LPASM	8:7	00b	LPASMDR/LPPAUSE(SERDES). The link partner's PAUSE capability is encoded in this field. 00b = No PAUSE. 01b = Symmetric PAUSE. 10b = Asymmetric PAUSE toward link partner. 11b = Both symmetric and asymmetric PAUSE toward local device.
Reserved	11:9	0x0	Reserved.
PRF	13:12	00b	LP Remote Fault (SerDes)[13:12]. The link partner's remote fault condition is encoded in this field. 00b = No error, link good. 10b = Link failure. 01b = Offline. 11b = Auto-negotiation error.
ACK	14	0b	Acknowledge (SerDes). The link partner has acknowledged page reception.
LPNEXTP	15	0b	LP Next Page Capable (SerDes). The link partner asserts this bit to indicate its ability to accept next pages.
Reserved	31:16	0x0	Reserved.

8.2.3.22.6 PCS_1G Auto Negotiation Next Page Transmit Register — PCS1GANNP (0x04220; RW)

Field	Bit(s)	Init Val	Description
CODE	10:0	0x0	Message/Unformatted Code Field. The message field is an 11-bit wide field that encodes 2048 possible messages. Unformatted code field is an 11-bit wide field, which can contain an arbitrary value.
TOGGLE	11	0b	Toggle. This bit is used to ensure synchronization with the link partner during a next page exchange. This bit always takes the opposite value of the *Toggle* bit in the previously exchanged link code word. The initial value of the *Toggle* bit in the first next page transmitted is the inverse of bit 11 in the base link code word and, therefore, can assume a value of 0b or 1b. The Toggle bit must be set as follows: 0b Previous value of the transmitted Link Code Word equaled 1b. 1b Previous value of the transmitted Link Code Word equaled 0b.
ACK2	12	0b	Acknowledge2. Acknowledge is used to indicate that a device has successfully received its link partner’s link code word.
PGTYPE	13	0b	Message/ Unformatted Page. This bit is used to differentiate a message page from an unformatted page. The encodings are: 0b = Unformatted page. 1b = Message page.
Reserved	14	0b	Reserved.



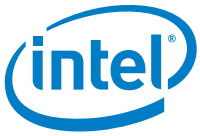
Field	Bit(s)	Init Val	Description
NXTPG	15	0b	Next Page. This bit is used to indicate whether or not this is the last next page to be transmitted. The encodings are: 0b = Last page. 1b = Additional next pages follow.
Reserved	31:16	0x0	Reserved.

8.2.3.22.7 PCS_1G Auto Negotiation LP's Next Page Register — PCS1GANLPNP (0x04224; RO)

Field	Bit(s)	Init Val	Description
CODE	10:0	0x0	Message/Unformatted Code Field. The message field is an 11-bit wide field that encodes 2048 possible messages. Unformatted code field is an 11-bit wide field, which can contain an arbitrary value.
TOGGLE	11	0bb	Toggle. This bit is used to ensure synchronization with the link partner during a next page exchange. This bit always takes the opposite value of the *Toggle* bit in the previously exchanged link code word. The initial value of the *Toggle* bit in the first next page transmitted is the inverse of bit 11 in the base link code word and, therefore, can assume a value of 0b or 1b. The Toggle bit must be set as follows: 0b = Previous value of the transmitted link code word equalled 1b. 1b = Previous value of the transmitted link code word equalled 0b.
ACK2	12	0	Acknowledge2. Acknowledge is used to indicate that a device has successfully received its link partner's link code word.
MSGPG	13	0bb	Message Page. This bit is used to differentiate a message page from an unformatted page. The encodings are: 0b = Unformatted page. 1b = Message page.
ACK	14	0	Acknowledge. The link partner has acknowledge next page reception.
NXTPG	15	0b	Next Page. This bit is used to indicate whether or not this is the last next page to be transmitted. The encodings are: 0b = Last page. 1b = Additional next pages follow.
Reserved	31:16	0x0	Reserved.

8.2.3.22.8 MAC Core Control 0 Register — HLREG0 (0x04240; RW)

Field	Bit(s)	Init Val	Description
TXCRCEN	0	1b	Tx CRC Enable. Enables a CRC to be appended by hardware to a Tx packet if requested by user. 0b = No CRC appended, packets always passed unchanged. 1b = Enable CRC by hardware (default).
Reserved	1	1b	Reserved.
RXCRCSTRP	1	1	Rx CRC STRIP. Causes the CRC to be stripped by HW from all packets The RDRXCTL.CRCStrip must be set the same as this bit. 0b = No CRC Strip by HW. 1b = Strip CRC by HW (Default).
JUMBOEN	2	0b	Jumbo Frame Enable. Enables frames up to the size specified in Reg MAXFRS (31:16). 0b = Disable jumbo frames (default). 1b = Enable jumbo frames.
Reserved	9:3	0x1	Reserved. Must be set to 0x1.
TXPADEN	10	1b	Tx Pad Frame Enable. Pad short Tx frames to 64 bytes if requested by user. 0b = Transmit short frames with no padding. 1b = Pad frames (default).
Reserved	14:11	0101b	Reserved.
LPBK	15	0b	LOOPBACK. Turn On Loopback Where Transmit Data Is Sent Back Through Receiver. 0b = Loopback disabled (Default). 1b = Loopback enabled.
MDCSPD	16	1b	MDC SPEED. High or Low Speed MDC Clock Frequency To PCS, XGXS, WIS, etc. **MDCSPD / Freq at 10 GbE / Freq at 1 GbEs / Freq at 100 Mb/s** 0b / 2.4 MHz / 240 KHz / 240 KHz 1b / 24 MHz / 2.4 MHz / 240 KHz *Note:* 1b = default.
CONTMDC	17	0b	Continuous MDC. Turn Off MDC Between MDIO Packets 0b = MDC Off Between Packets (default) 1b = Continuous MDC
Reserved	19:18	00b	Reserved.
PREPEND	23:20	0x0	Prepend Value. Number of 32-bit words starting after the preamble and SFD, to exclude from the CRC generator and checker (default – 0x0).
Reserved	24	0b	Reserved.
Reserved	26:25	00b	Reserved.



Field	Bit(s)	Init Val	Description
RXLNGTHERREN	27	1b	Rx Length Error Reporting. 0b = Disable reporting of all rx_length_err events. 1b = Enable reporting of rx_length_err events if length field < 0x0600.
RXPADSTRIPEN	28	0b	Rx Padding Strip Enable. 0b = Do not strip padding from Rx packets with length field < 64 (default). 1b = Strip padding from Rx packets with length field < 64 (debug only). *Note:* This functionality should be used as debug mode only. If Rx pad stripping is enabled, then the Rx CRC stripping needs to be enabled as well.
Reserved	31:29	0x0	Reserved.

8.2.3.22.9 MAC Core Status 1 Register- HLREG1 (0x04244; RO)

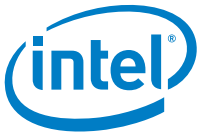
Field	Bit(s)	Init Val	Description
Reserved	3:0	0001b	Reserved.
Reserved	4	0b	Reserved.
RXERRSYM	5	0b	Rx Error Symbol. Error Symbol During Rx Packet (Latch High, Clear On Read). 0b = No error symbol (default). 1b = Error symbol received.
RXILLSYM	6	0b	Rx Illegal Symbol. Illegal Symbol During Rx Packet (Latch High, Clear On Read). 0b = No illegal symbol received (default). 1b = Illegal symbol received.
RXIDLERR	7	0b	Rx Idle Error. Non Idle Symbol During Idle Period (Latch High, Clear On Read). 0b = No idle errors received (default). 1b = Idle error received.
RXLCLFLT	8	0b	Rx Local Fault. Fault reported from PMD, PMA, or PCS (Latch High, Clear On Read). 0b = No local fault (default). 1b = Local fault is or was active.
RXRMTFLT	9	0b	Rx Remote Fault. Link Partner Reported Remote Fault (Latch High, Clear On Read). 0b = No remote fault (default). 1b = Remote fault is or was active.
Reserved	31:10	0x0	Reserved.

8.2.3.22.10 Pause and Pace Register — PAP (0x04248; RW)

Field	Bit(s)	Init Val	Description
Reserved	15:0	0xFFFF	Reserved.
PACE	19:16	0x0	0000b = 10 GbE (LAN) 0001b = 1 GbE 0010b = 2 GbE 0011b = 3 GbE 0100b = 4 GbE 0101b = 5 GbE 0110b = 6 GbE 0111b = 7 GbE 1000b = 8 GbE 1001b = 9 GbE 1111b = 9.294196 GbE (WAN) All other values are reserved.
Reserved	31:20	0x0	Reserved

8.2.3.22.11 MDI Single Command and Address — MSCA (0x0425C; RW)

Field	Bit(s)	Init Val	Description
MDIADD	15:0	0x0000	MDI Address. Address used for new protocol MDI accesses (default – 0x0000).
DEVADD	20:16	0x0	DeviceType/Register Address. Five bits representing either device type if STCODE = 00b or register address if STCODE = 01b.
PHYADD	25:21	0x0b	PHY Address. The address of the external device.
OPCODE	27:26	00	OP Code. Two bits identifying operation to be performed (default – 00b). 00b = Address cycle (new protocol only). 01b = Write operation. 10b = Read increment address (new protocol only) or read operation (old protocol only). 11b = Read operation (new protocol only).
STCODE	29:28	01b	ST Code. Two Bits Identifying Start Of Frame And Old Or New Protocol (Default – 01). 00b = New protocol. 01b = Old protocol. 1Xb = Illegal.



Field	Bit(s)	Init Val	Description
MDICMD	30	0b	MDI Command. Perform the MDIO Operation in this register, cleared when done. 0b = MDI Ready, operation complete (default). 1b = Perform operation, operation in progress.
Reserved	31	0b	Reserved.

8.2.3.22.12 MDI Single Read and Write Data — MSRWD (0x04260; RW)

Field	Bit(s)	Init Val	Description
MDIWRDATA	15:0	0x0	MDI Write Data. Write data For MDI writes to the external device.
MDIRDDATA	31:16	0x0	MDI Read Data. Read data from the external device (RO).

8.2.3.22.13 Max Frame Size — MAXFRS (0x04268; RW)

Field	Bit(s)	Init Val	Description
Reserved	15:0	0x0	Reserved.
MFS	31:16	0x5EE	This field defines the maximum frame size in bytes units from Ethernet MAC addresses up to inclusive the CRC. Frames received that are larger than this value are dropped. This field is meaningful when jumbo frames are enabled (HLREG0.JUMBOEN = 1b). When jumbo frames are not enabled the 82599 uses a hardwired value of 1518 for this field. The MFS does not include the 4 bytes of the VLAN header. Packets with VLAN header can be as large as MFS + 4. When double VLAN is enabled, the device adds 8 to the MFS for any packets. This value has no effect on transmit frames; it is the responsibility of software to limit the size of transmit frames.

8.2.3.22.14 XGXS Status 1 — PCSS1 (0x4288; RO)

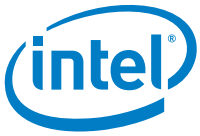
Field	Bit(s)	Init Val	Description
Reserved	1:0	00b	Reserved.
PCS Receive Link Status	2	0b	0b = PCS receive link down.The receive link status remains cleared until it is read (latching low). 1b = PCS receive link up. For 10BASE-X ->lanes de-skewed.
Reserved	6:3	0x0	Reserved.
Local Fault	7	1b	0b = No LF detected on receive path. 1b = LF detected on transmit or receive path. The *LF* bit is set to one when either of the local fault bits located in PCS Status 2 register are set to a 1b.
Reserved	31:8	0x0	Reserved.

8.2.3.22.15 XGXS Status 2 — PCSS2 (0x0428C; RO)

Field	Bit(s)	Init Val	Description
10GBASE-R Capable	0	0b	0b = PCS is not able to support 10GBASE-R port type. 1b = PCS is able to support 10GBASE-R port type.
10GBASE-X capable	1	1b	0b = PCS is not able to support 10GBASE-X port type. 1b = PCS is able to support 10GBASE-X port type.
10GBASE-W capable	2	0b	0b = PCS is not able to support 10GBASE-W port type. 1b = PCS is able to support 10GBASE-W port type.
Reserved	9:3	0x0	Reserved.
Receive local fault	10	1b	0b = No local fault condition on the receive path (latch high) 1b = Local fault condition on the receive path.
Transmit local fault	11	0b	0b = No local fault condition on the transmit path (latch high) 1b = Local fault condition on the transmit path.
Reserved	13:12	00b	Reserved.
Device present	15:14	10b	00b = No device responding at this address. 01b = No device responding at this address. 10b = Device responding at this address. 11b = No device responding at this address.
Reserved	31:16	0x0	Reserved.

8.2.3.22.16 10GBASE-X PCS Status — XPCSS (0x04290; RO)

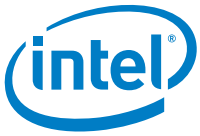
Field	Bit(s)	Init Val	Description
Lane 0 sync	0	0b	0b = Lane 0 is not synchronized. 1b = Lane 0 is synchronized.
Lane 1 sync	1	0b	0b = Lane 1 is not synchronized. 1b = Lane 1 is synchronized.
Lane 2 sync	2	0b	0b = Lane 2 is not synchronized. 1b = Lane 2 is synchronized.
Lane 3 sync	3	0b	0b = Lane 3 is not synchronized. 1b = Lane 3 is synchronized.
Reserved	11: 4	0b	Ignore when read.
10GBASE-X lane alignment status	12	0b	0b = 10GBASE-X PCS receive lanes not aligned. 1b = 10GBASE-X PCS receive lanes aligned (align_status – good).
Reserved	15:13	0x0	Reserved, ignore when read.



Field	Bit(s)	Init Val	Description
De-skew error	16	0b	0b = Indicates no de-skew error was detected (latch high). 1b = Indicates a de-skew error was detected.
Align column count 4	17	0b	0b = Indicates the align column count is less than four (latch high). 1b = Indicates the align column count has reached four.
Lane 0 invalid code	18	0b	0b = Indicates no invalid code was detected (latch high). 1b = Indicates an invalid code was detected for that lane.
Lane 1 invalid code	19	0b	0b = Indicates no invalid code was detected (latch high). 1b = Indicates an invalid code was detected for that lane.
Lane 2 invalid code	20	0b	0b = Indicates no invalid code was detected (latch high). 1b = Indicates an invalid code was detected for that lane.
Lane 3 invalid code	21	0b	0b = Indicates no invalid code was detected (latch high). 1b = Indicates an invalid code was detected for that lane.
Lane 0 comma count4	22	0b	0b = Indicates the comma count for that lane is less than four (latch high). 1b = Indicates the comma count for that lane has reached four.
Lane 1 comma count 4	23	0b	0b = Indicates the comma count for that lane is less than four (latch high). 1b = Indicates the comma count for that lane has reached four.
Lane 2 comma count 4	24	0b	0b = Indicates the comma count for that lane is less than four (latch high). 1b = Indicates the comma count for that lane has reached four.
Lane 3 comma count 4	25	0b	0b = Indicates the comma count for that lane is less than four (latch high). 1b = Indicates the comma count for that lane has reached four.
Lane 0 Signal Detect	26	0b	0b = Indicates noise, no signal is detected. 1b = Indicates a signal is detected.
Lane 1 Signal Detect	27	0b	0b = Indicates noise, no signal is detected. 1b = Indicates a signal is detected.
Lane 2 Signal Detect	28	0b	0b = Indicates noise, no signal is detected. 1b = Indicates a signal is detected.
Lane 3 Signal Detect	29	0b	0b = Indicates noise, no signal is detected. 1b = Indicates a signal is detected.
Reserved	31:30	0b	Reserved.

8.2.3.22.17 SerDes Interface Control Register — SERDESC (0x04298; RW)

Field	Bit(s)	Init Val	Description
Tx_lanes_polarity	3:0	0*	Bit 3 = Changes bits polarity of MAC Tx lane 3. Bit 2 = Changes bits polarity of MAC Tx lane 2. Bit 1 = Changes bits polarity of MAC Tx lane 1. Bit 0 = Changes bits polarity of MAC Tx lane 0. Changes bits polarity if set to 1b.
Rx_lanes_polarity	7:4	0*	Bit 7 = Changes bits polarity of MAC Rx lane 3. Bit 6 = Changes bits polarity of MAC Rx lane 2. Bit 5 = Changes bits polarity of MAC Rx lane 1. Bit 4 = Changes bits polarity of MAC Rx lane 0. Changes bits polarity if set to 1b.
swizzle_tx_lanes	11:8	0*	Bit 11 = Swizzles bits of MAC Tx lane 3. Bit 10 = Swizzles bits of MAC Tx lane 2. Bit 9 = Swizzles bits of MAC Tx lane 1. Bit 8 = Swizzles bits of MAC Tx lane 0. Swizzles bits if set to 1b. These bits are for debug only – software should not change the default EEPROM value.
swizzle_rx_lanes	15:12	0*	Bit 15 = Swizzles bits of MAC Rx lane 3. Bit 14 = Swizzles bits of MAC Rx lane 2. Bit 13 = Swizzles bits of MAC Rx lane 1. Bit 12 = Swizzles bits of MAC Rx lane 0. Swizzles bits if set to 1b. These bits are for debug only – software should not change the default EEPROM value.
swap_tx_lane_3	17:16	11b*	Determines Core destination Tx lane for MAC Tx lane 3.
swap_tx_lane_2	19:18	10b*	Determines Core destination Tx lane for MAC Tx lane 2.
swap_tx_lane_1	21:20	01b*	Determines Core destination Tx lane for MAC Tx lane 1.
swap_tx_lane_0	23:22	00b*	Determines Core destination Tx lane for MAC tx lane 0. 00b = MAC Tx lane 0 to Core Tx lane 0. 01b = MAC Tx lane 0 to Core Tx lane 1. 10b = MAC Tx lane 0 to Core Tx lane 2. 11b = MAC Tx lane 0 to Core Tx lane 3.
swap_rx_lane_3	25:24	11b*	Determines which Core lane is mapped to MAC Rx lane 3.
swap_rx_lane_2	27:26	10b*	Determines which Core lane is mapped to MAC Rx lane 2.



Field	Bit(s)	Init Val	Description
swap_rx_lane_1	29:28	01b*	Determines which Core lane is mapped to MAC Rx lane 1.
swap_rx_lane_0	31:30	00b*	Determines which Core lane is mapped to MAC Rx lane 0. 00b = Core Rx lane 0 to MAC Rx lane 0. 01b = Core Rx lane 1 to MAC Rx lane 0. 10b = Core Rx lane 2 to MAC Rx lane 0. 11b = Core Rx lane 3 to MAC Rx lane 0.

* Also programmable via EEPROM.

8.2.3.22.18 FIFO Status/CNTL Report Register — MACS (0x0429C; RW)

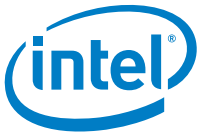
This register reports FIFO status in xgmii_mux.

Field	Bit(s)	Init Val	Description
XGXS SYNC Fix Disable	0	0b	Use shift-fsm control for the XGXS sync process. 0b = Normal functionality (default). 1b = Use shift-fsm control, disable fix (debug only).
XGMII-GMII Tx END Fix Disable	1	0b	Disable tx_end on link-down. 0b = Normal functionality, link down causes tx_end (default). 1b = Disable tx_end on link-down (debug only).
XGXS Deskew Fix Disable	2	0b	Disable align on invalid fix. 0b = Normal functionality (default). 1b = Disable align on invalid fix (debug only).
Nonce Match Disable	3	0b	Disable nonce match. 0b = Normal functionality (default). 1b = Disable nonce match (debug only).
Reserved	15:4	0x0	Reserved. On a write access to this field the SW should maintain the value of this field.
Config fault length	23:16	0x1F	Sets the length in clock cycles of LF stream.
Config FIFO threshold	27:24	0x6	Determines threshold for asynchronous FIFO (generation of data_available signal is determined by cfg_fifo_th[3:0]).
tx FIFO underrun	28	0b	Indicates FIFO under run in xgmii_mux_tx_fifo.
tx FIFO overrun	29	0b	Indicates FIFO overrun in xgmii_mux_tx_fifo.
rx FIFO underrun	30	0b	Indicates FIFO under run in xgmii_mux_rx_fifo.
rx FIFO overrun	31	0b	Indicates FIFO overrun in xgmii_mux_rx_fifo.

8.2.3.22.19 Auto Negotiation Control Register — AUTOC (0x042A0; RW)

Note: The 82599 Device Firmware may access AUTOC register in parallel to software driver and a synchronization between them is needed. For more information see Section 10.5.4.

Field	Bit(s)	Init Val	Description
FLU	0	0b	Force Link Up. 0b = Normal mode. 1b = MAC forced to link_up. Link is active in the speed configured in AUTOC.LMS. This setting forces the auto-negotiation arbitration state machine to AN_GOOD and sets the link_up indication regardless of the XGXS/ PCS_1G status.
ANACK2	1	0b*	Auto-Negotiation Ack2 field. This value is transmitted in the *Achnowledge2* field of the null next page that is transmitted during a next page handshake.
ANSF	6:2	00001b*	Auto-Negotiation Selector Field. This value will be used as the Selector Field in the Link Control Word during Clause 73 Backplane Auto–Negotiation process. (Default value set according to 802.3ap-2007).
10G_PMA_PMD_PARALLEL	8:7	01b*	Define 10 GbE PMA/PMD over four differential pairs (Tx and Rx each). 00b = XAUI PMA/PMD. 01 = KX4 PMA/PMD. 10 = CX4 PMA/PMD. 11 = Reserved.
1G_PMA_PMD	9	1b*	PMA/PMD used for 1 GbE. 0b = SFI PMA/PMD (the AUTOC.LMS should be set to 000b). 1b = KX or BX PMA/PMD.
D10GMP	10	0b*	Disables 10 GbE Parallel Detect on Dx (Dr/D3) without main–power. 0b = No specific action. 1b = Disables 10 GbE Parallel Detect when main power is removed. This bit is valid only if RATD is set. *Note:* If MNG_VETO bit is set, any low-power link mode changes will be hold off.
RATD	11	0b*	Restarts auto-negotiation on transition to Dx. This bit enables the functionality to restart KX/KX4/KR backplane auto-negotiation on transition to Dx (Dr/D3), targeting an 1GbE link. 0b = Does not restart auto-negotiation when the 82599 moves to the Dx state. 1b = Restarts auto-negotiation to reach a low–power link mode (1 GbE link) when the 82599 transitions to the Dx state. Only 1GbE will be advertised by auto-negotiation. In this case, if a partner doesn't have 1GbE capabilities, a link will not be established. 10GbE can still be achieved by Parallel Detect of a XAUI partner if D10GMP bit is clear. *Note:* If MNG_VETO bit is set, any low-power link mode changes will be hold off.



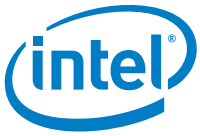
Field	Bit(s)	Init Val	Description
Restart_AN	12	0b*	Applies new link settings and restarts relative auto-negotiation process (self–clearing bit). 0b = No action needed. 1b = Applies new link settings and restarts auto-negotiation. *Note:* This bit must be set to make any new link settings affective as indicated in Section 3.7.4.2.
LMS	15:13	100b*	Link Mode Select. Selects the active link mode: 000b = 1 GbE link (no backplane auto-negotiation). 001b = 10 GbE parallel link (KX4 – no backplane auto-negotiation). 010b = 1 GbE link with clause 37 auto-negotiation enable (BX interface). 011b = 10 GbE serial link (SFI – no backplane auto-negotiation). 100b = KX/KX4/KR backplane auto-negotiation enable. 1 GbE (Clause 37) auto-negotiation disabled. 101b = SGMII 100M/1 GbE link. 110b = KX/KX4/KR backplane auto-negotiation enable. 1 GbE (Clause 37) auto-negotiation enable. 111b = KX/KX4/KR auto-negotiation enable. SGMII 100 Mb/s and 1GbE (in KX) enable.
KR_support	16	1b*	Configures the *A2* bit of the *Technology Ability Field* in the auto-negotiation word while *A0:A1* fields are configured in the KX_support field (bits 31:30): 0b = KR not supported. Value is Illegal if KX and KX4 are also not supported (AUTOC.KX_support – 00b). 1b = KR supported. *Note:* This bit is not relevant to the parallel detect process.
FECR	17	0b*	FEC Requested. Configures the *F1* bit in the backplane auto-negotiation base link code word. Should be set to 1b only if KR ability is set to 1b (AUTOC.KR = 1b). 0b = FEC not requested from link partner. 1b = FEC requested from link partner.
FECA	18	1b*	FEC Ability. Configures the *F0* bit in the backplane auto-negotiation base link code word. Should be set to 1b only if KR ability is set to 1b (AUTOC.KR = 1b). 0b = FEC not supported. 1b = FEC supported.
ANRXAT	22:19	0011b*	Backplane Auto-Negotiation Rx Align Threshold. Sets threshold to determine alignment is stable.
ANRXDM	23	1b*	Auto-Negotiation Rx Drift Mode. Enables following the drift caused by PPM in the Rx data. 0b = Disables drift mode. 1b = Enables drift mode.
ANRXLM	24	1b*	Auto-Negotiation Rx Loose Mode. Enables less restricted functionality (allow 9/11 bit symbols). 0b = Disables loose mode. 1b = Enables loose mode.

Field	Bit(s)	Init Val	Description
ANPDT	26:25	00b*	Auto-Negotiation Parallel Detect Timer. Configures the parallel detect counters. 00b = 1 ms 01b = 2 ms 10b = 5 ms 11b = 8 ms
RF	27	0b*	This bit is loaded to the RF of the auto-negotiation word.
PB	29:28	00b*	Pause Bits. The value of these bits is loaded to bits D11–D10 of the Link code word (pause data). Bit 29 is loaded to D11.
KX_support	31:30	11b*	Configures the A0:A1 bits of the *Technology Ability Field* of the backplane auto-negotiation word while A2 field is configured in the KR_support bit (bit 16): 00b= A0 – 0; A1 – 0. KX not supported. KX4 not supported. Value is Illegal if KR is also not supported (AUTOC.KR_support – 0b). 01b = A0 – 1; A1 – 0. KX supported. KX4 not supported. 10b = A0 – 0; A1 – 1. KX not supported. KX4 supported. 11b = A0 – 1; A1 – 1. KX supported. KX4 supported.

* Also programmable via EEPROM.

8.2.3.22.20 Link Status Register — LINKS (0x042A4; RO)

Field	Bit(s)	Init Val	Description
KX_SIG_DET	0	0b	Signal Detect of 1 GbE and 100 Mb/s. 0b = A signal is not present (Fail). 1b = A signal is present (OK).
FEC_SIG_DET	1	0b	Signal detect of FEC 0b = FEC reports signal not detected (failed). 1b = FEC reports signal detected (good).
FEC_BLOCK_LOCK	2	0b	10 GbE serial PCS FEC block lock. 0b = No FEC block lock. 1b = FEC reached block lock.
KR_HI_BERR	3	0b	10GbE serial KR_PCS high error rate (greater than 10^{-4}). 0b = Low BERR. 1b = High BERR.
KR_PCS_BLOCK_LOCK	4	0b	10 GbE serial PCS block lock. 0b = No KR_PCS block lock. 1b = KR_PCS reached block lock.
KX/KX4/KR Backplane AN Next Page received	5	0b	KX/KX4/KR AN Next Page Received. A new link partner next page was received during the backplane auto-negotiation process. Latch high, clear on read.

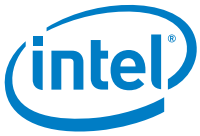


Field	Bit(s)	Init Val	Description
KX/KX4/KR Backplane AN Page received	6	0b	KX/KX4/KR Backplane Auto Negotiation Page Received. A new link partner page was received during the auto-negotiation process. Latch high, clear on read.
Link Status	7	0b	0b = Link is currently down or link was down since last time read. 1b = Link is Up and there was no link down from last time read. Self cleared upon read if the link is low and set if the link is up.
KX4_SIG_DET	11:8		Signal Detect of 10 GbE Parallel (KX4, CX4 or XAUI). Bit[11, 10, 9, 8] shows lane <3,2,1,0> status, respectively. For each bit: 0b = A signal is not present (failed). 1b = A signal is present (good).
KR_SIG_DET	12		Signal Detect of 10 GbE serial (KR or SFI). 0b = Signal not detected (failed). 1b = Signal detected (good).
10G lane sync_status	16:13		10G Parallel lane sync status. bit[16,15,14,13] show lane <3,2,1,0> status accordingly. per each bit: 0b = sync_status is FAILED (not synchronized to code-group). 1b = sync_status is OK (synchronized to code-group).
10G Align Status	17		10 GbE align_status. 0b = Align_status failed (deskew process not complete). 1b = Align_status good (all lanes are synchronized and aligned).
1G Sync Status	18		1G sync_status. 0b = Sync_status failed (not synchronized to code-group). 1b = Sync_status is good (synchronized to code-group).
KX/KX4/KR Backplane AN Receiver Idle	19		KX/KX4/KR Backplane Auto Negotiation Rx Idle. 0b = Receiver good. 1b = Receiver is in idle-waiting to align and sync on DME.
1G AN enabled (clause 37 AN)	20		PCS_1 GbE auto-negotiation is enabled (clause 37).
1G link Enabled PCS_1G	21		1 GbE PCS enabled for 1 GbE and SGMII operation.
10G link Enabled (XGXS)	22		XGXS Enabled for 10 GbE operation.
FEC_EN	23		Status of forward–error–correction in 10 GbE serial link (KR operating mode). 0b = FEC disabled. 1b = FEC enabled.
10G_SER_EN	24		Status of 10 GbE serial PCS (KR PCS) for KR or SFI operation. 0b = KR PCS disabled. 1b = KR PCS enabled.
SGMII_EN	25		Status of SGMII operation. 0b = SGMII disabled. 1b = SGMII enabled.

Field	Bit(s)	Init Val	Description
MLINK_MODE	27:26		MAC link mode status. 00b = 1 GbE 01b = 10 GbE parallel 10b = 10 GbE serial 11b = Auto-negotiation
LINK_SPEED	29:28		MAC link speed status. 00b = Reserved 01b = 100 Mb/s 10b = 1 GbE 11b = 10 GbE
Link Up	30	0b	link up 0b = Link is down. 1b = Link is up.
KX/KX4/KR Backplane AN Completed	31	0b	Indicates KX/KX4/KR backplane auto-negotiation has completed successfully.

8.2.3.22.21 Link Status Register 2 — LINKS2 (0x04324; RO)

Field	Bit(s)	Init Val	Description
MAC Rx Link Mode	1:0	00b	MAC link mode in the Core Rx path. 00b = 1 GbE 01b = 10 GbE parallel 10b = 10GbE serial 11b = Auto-negotiation
Reserved	2	0b	Reserved.
MAC Tx Link Mode	4:3	00b	MAC link mode in the Core Tx path. 00b = 1 GbE 01b = 10 GbE parallel 10b = 10GbE serial 11b = Auto-negotiation
Reserved	5	0b	Reserved.
Link-Partner AN	6	0b	Link Partner KX/KX4/KR Backplane Auto-Negotiation Ability. 0b = Link partner is not KX/KX4/KR backplane auto-negotiation capable. 1b = Link partner is KX/KX4/KR backplane auto-negotiation capable.
Reserved	31:7	0x0	Reserved.



8.2.3.22.22 Auto Negotiation Control 2 Register — AUTOC2 (0x042A8; RW)

Field	Bit(s)	Init Val	Description
Reserved	15:0	0b	Reserved.
10G_PMA_PMD_Serial	17:16	00b*	PMAPMD used for 10 GbE serial link operation: 00b = KR 01b = Reserved 10b = SFI 11b = Reserved
DDPT	18	0*	Disable DME Pages Transmit. Setting this bit disables the DME pages transmitting while the device in auto–negotiation mode (it transmits 0bs instead).
Reserved	27:19	0b	Reserved
FASM	28	0b	Force the auto-negotiation arbitration state machine to idle 0b = No Force (normal operation). 1b = Force state and keep constant forced state
Reserved	29	0b	Reserved.
PDD	30	0b*	Disable the parallel detect part in the KX/KX4/KR backplane auto-negotiation. When set to 1b the auto-negotiation process avoids any parallel detect activity, and relies only on the DME pages received and transmitted. 0b = Enable the parallel detect (normal operation). 1b = Disable the parallel detect (debug only).
Reserved	31	0b	Reserved.

* Loaded from the AUTOC2 word in the MAC EEPROM section

8.2.3.22.23 Auto Negotiation Link Partner Link Control Word 1 Register — ANLP1 (0x042B0; RO)

Field	Bit(s)	Init Val	Description
LP AN page D low	15:0	0x0	LP auto-negotiation advertisement page fields D[15:0]. [15] = NP [14] = Acknowledge [13] = RF [12] = Reserved [11:10] = Pause [9:5] = Echoed Nonce field [4:0] = Selector field
ANAS	19:16	0x0	Auto-Negotiation state machine status. If zero, it indicates that state machine is in idle state.
Reserved	31:20	0x0	Reserved.

To ensure that software has the ability to read the same Link Partner Link Control Word (located across two registers), once ANLP1 is read, ANLP2 is locked until the ANLP2 register is read. ANLP2 does not hold valid data before ANLP1 is read.

8.2.3.22.24 Auto Negotiation Link Partner Link Control Word 2 Register — ANLP2 (0x042B4; RO)

Field	Bit(s)	Init Val	Description
LP Transmitted Nonce Field	4:0	0x0	LP auto-negotiation advertisement page fields T[4:0].
LP Technology Ability Field Low	15:5	0x0	LP auto-negotiation advertisement page fields A[10:0].
LP Technology Ability Field High	31:16	0x0	LP auto-negotiation advertisement page fields A[26:11].

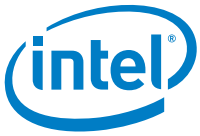
To ensure that software has the ability to read the same Link Partner Link Control Word (located across two registers), once ANLP1 is read, ANLP2 is locked until the ANLP2 register is read. ANLP2 does not hold valid data before ANLP1 is read.

8.2.3.22.25 MAC Manageability Control Register — MMNGC (0x042D0; Host-RO/MNG-RW)

Field	Bit(s)	Init Val	Description
MNG_VETO	0	0b	MNG_VETO (default 0b). Access read/write by manageability, read only to the host. 0b = No specific constraints on link from manageability. 1b = Hold off any low-power link mode changes. This is done to avoid link loss and interrupting manageability activity.
Reserved	31:1	0x0	Reserved.

8.2.3.22.26 Auto Negotiation Link Partner Next Page 1 Register — ANLPNP1 (0x042D4; RO)

Field	Bit(s)	Init Val	Description
LP AN Next Page Low	31:0	0x0	LP Auto-Negotiation Next Page Fields D[31:0]. [31:16] = Unformatted Code [15] = NP [14] = Acknowledge [13] = MP [12] = Acknowledge2 [11] = Toggle [10:0] = Message/Unformatted Code



To ensure that software has the ability to read the same Link Partner Link Control Word (located across two registers), once ANLP1 is read, ANLP2 is locked until the ANLP2 register is read. ANLP2 does not hold valid data before ANLP1 is read.

8.2.3.22.27 Auto Negotiation Link Partner Next Page 2 Register — ANLPNP2 (0x042D8; RO)

Field	Bit(s)	Init Val	Description
LP AN Next Page high	15:0	0x0	LP AN Next Page Fields D[47:32]. [15:0] = Unformatted Code.
Reserved	31:16	0x0	Reserved.

To ensure that software has the ability to read the same Link Partner Link Control Word (located across two registers), once ANLPNP1 is read, ANLPNP2 is locked until the ANLPNP2 register is read. ANLPNP2 does not hold valid data before ANLPNP1 is read.

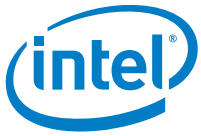
8.2.3.22.28 KR PCS and FEC Control Register — KRPCSFC (0x042EO; RW)

Field	Bit(s)	Init Val	Description
Reserved	10:0	0x0	Reserved. Bits should be written as 0x0 and ignored on read.
Reserved	15:11	0x0	Reserved.
FEC_ENABLE_ERR	16	1b	FEC Enable Error Indication to KR-PCS. 0b = Disabled. 1b = The FEC decoder indicates error to the KR-PCS by means of setting both sync bits to the value 11 in the 1st, 9th, 17th, 25th, and 32nd of the 32 decoded 64b/66b blocks from the corresponding erred FEC block.
Reserved	17	0b	Reserved.
FEC_N_CNT	19:18	00b	Good Parity Block Count. Indicates the number of good parity blocks required for block lock. 00b = 4 good blocks 01b = 2 good blocks 10b = 5 good blocks 11b = 7 good blocks
FEC_M_CNT	21:20	00b	Bad Parity Block Count. Indicates the number of bad parity blocks required for loss of block lock. 00b = 8 errors 01b = 4 errors 10b = 12 errors 11b =-15 errors
FEC_LOOSE_MODE	22	0b	Enables FEC Loose Mode 0b = All errors counted. 1b = Correctable errors are not counted.

Field	Bit(s)	Init Val	Description
FEC_RX_SWAP	23	0b	FEC Rx Bit Order Swap. Swaps the bit order of the FEC_RX inputs. Swaps both *din* and sync_in bit order.
FEC_TX_SWAP	24	0b	FEC Tx Bit Order Swap. Swaps the bit order of the FEC_TX inputs. Swaps both *din* and *sync_in* bit order.
Reserved	25	0b	Reserved.
SLIPASS	26	0b	Loss of Sync (frame_align) Idle Pass-Through Select. 0b = LF passed to XGMII output when loss of sync. 1b = Decoder output data passed to XGMII output when loss of sync.
SSYNC	27	0b	Rx Block Lock Override. Once block lock sync has been acquired on the Rx input, Rx input remains in block lock sync regardless of Rx input data.
Reserved	28	0b	Reserved.
Reserved	31:29	0x0	Reserved.

8.2.3.22.29 KR PCS Status Register — KRPCSS (0x042E4; RO)

Field	Bit(s)	Init Val	Description
Reserved	2:0	0x0	Reserved. Write 0 ignore read.
ERRCNT_BLK	10:3	0x0	Rx Decoder Error Counter. This counter does not rollover and holds its value until it is read if it reaches its maximum value. This count is cleared when this register is read.
BERBAD_CNTR	16:11	0x0	BER Bad Counter (count cleared on register read) Field indicates number of times BER_BAD state was entered.
RX_FIFO_ERR_LH	17	0b	Elastic Buffer Error (latched high, clear on read). 0b = No Rx elastic buffer overflow or underflow condition since last read. 1b = Indicates that Rx elastic buffer overflow or underflow condition occurred since last read.
RX_LF_DET	18	0b	RX_LF Detect (latched high, clear on read). 0b = No local fault message was detected in the Rx path since last read. 1b = Indicates that the local fault message was detected in the Rx path since last read.
RX_FRM_ALIGN_ERR	19	0b	Frame Align Error (latched high, clear on read). 0b = No hi_ber or miss of frame_lock occurred since last read. 1b = Indicates that the hi_ber or miss of frame_lock occurred since last time the register was read.
BLKLCK	20	0b	Rx Block Lock Status bit (latched low, set on read). 0b = Link lost block lock since last register read. 1b = Indicates that the link has remained in the block lock state since the last read of this register.



Field	Bit(s)	Init Val	Description
HBER_STS	21	0b	Rx High Bit Error Rate Status bit (latched high, clear on read). 0b = Link has not been in high BER state since previous read. 1b = Indicates that the link has been in the high BER state since the last time the register was read.
RX_LF_DET	22	0b	RX_LF Detect (latched high, clear on read). 0b = No local fault message was detected in the Rx path. 1b = Indicates that the local fault message was detected in the Rx path.
LNK_STS	23	0b	Rx Link Status (latched low, set on read). 0b = Indicates that the link has been lost since the last time the bit was read. 1b = No loss of link since last time bit was read.
RX_UNDERFLOW	24	0b	Rx Underflow Status (latched high, clear on read). 0b = No underflow condition in rx_fifo. 1b = Indicates that the rx_fifo has reached the underflow condition and data might have been lost/corrupted.
RX_OVERFLOW	25	0b	Rx Overflow Status (latched high, clear on read). 0b = No overflow condition in rx_fifo. 1b = Indicates that the rx_fifo has reached the overflow condition and data might have been lost or corrupted.
RX_FIFO_ERR	26	0b	Rx Elastic Buffer Error 0b = No elastic buffer error. 1b = Indicates that Rx elastic buffer is currently in the overflow or underflow condition. This bit is not latched and is asserted only when the FIFO is in the overflow or underflow condition.
RX_DATA_VALID	27	1b	Data Valid Status (latched low, set on read). This bit indicates that the rx_fifo has not experienced an overflow or underflow since the last time this register was read.
TX_UNDERFLOW	28	0b	Tx Underflow Status (latched high, clear on read). This bit indicates that the tx_fifo has reached the underflow condition and data might have been lost/corrupted.
TX_OVERFLOW	29	0b	Tx Overflow Status (latched high, clear on read). This bit indicates that the tx_fifo has reached the overflow condition and data might have been lost/corrupted.
TX_FIFO_ERR	30	0b	Unlatched FIFO Error Status. This bit indicates that the tx_fifo has reached the overflow or underflow condition and data might have been lost / corrupted. This bit is not latched and is only asserted while the FIFO is in the overflow or underflow condition.
TX_DATA_VALID	31	1b	Data Valid Status (latched low, set on read). 0b = tx_fifo has experienced an overflow or underflow since the last time this register was read. 1b = tx_fifo has not experienced an overflow or underflow since the last time this register was read.

8.2.3.22.30 FEC Status 1 Register — FECS1 (0x042E8; RC)

Field	Bit(s)	Init Val	Description
FEC_CR_OUT	31:0	0x0	FEC Correctable Error Counter. The FECS1 counts the correctable FEC data blocks, detected and corrected by the FEC Rx logic.

8.2.3.22.31 FEC Status 2 Register — FECS2 (0x042EC; RC)

Field	Bit(s)	Init Val	Description
FEC_UNCR_OUT	31:0	0x0	FEC Uncorrectable Error Counter. The FECS2 counts the bad uncorrectable FEC data blocks, detected by the FEC Rx logic.

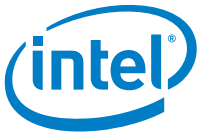
8.2.3.22.32 Core Analog Configuration Register — CoreCTL (0x014F00; RW)

Field	Bit(s)	Init Val	Description
Data	7:0	0x0	Data to Core Analog Registers. Data is ignored when bit 16 is set.
Address	15:8	0x0	Address to Core Analog Registers.
Latch address	16	0b	0b = Normal write operation. 1b = Latch this address for the next read transaction. Data is ignored and is not written on this transaction.
Reserved	31:17	0x0	Reserved.

Reading the Core registers must be done in two steps:

1. Send a Write command with bit 16 set, and the desired reading offset in the *Address* field (bits [15:8]).
2. Send a Read command to CoreCTL. The returned data is from the indirect address in the Core register space, which was provided in step (1).

To configure (write) registers in the Core block, the driver should write the proper address to CoreCTL.Address and data written to CoreCTL.Data.



8.2.3.22.33 Core Common Configuration Register — SMADARCTL (0x014F10; RW)

Field	Bit(s)	Init Val	Description
Data	7:0	0b	Data to Core Analog Registers. Data is ignored when bit 16 is set.
Address	15:8	0x0	Address to Core Analog Registers.
Latch address	16	0b	0b = Normal write operation. 1b = Latch this address for the next read transaction. Data is ignored and is not written on this transaction.
Reserved	31:17	0x0	Reserved.

Reading the Smadar registers must be done in two steps:

1. Send a Write command with bit 16 set, and the desired reading offset in the *Address* field (bits [15:8]).
2. Send a Read command to SMADARCTL. The returned data is from the indirect address in the Core register space, which was provided in step (1).

To configure (write) registers in the Smadar block, the driver should write the proper address to SMADARCTL.Address and data written to SMADARCTL.Data.

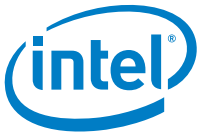
8.2.3.22.34 MAC Flow Control Register — MFLCN (0x04294; RW)

Field	Bit(s)	Init Val	Description
PMCF	0	0b	Pass MAC Control Frames. Filter out unrecognizable pause (flow control opcode doesn't match) and other control frames. 0b = Filter unrecognizable pause frames. 1b = Pass/forward unrecognizable pause frames.
DPF	1	0b	Discard Pause Frame When set to 0b, pause frames are sent to the host. Setting this bit to 1b causes pause frames to be discarded only when *RFCE* or *RPFCE* are set to 1b. If both *RFCE* and *RPFCE* are set to 0b, this bit has no effect on incoming pause frames.
RPFCE	2	0b	Receive Priority Flow Control Enable**.** Indicates that the 82599 responds to receiving PFC packets. If auto-negotiation is enabled, this bit should be set by software to the negotiated flow control value. *Note:* PFC should be enabled in DCB mode only. *Note:* Receive PFC and receive link flow control are mutually exclusive and programmers should not configure both of them to be enabled at the same time. *Note:* This bit should not be set if bit 3 is set.

Field	Bit(s)	Init Val	Description
RFCE	3	0b	Receive Flow Control Enable Indicates that the 82599 responds to the reception of link flow control packets. If auto-negotiation is enabled, this bit should be set by software to the negotiated flow control value. *Note:* This bit should not be set if bit 2 is set.
Reserved	31:4	0x0	Reserved.

8.2.3.22.35 SGMII Control Register — SGMIIC (0x04314; RW)

Field	Bit(s)	Init Val	Description
SRXRASSMP	3:0	0x0	Shift Rx Rate-Adapt Single Data Sampling. This value determines the sampling point of the sampled received data in the fast domain by the fast clock relative to the slow clock.
SRXRARSMP	7:4	0x0	Shift Rx Rate-Adapt Replicated Data Sampling. This value determines the sampling point of the received replicated data in the fast domain by the fast clock.
STXRASMP	11:8	0x0	Shift Tx Rate-Adapt Sampling. This value determines the sampling point of the transmitted data in the slow domain by the fast clock.
ANSFLU100	12	0b	AN SGMII Force Link Up 100 Mb/s. 0b = Normal mode. 1b = PGS_1G forced to 100 Mb/s link. This setting forces the PCS_1G Link_Ok indication and forced the 100 Mb/s speed indication toward the auto-negotiation ARB state machine regardless of the PCS_1G status.
ANSBYP	13	0b	AN SGMII Bypass. I f this bit is set, the IDLE detect state is bypassed during auto-negotiation (Clause 37) in SGMII mode. This reduces the acknowledge time in SGMII mode.
ANSTRIG	14	0b	AN SGMII Trigger. If this bit is set, auto-negotiation (Clause 37) is not automatically triggered in SGMII mode even if SYNC fails. Auto-negotiation is triggered only in response to PHY messages or by a manual setting like changing auto-negotiation *Enable*/*Restart* bits.
ANSLNKTMR	15	0b	AN SGMII Link-Timer (Configure the SGMII Link Timer). 0b = 1.6 ms 1b = 3.2 ms
Reserved	16	0b	Reserved.
ANIGNRRXRF	17	0b	Auto-Negotiation Ignore Received RF Field. 0b = If the received page contains RF != 00b, don't set link_up indication. 1b = Ignore from the received RF field content.
Reserved	31:18	0x0	Reserved.



8.2.3.23 Statistic Registers

General notes:

- All statistics registers are cleared on read. In addition, they stick at 0xFF...F when the maximum value is reached.
- For the receive statistics it should be noted that a packet is indicated as received if it passes the device filters and is placed into the packet buffer memory. A packet does not have to be DMA'd to host memory in order to be counted as received.
- Due to divergent paths between interrupt-generation and logging of relevant statistics counts, it might be possible to generate an interrupt to the system for a noteworthy event prior to the associated statistics count actually being incremented. This is extremely unlikely due to expected delays associated with the system interrupt-collection and ISR delay, but might be an explanation for interrupt statistics values that do not quite make sense. Hardware guarantees that any event noteworthy of inclusion in a statistics count is reflected in the appropriate count within 1 µs; a small time-delay prior to reading the statistics is required to avoid a potential mismatch between an interrupt and its cause.
- If RSC is enabled, statistics are collected before RSC is applied to the packets.
- If TSO is enabled, statistics are collected after segmentation.
- All byte (octet) counters composed of two registers can be fetched by two consecutive 32-bit accesses while reading the low 32-bit register first or a single 64-bit access.
- All receive statistic counters count the packets and bytes before coalescing by the RSC logic or FCoE DDP logic.
- All receive statistic counters in the filter unit (listed as follows) include also packets that might be dropped by the packet buffer or receive DMA. Same comment is valid for the byte counters associated with these packet counters: PRC64, PRC127, PRC255, PRC511, PRC1023, PRC1522, BPRC, MPRC, GPRC, RXNFGPC, RUC and ROC

8.2.3.23.1 CRC Error Count — CRCERRS (0x04000; RC)

Field	Bit(s)	Init Val	Description
CEC	31:0	0x0	CRC Error Count. Counts the number of receive packets with CRC errors. In order for a packet to be counted in this register, it must be 64 bytes or greater (from <Destination Address> through <CRC>, inclusively) in length. This register counts all packets received, regardless of L2 filtering and receive enablement.

8.2.3.23.2 Illegal Byte Error Count — ILLERRC (0x04004; RC)

Field	Bit(s)	Init Val	Description
IBEC	31:0	0x0	Illegal Byte Error Count. Counts the number of receive packets with illegal bytes errors (such as there is an illegal symbol in the packet). This registers counts all packets received, regardless of L2 filtering and receive enablement.

8.2.3.23.3 Error Byte Packet Count — ERRBC (0x04008; RC)

Field	Bit(s)	Init Val	Description
EBC	31:0	0x0	Error Byte Count. Counts the number of receive packets with error bytes (such as there is an error symbol in the packet). This registers counts all packets received, regardless of L2 filtering and receive enablement.

8.2.3.23.4 Rx Missed Packets Count — RXMPC[n] (0x03FA0 + 4*n, n=0...7; RC) DBU-Rx

Note: This is a RO register only.

8.2.3.23.5 MAC Local Fault Count — MLFC (0x04034; RC)

Field	Bit(s)	Init Val	Description
MLFC	31:0	0x0	Number of faults in the local MAC. This register is valid only when the link speed is 10 Gb/s.

8.2.3.23.6 MAC Remote Fault Count — MRFC (0x04038; RC)

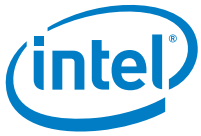
Field	Bit(s)	Init Val	Description
MRFC	31:0	0x0	Number of faults in the remote MAC. This register is valid only when the link speed is 10 Gb/s.

8.2.3.23.7 Receive Length Error Count — RLEC (0x04040; RC)

Field	Bit(s)	Init Val	Description
RLEC	31:0	0x0	Number of packets with receive length errors. A length error occurs if an incoming packet length field in the MAC header doesn't match the packet length. To enable the receive length error count, the HLREG.RXLNGTHERREN bit needs to be set to 1b. This registers counts all packets received, regardless of L2 filtering and receive enablement.

8.2.3.23.8 Switch Security Violation Packet Count — SSVPC (0x08780; RC)

Field	Bit(s)	Init Val	Description
SSVPC	31:0	0x0	Switch Security Violation Packet Count. This register counts Tx packets dropped due to switch security violations such as SA or VLAN anti-spoof filtering or a packet that has (inner) VLAN that contradicts with PFVMVIR register definitions. Valid only in VMDq or IOV mode.



8.2.3.23.9 Link XON Transmitted Count — LXONTXC (0x03F60; RC)

Note: This is a RO register only.

8.2.3.23.10 Link XON Received Count — LXONRXCNT (0x041A4; RC)

Note: This counter is similar to LXONRXC in the 82598 that was in address 0x0CF60.

Field	Bit(s)	Init Val	Description
XONRXC	15:0	0	Number of XON packets received. Sticks to 0xFFFF. XON packets can use the global address, or the station address. This register counts any XON packet whether it is a legacy XON or a priority XON. Each XON packet is counted once even if it is designated to a few priorities. If a priority FC packet contains both XOFF and XON, only the LXOFFRXCNT counter is incremented.
Reserved	31:16	0	Reserved.

8.2.3.23.11 Link XOFF Transmitted Count — LXOFFTXC (0x03F68; RC)

Note: This is a RO register only.

8.2.3.23.12 Link XOFF Received Count — LXOFFRXCNT (0x041A8; RC)

Note: This counter is similar to LXOFFRXC in the 82598 that was in address 0x0CF68.

Field	Bit(s)	Init Val	Description
XOFFRXC	15:0	0x0	Number of XOFF packets received. Sticks to 0xFFFF. XOFF packets can use the global address or the station address. This register counts any XOFF packet whether it is a legacy XOFF or a priority XOFF. Each XOFF packet is counted once even if it is designated to a few priorities. If a priority FC packet contains both XOFF and XON, only this counter is incremented.
Reserved	31:16	0x0	Reserved.

8.2.3.23.13 Priority XON Transmitted Count — PXONTXC[n] (0x03F00 + 4*n, n=0...7; RC)

Note: This is a RO register only.

8.2.3.23.14 Priority XON Received Count — PXONRXCNT[n] (0x04140 + 4*n, n=0...7; RC)

Note: These counters are similar to PXONRXC[n] in the 82598 that were in address 0x0CF00 + 4*n, n=0...7.

Field	Bit(s)	Init Val	Description
XONRXC	15:0	0x0	Number of XON packets received per UP. Sticks to 0xFFFF.
Reserved	31:16	0x0	Reserved.

8.2.3.23.15 Priority XOFF Transmitted Count — PXOFFTXCNT[n] (0x03F20 + 4*n, n=0...7; RC)

Note: This is a RO register only.

8.2.3.23.16 Priority XOFF Received Count — PXOFFRXCNT[n] (0x04160 + 4*n, n=0...7; RC)

Note: These counters are similar to PXOFFRXC[n] in the 82598 that were in address 0x0CF20 + 4*n, n=0...7.

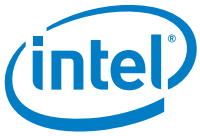
Field	Bit(s)	Init Val	Description
XOFFRXC	15:0	0x0	Number of XOFF packets received per UP. Sticks to 0xFFFF.
Reserved	31:16	0x0	Reserved.

8.2.3.23.17 Priority XON to XOFF Count — PXON2OFFCNT[n] (0x03240 + 4*n, n=0...7; RC)

Note: This is a RO register only.

8.2.3.23.18 Packets Received [64 Bytes] Count — PRC64 (0x0405C; RW)

Field	Bit(s)	Init Val	Description
PRC64	31:0	0x0	Number of good packets received that are 64 bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets.



8.2.3.23.19 Packets Received [65–127 Bytes] Count — PRC127 (0x04060; RW)

Field	Bit(s)	Init Val	Description
PRC127	31:0	0x0	Number of packets received that are 65-127 bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets.

8.2.3.23.20 Packets Received [128–255 Bytes] Count — PRC255 (0x04064; RW)

Field	Bit(s)	Init Val	Description
PRC255	31:0	0x0	Number of packets received that are 128-255 bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets.

8.2.3.23.21 Packets Received [256–511 Bytes] Count — PRC511 (0x04068; RW)

Field	Bit(s)	Init Val	Description
PRC511	31:0	0x0	Number of packets received that are 256-511 bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets.

8.2.3.23.22 Packets Received [512–1023 Bytes] Count — PRC1023 (0x0406C; RW)

Field	Bit(s)	Init Val	Description
PRC1023	31:0	0x0	Number of packets received that are 512-1023 bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets.

8.2.3.23.23 Packets Received [1024 to Max Bytes] Count — PRC1522 (0x04070; RW)

Field	Bit(s)	Init Val	Description
PRC1522	31:0	0x0	Number of packets received that are 1024-max bytes in length (from <Destination Address> through <CRC>, inclusively). This registers counts packets that pass L2 filtering regardless on receive enablement and does not include received flow control packets. The maximum is dependent on the current receiver configuration and the type of packet being received. If a packet is counted in receive oversized count, it is not counted in this register (see Section 8.2.3.23.52). Due to changes in the standard for maximum frame size for VLAN tagged frames in 802.3, this device accepts packets that have a maximum length of 1522 bytes. The RMON statistics associated with this range has been extended to count 1522 byte long packets.

8.2.3.23.24 Broadcast Packets Received Count — BPRC (0x04078; RO)

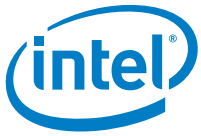
Field	Bit(s)	Init Val	Description
BPRC	31:0	0x0	Number of good (non-erred) broadcast packets received. This register does not count received broadcast packets when the broadcast address filter is disabled. The counter counts packets regardless on receive enablement.

8.2.3.23.25 Multicast Packets Received Count — MPRC (0x0407C; RO)

Field	Bit(s)	Init Val	Description
MPRC	31:0	0x0	Number of good (non-erred) multicast packets received that pass L2 filtering (excluding broadcast packets). This register does not count received flow control packets. This registers counts packets regardless on receive enablement.

8.2.3.23.26 Good Packets Received Count — GPRC (0x04074; RO)

Field	Bit(s)	Init Val	Description
GPRC	31:0	0x0	Number of good (non-erred) Rx packets (from the network) that pass L2 filtering and has a legal length as defined by *LongPacketEnable*. This registers counts packets regardless on receive enablement.



8.2.3.23.27 Good Octets Received Count Low — GORCL (0x04088; RC)

Field	Bit(s)	Init Val	Description
CNT_L	31:0	0x0	Lower 32 bits of the good octets received counter. The GORCL and GORCH registers make up a logical 36-bit octet counter of the packets counted by GPRC. This register includes bytes received in a packet from the <Destination Address> field through the <CRC> field, inclusively.

8.2.3.23.28 Good Octets Received Count High — GORCH (0x0408C; RC)

Field	Bit(s)	Init Val	Description
CNT_H	3:0	0x0	Higher four bits of the good octets received counter.
Reserved	31:4	0x0	Reserved

8.2.3.23.29 Good Rx Non-Filtered Packet Counter — RXNFGPC (0x041B0; RC)

Field	Bit(s)	Init Val	Description
GPC	31:0	0x0	Number of good (non-erred with legal length) Rx packets (from the network) regardless of packet filtering and receive enablement.

8.2.3.23.30 Good Rx Non-Filter Byte Counter Low — RXNFGBCL (0x041B4; RC)

Field	Bit(s)	Init Val	Description
BCL	31:0	0x0	Low 32 bits of the 36-bit byte counter of good (non-erred) Rx packets that match RXNFGPC. The counter counts all bytes from <Destination Address> field through the <CRC> field, inclusively.

8.2.3.23.31 Good Rx Non-Filter Byte Counter High — RXNFGBCH (0x041B8; RC)

Field	Bit(s)	Init Val	Description
BCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated with RXFGBCL.
Reserved	31:4	0x0	Reserved

8.2.3.23.32 DMA Good Rx Packet Counter — RXDGPC (0x02F50; RC)

Field	Bit(s)	Init Val	Description
GPC	31:0	0x0	Number of good (non-erred) Rx packets from the network posted to the host memory. In case of packet replication (or mirrored), the counter counts each packet only once. The counter counts packets directed to ALL Rx queues or specific Rx queues as defined by the RXDSTATCTRL register.

8.2.3.23.33 DMA Good Rx Byte Counter Low — RXDGBCL (0x02F54; RC)

Field	Bit(s)	Init Val	Description
GBCL	31:0	0x0	Lower 32 bits of the 36-bit byte counter of good (non-erred) Rx packets that match RXDGPC. The counter counts all bytes posted to the host before VLAN strip. Furthermore, bytes of RSC and FCoE are counted before coalescing or DDP.

8.2.3.23.34 DMA Good Rx Byte Counter High — RXDGBCH (0x02F58; RC)

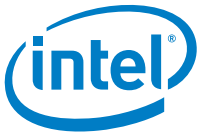
Field	Bit(s)	Init Val	Description
GBCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated with RXDGBCL.
Reserved	31:4	0x0	Reserved.

8.2.3.23.35 DMA Duplicated Good Rx Packet Counter — RXDDPC (0x02F5C; RC)

Field	Bit(s)	Init Val	Description
GPC	31:0	0x0	Number of replicated or mirrored packets that meet the RXDGPC conditions. The sum of RXDDPC and RXDGPC is the total good (non-erred) Rx packets from the network that are posted to the host. *Note:* The counter counts packets directed to ALL Rx queues or specific Rx queues as defined by the RXDSTATCTRL register.

8.2.3.23.36 DMA Duplicated Good Rx Byte Counter Low — RXDDBCL (0x02F60; RC)

Field	Bit(s)	Init Val	Description
GBCL	31:0	0x0	Lower 32 bits of the 36-bit byte counter of good (non-erred) Rx packets that match RXDDPC. The counter counts all bytes posted to the host before VLAN strip. Furthermore, bytes of RSC and FCoE are counted before coalescing or DDP.



8.2.3.23.37 DMA Duplicated Good Rx Byte Counter High — RXDDBCH (0x02F64; RC)

Field	Bit(s)	Init Val	Description
GBCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated with RXDDBCL.
Reserved	31:4	0x0	Reserved.

8.2.3.23.38 DMA Good Rx LPBK Packet Counter — RXLPBKPC (0x02F68; RC)

Field	Bit(s)	Init Val	Description
GPC	31:0	0x0	Number of good (non-erred) Rx packets from a local VM posted to the host memory. In case of packet replication (or mirrored), the counter counts each packet only once. The counter counts packets directed to ALL Rx queues or specific Rx queues as defined by the RXDSTATCTRL register. The counter is not affected by RSC and FCoE DDP since both functions are not supported for LPBK traffic.

8.2.3.23.39 DMA Good Rx LPBK Byte Counter Low — RXLPBKBCL (0x02F6C; RC)

Field	Bit(s)	Init Val	Description
GBCL	31:0	0x0	Lower 32 bits of the 36-bit byte counter of good (non-erred) Rx packets that match RXLPBKPC. The counter counts all bytes posted to the host before VLAN strip. Furthermore, bytes of RSC and FCoE are counted before coalescing or DDP.

8.2.3.23.40 DMA Good Rx LPBK Byte Counter High — RXLPBKBCH (0x02F70; RC)

Field	Bit(s)	Init Val	Description
GBCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated with RXLPBKBCL.
Reserved	31:4	0x0	Reserved.

8.2.3.23.41 DMA Duplicated Good Rx LPBK Packet Counter — RXDLPBKPC (0x02F74; RC)

Field	Bit(s)	Init Val	Description
GPC	31:0	0x0	Number of replicated or mirrored packets that meet the RXLPBKPC conditions. The sum of RXDLPBKPC and RXLPBKPC is the total good (non-erred) Rx packets from a local VM posted to the host. *Note:* The counter counts packets directed to ALL Rx queues or specific Rx queues as defined by the RXDSTATCTRL register.

8.2.3.23.42 DMA Duplicated Good Rx LPBK Byte Counter Low — RXDLPBKBCL (0x02F78; RC)

Field	Bit(s)	Init Val	Description
GBCL	31:0	0x0	Low 32 bits of the 36-bit byte counter of good (non-erred) Rx packets that match RXDLPBKPC. The counter counts all bytes posted to the host before VLAN strip. Furthermore, bytes of RSC and FCoE are counted before coalescing or DDP.

8.2.3.23.43 DMA Duplicated Good Rx LPBK Byte Counter High — RXDLPBKBCH (0x02F7C; RC)

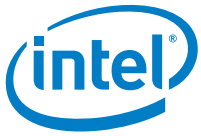
Field	Bit(s)	Init Val	Description
GBCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated with RXDLPBKBCL.
Reserved	31:4	0x0	Reserved.

8.2.3.23.44 Good Packets Transmitted Count — GPTC (0x04080; RC)

Field	Bit(s)	Init Val	Description
GPTC	31:0	0x0	Number of good packets transmitted. This register counts good (non-erred) transmitted packets. A good transmit packet is considered one that is 64 or more bytes (from <Destination Address> through <CRC>, inclusively) in length. The register counts transmitted clear packets, secure packets and FC packets.

8.2.3.23.45 Good Octets Transmitted Count Low — GOTCL (0x04090; RC)

Field	Bit(s)	Init Val	Description
CNT_L	31:0	0x0	Lower 32 bits of the good octets transmitted counter. See complete description in Section 8.2.3.23.46.



8.2.3.23.46 Good Octets Transmitted Count High — GOTCH (0x04094; RC)

Field	Bit(s)	Init Val	Description
CNT_H	3:0	0x0	Higher four bits of the good octets transmitted counter. The GOTCL and GOTCH registers make up a logical 36-bit counter of successfully transmitted octets (in packets counted by GPTC). This register includes transmitted bytes in a packet from the <Destination Address> field through the <CRC> field, inclusively.
Reserved	31:4	0x0	Reserved.

8.2.3.23.47 DMA Good Tx Packet Counter – TXDGPC (0x087A0; RC)

Field	Bit(s)	Init Val	Description
GPTC	31:0	0x0	Number of Tx packets from the host memory. This counter includes packets that are transmitted to the external network as well as packets that are transmitted only to local VMs. The later case can happen only in VT mode when the local switch is enabled. Packets dropped due to anti-spoofing filtering or VLAN tag validation (as described in Section 7.10.3.9.2) are not counted.

8.2.3.23.48 DMA Good Tx Byte Counter Low – TXDGBCL (0x087A4; RC)

Field	Bit(s)	Init Val	Description
BCL	31:0	0x0	Lower 32 bits of the 36-bit byte counter of the Tx packets that match TXDGPC. The counter counts all bytes posted by the host AND the VLAN (if bytes were added by hardware).

8.2.3.23.49 DMA Good Tx Byte Counter High – TXDGBCH (0x087A8; RC)

Field	Bit(s)	Init Val	Description
BCH	3:0	0x0	Higher four bits of the 36-bit byte counter associated to TXDGBCL.
Reserved	31:4	0x0	Reserved.

8.2.3.23.50 Receive Undersize Count — RUC (0x040A4; RC)

Field	Bit(s)	Init Val	Description
RUC	31:0	0x0	Receive Undersize Error. This register counts the number of received frames that are shorter than minimum size (64 bytes from <Destination Address> through <CRC>, inclusively), and had a valid CRC. This register counts packets regardless of L2 filtering and receive enablement.

8.2.3.23.51 Receive Fragment Count — RFC (0x040A8; RC)

Field	Bit(s)	Init Val	Description
RFC	31:0	0x0	Number of receive fragment errors (frame shorted than 64 bytes from <Destination Address> through <CRC>, inclusively) that have bad CRC (this is slightly different from the Receive Undersize Count register). This register counts packets regardless of L2 filtering and receive enablement.

8.2.3.23.52 Receive Oversize Count — ROC (0x040AC; RC)

Field	Bit(s)	Init Val	Description
ROC	31:0	0x0	Receive Oversize Error. This register counts the number of received frames that are longer than maximum size as defined by MAXFRS.MFS (from <Destination Address> through <CRC>, inclusively) and have valid CRC. This register counts packets regardless of L2 filtering and receive enablement.

8.2.3.23.53 Receive Jabber Count — RJC (0x040B0; RC)

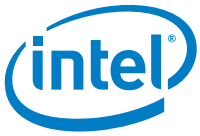
Field	Bit(s)	Init Val	Description
RJC	31:0	0x0	Number of receive jabber errors. This register counts the number of received packets that are greater than maximum size and have bad CRC (this is slightly different from the Receive Oversize Count register). The packets length is counted from <Destination Address> through <CRC>, inclusively. This register counts packets regardless of L2 filtering and receive enablement.

8.2.3.23.54 Management Packets Received Count — MNGPRC (0x040B4; RO)

Field	Bit(s)	Init Val	Description
MNGPRC	31:0	0x0	Number of management packets received. This register counts the total number of packets received that pass the management filters. Management packets include RMCP and ARP packets. Any packets with errors are not counted, except for the packets that are dropped because the management receive FIFO is full are counted.

8.2.3.23.55 Management Packets Dropped Count — MNGPDC (0x040B8; RO)

Field	Bit(s)	Init Val	Description
MPDC	31:0	0	Number of management packets dropped. This register counts the total number of packets received that pass the management filters and then are dropped because the management receive FIFO is full. Management packets include any packet directed to the manageability console (such as RMCP and ARP packets).



8.2.3.23.56 Management Packets Transmitted Count — MNGPTC (0x0CF90; RO)

Note: This is a RO register only.

8.2.3.23.57 Total Octets Received Low — TORL (0x040C0; RC)

Field	Bit(s)	Init Val	Description
CNT_L	31:0	0x0	Lower 32 bits of the total octets received counter. See complete description in Section 8.2.3.23.58.

8.2.3.23.58 Total Octets Received High — TORH (0x040C4; RC)

Field	Bit(s)	Init Val	Description
CNT_H	3:0	0x0	Higher four bits of the total octets received counter. The TORL and TORH registers make up a logical 36-bit counter of the total received octets (in the packets counted by the TPR counter). This register includes bytes received in a packet from the <Destination Address> field through the <CRC> field, inclusively.
Reserved	31:4	0x0	Reserved.

8.2.3.23.59 Total Packets Received — TPR (0x040D0; RC)

Field	Bit(s)	Init Val	Description
TPR	31:0	0x0	Number of all packets received. This register counts the total number of all packets received. All packets received are counted in this register, regardless of their length, whether they are erred, regardless on L2 filtering and receive enablement but excluding flow control packets. TPR can count packets interrupted by link disconnect although they have a CRC error.

8.2.3.23.60 Total Packets Transmitted — TPT (0x040D4; RC)

Field	Bit(s)	Init Val	Description
TPT	31:0	0x0	Number of all packets transmitted. This register counts the total number of all packets transmitted. This register counts all packets, including standard packets, secure packets, FC packets, and manageability packets.

8.2.3.23.61 Packets Transmitted (64 Bytes) Count — PTC64 (0x040D8; RC)

Field	Bit(s)	Init Val	Description
PTC64	31:0	0x0	Number of packets transmitted that are 64 bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, FC packets, and manageability packets.

8.2.3.23.62 Packets Transmitted [65–127 Bytes] Count — PTC127 (0x040DC; RC)

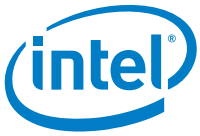
Field	Bit(s)	Init Val	Description
PTC127	31:0	0x0	Number of packets transmitted that are 65-127 bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, and manageability packets.

8.2.3.23.63 Packets Transmitted [128–255 Bytes] Count — PTC255 (0x040E0; RC)

Field	Bit(s)	Init Val	Description
PTC255	31:0	0x0	Number of packets transmitted that are 128-255 bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, and manageability packets.

8.2.3.23.64 Packets Transmitted [256–511 Bytes] Count — PTC511 (0x040E4; RC)

Field	Bit(s)	Init Val	Description
PTC511	31:0	0x0	Number of packets transmitted that are 256-511 bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, and manageability packets.



8.2.3.23.65 Packets Transmitted [512–1023 Bytes] Count — PTC1023 (0x040E8; RC)

Field	Bit(s)	Init Val	Description
PTC1023	31:0	0x0	Number of packets transmitted that are 512-1023 bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, and manageability packets.

8.2.3.23.66 Packets Transmitted [Greater Than 1024 Bytes] Count — PTC1522 (0x040EC; RC)

Field	Bit(s)	Init Val	Description
PTC1522	31:0	0x0	Number of packets transmitted that are 1024 or more bytes in length (from <Destination Address> through <CRC>, inclusively). This register counts all packets, including standard packets, secure packets, and manageability packets. Due to changes in the standard for maximum frame size for VLAN tagged frames in 802.3, this device transmits packets that have a maximum length of 1522 bytes. The RMON statistics associated with this range has been extended to count 1522 byte long packets. This register counts all packets, including standard and secure packets.

8.2.3.23.67 Multicast Packets Transmitted Count — MPTC (0x040F0; RC)

Field	Bit(s)	Init Val	Description
MPTC	31:0	0x0	Number of multicast packets transmitted. This register counts the number of multicast packets transmitted. This register counts all packets, including standard packets, secure packets, FC packets and manageability packets.

8.2.3.23.68 Broadcast Packets Transmitted Count — BPTC (0x040F4; RC)

Field	Bit(s)	Init Val	Description
BPTC	31:0	0x0	Number of broadcast packets transmitted count. This register counts all packets, including standard packets, secure packets, FC packets and manageability packets

8.2.3.23.69 MAC Short Packet Discard Count — MSPDC (0x04010; RC)

Field	Bit(s)	Init Val	Description
MSPDC	31:0	0x0	Number of MAC short packet discard packets received.

8.2.3.23.70 XSUM Error Count — XEC (0x04120; RC)

Field	Bit(s)	Init Val	Description
XEC	31:0	0x0	Number of receive IPv4, TCP, UDP or SCTP XSUM errors.

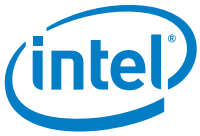
XSUM errors are not counted when a packet has any MAC error (CRC, length, under-size, over-size, byte error or symbol error).

8.2.3.23.71 Receive Queue Statistic Mapping Registers — RQSMR[n] (0x02300 + 4*n, n=0...31; RW)

These registers define the mapping of the receive queues to the per queue statistics. Several queues can be mapped to a single statistic register. Each statistic register counts the number of packets and bytes of all the queues that are mapped to that statistics. The registers counting Rx queue statistics are: QPRC, QBRC, and QPRDC.

Field	Bit(s)	Init Val	Description
Q_MAP[0]	3:0	0x0	For each register 'n', Q_MAP[0] defines the per queue statistic registers that are mapped to Rx queue '4*n+0'. (see examples that follow).
Reserved	7:4	0x0	Reserved.
Q_MAP[1]	11:8	0x0	For each register 'n', Q_MAP[1] defines the per queue statistic registers that are mapped to Rx queue '4*n+1'. (see examples that follow).
Reserved	15:12	0x0	Reserved.
Q_MAP[2]	19:16	0x0	For each register 'n', Q_MAP[2] defines the per queue statistic registers that are mapped to Rx queue '4*n+2'. (see examples that follow).
Reserved	23:20	0x0	Reserved.
Q_MAP[3]	27:24	0x0	For each register 'n', Q_MAP[3] defines the per queue statistic registers that are mapped to Rx queue '4*n+3'. (see examples that follow).
Reserved	31:28	0x0	Reserved.

For example, setting RQSMR[0].Q_MAP[0] to 3 maps Rx queue 0 to the counters QPRC[3], QBRC[3], and QPRDC[3]. Setting RQSMR[2].Q_MAP[1] to 5 maps Rx queue 9 to the QPRC[5], QBRC[5], and QPRDC[5].



8.2.3.23.72 Rx DMA Statistic Counter Control — RXDSTATCTRL (0x02F40; RW)

Field	Bit(s)	Init Val	Description
QSEL	4:0	0x0	The *Queue Select* field controls which Rx queues are considered for the DMA good Rx and DMA duplicated counters as follows: 00000b ... 01111b = The counters relates to the same queues that are directed to the QPRC[QSEL] counter as defined by the RQSMR[n] registers. 10000b = The counters relates to all Rx queues. All other values are reserved.
Reserved	31:5	0x0	Reserved.

8.2.3.23.73 Transmit Queue Statistic Mapping Registers — TQSM[n] (0x08600 + 4*n, n=0...31; RW)

These registers define the mapping of the transmit queues to the per queue statistics. Several queues can be mapped to a single statistic register. Each statistic register counts the number of packets and bytes of all the queues that are mapped to that statistics. The registers counting Tx queue statistics are: QPTC and QBTC.

Field	Bit(s)	Init Val	Description
Q_MAP[0]	3:0	0x0	For each register 'n', Q_MAP[0] defines the per queue statistic registers that are mapped to Tx queue '4*n+0'.
Reserved	7:4	0x0	Reserved.
Q_MAP[1]	11:8	0x0	For each register 'n', Q_MAP[1] defines the per queue statistic registers that are mapped to Tx queue '4*n+1'.
Reserved	15:12	0x0	Reserved.
Q_MAP[2]	19:16	0x0	For each register 'n', Q_MAP[2] defines the per queue statistic registers that are mapped to Tx queue '4*n+2'.
Reserved	23:20	0x0	Reserved.
Q_MAP[3]	27:24	0x0	For each register 'n', Q_MAP[3] defines the per queue statistic registers that are mapped to Tx queue '4*n+3'.
Reserved	31:28	0x0	Reserved.

8.2.3.23.74 Queue Packets Received Count — QPRC[n] (0x01030 + 0x40*n, n=0...15; RC)

Field	Bit(s)	Init Val	Description
PRC	31:0	0x0	Number of packets received for the queue. FCoE packets are counted in QRPC even if they are posted only to the DDP queue (with no traces in the legacy queue).

8.2.3.23.75 Queue Packets Received Drop Count — QPRDC[n] (0x01430 + 0x40*n, n=0...15; RC)

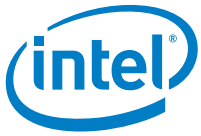
Field	Bit(s)	Init Val	Description
PRDC	31:0	0x0	Total number of receive packets dropped for the queue. Packets can be dropped for the following reasons: 1. Rx queue is disabled in the RXDCTL[n] register. 2. No free descriptors in the Rx queue while hardware is set to *Drop En* in the SRRCTL[n] register or in the PFQDE register.

8.2.3.23.76 Queue Bytes Received Count Low — QBRC_L[n] (0x01034 + 0x40*n, n=0...15; RC)

Field	Bit(s)	Init Val	Description
BRC_L	31:0	0x0	Lower 32 bits of the statistic counter. The QBRC_L[n] and QBRC_H[n] registers make up a logical 36-bit counter of received bytes that were posted to the programmed Rx queues of the packets counted by QPRC[n]. The counter counts all bytes posted to the host before VLAN strip. Furthermore, bytes of RSC and FCoE are counted before coalescing or DDP.

8.2.3.23.77 Queue Bytes Received Count High — QBRC_H[n] (0x01038 + 0x40*n, n=0...15; RC)

Field	Bit(s)	Init Val	Description
BRC_H	3:0	0x0	Higher four bits of the statistic counter described in QBRC_L.
Reserved	31:4	0x0	Reserved.



8.2.3.23.78 Queue Packets Transmitted Count — QPTC[n] (0x08680 + 0x4*n, n=0...15 / 0x06030 + 0x40*n, n=0...15; RC)

These registers are also mapped to 0x06030 to maintain compatibility with the 82598.

Field	Bit(s)	Init Val	Description
PTC	31:0	0x0	Number of packets transmitted for the queue. A packet is considered as transmitted if it is was forwarded to the MAC unit for transmission to the network and/or is accepted by the internal Tx to Rx switch enablement logic. Packets dropped due to anti-spoofing filtering or VLAN tag validation (as described in Section 7.10.3.9.2) are not counted.

8.2.3.23.79 Queue Bytes Transmitted Count Low — QBTC_L[n] (0x08700 + 0x8*n, n=0...15; RC)

Field	Bit(s)	Init Val	Description
BTC_L	31:0	0x0	Lower 32 bits of the statistic counter. The QBTC_L and QBTC_H registers make up a logical 36-bit counter of transmitted bytes of the packets counted by the matched QPTC counter. These registers count all bytes in the packets from the <Destination Address> field through the <CRC> field, inclusively. These registers must be accessed as two consecutive 32-bit entities while the QBTC_L register is read first, or a single 64-bit read cycle. Each register is read cleared. In addition, it sticks at 0xFF...F to avoid overflow.

8.2.3.23.80 Queue Bytes Transmitted Count High — QBTC_H[n] (0x08704 + 0x8*n, n=0...15; RC)

Field	Bit(s)	Init Val	Description
BTC_H	3:0	0x0	Higher four bits of the statistic counter described in QBTC_L.
Reserved	31:4	0x0	Reserved.

8.2.3.23.81 FC CRC Error Count — FCCRC (0x05118; RC)

Field	Bit(s)	Init Val	Description
CRC_CNT	15:0	0x0	FC CRC Count. Count the number of packets with good Ethernet CRC and bad FC CRC.
Reserve	31:16	N/A	Reserved.

8.2.3.23.82 FCoE Rx Packets Dropped Count — FCOERPDC (0x0241C; RC)

Field	Bit(s)	Init Val	Description
RPDC	31:0	0x0	Number of Rx packets dropped due to lack of descriptors.

8.2.3.23.83 FC Last Error Count — FCLAST (0x02424; RC)

Field	Bit(s)	Init Val	Description
Last_CNT	15:0	0x0	Number of packets received to valid FCoE contexts while their user buffers are exhausted.
Reserve	31:16	N/A	Reserved.

8.2.3.23.84 FCoE Packets Received Count — FCOEPRC (0x02428; RC)

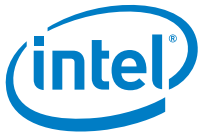
Field	Bit(s)	Init Val	Description
PRC	31:0	0x0	Number of FCoE packets posted to the host. In normal operation (no save bad frames) it equals to the number of good packets.

8.2.3.23.85 FCOE DWord Received Count — FCOEDWRC (0x0242C; RC)

Field	Bit(s)	Init Val	Description
DWRC	31:0	0x0	Number of DWords count in good received packets with no Ethernet CRC or FC CRC errors. The counter relates to FCoE packets starting at the FC header up to and including the FC CRC (it excludes Ethernet encapsulation).

8.2.3.23.86 FCoE Packets Transmitted Count — FCOEPTC (0x08784; RC)

Field	Bit(s)	Init Val	Description
PTC	31:0	0x0	Number of FCoE packets transmitted. *Note:* The counter does not include packets dropped due to anti-spoofing filtering or VLAN tag validation as described in Section 7.10.3.9.2. This rule is applicable if FCoE traffic is sent by a VF.



8.2.3.23.87 FCoE DWord Transmitted Count — FCOEDWTC (0x08788; RC)

Field	Bit(s)	Init Val	Description
DWTC	31:0	0x0	Number of DWords count in transmitted packets. The counter relates to FCoE packets starting at the FC header up to and including the FC CRC (it excludes Ethernet encapsulation).

8.2.3.24 Wake Up Control Registers

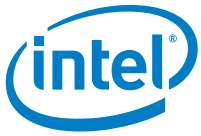
8.2.3.24.1 Wake Up Control Register — WUC (0x05800; RW)

Field	Bit(s)	Init Val	Description
Reserved	0	0b	Reserved .
PME_En	1	0b	PME_En. This bit is used by the driver to enable wakeup capabilities as programmed by the WUFC register. Wakeup is further gated by the PME_En bit of the PMCS register. *Note:* Setting the PME_En bit in the PMCSR register also sets this bit.
PME_Status (RO)	2	0b	PME_Status. This bit is set when the 82599 receives a wake-up event. It is the same as the PME_Status bit in the PMCSR. Writing a 1b to this bit clears it. The *PME_Status* bit in the PMCSR is also cleared.
Reserved	3	0b	Reserved.
WKEN	4	1b	WKEN This bit can be cleared to disable PE_WAKE_N pin de-assertion even if APM is enabled in the EEPROM. In this case, PMCSR wake-up status will be invalid. Refer to Section 5.3 for the correct way to enable APM with valid status. *Note:* This bit should not be cleared while in ACPI mode.
Reserved	31:5	0x0	Reserved.

The *PME_En* and *PME_Status* bits are reset when LAN_PWR_GOOD is 0b. When AUX_PWR=0b these bits are also reset by the assertion of PE_RST_N.

8.2.3.24.2 Wake Up Filter Control Register — WUFC (0x05808; RW)

Field	Bit(s)	Init Val	Description
LNKC	0	0b	Link Status Change Wake Up Enable.
MAG	1	0b	Magic Packet Wake Up Enable.
EX	2	0b	Directed Exact Wake Up Enable.
MC	3	0b	Directed Multicast Wake Up Enable. Setting this bit does not enable broadcast packets that are enabled by the *BC* bit in this register.
BC	4	0b	Broadcast Wake Up Enable.
ARP	5	0b	ARP/IPv4 Request Packet Wake Up Enable.
IPV4	6	0b	Directed IPv4 Packet Wake Up Enable.
IPV6	7	0b	Directed IPv6 Packet Wake Up Enable.



Field	Bit(s)	Init Val	Description
Reserved	14:8	0x0	Reserved.
NoTCO	15	0b	Ignore TCO Packets for TCO.
FLX0	16	0b	Flexible Filter 0 Enable.
FLX1	17	0b	Flexible Filter 1 Enable.
FLX2	18	0b	Flexible Filter 2 Enable.
FLX3	19	0b	Flexible Filter 3 Enable.
FLX4	20	0b	Flexible Filter 4 Enable.
FLX5	21	0b	Flexible Filter 5 Enable.
Reserved	31:22	0b	Reserved.

This register is used to enable each of the pre-defined and flexible filters for wake up support. A value of one means the filter is turned on, and a value of zero means the filter is turned off.

If the *NoTCO* bit is set, then any packet that passes the manageability packet filtering does not cause a wake up event even if it passes one of the wake up filters.

8.2.3.24.3 Wake Up Status Register — WUS (0x05810; RW1C)

Field	Bit(s)	Init Val	Description
Reserved	31:0	0x0	Reserved.

Note: This register is de-featured and software should not read it. To enable ACPI, this register must be cleared by writing 0x3F01FF.

8.2.3.24.4 IP Address Valid — IPAV (0x5838; RW)

The IP address valid indicates whether the IP addresses in the IP address table are valid:

Field	Bit(s)	Init Val	Description
V40	0	0b[1]	IPv4 Address 0 Valid.
V41	1	0b	IPv4 Address 1 Valid.
V42	2	0b	IPv4 Address 2 Valid.
V43	3	0b	IPv4 Address 3 Valid.
Reserved	15:4	0x0	Reserved

Field	Bit(s)	Init Val	Description
V60	16	0b	IPv6 Address 0 Valid.
Reserved	31:17	0x0	Reserved

1. Loaded from EEPROM

8.2.3.24.5 IPv4 Address Table — IP4AT[n] (0x05840 + 8*n, n = 0...3; RW)

4 x IPv4 addresses for ARP/IPv4 request packet and directed IPv4 packet wake up. IPv4[0] is loaded from MIPAF words in the EEPROM.

Field	Bit(s)	Init Val	Description
IPV4ADDR	31:0	X	IPv4 Address ‘n’, ‘n’ = 0...3.

8.2.3.24.6 IPv6 Address Table — IP6AT[n] (0x05880 + 4*n, n = 0...3; RW)

1 x IPv6 addresses for a neighbor discovery packet filtering and directed IPv6 packet wake up. According to the power management section; one Ipv6 address is supported and it is programmed in the Ipv6 Address Table (IP6AT)

Field	Bit(s)	Init Val	Description
IPV6ADDR	31:0	X	4 x Register IPv6 filter. Register ‘n’ contains bytes ‘4*n’ up to ‘4*n+3’ of the IPv6 address. LS byte of register ‘0’ is first on the wire.

8.2.3.24.7 Wake Up Packet Length — WUPL (0x05900; RO)

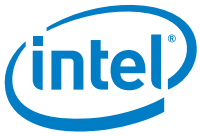
This register is de-featured and software should not access it (not read nor write)

8.2.3.24.8 Wake Up Packet Memory (128 Bytes) — WUPM[n] (0x05A00 + 4*n, n=0...31; RO)

This register is de-featured and software should not access it (not read nor write)

8.2.3.24.9 Flexible Host Filter Table Registers — FHFT (0x09000 — 0x093FC and 0x09800 — 0x099FC; RW)

Each of the six Flexible Host Filters Table (FHFT) registers contains a 128-byte pattern and a corresponding 128-bit mask array. If enabled, the first 128 bytes of the received packet are compared against the non-masked bytes in the FHFT register.



Each 128-byte filter is composed of 32 Dword entries, where each two Dwords are accompanied by an 8-bit mask, one bit per filter byte.

Note: The *Length* field must be eight byte-aligned. For filtering packets shorter than eight byte-aligned the values should be rounded up to the next eight byte-aligned value, hardware implementation compares eight bytes at a time so it should get extra zero masks (if needed) until the end of the length value.

If the actual length, which is defined by the Length Field register and the mask bits is not eight byte-aligned, there might be a case that a packet, which is shorter then the actual required length pass the flexible filter. This can happen due to a comparison of up to seven bytes that come after the packet but are not a real part of the packet.

The last Dword of each filter contains a *Length* field defining the number of bytes from the beginning of the packet compared by this filter, the *Length* field should be an eight byte-aligned value. If the actual packet length is less than (length — 8) (length is the value specified by the *Length* field), the filter fails. Otherwise, it depends on the result of actual byte comparison. The value should not be greater than 128.

31 0	31 8	7 0	31 0	31 0
Reserved	Reserved	Mask [7:0]	Dword 1	Dword 0
Reserved	Reserved	Mask [15:8]	Dword 3	Dword 2
Reserved	Reserved	Mask [23:16]	Dword 5	Dword 4
Reserved	Reserved	Mask [31:24]	Dword 7	Dword 6

. . .

31 7	6 0	31 8	7 0	31 0	31 0
Reserved	Reserved	Reserved	Mask [127:120]	Dword 29	Dword 28
Reserved	Length	Reserved	Mask [127:120]	Dword 31	Dword 30

Each of the filters have allocated addresses as follows:

- Filter 0 — 0x09000 — 0x090FF
- Filter 1 — 0x09100 — 0x091FF
- Filter 2 — 0x09200 — 0x092FF
- Filter 3 — 0x09300 — 0x093FF
- Filter 4 — 0x09800 — 0x098FF
- Filter 5 — 0x09900 — 0x099FF

The following table lists the addresses used for filter 0.

Field	Dword	Address	Bit(s)	Initial Value
Filter 0 DW0	0	0x09000	31:0	X
Filter 0 DW1	1	0x09004	31:0	X
Filter 0 Mask[7:0]	2	0x09008	7:0	X
Reserved	3	0x0900C		X
Filter 0 DW2	4	0x09010	31:0	X
…				
Filter 0 DW30	60	0x090F0	31:0	X
Filter 0 DW31	61	0x090F4	31:0	X
Filter 0 Mask[127:120]	62	0x090F8	7:0	X
Length	63	0x090FC	6:0	X

Accessing the FHFT registers during filter operation can result in a packet being mis-classified if the write operation collides with packet reception. As a result, it is recommended that the flex filters be disabled prior to changing their setup.

8.2.3.25 Management Filters Registers

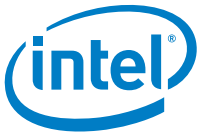
The Management Filters registers are RO for the host. These registers are initialized at LAN Power Good and can be loaded from the EEPROM by the manageability firmware.

8.2.3.25.1 Management VLAN TAG Value — MAVTV[n] (0x5010 +4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
VID	11:0	0x0	Contain the VLAN ID that should be compared with the incoming packet if the corresponding bit in MFVAL.VLAN is set.
Reserved	31:12	0x0	Reserved.

8.2.3.25.2 Management Flex UDP/TCP Ports — MFUTP[n] (0x5030 + 4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
MFUTP[2n]	15:0	0x0	(2n)-th Management Flex UDP/TCP port.
MFUTP[2n+1]	31:16	0x0	(2n+1)-th Management Flex UDP/TCP port.



Each 32-bit register (n=0,…,7) refers to two port filters (register 0 refers to ports 0 and 1, register 2 refers to ports 2 and 3, etc.). Note that SCTP packets do not match the MFUTP filters.

8.2.3.25.3 Management Ethernet Type Filters- METF[n] (0x05190 + 4*n, n=0...3; RW)

Field	Bit(s)	Init Val	Description
EType	15:0	0x0	EtherType value to be compared against the L2 *EtherType* field in the Rx packet. *Note:* Appears in little endian order (high byte first on the wire).
Reserved	29:16	0x0	Reserved.
Polarity	30	0b	0b = Positive filter. Filter enters the decision filters if a match occurred. 1b = Negative filter. Filter enters the decision filters if a match did not occur.
Reserved	31	0b	Reserved.

8.2.3.25.4 Management Control Register — MANC (0x05820; RW)

Field	Bit(s)	Init Val	Description
Reserved	16:0	0x0	Reserved.
RCV_TCO_EN	17	0b	Receive TCO Packets Enabled. When this bit is set it enables the receive flow from the wire to the manageability block.
Reserved	18	0b	Reserved.
RCV_ALL	19	0b	Receive All Enable. When set, all packets are received from the wire and passed to the manageability block.
MCST_PASS_L2	20	0b	Receive All Multicast. When set, all received multicast packets pass L2 filtering and can be directed to the MNG or Host by ~~a~~ one of the decision filters. Broadcast packets are not forwarded by this bit.
EN_MNG2HOST	21	0b	Enable manageability packets to host memory. This bit enables the functionality of the MANC2H register. When set the packets that are specified in the MANC2H registers are also forwarded to host memory, if they pass manageability filters.
Bypass VLAN	22	0b	When set, VLAN filtering is bypassed for MNG packets.
EN_XSUM_FILTER	23	0b	When set, this bit enables Xsum filtering to manageability. Meaning, only packets that pass L3, L4 checksum are sent to the manageability block. *Note:* This capability is not provided for tunneled packets.
EN_IPv4_FILTER	24	0b	Enable IPv4 address Filters. When set, the last 128 bits of the MIPAF register are used to store four IPv4 addresses for IPv4 filtering. When cleared, these bits store a single IPv6 filter.

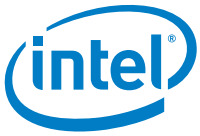
Field	Bit(s)	Init Val	Description
FIXED_NET_TYPE	25	0b	Fixed Next Type. If set, only packets matching the net type defined by the NET_TYPE field pass to manageability. Otherwise, both tagged and un-tagged packets can be forwarded to the manageability engine.
NET_TYPE	26	0b	Net Type. 0b = Pass only un-tagged packets. 1b = Pass only VLAN tagged packets. Valid only if FIXED_NET_TYPE is set.
Reserved	31:27	0x0	Reserved.

8.2.3.25.5 Manageability Filters Valid — MFVAL (0x5824; RW)

Field	Bit(s)	Init Val	Description
MAC	3:0	0x0	MAC. Indicates if the MAC unicast filter registers (MMAH, MMAL) contain valid Ethernet MAC Addresses. Bit 0 corresponds to filter 0, etc.
Reserved	7:4	0x0	Reserved.
VLAN	15:8	0x0	VLAN. Indicates if the VLAN filter registers (MAVTV) contain valid VLAN tags. Bit 8 corresponds to filter 0, etc.
IPv4	19:16	0x0	IPv4. Indicates if the IPv4 address filters (MIPAF) contain valid IPv4 addresses. Bit 16 corresponds to IPv4 address 0. These bits apply only when IPv4 address filters are enabled (MANC.EN_IPv4_FILTER=1).
Reserved	23:20	0x0	Reserved.
IPv6	27:24	0x0	IPv6. Indicates if the IPv6 address filter registers (MIPAF) contain valid IPv6 addresses. Bit 24 corresponds to address 0, etc. Bit 27 (filter 3), applies only when IPv4 address filters are not enabled. (MANC.EN_IPv4_FILTER=0).
Reserved	31:28	0x0	Reserved.

8.2.3.25.6 Management Control To Host Register — MANC2H (0x5860; RW)

Field	Bit(s)	Init Val	Description
Host Enable	7:0	0x0	Host Enable. When set, indicates that packets routed by the manageability filters to manageability are also sent to the host. Bit 0 corresponds to decision filter (MDEF[0] and MDEF_EXT[0]), bit 1 corresponds to decision filter (MDEF[1] and MDEF_EXT[1]), etc. The MANC2H routing is further enabled by a global MANC.EN_MNG2HOST bit.
Reserved	31:8	0x0	Reserved.



8.2.3.25.7 Manageability Decision Filters- MDEF[n] (0x5890 + 4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
Unicast (AND)	0	0b	Unicast. Controls the inclusion of unicast address filtering in the manageability filter decision (AND section).
Broadcast (AND)	1	0b	Broadcast. Controls the inclusion of broadcast address filtering in the manageability filter decision (AND section).
VLAN (AND)	2	0b	VLAN. Controls the inclusion of VLAN address filtering in the manageability filter decision (AND section).
IP Address (AND)	3	0b	IP Address. Controls the inclusion of IP address filtering in the manageability filter decision (AND section).
Unicast (OR)	4	0b	Unicast. Controls the inclusion of unicast address filtering in the manageability filter decision (OR section).
Broadcast (OR)	5	0b	Broadcast. Controls the inclusion of broadcast address filtering in the manageability filter decision (OR section).
Multicast (AND)	6	0b	Multicast. Controls the inclusion of multicast address filtering in the manageability filter decision (AND section). Broadcast packets are not included by this bit. The packet must pass some L2 filtering to be included by this bit – either by the MANC.MCST_PASS_L2 or by some dedicated Ethernet MAC Address.
ARP Request (OR)	7	0b	ARP Request. Controls the inclusion of ARP request filtering in the manageability filter decision (OR section).
ARP Response (OR)	8	0b	ARP Response. Controls the inclusion of ARP response filtering in the manageability filter decision (OR section).
Neighbor Discovery (OR)	9	0b	Neighbor Discovery. Controls the inclusion of neighbor discovery filtering in the manageability filter decision (OR section). The neighbor types accepted by this filter are types 0x86, 0x87, 0x88 and 0x89.
Port 0x298 (OR)	10	0b	Port 0x298. Controls the inclusion of port 0x298 filtering in the manageability filter decision (OR section).
Port 0x26F (OR)	11	0b	Port 0x26F. Controls the inclusion of port 0x26F filtering in the manageability filter decision (OR section).

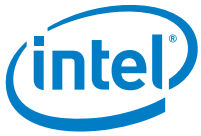
Field	Bit(s)	Init Val	Description
Flex port (OR)	27:12	0x0	Flex Port. Controls the inclusion of flex port filtering in the manageability filter decision (OR section). Bit 12 corresponds to flex port 0, etc.
Flex TCO (OR)	31:28	0x0	Flex TCO. Controls the inclusion of Flex TCO filtering in the manageability filter decision (OR section). Bit 28 corresponds to Flex TCO filter 0, etc.

8.2.3.25.8 Manageability Decision Filters- MDEF_EXT[n] (0x05160 + 4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
L2 EtherType (AND)	3:0	0x0	L2 EtherType. Controls the inclusion of L2 EtherType filtering in the manageability filter decision (AND section).
Reserved	7:4	0x0	Reserved for additional L2 EtherType AND filters.
L2 EtherType (OR)	11:8	0x0	L2 EtherType. Controls the inclusion of L2 EtherType filtering in the manageability filter decision (OR section).
Reserved	15:12	0x0	Reserved for additional L2 EtherType OR filters.
Reserved	31:16	0x0	Reserved.

8.2.3.25.9 Manageability IP Address Filter — MIPAF[m,n] (0x58B0 + 0x10*m + 4*n, m=0...3, n=0...3; RW)

Field	Bit(s)	Init Val	Description
IP_ADDR	31:0	X	Manageability IP Address Filters. For each n, m, m=0...3, n=0...3 while MANC.EN_IPv4_FILTER = 0, MIPAF[m,n] register holds Dword ‘n’ of IPv6 filter ‘m’ (4 x IPv6 filters). For each n, m, m=0...3, n=0...3 while MANC.EN_IPv4_FILTER = 1, MIPAF[m,n] registers for m=0,1,2 is the same as the previous case (3 x IPv6 filters). And MIPAF[3,n] registers holds IPv4 filter ‘n’ (4 x IPv4 filters). *Note:* These registers appear in big endian order (LS byte, LS address is first on the wire).



8.2.3.25.10 Manageability Ethernet MAC Address Low — MMAL[n] (0x5910 + 8*n, n=0...3; RW)

Field	Bit(s)	Init Val	Description
MMAL	31:0	X	Manageability Ethernet MAC Address Low. The lower 32 bits of the 48-bit Ethernet MAC address. *Note:* Appears in big endian order (LS byte of MMAL is first on the wire).

8.2.3.25.11 Manageability Ethernet MAC Address High — MMAH[n] (0x5914 + 8*n, n=0...3; RW)

Field	Bit(s)	Init Val	Description
MMAH	15:0	X	Manageability Ethernet MAC Address High. The upper 16 bits of the 48-bit Ethernet MAC address. *Note:* Appears in big endian order (MS byte of MMAH is last on the wire).
Reserved	31:16	0x0	Reserved. Reads as 0x0. Ignored on write.

8.2.3.25.12 Flexible TCO Filter Table Registers — FTFT (0x09400-0x097FC; RW)

Each of the four Flexible TCO Filters Table (FTFT) registers contains a 128-byte pattern and a corresponding 128-bit mask array. If enabled, the first 128 bytes of the received packet are compared against the non-masked bytes in the FTFT register.

Note: FTFT registers are configured by firmware. Host write/read access to these registers should be avoided.

Each 128-byte filter is composed of 32 Dword entries, where each two Dwords are accompanied by an 8-bit mask, one bit per filter byte. 15:8] etc. The *Mask* field is set so that bit 0 in the mask masks byte 0, bit 1 masks byte 1 etc. A value of one in the *Mask* field means that the appropriate byte in the filter should be compared to the appropriate byte in the incoming packet.

Notes: The *Mask* field must be eight byte-aligned even if the *Length* field is not eight byte-aligned as the hardware implementation compares eight bytes at a time so it should get extra masks until the end of the next Qword. Any *Mask* bit that is located after the length should be set to zero indicating no comparison should be done.

If the actual length, which is defined by the Length Field register and the mask bits is not eight byte-aligned, there might be a case where a packet, which is shorter then the actual required length passes the flexible filter. This can happen due to a comparison of up to seven bytes that come after the packet but are not a real part of the packet.

The last Dword of each filter contains a *Length* field defining the number of bytes from the beginning of the packet compared by this filter. If actual packet length is less than the length specified by this field, the filter fails. Otherwise, it depends on the result of actual byte comparison. The value should not be greater than 128.

31 0	31 8	7 0	31 0	31 0
Reserved	Reserved	Mask [7:0]	Dword 1	Dword 0
Reserved	Reserved	Mask [15:8]	Dword 3	Dword 2
Reserved	Reserved	Mask [23:16]	Dword 5	Dword 4
Reserved	Reserved	Mask [31:24]	Dword 7	Dword 6

. . .

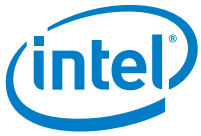
31 0	31 8	7 0	31 0	31 0
Reserved	Reserved	Mask [127:120]	Dword 29	Dword 28
Length	Reserved	Mask [127:120]	Dword 31	Dword 30

Field	Dword	Address	Bit(s)	Initial Value
Filter 0 DW0	0	0x09400	31:0	X
Filter 0 DW1	1	0x09404	31:0	X
Filter 0 Mask[7:0]	2	0x09408	7:0	X
Reserved	3	0x0940C		X
Filter 0 DW2	4	0x09410	31:0	X
…				
Filter 0 DW30	60	0x094F0	31:0	X
Filter 0 DW31	61	0x094F4	31:0	X
Filter 0 Mask[127:120]	62	0x094F8	7:0	X
Length	63	0x094FC	6:0	X

8.2.3.25.13 LinkSec Software/Firmware Interface — LSWFW (0x015F14; RO)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
Lock LinkSec Logic	0	0b	Block LinkSec 0b = Host can access LinkSec registers. 1b = Host cannot access LinkSec registers.
Block host traffic	1	0b	When set, all host traffic (Tx and Rx) is blocked.
Request LinkSec (SC)	2	0b	When set, a message is sent to the MC, requesting access to the LinkSec registers.
Release LinkSec (SC)	3	0b	When set, a message is sent to the MC, releasing ownership of the LinkSec registers.



Field	Bit(s)	Init Val	Description
Reserved	7:4	0x0	Reserved.
LinkSec Ownership	8	0b	Set by firmware to indicate the status of the LinkSec ownership: 0b = LinkSec owned by host (default). 1b = LinkSec owned by MC.
Reserved	31:9	0x0	Reserved.

Note: The access rules on this register are for the driver software.

8.2.3.26 Time Sync (IEEE 1588) Registers

8.2.3.26.1 Rx Time Sync Control Register — TSYNCRXCTL (0x05188; RW)

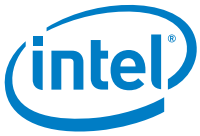
Field	Bit(s)	Init Val	Description
RXTT(RO/V)	0	0b	Rx Time Stamp Valid. Equals 1b when a valid value for Rx time stamp is captured in the Rx Time Stamp register. Cleared by read of Rx Time Stamp (RXSTMPH) register.
Type	3:1	0x0	Type of packets to time stamp: 000b = Time stamp L2 (V2) packets only (sync or Delay_req depends on message type in Section 8.2.3.26.6 and packets with message ID 2 and 3). 001b = Time stamp L4 (V1) packets only (sync or Delay_req depends on message type in Section 8.2.3.26.6). 010b = Time stamp V2 (L2 and L4) packets (sync or Delay_req depends on message type in Section 8.2.3.26.6 and packets with message ID 2 and 3). 101b = Time stamp all packets in which message ID bit 3 is zero, which means time stamp all event packets. This is applicable for V2 packets only. 011b = Reserved 100b = Reserved 110b = Reserved 111b = Reserved
En	4	0b	Enable Rx Time Stamp. 0x0 = Time stamping disabled. 0x1 = Time stamping enabled.
RSV	31:5	0x0	Reserved.

8.2.3.26.2 Rx Time Stamp Low — RXSTMPL (0x051E8; RO)

Field	Bit(s)	Init Val	Description
RXSTMPL	31:0	0x0	Rx time stamp LSB value.

8.2.3.26.3 Rx Time Stamp High — RXSTMPH (0x051A4; RO)

Field	Bit(s)	Init Val	Description
RXSTMPH	31:0	0x0	Rx time stamp MSB value.



8.2.3.26.4 Rx Time Stamp Attributes Low — RXSATRL (0x051A0; RO)

Field	Bit(s)	Init Val	Description
SourceIDL	31:0	0x0	Sourceuuid Low. Captured bytes 24-27 in the PTP message as listed in Section 7.9.5 while the MS byte is last on the wire. In a V1 PTP packet it is the 4 LS bytes of the *Sourceuuid* field and in V2 PTP packet it is part of the *Source Port ID* field.

8.2.3.26.5 Rx Time Stamp Attributes High- RXSATRH (0x051A8; RO)

Field	Bit(s)	Init Val	Description
SourceIDH	15:0	0x0	Sourceuuid High. Captured bytes 22-23 in the PTP message as listed in Section 7.9.5 while the LS byte is first on the wire. In a V1 PTP packet it is the 2 MS bytes of the *Sourceuuid* field and in V2 PTP packet it is part of the *Source Port ID* field.
SequenceID	31:16	0x0	Sequence Id. Captured value of the *SequenceID* field in the PTP Rx packet while LS byte first on the wire.

8.2.3.26.6 Rx Message Type Register Low — RXMTRL (0x05120; RW)

Field	Bit(s)	Init Val	Description
CTRLT	7:0	0x0	V1 control to time stamp.
MSGT	15:8	0x0	V2 message ID to time stamp.
UDPT	31:16	0x319	UDP port number to time stamp.

8.2.3.26.7 Tx Time Sync Control Register — TSYNCTXCTL (0x08C00; RW)

Field	Bit(s)	Init Val	Description
TXTT(RO/V)	0	0b	Tx Time Stamp Valid. Equals 1b when a valid value for Tx time stamp is captured in the Tx Time Stamp register. Cleared by read of Tx Time Stamp (TXSTMPH) register.
RSV	3:1	0x0	Reserved.

Field	Bit(s)	Init Val	Description
EN	4	0x0	Enable Tx Time Stamp. 0x0 Time stamping disabled. 0x1 Time stamping enabled.
RSV	31:5	0x0	Reserved.

8.2.3.26.8 Tx Time Stamp Value Low — TXSTMPL (0x08C04; RO)

Field	Bit(s)	Init Val	Description
TXSTMPL	31:0	0x0	Tx time stamp LSB value.

8.2.3.26.9 Tx Time Stamp Value High — TXSTMPH (0x08C08; RO)

Field	Bit(s)	Init Val	Description
TXSTMPH	31:0	0x0	Tx time stamp MSB value.

8.2.3.26.10 System Time Register Low — SYSTIML (0x08C0C; RW)

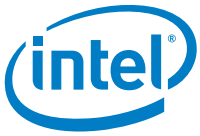
Field	Bit(s)	Init Val	Description
STL	31:0	0x0	System time LSB register.

8.2.3.26.11 System Time Register High — SYSTIMH (0x08C10; RW)

Field	Bit(s)	Init Val	Description
STH	31:0	0x0	System time MSB register.

8.2.3.26.12 Increment Attributes Register — TIMINCA (0x08C14; RW)

Field	Bit(s)	Init Val	Description
IV	23:0	0x0	Increment Value (*incvalue).*
IP	31:24	0x0	Increment Period (*incperiod)*. *Note:* The minimum permitted functional value is two.



8.2.3.26.13 Time Adjustment Offset Register Low — TIMADJL (0x08C18; RW)

Field	Bit(s)	Init Val	Description
TADJL	31:0	0x0	Time Adjustment Value Low.

8.2.3.26.14 Time Adjustment Offset Register High — TIMADJH (0x08C1C; RW)

Field	Bit(s)	Init Val	Description
TADJH	30:0	0x0	Time Adjustment Value High.
Sign	31	0x0	Sign (“0”=”+”, “1”=”-“).

8.2.3.26.15 TimeSync Auxiliary Control Register — TSAUXC (0x08C20; RW)

Field	Bit(s)	Init Val	Description
EN_TT0	0	0b	Enable Target Time 0.
EN_TT1	1	0b	Enable Target Time 1.
Reserved	2	0b	Reserved.
UTT0	3	0b	Use target time 0 to clear clk_out 0 down counter.
ST0	4	0b	Start clock out toggle only if target of clock out occurs.
Reserved	5	0b	Reserved.
UTT1	6	0b	Use target time 1 to clear clk_out 1 down counter.
ST1	7	0b	Start clock out toggle only on target time 1, at this point a rising edge of clock out occurs.
EN_TS0	8	0b	Enable Hardware Time Stamp 0.
AUTT0	9	0b	Auxiliary Time Stamp Taken. Cleared when read after an auxiliary time stamp 0 occurred.
EN_TS1	10	0b	Enable Hardware Time Stamp 1.
AUTT1	11	0b	Auxiliary Time Stamp Taken. Cleared when read after auxiliary time stamp 1 occurred.

Field	Bit(s)	Init Val	Description
Mask	16:12	0b	Masking Value for Target Time. The value in this field determines the masked bits in the comparison of the system time and target time (where 0 = no masking, 1 = bit 0 is masked, 2 = bit 0 and 1 are masked and so on up to 24 in which bits 0 through bit 23 are masked. Any value higher than 24 are reserved).
RSV	31:17	0b	Reserved.

8.2.3.26.16 Target Time Register 0 Low — TRGTTIML0 (0x08C24; RW)

Field	Bit(s)	Init Val	Description
TTL	31:0	0x0	Target time 0 LSB register.

8.2.3.26.17 Target Time Register 0 High — TRGTTIMH0 (0x08C28; RW)

Field	Bit(s)	Init Val	Description
TTH	31:0	0x0	Target time 0 MSB register.

8.2.3.26.18 Target Time Register 1 Low — TRGTTIML1 (0x08C2C; RW)

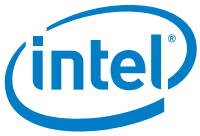
Field	Bit(s)	Init Val	Description
TTL	31:0	0x0	Target time 1 LSB register.

8.2.3.26.19 Target Time Register 1 High — TRGTTIMH1 (0x08C30; RW)

Field	Bit(s)	Init Val	Description
TTH	31:0	0x0	Target time 1 MSB register.

8.2.3.26.20 Frequency Out 0 Control Register — FREQOUT0 (0x08C34; RW) SEC-Tx

Field	Bit(s)	Init Val	Description
RLV	31:0	0x0	Reload value for frequency out zero down counter.



8.2.3.26.21 Frequency Out 1 Control Register — FREQOUT1 (0x08C38; RW) SEC-Tx

Field	Bit(s)	Init Val	Description
RLV	31:0	0x0	Reload value for frequency out one down counter.

8.2.3.26.22 Auxiliary Time Stamp 0 Register Low — AUXSTMPL0 (0x08C3C; RO)

Field	Bit(s)	Init Val	Description
TST_Low	31:0	0x0	Auxiliary time stamp 0 LSB value.

8.2.3.26.23 Auxiliary Time Stamp 0 Register High — AUXSTMPH0 (0x08C40; RO)

Field	Bit(s)	Init Val	Description
TST_Hi	31:0	0x0	Auxiliary time stamp 0 MSB value.

8.2.3.26.24 Auxiliary Time Stamp 1 Register Low — AUXSTMPL1 (0x08C44; RO)

Field	Bit(s)	Init Val	Description
TST_Low	31:0	0x0	Auxiliary time stamp 1 LSB value.

8.2.3.26.25 Auxiliary Time Stamp 1 Register High — AUXSTMPH1 (0x08C48; RO)

Field	Bit(s)	Init Val	Description
TST_Hi	31:0	0x0	Auxiliary time stamp 1 MSB value.

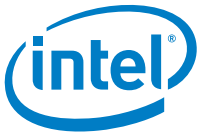
8.2.3.27 Virtualization PF Registers

8.2.3.27.1 VT Control Register — PFVTCTL (0x051B0; RW)

Field	Bit(s)	Init Val	Description
VT_Ena	0	0b	Virtualization Enabled Mode. When set, the 82599 supports either 16, 32, or 64 pools. When cleared, Rx traffic is handled internally as if it belongs to VF zero while VF zero is enabled. This bit should be set the same as MTQC.VT_Ena.
Reserved	6:1	0x0	Reserved.
DEF_PL	12:7	0x0	Default Pool. Pool assignment for packets that do not pass any pool queuing decision. Enabled by the *Dis_Def_Pool* bit.
Reserved	28:13	0x0	Reserved.
Dis_Def_Pool	29	0b	Disable Default Pool. Determines the behavior of an Rx packet that does not match any Rx filter and is therefore not allocated a destination pool. 0b = Packet is assigned to the default pool (see DEF_PL). 1b = Packet is dropped.
Rpl_En	30	0b	Replication Enable, when set to 1b.
Reserved	31	0b	Reserved.

8.2.3.27.2 PF Mailbox — PFMailbox[n] (0x04B00 + 4*n, n=0...63; RW)

Field	Bit(s)	Init Val	Description
Sts (WO)	0	0b	Status/Command from PF ready. Setting this bit causes an interrupt to the relevant VF. This bit always read as zero. Setting this bit sets the *PFSTS* bit in VFMailbox.
Ack (WO)	1	0b	VF message received. Setting this bit, causes an interrupt to the relevant VF. This bit always read as zero. Setting this bit sets the *PFACK* bit in VFMailbox.
VFU	2	0b	Buffer is taken by VF. This bit is RO for the PF and is a mirror of the *VFU* bit in the VFMailbox register.
PFU	3	0b	Buffer is taken by PF. This bit can be set only if the *VFU* bit is cleared and is mirrored in the *PFU* bit of the VFMailbox register.



Field	Bit(s)	Init Val	Description
RVFU (WO)	4	0b	Reset VFU. Setting this bit clears the *VFU* bit in the corresponding VFMailbox register. This bit should be used only if the VF driver is not operational. Setting this bit also resets the corresponding bits in the PFMBICR *VFREQ* and *VFACK* fields.
Reserved	31:5	0x0	Reserved.

8.2.3.27.3 PF Mailbox Interrupt Causes Register — PFMBICR[n] (0x00710 + 4*n, n=0...3; RW1C)

Each register handles 16 VFs and are defined as follows.

Field	Bit(s)	Init Val	Description
VFREQ	15:0	0x0	Each bit in the *VFREQ* field is set when VF number (16*n+j) wrote a message in its mailbox. While 'n' is the register index, n=0...3 and 'j' is the index of the bits in the VFREQ, j=0...15.
VFACK	31:16	0x0	Each bit in the *VFACK* field is set when VF number (16*n+j) acknowledged a PF message. While 'n' is the register index, n=0...3 and '16+j' is the index of the bits in the VFACK, j=0...15.

8.2.3.27.4 PF Mailbox Interrupt Mask Register — PFMBIMR[n] (0x00720 + 4*n, n=0...1; RW)

Field	Bit(s)	Init Val	Description
VFIM	31:0	0xFF	Mailbox interrupt enable from VF # 32*n+j, while 'n' is the register index and 'j' is the bit number.

8.2.3.27.5 PF VFLR Events Indication — PFVFLRE[n] (0x00600, 0x001C0; RO)

Field	Bit(s)	Init Val	Description
VFLE	31:0	0x0	When set, bit 'i' in register 'n' reflects an FLR event on VF# 32*n+i. These bits are accessible only to the PF and are cleared by writing 0x1 to the matched bit in the PFVFLREC registers.

8.2.3.27.6 PF VFLR Events Clear — PFVFLREC[n] (0x00700 + 4*n, n=0...1; W1C)

Field	Bit(s)	Init Val	Description
Clear VFLE	31:0	X	Writing a 0x1 to bit 'i' in register 'n' clears the FLR event on VF# 32*n+i indicated in the PFVFLRE[n] registers.

8.2.3.27.7 PF VF Receive Enable — PFVFRE[n] (0x051E0 + 4*n, n=0...1; RW)

This register is reset on common reset cases and on per-function reset cases. Respective bits per VF are reset on VFLR, BME bit clear or on VF software reset. See Section 4.2.2.2 for more details.

Field	Bit(s)	Init Val	Description
VFRE	31:0	0x0	Bit j. Enables receiving packets to VF# (32*n+j). Each bit is cleared by the relevant VFLR.

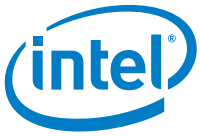
8.2.3.27.8 PF VF Transmit Enable — PFVFTE[n] (0x08110 + 4*n, n=0...1; RW)

This register is reset on common reset cases and on per-function reset cases. Respective bits per VF are reset on VFLR, BME bit clear or on VF software reset. See Section 4.2.2.2 for more details.

Field	Bit(s)	Init Val	Description
VFTE	31:0	0x0	Bit j. Enables transmitting packets from VF# (32*n+j). Each bit is cleared by the relevant VFLR.

8.2.3.27.9 PF PF Queue Drop Enable Register — PFQDE (0x02F04; RW)

Field	Bit(s)	Init Val	Description
QDE	0	0b	Enable drop of packets from Rx queue Queue_Index. This bit overrides the SRRCTL.drop_en bit of each queue. For example, if either of the bits is set, a packet received when no descriptor is available is dropped.
Reserved	3:1	0x0	Reserved (see *WE* and *RE* bit descriptions).
Reserved	7:4	0x0	Reserved.
Queue Index	14:8	0x0	Indicates the queue referenced upon WE/RE commands.



Field	Bit(s)	Init Val	Description
Reserved	15	0b	Reserved.
WE	16	0b	Write Enable. When this bit is set, the content of bits 3:0 are written into the relevant queue context. Bits 3:1 are reserved. This bit should never be set together with the *RE* bit in this register.
RE	17	0b	Read Enable. When this bit is set, the content of bits 3:0 are read from the relevant queue context. Bits 3:1 are reserved. This bit should never be set together with the *WE* bit in this register.
Reserved	31:18	0x0	Reserved.

8.2.3.27.10 PF VM Tx Switch Loopback Enable — PFVMTXSW[n] (0x05180 + 4*n, n=0...1; RW)

Field	Bit(s)	Init Val	Description
LLE	31:0	0x0	Local Loopback Enable. For each register 'n', and bit 'i', i=0..31, enables Local loopback for pool 32*n+1. When set, a packet originating from a specific pool and destined to the same pool is allowed to be looped back. If cleared, the packet is dropped.

8.2.3.27.11 PF VF Anti Spoof Control — PFVFSPOOF[n] (0x08200 + 4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
MACAS	7:0	0x0	For each register 'n', and bit 'i', i=0..7, enables anti-spoofing filter on Ethernet MAC addresses for VF(8*n+1).
VLANAS	15:8	0x0	For each register 'n', and bit '8+i', i=0..7, enables anti-spoofing filter on VLAN tag for VF(8*n+i). *Note:* If *VLANAS* is set for a specific pool, then the respective *MACAS* bit must be set as well.
Reserved	31:16	0x0	Reserved.

8.2.3.27.12 PFDMA Tx General Switch Control — PFDTXGSWC (0x08220; RW)

Field	Bit(s)	Init Val	Description
LBE	0	0b	Enables VMDQ loopback.
Reserved	31:1	0x0	Reserved.

8.2.3.27.13 PF VM VLAN Insert Register — PFVMVIR[n] (0x08000 + 4*n, n=0...63; RW)

Field	Bit(s)	Init Val	Description
Port VLAN ID	15:0	0x0	Port VLAN tag to insert if the *VLANA* field = 01b.
Reserved	29:16	0x0	Reserved.
VLANA	31:30	0x0	VLAN action. 00b = Use descriptor command. 01b = Always insert default VLAN. 10b = Never insert VLAN. 11b = Reserved.

8.2.3.27.14 PF VM L2 Control Register — PFVML2FLT[n] (0x0F000 + 4*n, n=0...63; RW)

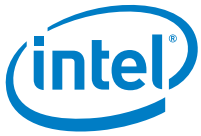
This register controls per VM Inexact L2 Filtering.

Field	Bit(s)	Init Val	Description
Reserved	23:0	0x0	Reserved.
AUPE	24	0b	Accept Untagged Packets Enable. When set, packets without a VLAN tag can be forwarded to this queue, assuming they pass the Ethernet MAC address queuing mechanism.
ROMPE	25	0b	Receive Overflow Multicast Packets. Accept packets that match the MTA table.
ROPE	26	0b	Receive MAC Filters Overflow. Accept packets that match the PFUTA table.
BAM	27	0b	Broadcast Accept.
MPE	28	0b	Multicast Promiscuous.
Reserved	31:29	0x0	Reserved.

8.2.3.27.15 PF VM VLAN Pool Filter — PFVLVF[n] (0x0F100 + 4*n, n=0...63; RW)

Software should initialize these registers before transmit and receive are enabled.

Field	Bit(s)	Init Val	Description
VLAN_Id	11:0	X	Defines a VLAN tag for pool VLAN filter n. The bitmap defines which pools belong to this VLAN. *Note:* Appears in little endian order (LS byte last on the wire).



Field	Bit(s)	Init Val	Description
Reserved	30:12	X	Reserved.
VI_En	31	X	VLAN Id Enable — this filter is valid.

8.2.3.27.16 PF VM VLAN Pool Filter Bitmap — PFVLVFB[n] (0x0F200 + 4*n, n=0...127; RW)

Software should initialize these registers before transmit and receive are enabled.

Field	Bit(s)	Init Val	Description
POOL_ENA	31:0	x	Pool Enable Bit Array. Each couple of registers '2*n' and '2*n+1' enables routing of packets that match a PFVLVF[n] filter to a pool list. Each bit when set, enables packet reception with the associated pools as follows: • Bit 'i' in register '2*n' is associated with POOL 'i'. • Bit 'i' in register '2*n+1' is associated with POOL '32+i'.

8.2.3.27.17 PF Unicast Table Array — PFUTA[n] (0x0F400 + 4*n, n=0...127; RW)

There is one register per 32 bits of the unicast address table for a total of 128 registers (the PFUTA[127:0] designation). Software must mask to the desired bit on reads and supply a 32-bit word on writes. The first bit of the address used to access the table is set according to the MCSTCTRL.MO field.

The seven MS bits of the Ethernet MAC address (out of the 12 bits) selects the register index while the five LS bits (out of the 12 bits) selects the bit within a register.

Note: All accesses to this table must be 32 bit.

The look-up algorithm is the same one used for the MTA table.

This table should be zeroed by software before start of operation.

Field	Bit(s)	Init Val	Description
Bit Vector	31:0	X	Word wide bit vector specifying 32 bits in the unicast destination address filter table.

8.2.3.27.18 PF Mirror Rule Control — PFMRCTL[n] (0x0F600 + 4*n, n= 0...3; RW)

This register defines mirroring rules for each of four destination pools.

Field	Bit(s)	Init Val	Description
VPME	0	0b	Virtual Pool Mirroring Enable. Enables mirroring of certain pools as defined in the PFMRVM registers.
UPME	1	0b	Uplink Port Mirroring Enable. Enables mirroring of all traffic received from the network.
DPME	2	0b	Downlink Port Mirroring Enable. Enables mirroring of all traffic transmitted to the network.
VLME	3	0b	VLAN Mirroring Enable. Enables mirroring of a set of given VLANs as defined in the PFMRVLAN registers.
Reserved	7:4	0x0	Reserved.
MP	13:8	0x0	Mirror Pool. Defines the destination pool for this mirror rule.
Reserved	31:14	0x0	Reserved.

8.2.3.27.19 PF Mirror Rule VLAN — PFMRVLAN[n] (0x0F610 + 4*n, n= 0...7; RW)

This register defines the VLAN values as listed in the PFVLVF table taking part in the VLAN mirror rule.

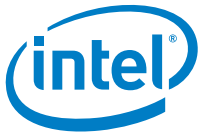
Registers 0, 4 correspond to rule 0, registers 1, 5 correspond to rule 1, etc. Registers 0-3 correspond to the LSB in the PFVLVF table. For example, register 0 corresponds to VLAN filters 31:0, while register 4 corresponds to VLAN filters 63:32.

Field	Bit(s)	Init Val	Description
VLAN	31:0	0x0	Bitmap listing which VLANs participate in the mirror rule.

8.2.3.27.20 PF Mirror Rule Pool — PFMRVM[n] (0x0F630 + 4*n, n= 0...7; RW)

This register defines which pools are being mirrored to the destination pool.

Registers 0, 4 correspond to rule 0, registers 1, 5 correspond to rule 1, etc. Registers 0-3 correspond to the LSB in the pool list. For example, register 0 corresponds to pools 31:0, while register 4 corresponds to pools 63:32.



Field	Bit(s)	Init Val	Description
Pool	31:0	0x0	Bitmap listing which pools participate in the mirror rule.