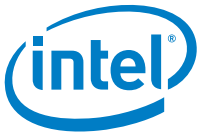
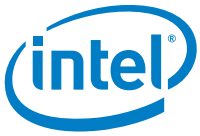


Field	Bit(s)	Init Val	Description
SDP5_IODIR	13	0b	SDP5 Pin Directionality. Controls whether or not software-controlled pin SDP5 is configured as an input or output. 0b = Input 1b = Output
SDP6_IODIR	14	0b	SDP6 Pin Directionality. Controls whether or not software-controlled pin SDP6 is configured as an input or output. 0b = Input 1b = Output
SDP7_IODIR	15	0b	SDP7 Pin Directionality. Controls whether or not software-controlled pin SDP7 is configured as an input or output. 0b = Input 1b = Output
SDP0_NATIVE	16	0b	SDP0 Operating Mode. 0b = Generic software controlled I/O by SDP0_DATA and SDP0_IODIR. 1b = Reserved.
SDP1_NATIVE	17	0b[1]	SDP1 Operating Mode. 0b = Generic software controlled I/O by SDP1_DATA and SDP1_IODIR. 1b = Native mode operation (connected to hardware function). In this mode, the SDP1_IODIR must be set to 1b.
SDP2_NATIVE	18	0b	SDP2 operating mode. 0b = Generic software controlled IO by SDP2_DATA and SDP2_IODIR. 1b = Native mode operation (Connected to hardware function). In this mode pin functions as defined by the SDP2_TSync_TT1 bit
SDP3_NATIVE	19	0b	SDP3 Operating Mode. 0b = Generic software controlled I/O by SDP3_DATA and SDP3_IODIR. 1b = Native mode operation (connected to hardware function). In this mode pin functions as defined by the SDP3_TSync_TT0 bit.
SDP4_NATIVE[2]	20	0b	SDP4 Operating Mode. 0b = Generic software controlled I/O by SDP4_DATA and SDP4_IODIR. 1b = Native mode operation (connected to hardware function). Drives optical module reset according to functionality defined by the SDP4_Function bit.
SDP5_NATIVE	21	0b	SDP5 Operating Mode. 0b = Generic software controlled I/O by SDP5_DATA and SDP5_IODIR. 1b = Native mode operation (connected to hardware function). Drives optical module transmit disable according to functionality defined by the SDP5_Function bit.
SDP6_NATIVE	22	0b	SDP6 Operating Mode. 0b = Generic software controlled I/O by SDP6_DATA and SDP6_IODIR. 1b = Native mode operation (connected to hardware function). In this mode, pin functions as defined by the SDP6_TSync_TT1 bit.
SDP7_NATIVE	23	0b	SDP7 Operating Mode. 0b = Generic software controlled I/O by SDP7_DATA and SDP7_IODIR. 1b = Native mode operation (connected to hardware function). In this mode, pin functions as defined by the SDP7_TSync_TT0 bit.
Reserved	25:24	0	Reserved.

Field	Bit(s)	Init Val	Description
SDP2_TSync_TT1	26	0b	SDP2 Native Mode Functionality (SDP2_NATIVE = 1). 0b = TS0 functionality. Samples IEEE 1588 time stamp into Auxiliary Time Stamp 0 register on level change of SDP2 signal (For TS0 functionality, SDP2_IODIR should be configured as input). 1b = TT1 functionality. Asserts SDP2 to 1 when IEEE 1588 time stamp equals Target Time register 1 (For TT1 functionality, SDP2_IODIR should be configured as output).
SDP3_TSync_TT0	27	0b	SDP3 Native Mode Functionality (SDP3_NATIVE = 1). 0b = TS1 functionality. Samples IEEE 1588 time stamp into Auxiliary Time Stamp 1 register on level change of SDP3 signal (For TS1 functionality, SDP3_IODIR should be configured as input). 1b = TT0 functionality. Asserts SDP3 to 1b when IEEE 1588 time stamp equals Target Time register 0 (For TT0 functionality, SDP3_IODIR should be configured as output).
SDP4_Function[2]	28	0b	SDP4 Native Mode Functionality (SDP4_NATIVE = 1). 0b = Pin functionality is driven by software (SDP4_data bit) except when the MAC is reset or when entering D3 power state when management functionality is disabled. In the previous case SDP4 pin moves to tri-state (by resetting SDP4_IODIR bit) and optical module is reset by placing an appropriate external pull-up or pull-down resistor on the SDP4 pin. 1b = SDP4 pin is driven high when the MAC is reset or powered down (D3 state). SDP4_IODIR should be configured as output for this functionality.
SDP5_Function	29	0b	SDP5 Native Mode Functionality (SDP5_NATIVE = 1). 0b = Pin functionality is driven by software (SDP5_data bit) except when the MAC is reset or when entering D3 power state when management functionality is disabled. In the previous case, SDP5 pin moves to tri-state (by resetting SDP5_IODIR bit) and optical module transmission is disabled by placing an appropriate external pull-up or pull-down resistor on the SDP5 pin. 1b = SDP5 pin is driven high when the MAC is reset or powered down (D3 state). SDP5_IODIR should be configured as output for this functionality.
SDP6_TSync_TT1	30	0b	SDP6 Native Mode Functionality (SDP6_NATIVE = 1). 0b = CLK0 functionality. Drives a reference clock with the frequency defined in the Frequency Out 0 Control register (For CLK0 functionality, SDP6_IODIR should be configured as output). 1b = TT1 functionality. Asserts SDP6 to 1b when IEEE 1588 time stamp equals Target Time register 1 (For TT1 functionality, SDP6_IODIR should be configured as output).
SDP7_TSync_TT0	31	0b	SDP7 Native Mode Functionality (SDP7_NATIVE = 1). 0b = CLK1 functionality. Drives a reference clock with the frequency defined in the Frequency Out 1 Control register (for CLK1 functionality, SDP7_IODIR should be configured as output). 1b = TT0 functionality. Asserts SDP7 to 1b when IEEE 1588 time stamp equals Target Time register 1 (For TT0 functionality, SDP7_IODIR should be configured as output).

1. Initial value can be configured using the EEPROM.
2. SDP4 in port 0 is a dedicated input pin for Security enablement. See Section 4.6.12.



8.2.3.1.5 I2C Control — I2CCTL (0x00028; RW)

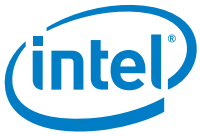
Field	Bit(s)	Init Val	Description
I2C_CLK_IN	0	0b	I2C_CLK In Value. Provides the value of I2C_CLK (input from external PAD). This bit is RO.
I2C_CLK_OUT	1	1b	I2C_CLK Out Value. Used to drive the value of I2C_CLK (output to PAD).
I2C_DATA_IN	2	0b	I2C_DATA In Value. Provides the value of I2C_DATA (input from external PAD). This bit is RO.
I2C_DATA_OUT	3	1b	I2C_DATA Out Value. Used to drive the value of I2C_DATA (output to PAD).
Reserved	31:4	0x0	Reserved.

8.2.3.1.6 LED Control — LEDCTL (0x00200; RW)

Field	Bit(s)	Init Val	Description
LED0_MODE	3:0	0x0[1]	LED0 Mode. This field specifies the control source for the LED0 output. An initial value of 0000b selects the LINK_UP indication.
Reserved	4	0b[1]	Reserved.
GLOBAL_BLINK_MODE	5	0b[1]	GLOBAL Blink Mode. This field specifies the blink mode of all LEDs. 0b = Blink at 200 ms on and 200 ms off. 1b = Blink at 83 ms on and 83 ms off.
LED0_IVRT	6	0b[1]	LED0 Invert. This field specifies the polarity/inversion of the LED source prior to output or blink control. By default the output drives the cathode of the LED so when the LED output is 0b the LED is on. 0b = LED output is active low. 1b = LED output is active high.
LED0_BLINK	7	0b[1]	LED0 Blink. This field specifies whether or not to apply blink logic to the (inverted) LED control source prior to the LED output. 0b = Do not blink LED output. 1b = Blink LED output.
LED1_MODE	11:8	0x1[1]	LED1 Mode. This field specifies the control source for the LED1 output. An initial value of 0001b selects the 10 Gb/s link indication.
Reserved	13:12	0b[1]	Reserved.

Field	Bit(s)	Init Val	Description
LED1_IVRT	14	0b[1]	LED1 Invert. This field specifies the polarity/inversion of the LED source prior to output or blink control. By default the output drives the cathode of the LED so when the LED output is 0b the LED is on. 0b = LED output is active low. 1b = LED output is active high.
LED1_BLINK	15	1b[1]	LED1 Blink. This field specifies whether or not to apply blink logic to the (inverted) LED control source prior to the LED output. 0b = Do not blink LED output. 1b = Blink LED output.
LED2_MODE	19:16	0x4[1]	LED2 Mode. This field specifies the control source for the LED0 output. An initial value of 0100 selects LINK/ACTIVITY indication.
Reserved	21:20	0[1]	Reserved
LED2_IVRT	22	0[1]	LED2 Invert. This field specifies the polarity/inversion of the LED source prior to output or blink control. By default the output drives the cathode of the LED so when the LED output is 0b the LED is on. 0b = LED output is active low. 1b = LED output is active high.
LED2_BLINK	23	0[1]	LED2 Blink. This field specifies whether or not to apply blink logic to the (inverted) LED control source prior to the LED output. 0b = Do not blink LED output. 1b = Blink LED output.
LED3_MODE	27:24	0x5[1]	LED3 Mode. This field specifies the control source for the LED0 output. An initial value of 0101b selects the 1 Gb/s link indication.
Reserved	29:28	0b[1]	Reserved.
LED3_IVRT	30	0b[1]	LED3 Invert. This field specifies the polarity/inversion of the LED source prior to output or blink control. By default the output drives the cathode of the LED so when the LED output is 0b the LED is on. 0b = LED output is active low. 1b = LED output is active high.
LED3_BLINK	31	0b[1]	LED3 Blink. This field specifies whether or not to apply blink logic to the (inverted) LED control source prior to the LED output. 0b = Do not blink LED output. 1b = Blink LED output.

1. These bits are read from the EEPROM.



The following mapping is used to specify the LED control source (MODE) for each LED output:

MODE	Selected Mode	Source Indication
0000b	LINK_UP	Asserted or blinking according to the LEDx_BLINK setting when any speed link is established and maintained.
0001b	LINK_10G	Asserted or blinking according to the LEDx_BLINK setting when a 10 Gb/s link is established and maintained.
0010b	MAC_ACTIVITY	Active when link is established and packets are being transmitted or received. In this mode, the LEDx_BLINK must be set.
0011b	FILTER_ACTIVITY	Active when link is established and packets are being transmitted or received that passed MAC filtering. In this mode, the LEDx_BLINK must be set.
0100b	LINK/ACTIVITY	Asserted steady when link is established and there is no transmit or receive activity. Blinking when there is link and receive or Transmit activity.
0101b	LINK_1G	Asserted or blinking according to the LEDx_BLINK setting when a 1 Gb/s link is established and maintained.
0110	LINK_100	Asserted or blinking according to the LEDx_BLINK setting when a 100 Mb/s link is established and maintained.
0111b:1101b	Reserved	Reserved.
1110b	LED_ON	Always asserted or blinking according to the LEDx_BLINK setting.
1111b	LED_OFF	Always de-asserted.

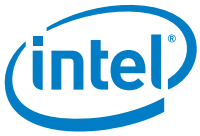
8.2.3.1.7 Extended VLAN Ether Type — EXVET (0x05078; RW)

Field	Bit(s)	Init Val	Description
Reserved	15:0	0x0	Reserved.
VET EXT	31:16	0x8100	Outer-VLAN Ether Type (VLAN Tag Protocol Identifier - TPID). *Note:* This field appears in little endian (MS byte first on the wire).

8.2.3.2 EEPROM/Flash Registers

8.2.3.2.1 EEPROM/Flash Control Register — EEC (0x10010; RW)

Field	Bit(s)	Init Val	Description
EE_SK	0	0b	Clock input to the EEPROM. When EE_GNT is set to 1b, the EE_SK output signal is mapped to this bit and provides the serial clock input to the EEPROM. Software clocks the EEPROM via toggling this bit with successive writes.
EE_CS	1	0b	Chip select input to the EEPROM. When EE_GNT is set to 1b, the EE_CS output signal is mapped to the chip select of the EEPROM device. Software enables the EEPROM by writing a 0b to this bit.
EE_DI	2	0b	Data input to the EEPROM. When EE_GNT is set to 1b, the EE_DI output signal is mapped directly to this bit. Software provides data input to the EEPROM via writes to this bit.
EE_DO (RO field)	3	X	Data output bit from the EEPROM. The EE_DO input signal is mapped directly to this bit in the register and contains the EEPROM data output. This bit is read-only from a software perspective; writes to this bit have no effect.
FWE	5:4	01b	Flash Write Enable Control. These two bits control whether or not writes to the Flash are allowed. 00b = Flash erase (along with bit 31 in the FLA register). 01b = Flash writes disabled. 10b = Flash writes enabled. 11b = Not allowed.
EE_REQ	6	0b	Request EEPROM Access. Software must write a 1b to this bit to get direct EEPROM access. It has access when EE_GNT is set to 1b. When software completes the access, it must then write a 0b.
EE_GNT (RO field)	7	0b	Grant EEPROM Access. When this bit is set to 1b, software can access the EEPROM using the EE_SK, EE_CS, EE_DI, and EE_DO bits.
EE_PRES (RO field)	8	(see desc.)	EEPROM Present. Setting this bit to 1b indicates that an EEPROM is present and has the correct signature field. This bit is read-only.
Auto_RD (RO field)	9	0b	EEPROM Auto-Read Done. When set to 1b, this bit indicates that the auto-read by hardware from the EEPROM is done. This bit is also set when the EEPROM is not present or when its signature field is not valid.
Reserved	10	1b	Reserved.
EE_Size (RO field)	14:11	0010b[1]	EEPROM Size. This field defines the size of the EEPROM (see Table 8-3).



Field	Bit(s)	Init Val	Description
PCI _ANA_done (RO field)	15	0b	PCIe Analog Done. When set to 1b, indicates that the PCIe analog section read from EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid.
PCI _Core_done (RO field)	16	0b	PCIe Core Done. When set to 1b, indicates that the Core analog section read from EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid. *Note:* This bit returns the relevant done indication for the function that reads the register.
PCI _genarl_done (RO field)	17	0b	PCIe General Done. When set to 1b, indicates that the PCIe general section read from the EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid.
PCI_FUNC_DONE (RO field)	18	0b	PCIe Function Done. When set to 1b, indicates that the PCIe function section read from EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid. *Note:* This bit returns the relevant done indication for the function that reads the register.
CORE_DONE (RO field)	19	0b	Core Done. When set to 1b, indicates that the Core analog section read from the EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid. *Note:* This bit returns the relevant done indication for the function that reads the register.
CORE_CSR_DONE (RO field)	20	0b	Core CSR Done. When set to 1b, indicates that the Core CSR section read from the EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid. *Note:* This bit returns the relevant done indication for the function that reads the register.
MAC_DONE (RO field)	21	0b	MAC Done. When set to 1b, indicates that the MAC section read from the EEPROM is done. This bit is cleared when auto-read starts. This bit is also set when the EEPROM is not present or when its signature field is not valid. *Note:* This bit returns the relevant done indication for the function that reads the register.
Reserved	31:22	0x0	Reserved. Reads as 0b.

1. These bits are read from the EEPROM.

Table 8-3 EEPROM Sizes (Bits 14:11)

Field Value	EEPROM Size	EEPROM Address Size
0100b	16 Kb	2 bytes
0101b	32 Kb	2 bytes
0110b	64 Kb	2 bytes
0111b	128 Kb	2 bytes
1000b	256 Kb	2 bytes
1001b:1111b	Reserved	Reserved

This register provides software-direct access to the EEPROM. Software can control the EEPROM by successive writes to this register. Data and address information is clocked into the EEPROM by software toggling the EESK bit (2) of this register. Data output from the EEPROM is latched into bit 3 of this register via the internal 62.5 MHz clock and can be accessed by software via reads of this register.

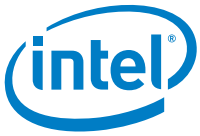
Note: Attempts to write to the Flash device when writes are disabled (FWE = 01b) should not be attempted. Behavior after such an operation is undefined, and might result in component and/or system hangs.

8.2.3.2.2 EEPROM Read Register — EERD (0x10014; RW)

Field	Bit(s)	Init Val	Description
START	0	0b	Start Read. Writing a 1b to this bit causes the EEPROM to read a 16-bit word at the address stored in the EE_ADDR field and then stores the result in the EE_DATA field. This bit is self-clearing.
DONE	1	0b	Read Done. Set this bit to 1b when the EEPROM read completes. Set this bit to 0b when the EEPROM read is in progress. *Note:* Writes by software are ignored.
ADDR	15:2	0x0	Read Address. This field is written by software along with *Start Read* to indicate that the address of the word to read.
DATA	31:16	0x0	Read Data. Data returned from the EEPROM read.

This register is used by software to cause the 82599 to read individual words in the EEPROM. To read a word, software writes the address to the *Read Address* field and simultaneously writes a 1b to the Start Read field. The 82599 reads the word from the EEPROM and places it in the *Read Data* field, setting the *Read Done* field to 1b. Software can poll this register, looking for a 1b in the *Read Done* field and then using the value in the *Read Data* field.

When this register is used to read a word from the EEPROM, that word is not written to any of the 82599's internal registers even if it is normally a hardware-accessed word.



8.2.3.2.3 Flash Access Register — FLA (0x1001C; RW)

Field	Bit(s)	Init Val	Description
FL_SCK	0	0b	Clock input to the Flash. When FL_GNT is set to 1b, the FL_SCK output signal is mapped to this bit and provides the serial clock input to the Flash. Software clocks the Flash via toggling this bit with successive writes.
FL_CE	1	0b	Chip select input to the Flash. When FL_GNT is set to 1b, the FL_CE output signal is mapped to the chip select of the Flash device. Software enables the Flash by writing a 0b to this bit.
FL_SI	2	0b	Data input to the Flash. When FL_GNT is set to 1b, the FL_SI output signal is mapped directly to this bit. Software provides data input to the Flash via writes to this bit.
FL_SO	3	X	Data output bit from the Flash. The FL_SO input signal is mapped directly to this bit in the register and contains the Flash serial data output. This bit is read-only from a software perspective. *Note:* Writes to this bit have no effect.
FL_REQ	4	0b	Request Flash Access. Software must write a 1b to this bit to get direct Flash access. It has access when FL_GNT is set to 1b. When software completes the access, it must then write a 0b.
FL_GNT	5	0b	Grant Flash Access. When this bit is set to 1b, software can access the Flash using the FL_SCK, FL_CE, FL_SI, and FL_SO bits.
Reserved	29:6	0b	Reserved. Reads as 0b.
FL_BUSY	30	0b	Flash Busy. This bit is set to 1b while a write or an erase to the Flash is in progress, While this bit is cleared (reads as 0b), software can access to write a new byte to the Flash. *Note:* This bit is read-only from a software perspective.
FL_ER	31	0b	Flash Erase Command. This command is sent to the Flash only if bits 5:4 of register EEC are also set to 00b. This bit is auto-cleared and reads as 0b.

This register provides software direct access to the Flash. Software can control the Flash by successive writes to this register. Data and address information is clocked into the EEPROM by software toggling FL_SCK in this register. Data output from the Flash is latched into bit 3 of this register via the internal 125 MHz clock and can be accessed by software via reads of this register.

Note: In the 82599, the FLA register is only reset at LAN_PWR_GOOD as opposed to legacy devices at software reset.

8.2.3.2.4 Manageability EEPROM Control Register — EEMNGCTL (0x10110; RW)

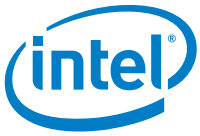
Note: This register can be read/write by manageability firmware and is read-only to host software.

Field	Bit(s)	Init Val	Description
ADDR	14:0	0x0	Address. This field is written by manageability along with *Start* bit and the *Write* bit to indicate which EEPROM address to read or write.
START	15	0b	Start. Writing a 1b to this bit causes the EEPROM to start the read or write operation according to the write bit. This bit is self cleared by hardware.
WRITE	16	0b	Write. This bit signals the EEPROM if the current operation is read or write. 0b = Read. 1b = Write.
EEBUSY	17	0b	EPROM Busy. This bit indicates that the EEPROM is busy processing an EEPROM transaction and should not be accessed.
Reserved	30:18	0x0	Reserved.
DONE	31	1b	Transaction Done. This bit is cleared after the *Start* bit and *Write* bit are set by manageability and is set back again when the EEPROM write or read transaction completes.

8.2.3.2.5 Manageability EEPROM Read/Write Data — EEMNGDATA (0x10114; RW)

Note: This register can be read/write by manageability firmware and is read-only to host software.

Field	Bit(s)	Init Val	Description
WRDATA	15:0	0x0	Write Data. Data to be written to the EEPROM.
RDDATA	31:16	X	Read Data. Data returned from the EEPROM read. *Note:* This field is read only.



8.2.3.2.6 Manageability Flash Control Register — FLMNGCTL (0x10118; RW)

Note: This register can be read/write by manageability firmware and is read-only to host software.

Field	Bit(s)	Init Val	Description
ADDR	23:0	0x0	Address. This field is written by manageability along with CMD and CMDV to indicate which Flash address to read or write.
CMD	25:24	00b	Command. Indicates which command should be executed. Valid only when the *CMDV* bit is set. 00b = Read command. 01b = Write command (single byte). 10b = Sector erase. *Note:* Sector erase is applicable only for Atmel Flashes. 11b = Erase.
CMDV	26	0b	Command Valid. When set, indicates that the manageability firmware issues a new command and is cleared by hardware at the end of the command.
FLBUSY	27	0b	Flash Busy. This bit indicates that the Flash is busy processing a Flash transaction and should not be accessed.
Reserved	29:28	00b	Reserved.
DONE	30	1b	Read Done. This bit is cleared by firmware when it sets the *CMDV* bit. It is set by hardware for each Dword read that completes. This bit is read/clear by hardware enabling the multiple Dword read flow.
WRDONE	31	1b	Global Done. This bit clears after the *CMDV* bit is set by manageability and is set back again after all Flash transactions complete. For example, the Flash device finished reading all the requested read or other accesses (write and erase).

8.2.3.2.7 Manageability Flash Read Data — FLMNGDATA (0x1011C; RW)

Note: This register can be read/write by manageability firmware and is read-only to host software.

Field	Bit(s)	Init Val	Description
DATA	31:0	0x0	Read/Write Data On a read transaction, this register contains the data returned from the Flash read. On write transactions, bits 7:0 are written to the Flash.

8.2.3.2.8 Flash Opcode Register — FLOP (0x01013C; RW)

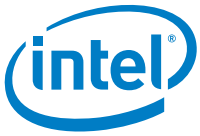
This register enables the host or firmware to define the op-code used in order to erase a sector of the Flash or erase the entire Flash. This register is reset only at power on or during LAN_PWR_GOOD assertion.

Field	Bit(s)	Init Val	Description
SERASE	7:0	0x52	Flash Block Erase Instruction. The op-code for the Flash block erase instruction and is relevant only to Flash access by manageability.
DERASE	15:8	0x62	Flash Device Erase Instruction. The op-code for the Flash erase instruction.
Reserved	31:16	0x0	Reserved.

8.2.3.2.9 General Receive Control — GRC (0x10200; RW)

Field	Bit(s)	Init Val	Description
MNG_EN	0	1b[1]	Manageability Enable. This read-only bit indicates whether or not manageability functionality is enabled.
APME	1	0b[1]	Advance Power Management Enable. If set to 1b, APM wake up is enabled. When APM wake up is enabled and The 82599 receives a matching magic packet, it sets the *PME_Status* bit in the Power Management Control/Status register (PMCSR) and asserts the PE_WAKE_N pin. It is a single read/write bit in a single register, but has two values depending on the function that accesses the register.
Reserved	31:2	0x0	Reserved.

1. Loaded from the EEPROM.



8.2.3.3 Flow Control Registers

8.2.3.3.1 Priority Flow Control Type Opcode — PFCTOP (0x0431C / 0x03008; RW)

This register is also mapped to address 0x0431C to maintain compatibility with the 82598.

Field	Bit(s)	Init Val	Description
FCT	15:0	0x8808	Priority Flow Control EtherType. *Note:* This field appears in little endian (MS byte first on the wire).
FCOP	31:16	0x0101	Priority Flow Control Opcode. *Note:* This field appears in big endian (LS byte first on the wire).

This register contains the *Type* and *Opcode* fields that are matched against a recognized priority flow control packet.

8.2.3.3.2 Flow Control Transmit Timer Value n — FCTTVn (0x03200 + 4*n, n=0...3; RW)

Each 32-bit register (n=0… 3) refers to two timer values (register 0 refers to timer 0 and 1, register 1 refers to timer 2 and 3, etc.).

Field	Bit(s)	Init Val	Description
TTV(2n)	15:0	0x0	Transmit Timer Value 2n. Timer value included in XOFF frames as Timer (2n). The same value shall be set to User Priorities attached to the same TC, as defined in RTTUP2TC register. For legacy 802.3X flow control packets, TTV0 is the only timer that is used.
TTV(2n+1)	31:16	0x0	Transmit Timer Value 2n+1. Timer value included in XOFF frames as Timer 2n+1. The same value shall be set to User Priorities attached to the same TC, as defined in RTTUP2TC register.

The 16-bit value in the *TTV* field is inserted into a transmitted frame (either XOFF frames or any pause frame value in any software transmitted packets). It counts in units of slot time (usually 64 bytes).

Note: The 82599 uses a fixed slot time value of 64 byte times.

8.2.3.3.3 Flow Control Receive Threshold Low — FCRTL[n] (0x03220 + 4*n, n=0...7; RW)

Each 32-bit register (n=0… 7) refers to a different receive packet buffer.

Field	Bit(s)	Init Val	Description
Reserved	4:0	0x0	Reserved.
RTL	18:5	0x0	Receive Threshold Low n. Receive packet buffer n FIFO low water mark for flow control transmission (32 bytes granularity).
Reserved	30:19	0x0	Reserved.
XONE	31	0b	XON Enable n. Per the receive packet buffer XON enable. 0b = Disabled. 1b = Enabled.

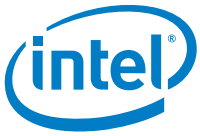
This register contains the receive threshold used to determine when to send an XON packet and counts in units of bytes. The lower four bits must be programmed to 0x0 (16-byte granularity). Software must set XONE to enable the transmission of XON frames. Each time incoming packets cross the receive high threshold (become more full), and then crosses the receive low threshold, with XONE enabled (1b), hardware transmits an XON frame.

8.2.3.3.4 Flow Control Receive Threshold High — FCRTH[n] (0x03260 + 4*n, n=0...7; RW)

Each 32-bit register (n=0…7) refers to a different receive packet buffer.

Field	Bit(s)	Init Val	Description
Reserved	4:0	0x0	Reserved.
RTH	18:5	0x0	Receive Threshold High n. Receive packet buffer n FIFO high water mark for flow control transmission (32 bytes granularity).
Reserved	30:19	0x0	Reserved.
FCEN	31	0b	Transmit flow control enable for packet buffer n.

This register contains the receive threshold used to determine when to send an XOFF packet and counts in units of bytes. This value must be at least eight bytes less than the maximum number of bytes allocated to the receive packet buffer and the lower four bits must be programmed to 0x0 (16-byte granularity). Each time the receive FIFO reaches the fullness indicated by RTH, hardware transmits a pause frame if the transmission of flow control frames is enabled.



8.2.3.3.5 Flow Control Refresh Threshold Value — FCRTV (0x032A0; RW)

Field	Bit(s)	Init Val	Description
FC_refresh_th	15:0	0x0	Flow Control Refresh Threshold. This value is used to calculate the actual refresh period for sending the next pause frame if conditions for a pause state are still valid (buffer fullness above low threshold value). The formula for the refresh period for priority group N is — FCTTV[N/2].TTV[Nmod2] — FCRTV.FC_refresh_th *Note:* The FC_refresh_th must be smaller than TTV of the TC and larger than the max packet size in the TC + FC packet size + link latency and Tx latency and Rx latency in 64 byte units.
Reserved	31:16	0x0	Reserved.

8.2.3.3.6 Transmit Flow Control Status — TFCS (0x0CE00; RO)

Field	Bit(s)	Init Val	Description
TC_XON	7:0	0xFF	Set if flow control is in XON state. If in link flow control mode, only bit 0 should be used. In case of priority flow control mode, each bit represents a TC.
Reserved	31:9	0x0	Reserved.

8.2.3.3.7 Flow Control Configuration — FCCFG (0x03D00; RW)

Field	Bit(s)	Init Val	Description
Reserved	2:0	0x0	Reserved.
TFCE	4:3	0x0	Transmit Flow Control Enable. These bits Indicate that the 82599 transmits flow control packets (XON/XOFF frames) based on receive fullness. If auto-negotiation is enabled, then this bit should be set by software to the negotiated flow control value. 00b = Transmit flow control disabled. 01b = Link flow control enabled. 10b = Priority flow control enabled. 11b = Reserved. *Note:* Priority flow control should be enabled in DCB mode only.
Reserved	31:5	0x0	Reserved.

8.2.3.4 PCIe Registers

8.2.3.4.1 PCIe Control Register — GCR (0x11000; RW)

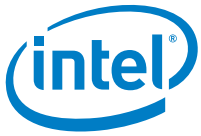
This register is shared for both LAN ports.

Field	Bit (s)	Init Val	Description
Reserved	2:0	100b	Reserved
Reserved	8:3	X	Reserved.
Completion Timeout resend enable	9	1b	When set, enables a resend request after the completion timeout expires. This field is loaded from the *Completion Timeout Resend* bit in the EEPROM (PCIe General Config word 5 bit 15).
Reserved	10	0b	Reserved.
Number of resends	12:11	11b	The number of resends in case of timeout or poisoned.
Reserved	17:13	0x0	Reserved.
PCIe Capability Version	18	1b[1]	Read only field reporting supported PCIe capability version. 0b = Capability version: 0x1. 1b = Capability version: 0x2.
Reserved	20:19	0b	Reserved.
hdr_log inversion	21	0b	If set, the header log in error reporting is written as 31:0 to log1, 63:32 in log2, etc. If not, the header is written as 127:96 in log1, 95:64 in log 2, etc.
Reserved	31:22	0	Reserved.

8.2.3.4.2 PCIe Statistic Control Register #1 — GSCL_1 (0x11010; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
GIO_COUNT_EN_0	0	0b	Enables PCIe statistic counter number 0.
GIO_COUNT_EN_1	1	0b	Enables PCIe statistic counter number 1.
GIO_COUNT_EN_2	2	0b	Enables PCIe statistic counter number 2.
GIO_COUNT_EN_3	3	0b	Enables PCIe statistic counter number 3.



Field	Bit(s)	Init Val	Description
LBC Enable 0	4	0b	When set, statistics counter 0 operates in leaky bucket mode. In this mode there is an internal counter that is incremented by one for each event and is decremented by one each time the LBC timer n (n=0) expires. When the internal counter reaches the value of LBC threshold n (n=0) the internal counter is cleared and the visible associated statistic counter GSCN_0_3[0] is incremented by one. When cleared, Leaky Bucket mode is disabled and the counter is incremented by one for each event.
LBC Enable 1	5	0b	When set, statistics counter 1 operates in leaky bucket mode. See detailed description for LBC Enable 0.
LBC Enable 2	6	0b	When set, statistics counter 2 operates in leaky bucket mode. See detailed description for LBC Enable 0.
LBC Enable 3	7	0b	When set, statistics counter 3 operates in leaky bucket mode. See detailed description for LBC Enable 0.
Reserved	26:8	0x0	Reserved.
GIO_COUNT_TEST	27	0b	Reserved.
GIO_64_BIT_EN	28	0b	Enables two 64-bit counters instead of four 32-bit counters.
GIO_COUNT_RESET	29	0b	Reset indication of PCIe statistic counters.
GIO_COUNT_STOP	30	0b	Stop indication of PCIe statistic counters.
GIO_COUNT_START	31	0b	Start indication of PCIe statistic counters.

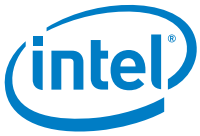
8.2.3.4.3 PCIe Statistic Control Registers #2- GSCL_2 (0x11014; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
GIO_EVENT_NUM_0	7:0	0x0	Event number that counter 0 counts (GSCN_0).
GIO_EVENT_NUM_1	15:8	0x0	Event number that counter 1 counts (GSCN_1).
GIO_EVENT_NUM_2	23:16	0x0	Event number that counter 2 counts (GSCN_2).
GIO_EVENT_NUM_3	31:24	0x0	Event number that counter 3 counts (GSCN_3).

Table 8-4 PCIe Statistic Events Encoding

Transaction layer Events	Event Mapping (Hex)	Description
Bad TLP from LL	00	For each cycle, the counter increases by one, if a bad TLP is received (bad CRC, error reported by AL, misplaced special character, reset in thI of received tlp).
Requests that reached timeout	10	Number of requests that reached time out.
NACK DLLP received	20	For each cycle, the counter increases by one, if a message was transmitted.
Replay happened in retry buffer	21	Occurs when a replay happened due to timeout (not asserted when replay initiated due to NACK.
Receive error	22	Set when one of the following occurs: 1. Decoder error occurred during training in the PHY. It is reported only when training ends. 2. Decoder error occurred during link-up or until the end of the current packet (in case the link failed). This error is masked when entering/ exiting Electrical Idle (EI).
Replay roll over	23	Occurs when replay was initiated for more than three times (threshold is configurable by the PHY CSRs).
Re-sending packets	24	Occurs when TLP is resent in case of completion timeout.
Surprise link down	25	Occurs when link is unpredictably down (not because of reset or DFT).
LTSSM in L0s in both Rx and Tx	30	Occurs when LTSSM enters L0s state in both Tx & Rx.
LTSSM in L0s in Rx	31	Occurs when LTSSM enters L0s state in Rx.
LTSSM in L0s in Tx	32	Occurs when LTSSM enters L0s state in Tx.
LTSSM in L1 active	33	Occurs when LTSSM enters L1-active state (requested from host side).
LTSSM in L1 software	34	Occurs when LTSSM enters L1-switch (requested from switch side).
LTSSM in recovery	35	Occurs when LTSSM enters recovery state.



8.2.3.4.4 PCIe Statistic Control Register #5...#8 — GSCL_5_8 (0x011030 + 4*n, n=0...3; RW)

Note: These registers are shared for both LAN ports.

These registers control the operation of the leaky bucket counter n. While it is GSCL_5 for n=0. GSCL_6 for n=1, GSCL_7 for n=2 and GSCL_8 for n=3. Note that there are no GSCL_3 and GSCL_4 registers.

Field	Bit(s)	Init Val	Description
LBC threshold n	15:0	0x0	Threshold for the leaky bucket counter n.
LBC timer n	31:16	0x0	Time period between decrementing the value in leaky bucket Counter n. The time period is defined in µS units.

8.2.3.4.5 PCIe Statistic Counter Registers #0...#3 — GSCN_0_3 (0x11020 + 4*n, n=0...3; RO)

Note: This register is shared for both LAN ports.

While it is GSCN_0 for n=0. GSCN_1 for n=1, GSCN_2 for n=2 and GSCN_3 for n=3.

Field	Bit(s)	Init Val	Description
Event Counter	31:0	0x0	Event counter as defined in GSCL_2.GIO_EVENT_NUM fields. These registers are stuck at their maximum value of 0xFF...F and cleared on read.

8.2.3.4.6 Function Active and Power State to Manageability — FACTPS (0x10150; RO)

Register for use by the device firmware for configuration.

Field	Bit(s)	Init Val	Description
Func0 Power State	1:0	00b	Power state indication of function 0. 00b = DR 01b = D0u 10b = D0a 11b = D3
LAN0 Valid	2	0b	LAN 0 Enable. When this bit is set to 0b, it indicates that the LAN 0 function is disabled. When the function is enabled, the bit is set to 1b. This bit is reflected if the function is disabled through the external pad.
Func0 Aux_En	3	0b	Function 0 *Auxiliary (AUX) Power PM Enable* bit shadow from the configuration space.
Reserved	5:4	00b	Reserved.

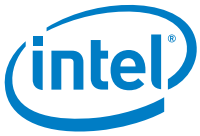
Field	Bit(s)	Init Val	Description
Func1 Power State	7:6	00b	Power state indication of function 1. 00b = DR 01b = D0u 10b = D0a 11b = D3
LAN1 Valid	8	0b	LAN 1 Enable. When this bit is set to 0b, it indicates that the LAN 1 function is disabled. When the function is enabled, the bit is set to 1b. This bit is reflected if the function is disabled through the external pad.
Func1 Aux_En	9	0b	Function 1 *Auxiliary (AUX) Power PM Enable* bit shadow from the configuration space.
Reserved	28:10	0x0	Reserved.
MNGCG	29	0b	Manageability Clock Gated. When set, indicates that the manageability clock is gated.
LAN Function Sel	30	0b[1]	When both LAN ports are enabled and *LAN Function Sel* equals 0b, LAN 0 is routed to PCI function 0 and LAN 1 is routed to PCI function 1. If *LAN Function Sel* equals 1b, LAN 0 is routed to PCI function 1 and LAN 1 is routed to PCI function 0. This bit is loaded from the *LAN Function Select* bit in the PCIe Control 2 EEPROM word at offset 0x05.
PM State changed	31	0b	Indication that one or more of the functions power states had changed. This bit is also a signal to the manageability unit to create an interrupt. This bit is cleared on read, and is not set for at least eight cycles after it was cleared.

1. Loaded from the EEPROM.

8.2.3.4.7 PCIe Analog Configuration Register — PCIEPHYADR (0x11040; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
Address	11:0	0x0	The indirect access' address.
Reserved	24:12	0x0	Reserved
Byte Enable	28:25	0x0	The indirect access' byte enable (4-bit).
Read enable	29	0b	The indirect access is read transaction.
Write enable	30	0b	The indirect access is write transaction.
Done indication	31	0b	Acknowledge for the indirect access to the CSR.



8.2.3.4.8 PCIe PHY Data Register — PCIEPHYDAT (0x11044; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
Data	31:0	0x0	The data to write in the indirect access or the returned data of the indirect read.

8.2.3.4.9 Software Semaphore Register — SWSM (0x10140; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
SMBI	0	0b	Semaphore Bit. This bit is set by hardware, when this register is read by the device driver (one of two PCI functions) and cleared when the host driver writes 0b to it. The first time this register is read, the value is 0b. In the next read the value is 1b (hardware mechanism). The value remains 1b until the device driver clears it. This bit can be used as a semaphore between the two device's drivers. This bit is cleared on PCIe reset.
SWESMBI	1	0b	Software Semaphore bit. This bit is set by the device driver (read only to the firmware) before accessing the SW_FW_SYNC register. This bit can be read as 1b only if the FWSM.FWSMBI bit is cleared. The device driver should clear this bit after accessing the SW_FW_SYNC register as described in Section 10.5.4. Hardware clears this bit on PCIe reset.
RSV	31:2	0x0	Reserved.

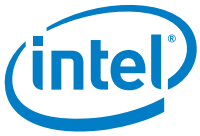
8.2.3.4.10 Firmware Semaphore Register — FWSM (0x10148; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
FWSMBI	0	0b	Firmware Semaphore. Firmware should set this bit to 1b before accessing the SW_FW_SYNC register. This bit can be read as 1b only if the SWSM.SMBI is cleared. Firmware should set it back to 0b after modifying the SW_FW_SYNC register as described in Section 10.5.4.
FW_mode	3:1	000b	Firmware Mode. Indicates the firmware mode as follows: 0x0 = None (manageability off). 0x1 = Reserved. 0x2 = PT mode. 0x3 = Reserved. 0x4 = Host interface enable only. Else = Reserved.
Reserved	5:4	00b	Reserved.

Field	Bit(s)	Init Val	Description
EEP_reload_ ind	6	0b	EEPROM Reloaded Indication. Set to 1b after firmware re-loads the EEPROM. Cleared by firmware once the *Clear Bit* host command is received from host software.
Reserved	14:7	0x0	Reserved.
FW_Val_bit	15	0b	Firmware Valid Bit. Hardware clears this bit in reset de-assertion so software can know firmware mode (bits 1-5) is invalid. firmware should set this bit to 1b when it is ready (end of boot sequence).
Reset_cnt	18:16	000b	Reset Counter. Firmware increments this counter after every reset.
Ext_err_ind	24:19	0x0	External Error Indication. Firmware uses this register to store the reason that the firmware has reset / clock gated (such as EEPROM, Flash, patch corruption, etc.). Possible values: 0x00 = No error. 0x01 = Invalid EEPROM checksum. 0x02 = Unlocked secured EEPROM. 0x03 = Clock off host command. 0x04 = Invalid Flash checksum. 0x05 = C0 checksum failed. 0x06 = C1 checksum failed. 0x07 = C2 checksum failed. 0x08 = C3 checksum failed. 0x09 = TLB table exceeded. 0x0A = DMA load failed. 0x0B = Bad hardware version in patch load. 0x0C = Flash device not supported in the 82599. 0x0D = Unspecified error. 0x3F = Reserved (maximum error value).
PCIe_config_ err_ind	25	0b	PCIe Configuration Error Indication. Set to 1b by firmware when it fails to configure PCIe interface. Cleared by firmware upon successful configuration of PCIe interface.
PHY_SERDES0_config_ err_ind	26	0b	PHY/SERDES0 Configuration Error Indication. Set to 1b by firmware when it fails to configure PHY/SERDES of LAN0. Cleared by firmware upon successful configuration of PHY/SERDES of LAN0.
PHY_SERDES1_config_ err_ind	27	0b	PHY/SERDES1 Configuration Error Indication. Set to 1b by firmware when it fails to configure PHY/SERDES of LAN1. Cleared by firmware upon successful configuration of PHY/SERDES of LAN1.
Reserved	31:28	0000b	Reserved.

Notes: This register should be written only by the manageability firmware. The device driver should only read this register.



The firmware ignores the EEPROM semaphore in operating system hung states.

Bits 15:0 are cleared on firmware reset.

8.2.3.4.11 Software–Firmware Synchronization — SW_FW_SYNC (0x10160; RW)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
SMBITS	9:0	0x0	Semaphore Bits. Each bit represents a different software semaphore agreed between software and firmware as listed. Bits 4:0 are owned by software while bits 9:5 are owned by firmware. *Note:* Hardware does not lock access to these bits. Bit 0 = SW_EEP_SM - at 1b, EEPROM access is owned by software. Bit 1 = SW_PHY_SM0 - at 1b, PHY 0 access is owned by software. Bit 2 = SW_PHY_SM1 - at 1b, PHY 1 access is owned by software. Bit 3 = SW_MAC_CSR_SM - at 1b, Software owns access to shared CSRs. Bit 4 = SW_FLASH_SM - Software Flash semaphore. Bit 5 = FW_EEP_SM - at 1b, EEPROM access is owned by firmware. Bit 6 = FW_PHY_SM0 - at 1b, PHY 0 access is owned by firmware. Bit 7 = FW_PHY_SM1 - at 1b, PHY 1 access is owned by firmware. Bit 8 = FW_MAC_CSR_SM - at 1b, firmware owns access to shared CSRs. Bit 9 = FW_FLASH_SM - at 1b, firmware owns access to the Flash. *Note:* Currently the FW does not access the FLASH.
Reserved	30:10	0x0	Reserved for future use.
Reserved	31	0b	Reserved.

See Section 10.5.4 for more details on software and firmware synchronization.

8.2.3.4.12 PCIe Control Extended Register — GCR_EXT (0x11050; RW)

Field	Bit(s)	Init Val	Description
VT_Mode	1:0	00b	VT mode of operation defines the allocation of physical registers to the VFs. Software must set this field the same as GPIE.VT_Mode. 00b = No VT - Reserved for the case that STSTUS.IOV Ena is not set. 01b = VT16 - Resources are allocated to 16 VFs. 10b = VT32 - Resources are allocated to 32 VFs. 11b = VT64 - Resources are allocated to 64 VFs.
Reserved	3:2	00b	Reserved.

Field	Bit(s)	Init Val	Description
APBACD	4	0b	Auto PBA Clear Disable. When set to 1b, Software can clear the PBA only by direct write to clear access to the *PBA* bit. When set to 0b, any active PBA entry is cleared on the falling edge of the appropriate interrupt request to the PCIe block. The appropriate interrupt request is cleared when software sets the associated interrupt mask bit in the EIMS (re-enabling the interrupt) or by direct write to clear to the PBA.
Reserved	29:5	0x0	Reserved.
Buffers Clear Func	30	0	Initiate a cleaning flow for the buffers in the transaction layer for both the read & write flows. *Note:* Should be only used during Master disable flow. See Section 5.2.5.3.2, Master Disable.
Reserved	31	0	Reserved.

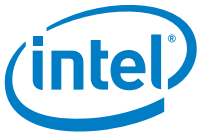
8.2.3.4.13 Mirrored Revision ID- MREVID (0x11064; RO)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
EEPROM_RevID	7:0	0x0	Mirroring of rev ID loaded from EEPROM.
DEFAULT_RevID	15:8	0x0	Mirroring of default rev ID, before EEPROM load (0x0 for the 82599 A0).
Reserved	31:16	0x0	Reserved.

8.2.3.4.14 PCIe Interrupt Cause — PICAUSE (0x110B0; RW1/C)

Field	Bit(s)	Init Val	Description
CA	0	0b	PCI completion abort exception.
UA	1	0b	Unsupported I/O address exception.
BE	2	0b	Wrong byte-enable exception in the FUNC unit.
TO	3	0b	PCI timeout exception in the FUNC unit.
BMEF	4	0b	Asserted when bus master enable of the PF or one of the VFs is de-asserted.
Reserved	31:5	0x0	Reserved



8.2.3.4.15 PCIe Interrupt Enable — PIENA (0x110B8; RW)

Field	Bit(s)	Init Val	Description
CA	0	0b	When set to 1b, the PCI completion abort interrupt is enabled.
UA	1	0b	When set to 1b, the unsupported I/O address interrupt is enabled.
BE	2	0b	When set to 1b, the wrong byte-enable interrupt is enabled.
TO	3	0b	When set to 1b, the PCI timeout interrupt is enabled.
BMEF	4	0b	When set to 1b, the bus master enable interrupt is enabled.
Reserved	31:5	0x0	Reserved

8.2.3.5 Interrupt Registers

8.2.3.5.1 Extended Interrupt Cause Register- EICR (0x00800; RW1C)

The EICR register is RW1C and can be optionally cleared on a read depending on the ODC flag setting in the GPIE register.

Field	Bit(s)	Init Val	Description
RTxQ	15:0	0x0	Receive/Transmit Queue Interrupts. One bit per queue or a bundle of queues, activated on receive/transmit events. The mapping of the queue to the RTxQ bits is done by the IVAR registers.
Flow Director	16	0b	Flow director exception is activated by one of the following events: 1. Filter Removal failed (no matched filter to be removed). 2. The number of remaining free filters in the flexible filter table exceeds (goes below) the FDIRCTRL.Full-Thresh. 3.
Rx Miss	17	0b	Missed packet interrupt is activated for each received packet that overflows the Rx packet buffer (overrun). *Note:* The packet is dropped and also increments the associated RXMPC[n] counter.
PCI Exception	18	0b	The PCI timeout exception is activated by one of the following events while the specific PCI event is reported in the INTRPT_CSR register: 1. I/O completion abort (write to Flash when Flash is write-disabled). 2. Unsupported I/O request (wrong address). 3. Byte-Enable Error. Access to a client that does not support partial byte-enable access (all but Flash, MSI-X and PCIe target). 4. Timeout occurred in the FUNC block.
MailBox	19	0b	VF to PF MailBox Interrupt. Cause by a VF write access to the PF mailbox.
LSC	20	0b	Link Status Change. This bit is set each time the link status changes (either from up to down, or from down to up).
LinkSec	21	0b	Indicates that the Tx LinkSec packet counter reached the threshold requiring key exchange.
MNG	22	0b	Manageability Event Detected. Indicates that a manageability event happened. When the device is at power down mode, the MC might generate a PME for the same events that would cause an interrupt when the device is at the D0 state.
Reserved	23	0b	Reserved.
GPI_SDP0	24	0b	General Purpose Interrupt on SDP0. If GPI interrupt detection is enabled on this pin (via GPIE), this interrupt cause is set when the SDP0 is sampled high.
GPI_SDP1	25	0b	General Purpose Interrupt on SDP1. If GPI interrupt detection is enabled on this pin (via GPIE), this interrupt cause is set when the SDP1 is sampled high.