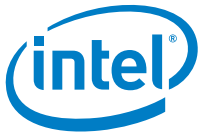


8.2.3.23.72 Rx DMA Statistic Counter Control — RXDSTATCTRL (0x02F40; RW)

Field	Bit(s)	Init Val	Description
QSEL	4:0	0x0	The *Queue Select* field controls which Rx queues are considered for the DMA good Rx and DMA duplicated counters as follows: 00000b ... 01111b = The counters relates to the same queues that are directed to the QPRC[QSEL] counter as defined by the RQSMR[n] registers. 10000b = The counters relates to all Rx queues. All other values are reserved.
Reserved	31:5	0x0	Reserved.

8.2.3.23.73 Transmit Queue Statistic Mapping Registers — TQSM[n] (0x08600 + 4*n, n=0...31; RW)

These registers define the mapping of the transmit queues to the per queue statistics. Several queues can be mapped to a single statistic register. Each statistic register counts the number of packets and bytes of all the queues that are mapped to that statistics. The registers counting Tx queue statistics are: QPTC and QBTC.

Field	Bit(s)	Init Val	Description
Q_MAP[0]	3:0	0x0	For each register 'n', Q_MAP[0] defines the per queue statistic registers that are mapped to Tx queue '4*n+0'.
Reserved	7:4	0x0	Reserved.
Q_MAP[1]	11:8	0x0	For each register 'n', Q_MAP[1] defines the per queue statistic registers that are mapped to Tx queue '4*n+1'.
Reserved	15:12	0x0	Reserved.
Q_MAP[2]	19:16	0x0	For each register 'n', Q_MAP[2] defines the per queue statistic registers that are mapped to Tx queue '4*n+2'.
Reserved	23:20	0x0	Reserved.
Q_MAP[3]	27:24	0x0	For each register 'n', Q_MAP[3] defines the per queue statistic registers that are mapped to Tx queue '4*n+3'.
Reserved	31:28	0x0	Reserved.

8.2.3.23.74 Queue Packets Received Count — QPRC[n] (0x01030 + 0x40*n, n=0...15; RC)

Field	Bit(s)	Init Val	Description
PRC	31:0	0x0	Number of packets received for the queue. FCoE packets are counted in QRPC even if they are posted only to the DDP queue (with no traces in the legacy queue).

8.2.3.23.75 Queue Packets Received Drop Count — QPRDC[n] (0x01430 + 0x40*n, n=0...15; RC)

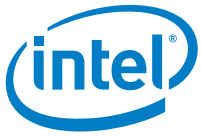
Field	Bit(s)	Init Val	Description
PRDC	31:0	0x0	Total number of receive packets dropped for the queue. Packets can be dropped for the following reasons: 1. Rx queue is disabled in the RXDCTL[n] register. 2. No free descriptors in the Rx queue while hardware is set to *Drop En* in the SRRCTL[n] register or in the PFQDE register.

8.2.3.23.76 Queue Bytes Received Count Low — QBRC_L[n] (0x01034 + 0x40*n, n=0...15; RC)

Field	Bit(s)	Init Val	Description
BRC_L	31:0	0x0	Lower 32 bits of the statistic counter. The QBRC_L[n] and QBRC_H[n] registers make up a logical 36-bit counter of received bytes that were posted to the programmed Rx queues of the packets counted by QPRC[n]. The counter counts all bytes posted to the host before VLAN strip. Furthermore, bytes of RSC and FCoE are counted before coalescing or DDP.

8.2.3.23.77 Queue Bytes Received Count High — QBRC_H[n] (0x01038 + 0x40*n, n=0...15; RC)

Field	Bit(s)	Init Val	Description
BRC_H	3:0	0x0	Higher four bits of the statistic counter described in QBRC_L.
Reserved	31:4	0x0	Reserved.



8.2.3.23.78 Queue Packets Transmitted Count — QPTC[n] (0x08680 + 0x4*n, n=0...15 / 0x06030 + 0x40*n, n=0...15; RC)

These registers are also mapped to 0x06030 to maintain compatibility with the 82598.

Field	Bit(s)	Init Val	Description
PTC	31:0	0x0	Number of packets transmitted for the queue. A packet is considered as transmitted if it is was forwarded to the MAC unit for transmission to the network and/or is accepted by the internal Tx to Rx switch enablement logic. Packets dropped due to anti-spoofing filtering or VLAN tag validation (as described in Section 7.10.3.9.2) are not counted.

8.2.3.23.79 Queue Bytes Transmitted Count Low — QBTC_L[n] (0x08700 + 0x8*n, n=0...15; RC)

Field	Bit(s)	Init Val	Description
BTC_L	31:0	0x0	Lower 32 bits of the statistic counter. The QBTC_L and QBTC_H registers make up a logical 36-bit counter of transmitted bytes of the packets counted by the matched QPTC counter. These registers count all bytes in the packets from the <Destination Address> field through the <CRC> field, inclusively. These registers must be accessed as two consecutive 32-bit entities while the QBTC_L register is read first, or a single 64-bit read cycle. Each register is read cleared. In addition, it sticks at 0xFF...F to avoid overflow.

8.2.3.23.80 Queue Bytes Transmitted Count High — QBTC_H[n] (0x08704 + 0x8*n, n=0...15; RC)

Field	Bit(s)	Init Val	Description
BTC_H	3:0	0x0	Higher four bits of the statistic counter described in QBTC_L.
Reserved	31:4	0x0	Reserved.

8.2.3.23.81 FC CRC Error Count — FCCRC (0x05118; RC)

Field	Bit(s)	Init Val	Description
CRC_CNT	15:0	0x0	FC CRC Count. Count the number of packets with good Ethernet CRC and bad FC CRC.
Reserve	31:16	N/A	Reserved.

8.2.3.23.82 FCoE Rx Packets Dropped Count — FCOERPDC (0x0241C; RC)

Field	Bit(s)	Init Val	Description
RPDC	31:0	0x0	Number of Rx packets dropped due to lack of descriptors.

8.2.3.23.83 FC Last Error Count — FCLAST (0x02424; RC)

Field	Bit(s)	Init Val	Description
Last_CNT	15:0	0x0	Number of packets received to valid FCoE contexts while their user buffers are exhausted.
Reserve	31:16	N/A	Reserved.

8.2.3.23.84 FCoE Packets Received Count — FCOEPRC (0x02428; RC)

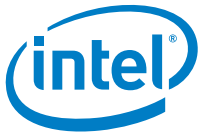
Field	Bit(s)	Init Val	Description
PRC	31:0	0x0	Number of FCoE packets posted to the host. In normal operation (no save bad frames) it equals to the number of good packets.

8.2.3.23.85 FCOE DWord Received Count — FCOEDWRC (0x0242C; RC)

Field	Bit(s)	Init Val	Description
DWRC	31:0	0x0	Number of DWords count in good received packets with no Ethernet CRC or FC CRC errors. The counter relates to FCoE packets starting at the FC header up to and including the FC CRC (it excludes Ethernet encapsulation).

8.2.3.23.86 FCoE Packets Transmitted Count — FCOEPTC (0x08784; RC)

Field	Bit(s)	Init Val	Description
PTC	31:0	0x0	Number of FCoE packets transmitted. *Note:* The counter does not include packets dropped due to anti-spoofing filtering or VLAN tag validation as described in Section 7.10.3.9.2. This rule is applicable if FCoE traffic is sent by a VF.



8.2.3.23.87 FCoE DWord Transmitted Count — FCOEDWTC (0x08788; RC)

Field	Bit(s)	Init Val	Description
DWTC	31:0	0x0	Number of DWords count in transmitted packets. The counter relates to FCoE packets starting at the FC header up to and including the FC CRC (it excludes Ethernet encapsulation).

8.2.3.24 Wake Up Control Registers

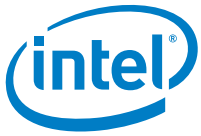
8.2.3.24.1 Wake Up Control Register — WUC (0x05800; RW)

Field	Bit(s)	Init Val	Description
Reserved	0	0b	Reserved .
PME_En	1	0b	PME_En. This bit is used by the driver to enable wakeup capabilities as programmed by the WUFC register. Wakeup is further gated by the PME_En bit of the PMCS register. *Note:* Setting the PME_En bit in the PMCSR register also sets this bit.
PME_Status (RO)	2	0b	PME_Status. This bit is set when the 82599 receives a wake-up event. It is the same as the PME_Status bit in the PMCSR. Writing a 1b to this bit clears it. The *PME_Status* bit in the PMCSR is also cleared.
Reserved	3	0b	Reserved.
WKEN	4	1b	WKEN This bit can be cleared to disable PE_WAKE_N pin de-assertion even if APM is enabled in the EEPROM. In this case, PMCSR wake-up status will be invalid. Refer to Section 5.3 for the correct way to enable APM with valid status. *Note:* This bit should not be cleared while in ACPI mode.
Reserved	31:5	0x0	Reserved.

The *PME_En* and *PME_Status* bits are reset when LAN_PWR_GOOD is 0b. When AUX_PWR=0b these bits are also reset by the assertion of PE_RST_N.

8.2.3.24.2 Wake Up Filter Control Register — WUFC (0x05808; RW)

Field	Bit(s)	Init Val	Description
LNKC	0	0b	Link Status Change Wake Up Enable.
MAG	1	0b	Magic Packet Wake Up Enable.
EX	2	0b	Directed Exact Wake Up Enable.
MC	3	0b	Directed Multicast Wake Up Enable. Setting this bit does not enable broadcast packets that are enabled by the *BC* bit in this register.
BC	4	0b	Broadcast Wake Up Enable.
ARP	5	0b	ARP/IPv4 Request Packet Wake Up Enable.
IPV4	6	0b	Directed IPv4 Packet Wake Up Enable.
IPV6	7	0b	Directed IPv6 Packet Wake Up Enable.



Field	Bit(s)	Init Val	Description
Reserved	14:8	0x0	Reserved.
NoTCO	15	0b	Ignore TCO Packets for TCO.
FLX0	16	0b	Flexible Filter 0 Enable.
FLX1	17	0b	Flexible Filter 1 Enable.
FLX2	18	0b	Flexible Filter 2 Enable.
FLX3	19	0b	Flexible Filter 3 Enable.
FLX4	20	0b	Flexible Filter 4 Enable.
FLX5	21	0b	Flexible Filter 5 Enable.
Reserved	31:22	0b	Reserved.

This register is used to enable each of the pre-defined and flexible filters for wake up support. A value of one means the filter is turned on, and a value of zero means the filter is turned off.

If the *NoTCO* bit is set, then any packet that passes the manageability packet filtering does not cause a wake up event even if it passes one of the wake up filters.

8.2.3.24.3 Wake Up Status Register — WUS (0x05810; RW1C)

Field	Bit(s)	Init Val	Description
Reserved	31:0	0x0	Reserved.

Note: This register is de-featured and software should not read it. To enable ACPI, this register must be cleared by writing 0x3F01FF.

8.2.3.24.4 IP Address Valid — IPAV (0x5838; RW)

The IP address valid indicates whether the IP addresses in the IP address table are valid:

Field	Bit(s)	Init Val	Description
V40	0	0b[1]	IPv4 Address 0 Valid.
V41	1	0b	IPv4 Address 1 Valid.
V42	2	0b	IPv4 Address 2 Valid.
V43	3	0b	IPv4 Address 3 Valid.
Reserved	15:4	0x0	Reserved

Field	Bit(s)	Init Val	Description
V60	16	0b	IPv6 Address 0 Valid.
Reserved	31:17	0x0	Reserved

1. Loaded from EEPROM

8.2.3.24.5 IPv4 Address Table — IP4AT[n] (0x05840 + 8*n, n = 0...3; RW)

4 x IPv4 addresses for ARP/IPv4 request packet and directed IPv4 packet wake up. IPv4[0] is loaded from MIPAF words in the EEPROM.

Field	Bit(s)	Init Val	Description
IPV4ADDR	31:0	X	IPv4 Address ‘n’, ‘n’ = 0...3.

8.2.3.24.6 IPv6 Address Table — IP6AT[n] (0x05880 + 4*n, n = 0...3; RW)

1 x IPv6 addresses for a neighbor discovery packet filtering and directed IPv6 packet wake up. According to the power management section; one Ipv6 address is supported and it is programmed in the Ipv6 Address Table (IP6AT)

Field	Bit(s)	Init Val	Description
IPV6ADDR	31:0	X	4 x Register IPv6 filter. Register ‘n’ contains bytes ‘4*n’ up to ‘4*n+3’ of the IPv6 address. LS byte of register ‘0’ is first on the wire.

8.2.3.24.7 Wake Up Packet Length — WUPL (0x05900; RO)

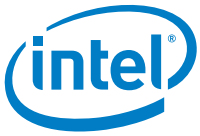
This register is de-featured and software should not access it (not read nor write)

8.2.3.24.8 Wake Up Packet Memory (128 Bytes) — WUPM[n] (0x05A00 + 4*n, n=0...31; RO)

This register is de-featured and software should not access it (not read nor write)

8.2.3.24.9 Flexible Host Filter Table Registers — FHFT (0x09000 — 0x093FC and 0x09800 — 0x099FC; RW)

Each of the six Flexible Host Filters Table (FHFT) registers contains a 128-byte pattern and a corresponding 128-bit mask array. If enabled, the first 128 bytes of the received packet are compared against the non-masked bytes in the FHFT register.



Each 128-byte filter is composed of 32 Dword entries, where each two Dwords are accompanied by an 8-bit mask, one bit per filter byte.

Note: The *Length* field must be eight byte-aligned. For filtering packets shorter than eight byte-aligned the values should be rounded up to the next eight byte-aligned value, hardware implementation compares eight bytes at a time so it should get extra zero masks (if needed) until the end of the length value.

If the actual length, which is defined by the Length Field register and the mask bits is not eight byte-aligned, there might be a case that a packet, which is shorter then the actual required length pass the flexible filter. This can happen due to a comparison of up to seven bytes that come after the packet but are not a real part of the packet.

The last Dword of each filter contains a *Length* field defining the number of bytes from the beginning of the packet compared by this filter, the *Length* field should be an eight byte-aligned value. If the actual packet length is less than (length — 8) (length is the value specified by the *Length* field), the filter fails. Otherwise, it depends on the result of actual byte comparison. The value should not be greater than 128.

31 0	31 8	7 0	31 0	31 0
Reserved	Reserved	Mask [7:0]	Dword 1	Dword 0
Reserved	Reserved	Mask [15:8]	Dword 3	Dword 2
Reserved	Reserved	Mask [23:16]	Dword 5	Dword 4
Reserved	Reserved	Mask [31:24]	Dword 7	Dword 6

. . .

31 7	6 0	31 8	7 0	31 0	31 0
Reserved	Reserved	Reserved	Mask [127:120]	Dword 29	Dword 28
Reserved	Length	Reserved	Mask [127:120]	Dword 31	Dword 30

Each of the filters have allocated addresses as follows:

- Filter 0 — 0x09000 — 0x090FF
- Filter 1 — 0x09100 — 0x091FF
- Filter 2 — 0x09200 — 0x092FF
- Filter 3 — 0x09300 — 0x093FF
- Filter 4 — 0x09800 — 0x098FF
- Filter 5 — 0x09900 — 0x099FF

The following table lists the addresses used for filter 0.

Field	Dword	Address	Bit(s)	Initial Value
Filter 0 DW0	0	0x09000	31:0	X
Filter 0 DW1	1	0x09004	31:0	X
Filter 0 Mask[7:0]	2	0x09008	7:0	X
Reserved	3	0x0900C		X
Filter 0 DW2	4	0x09010	31:0	X
…				
Filter 0 DW30	60	0x090F0	31:0	X
Filter 0 DW31	61	0x090F4	31:0	X
Filter 0 Mask[127:120]	62	0x090F8	7:0	X
Length	63	0x090FC	6:0	X

Accessing the FHFT registers during filter operation can result in a packet being mis-classified if the write operation collides with packet reception. As a result, it is recommended that the flex filters be disabled prior to changing their setup.

8.2.3.25 Management Filters Registers

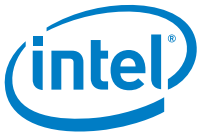
The Management Filters registers are RO for the host. These registers are initialized at LAN Power Good and can be loaded from the EEPROM by the manageability firmware.

8.2.3.25.1 Management VLAN TAG Value — MAVTV[n] (0x5010 +4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
VID	11:0	0x0	Contain the VLAN ID that should be compared with the incoming packet if the corresponding bit in MFVAL.VLAN is set.
Reserved	31:12	0x0	Reserved.

8.2.3.25.2 Management Flex UDP/TCP Ports — MFUTP[n] (0x5030 + 4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
MFUTP[2n]	15:0	0x0	(2n)-th Management Flex UDP/TCP port.
MFUTP[2n+1]	31:16	0x0	(2n+1)-th Management Flex UDP/TCP port.



Each 32-bit register (n=0,…,7) refers to two port filters (register 0 refers to ports 0 and 1, register 2 refers to ports 2 and 3, etc.). Note that SCTP packets do not match the MFUTP filters.

8.2.3.25.3 Management Ethernet Type Filters- METF[n] (0x05190 + 4*n, n=0...3; RW)

Field	Bit(s)	Init Val	Description
EType	15:0	0x0	EtherType value to be compared against the L2 *EtherType* field in the Rx packet. *Note:* Appears in little endian order (high byte first on the wire).
Reserved	29:16	0x0	Reserved.
Polarity	30	0b	0b = Positive filter. Filter enters the decision filters if a match occurred. 1b = Negative filter. Filter enters the decision filters if a match did not occur.
Reserved	31	0b	Reserved.

8.2.3.25.4 Management Control Register — MANC (0x05820; RW)

Field	Bit(s)	Init Val	Description
Reserved	16:0	0x0	Reserved.
RCV_TCO_EN	17	0b	Receive TCO Packets Enabled. When this bit is set it enables the receive flow from the wire to the manageability block.
Reserved	18	0b	Reserved.
RCV_ALL	19	0b	Receive All Enable. When set, all packets are received from the wire and passed to the manageability block.
MCST_PASS_L2	20	0b	Receive All Multicast. When set, all received multicast packets pass L2 filtering and can be directed to the MNG or Host by ~~a~~ one of the decision filters. Broadcast packets are not forwarded by this bit.
EN_MNG2HOST	21	0b	Enable manageability packets to host memory. This bit enables the functionality of the MANC2H register. When set the packets that are specified in the MANC2H registers are also forwarded to host memory, if they pass manageability filters.
Bypass VLAN	22	0b	When set, VLAN filtering is bypassed for MNG packets.
EN_XSUM_FILTER	23	0b	When set, this bit enables Xsum filtering to manageability. Meaning, only packets that pass L3, L4 checksum are sent to the manageability block. *Note:* This capability is not provided for tunneled packets.
EN_IPv4_FILTER	24	0b	Enable IPv4 address Filters. When set, the last 128 bits of the MIPAF register are used to store four IPv4 addresses for IPv4 filtering. When cleared, these bits store a single IPv6 filter.

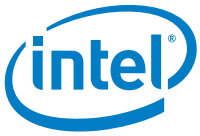
Field	Bit(s)	Init Val	Description
FIXED_NET_TYPE	25	0b	Fixed Next Type. If set, only packets matching the net type defined by the NET_TYPE field pass to manageability. Otherwise, both tagged and un-tagged packets can be forwarded to the manageability engine.
NET_TYPE	26	0b	Net Type. 0b = Pass only un-tagged packets. 1b = Pass only VLAN tagged packets. Valid only if FIXED_NET_TYPE is set.
Reserved	31:27	0x0	Reserved.

8.2.3.25.5 Manageability Filters Valid — MFVAL (0x5824; RW)

Field	Bit(s)	Init Val	Description
MAC	3:0	0x0	MAC. Indicates if the MAC unicast filter registers (MMAH, MMAL) contain valid Ethernet MAC Addresses. Bit 0 corresponds to filter 0, etc.
Reserved	7:4	0x0	Reserved.
VLAN	15:8	0x0	VLAN. Indicates if the VLAN filter registers (MAVTV) contain valid VLAN tags. Bit 8 corresponds to filter 0, etc.
IPv4	19:16	0x0	IPv4. Indicates if the IPv4 address filters (MIPAF) contain valid IPv4 addresses. Bit 16 corresponds to IPv4 address 0. These bits apply only when IPv4 address filters are enabled (MANC.EN_IPv4_FILTER=1).
Reserved	23:20	0x0	Reserved.
IPv6	27:24	0x0	IPv6. Indicates if the IPv6 address filter registers (MIPAF) contain valid IPv6 addresses. Bit 24 corresponds to address 0, etc. Bit 27 (filter 3), applies only when IPv4 address filters are not enabled. (MANC.EN_IPv4_FILTER=0).
Reserved	31:28	0x0	Reserved.

8.2.3.25.6 Management Control To Host Register — MANC2H (0x5860; RW)

Field	Bit(s)	Init Val	Description
Host Enable	7:0	0x0	Host Enable. When set, indicates that packets routed by the manageability filters to manageability are also sent to the host. Bit 0 corresponds to decision filter (MDEF[0] and MDEF_EXT[0]), bit 1 corresponds to decision filter (MDEF[1] and MDEF_EXT[1]), etc. The MANC2H routing is further enabled by a global MANC.EN_MNG2HOST bit.
Reserved	31:8	0x0	Reserved.



8.2.3.25.7 Manageability Decision Filters- MDEF[n] (0x5890 + 4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
Unicast (AND)	0	0b	Unicast. Controls the inclusion of unicast address filtering in the manageability filter decision (AND section).
Broadcast (AND)	1	0b	Broadcast. Controls the inclusion of broadcast address filtering in the manageability filter decision (AND section).
VLAN (AND)	2	0b	VLAN. Controls the inclusion of VLAN address filtering in the manageability filter decision (AND section).
IP Address (AND)	3	0b	IP Address. Controls the inclusion of IP address filtering in the manageability filter decision (AND section).
Unicast (OR)	4	0b	Unicast. Controls the inclusion of unicast address filtering in the manageability filter decision (OR section).
Broadcast (OR)	5	0b	Broadcast. Controls the inclusion of broadcast address filtering in the manageability filter decision (OR section).
Multicast (AND)	6	0b	Multicast. Controls the inclusion of multicast address filtering in the manageability filter decision (AND section). Broadcast packets are not included by this bit. The packet must pass some L2 filtering to be included by this bit – either by the MANC.MCST_PASS_L2 or by some dedicated Ethernet MAC Address.
ARP Request (OR)	7	0b	ARP Request. Controls the inclusion of ARP request filtering in the manageability filter decision (OR section).
ARP Response (OR)	8	0b	ARP Response. Controls the inclusion of ARP response filtering in the manageability filter decision (OR section).
Neighbor Discovery (OR)	9	0b	Neighbor Discovery. Controls the inclusion of neighbor discovery filtering in the manageability filter decision (OR section). The neighbor types accepted by this filter are types 0x86, 0x87, 0x88 and 0x89.
Port 0x298 (OR)	10	0b	Port 0x298. Controls the inclusion of port 0x298 filtering in the manageability filter decision (OR section).
Port 0x26F (OR)	11	0b	Port 0x26F. Controls the inclusion of port 0x26F filtering in the manageability filter decision (OR section).

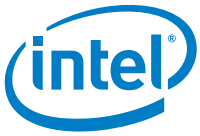
Field	Bit(s)	Init Val	Description
Flex port (OR)	27:12	0x0	Flex Port. Controls the inclusion of flex port filtering in the manageability filter decision (OR section). Bit 12 corresponds to flex port 0, etc.
Flex TCO (OR)	31:28	0x0	Flex TCO. Controls the inclusion of Flex TCO filtering in the manageability filter decision (OR section). Bit 28 corresponds to Flex TCO filter 0, etc.

8.2.3.25.8 Manageability Decision Filters- MDEF_EXT[n] (0x05160 + 4*n, n=0...7; RW)

Field	Bit(s)	Init Val	Description
L2 EtherType (AND)	3:0	0x0	L2 EtherType. Controls the inclusion of L2 EtherType filtering in the manageability filter decision (AND section).
Reserved	7:4	0x0	Reserved for additional L2 EtherType AND filters.
L2 EtherType (OR)	11:8	0x0	L2 EtherType. Controls the inclusion of L2 EtherType filtering in the manageability filter decision (OR section).
Reserved	15:12	0x0	Reserved for additional L2 EtherType OR filters.
Reserved	31:16	0x0	Reserved.

8.2.3.25.9 Manageability IP Address Filter — MIPAF[m,n] (0x58B0 + 0x10*m + 4*n, m=0...3, n=0...3; RW)

Field	Bit(s)	Init Val	Description
IP_ADDR	31:0	X	Manageability IP Address Filters. For each n, m, m=0...3, n=0...3 while MANC.EN_IPv4_FILTER = 0, MIPAF[m,n] register holds Dword ‘n’ of IPv6 filter ‘m’ (4 x IPv6 filters). For each n, m, m=0...3, n=0...3 while MANC.EN_IPv4_FILTER = 1, MIPAF[m,n] registers for m=0,1,2 is the same as the previous case (3 x IPv6 filters). And MIPAF[3,n] registers holds IPv4 filter ‘n’ (4 x IPv4 filters). *Note:* These registers appear in big endian order (LS byte, LS address is first on the wire).



8.2.3.25.10 Manageability Ethernet MAC Address Low — MMAL[n] (0x5910 + 8*n, n=0...3; RW)

Field	Bit(s)	Init Val	Description
MMAL	31:0	X	Manageability Ethernet MAC Address Low. The lower 32 bits of the 48-bit Ethernet MAC address. *Note:* Appears in big endian order (LS byte of MMAL is first on the wire).

8.2.3.25.11 Manageability Ethernet MAC Address High — MMAH[n] (0x5914 + 8*n, n=0...3; RW)

Field	Bit(s)	Init Val	Description
MMAH	15:0	X	Manageability Ethernet MAC Address High. The upper 16 bits of the 48-bit Ethernet MAC address. *Note:* Appears in big endian order (MS byte of MMAH is last on the wire).
Reserved	31:16	0x0	Reserved. Reads as 0x0. Ignored on write.

8.2.3.25.12 Flexible TCO Filter Table Registers — FTFT (0x09400-0x097FC; RW)

Each of the four Flexible TCO Filters Table (FTFT) registers contains a 128-byte pattern and a corresponding 128-bit mask array. If enabled, the first 128 bytes of the received packet are compared against the non-masked bytes in the FTFT register.

Note: FTFT registers are configured by firmware. Host write/read access to these registers should be avoided.

Each 128-byte filter is composed of 32 Dword entries, where each two Dwords are accompanied by an 8-bit mask, one bit per filter byte. 15:8] etc. The *Mask* field is set so that bit 0 in the mask masks byte 0, bit 1 masks byte 1 etc. A value of one in the *Mask* field means that the appropriate byte in the filter should be compared to the appropriate byte in the incoming packet.

Notes: The *Mask* field must be eight byte-aligned even if the *Length* field is not eight byte-aligned as the hardware implementation compares eight bytes at a time so it should get extra masks until the end of the next Qword. Any *Mask* bit that is located after the length should be set to zero indicating no comparison should be done.

If the actual length, which is defined by the Length Field register and the mask bits is not eight byte-aligned, there might be a case where a packet, which is shorter then the actual required length passes the flexible filter. This can happen due to a comparison of up to seven bytes that come after the packet but are not a real part of the packet.

The last Dword of each filter contains a *Length* field defining the number of bytes from the beginning of the packet compared by this filter. If actual packet length is less than the length specified by this field, the filter fails. Otherwise, it depends on the result of actual byte comparison. The value should not be greater than 128.

31 0	31 8	7 0	31 0	31 0
Reserved	Reserved	Mask [7:0]	Dword 1	Dword 0
Reserved	Reserved	Mask [15:8]	Dword 3	Dword 2
Reserved	Reserved	Mask [23:16]	Dword 5	Dword 4
Reserved	Reserved	Mask [31:24]	Dword 7	Dword 6

. . .

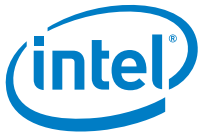
31 0	31 8	7 0	31 0	31 0
Reserved	Reserved	Mask [127:120]	Dword 29	Dword 28
Length	Reserved	Mask [127:120]	Dword 31	Dword 30

Field	Dword	Address	Bit(s)	Initial Value
Filter 0 DW0	0	0x09400	31:0	X
Filter 0 DW1	1	0x09404	31:0	X
Filter 0 Mask[7:0]	2	0x09408	7:0	X
Reserved	3	0x0940C		X
Filter 0 DW2	4	0x09410	31:0	X
…				
Filter 0 DW30	60	0x094F0	31:0	X
Filter 0 DW31	61	0x094F4	31:0	X
Filter 0 Mask[127:120]	62	0x094F8	7:0	X
Length	63	0x094FC	6:0	X

8.2.3.25.13 LinkSec Software/Firmware Interface — LSWFW (0x015F14; RO)

Note: This register is shared for both LAN ports.

Field	Bit(s)	Init Val	Description
Lock LinkSec Logic	0	0b	Block LinkSec 0b = Host can access LinkSec registers. 1b = Host cannot access LinkSec registers.
Block host traffic	1	0b	When set, all host traffic (Tx and Rx) is blocked.
Request LinkSec (SC)	2	0b	When set, a message is sent to the MC, requesting access to the LinkSec registers.
Release LinkSec (SC)	3	0b	When set, a message is sent to the MC, releasing ownership of the LinkSec registers.



Field	Bit(s)	Init Val	Description
Reserved	7:4	0x0	Reserved.
LinkSec Ownership	8	0b	Set by firmware to indicate the status of the LinkSec ownership: 0b = LinkSec owned by host (default). 1b = LinkSec owned by MC.
Reserved	31:9	0x0	Reserved.

Note: The access rules on this register are for the driver software.

8.2.3.26 Time Sync (IEEE 1588) Registers

8.2.3.26.1 Rx Time Sync Control Register — TSYNCRXCTL (0x05188; RW)

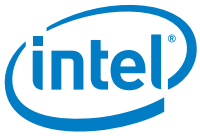
Field	Bit(s)	Init Val	Description
RXTT(RO/V)	0	0b	Rx Time Stamp Valid. Equals 1b when a valid value for Rx time stamp is captured in the Rx Time Stamp register. Cleared by read of Rx Time Stamp (RXSTMPH) register.
Type	3:1	0x0	Type of packets to time stamp: 000b = Time stamp L2 (V2) packets only (sync or Delay_req depends on message type in Section 8.2.3.26.6 and packets with message ID 2 and 3). 001b = Time stamp L4 (V1) packets only (sync or Delay_req depends on message type in Section 8.2.3.26.6). 010b = Time stamp V2 (L2 and L4) packets (sync or Delay_req depends on message type in Section 8.2.3.26.6 and packets with message ID 2 and 3). 101b = Time stamp all packets in which message ID bit 3 is zero, which means time stamp all event packets. This is applicable for V2 packets only. 011b = Reserved 100b = Reserved 110b = Reserved 111b = Reserved
En	4	0b	Enable Rx Time Stamp. 0x0 = Time stamping disabled. 0x1 = Time stamping enabled.
RSV	31:5	0x0	Reserved.

8.2.3.26.2 Rx Time Stamp Low — RXSTMPL (0x051E8; RO)

Field	Bit(s)	Init Val	Description
RXSTMPL	31:0	0x0	Rx time stamp LSB value.

8.2.3.26.3 Rx Time Stamp High — RXSTMPH (0x051A4; RO)

Field	Bit(s)	Init Val	Description
RXSTMPH	31:0	0x0	Rx time stamp MSB value.



8.2.3.26.4 Rx Time Stamp Attributes Low — RXSATRL (0x051A0; RO)

Field	Bit(s)	Init Val	Description
SourceIDL	31:0	0x0	Sourceuuid Low. Captured bytes 24-27 in the PTP message as listed in Section 7.9.5 while the MS byte is last on the wire. In a V1 PTP packet it is the 4 LS bytes of the *Sourceuuid* field and in V2 PTP packet it is part of the *Source Port ID* field.

8.2.3.26.5 Rx Time Stamp Attributes High- RXSATRH (0x051A8; RO)

Field	Bit(s)	Init Val	Description
SourceIDH	15:0	0x0	Sourceuuid High. Captured bytes 22-23 in the PTP message as listed in Section 7.9.5 while the LS byte is first on the wire. In a V1 PTP packet it is the 2 MS bytes of the *Sourceuuid* field and in V2 PTP packet it is part of the *Source Port ID* field.
SequenceID	31:16	0x0	Sequence Id. Captured value of the *SequenceID* field in the PTP Rx packet while LS byte first on the wire.

8.2.3.26.6 Rx Message Type Register Low — RXMTRL (0x05120; RW)

Field	Bit(s)	Init Val	Description
CTRLT	7:0	0x0	V1 control to time stamp.
MSGT	15:8	0x0	V2 message ID to time stamp.
UDPT	31:16	0x319	UDP port number to time stamp.

8.2.3.26.7 Tx Time Sync Control Register — TSYNCTXCTL (0x08C00; RW)

Field	Bit(s)	Init Val	Description
TXTT(RO/V)	0	0b	Tx Time Stamp Valid. Equals 1b when a valid value for Tx time stamp is captured in the Tx Time Stamp register. Cleared by read of Tx Time Stamp (TXSTMPH) register.
RSV	3:1	0x0	Reserved.

Field	Bit(s)	Init Val	Description
EN	4	0x0	Enable Tx Time Stamp. 0x0 Time stamping disabled. 0x1 Time stamping enabled.
RSV	31:5	0x0	Reserved.

8.2.3.26.8 Tx Time Stamp Value Low — TXSTMPL (0x08C04; RO)

Field	Bit(s)	Init Val	Description
TXSTMPL	31:0	0x0	Tx time stamp LSB value.

8.2.3.26.9 Tx Time Stamp Value High — TXSTMPH (0x08C08; RO)

Field	Bit(s)	Init Val	Description
TXSTMPH	31:0	0x0	Tx time stamp MSB value.

8.2.3.26.10 System Time Register Low — SYSTIML (0x08C0C; RW)

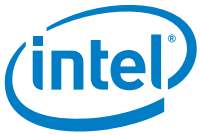
Field	Bit(s)	Init Val	Description
STL	31:0	0x0	System time LSB register.

8.2.3.26.11 System Time Register High — SYSTIMH (0x08C10; RW)

Field	Bit(s)	Init Val	Description
STH	31:0	0x0	System time MSB register.

8.2.3.26.12 Increment Attributes Register — TIMINCA (0x08C14; RW)

Field	Bit(s)	Init Val	Description
IV	23:0	0x0	Increment Value (*incvalue).*
IP	31:24	0x0	Increment Period (*incperiod)*. *Note:* The minimum permitted functional value is two.



8.2.3.26.13 Time Adjustment Offset Register Low — TIMADJL (0x08C18; RW)

Field	Bit(s)	Init Val	Description
TADJL	31:0	0x0	Time Adjustment Value Low.

8.2.3.26.14 Time Adjustment Offset Register High — TIMADJH (0x08C1C; RW)

Field	Bit(s)	Init Val	Description
TADJH	30:0	0x0	Time Adjustment Value High.
Sign	31	0x0	Sign (“0”=”+”, “1”=”-“).

8.2.3.26.15 TimeSync Auxiliary Control Register — TSAUXC (0x08C20; RW)

Field	Bit(s)	Init Val	Description
EN_TT0	0	0b	Enable Target Time 0.
EN_TT1	1	0b	Enable Target Time 1.
Reserved	2	0b	Reserved.
UTT0	3	0b	Use target time 0 to clear clk_out 0 down counter.
ST0	4	0b	Start clock out toggle only if target of clock out occurs.
Reserved	5	0b	Reserved.
UTT1	6	0b	Use target time 1 to clear clk_out 1 down counter.
ST1	7	0b	Start clock out toggle only on target time 1, at this point a rising edge of clock out occurs.
EN_TS0	8	0b	Enable Hardware Time Stamp 0.
AUTT0	9	0b	Auxiliary Time Stamp Taken. Cleared when read after an auxiliary time stamp 0 occurred.
EN_TS1	10	0b	Enable Hardware Time Stamp 1.
AUTT1	11	0b	Auxiliary Time Stamp Taken. Cleared when read after auxiliary time stamp 1 occurred.

Field	Bit(s)	Init Val	Description
Mask	16:12	0b	Masking Value for Target Time. The value in this field determines the masked bits in the comparison of the system time and target time (where 0 = no masking, 1 = bit 0 is masked, 2 = bit 0 and 1 are masked and so on up to 24 in which bits 0 through bit 23 are masked. Any value higher than 24 are reserved).
RSV	31:17	0b	Reserved.

8.2.3.26.16 Target Time Register 0 Low — TRGTTIML0 (0x08C24; RW)

Field	Bit(s)	Init Val	Description
TTL	31:0	0x0	Target time 0 LSB register.

8.2.3.26.17 Target Time Register 0 High — TRGTTIMH0 (0x08C28; RW)

Field	Bit(s)	Init Val	Description
TTH	31:0	0x0	Target time 0 MSB register.

8.2.3.26.18 Target Time Register 1 Low — TRGTTIML1 (0x08C2C; RW)

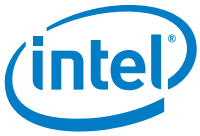
Field	Bit(s)	Init Val	Description
TTL	31:0	0x0	Target time 1 LSB register.

8.2.3.26.19 Target Time Register 1 High — TRGTTIMH1 (0x08C30; RW)

Field	Bit(s)	Init Val	Description
TTH	31:0	0x0	Target time 1 MSB register.

8.2.3.26.20 Frequency Out 0 Control Register — FREQOUT0 (0x08C34; RW) SEC-Tx

Field	Bit(s)	Init Val	Description
RLV	31:0	0x0	Reload value for frequency out zero down counter.



8.2.3.26.21 Frequency Out 1 Control Register — FREQOUT1 (0x08C38; RW) SEC-Tx

Field	Bit(s)	Init Val	Description
RLV	31:0	0x0	Reload value for frequency out one down counter.

8.2.3.26.22 Auxiliary Time Stamp 0 Register Low — AUXSTMPL0 (0x08C3C; RO)

Field	Bit(s)	Init Val	Description
TST_Low	31:0	0x0	Auxiliary time stamp 0 LSB value.

8.2.3.26.23 Auxiliary Time Stamp 0 Register High — AUXSTMPH0 (0x08C40; RO)

Field	Bit(s)	Init Val	Description
TST_Hi	31:0	0x0	Auxiliary time stamp 0 MSB value.

8.2.3.26.24 Auxiliary Time Stamp 1 Register Low — AUXSTMPL1 (0x08C44; RO)

Field	Bit(s)	Init Val	Description
TST_Low	31:0	0x0	Auxiliary time stamp 1 LSB value.

8.2.3.26.25 Auxiliary Time Stamp 1 Register High — AUXSTMPH1 (0x08C48; RO)

Field	Bit(s)	Init Val	Description
TST_Hi	31:0	0x0	Auxiliary time stamp 1 MSB value.

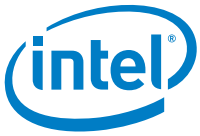
8.2.3.27 Virtualization PF Registers

8.2.3.27.1 VT Control Register — PFVTCTL (0x051B0; RW)

Field	Bit(s)	Init Val	Description
VT_Ena	0	0b	Virtualization Enabled Mode. When set, the 82599 supports either 16, 32, or 64 pools. When cleared, Rx traffic is handled internally as if it belongs to VF zero while VF zero is enabled. This bit should be set the same as MTQC.VT_Ena.
Reserved	6:1	0x0	Reserved.
DEF_PL	12:7	0x0	Default Pool. Pool assignment for packets that do not pass any pool queuing decision. Enabled by the *Dis_Def_Pool* bit.
Reserved	28:13	0x0	Reserved.
Dis_Def_Pool	29	0b	Disable Default Pool. Determines the behavior of an Rx packet that does not match any Rx filter and is therefore not allocated a destination pool. 0b = Packet is assigned to the default pool (see DEF_PL). 1b = Packet is dropped.
Rpl_En	30	0b	Replication Enable, when set to 1b.
Reserved	31	0b	Reserved.

8.2.3.27.2 PF Mailbox — PFMailbox[n] (0x04B00 + 4*n, n=0...63; RW)

Field	Bit(s)	Init Val	Description
Sts (WO)	0	0b	Status/Command from PF ready. Setting this bit causes an interrupt to the relevant VF. This bit always read as zero. Setting this bit sets the *PFSTS* bit in VFMailbox.
Ack (WO)	1	0b	VF message received. Setting this bit, causes an interrupt to the relevant VF. This bit always read as zero. Setting this bit sets the *PFACK* bit in VFMailbox.
VFU	2	0b	Buffer is taken by VF. This bit is RO for the PF and is a mirror of the *VFU* bit in the VFMailbox register.
PFU	3	0b	Buffer is taken by PF. This bit can be set only if the *VFU* bit is cleared and is mirrored in the *PFU* bit of the VFMailbox register.



Field	Bit(s)	Init Val	Description
RVFU (WO)	4	0b	Reset VFU. Setting this bit clears the *VFU* bit in the corresponding VFMailbox register. This bit should be used only if the VF driver is not operational. Setting this bit also resets the corresponding bits in the PFMBICR *VFREQ* and *VFACK* fields.
Reserved	31:5	0x0	Reserved.

8.2.3.27.3 PF Mailbox Interrupt Causes Register — PFMBICR[n] (0x00710 + 4*n, n=0...3; RW1C)

Each register handles 16 VFs and are defined as follows.

Field	Bit(s)	Init Val	Description
VFREQ	15:0	0x0	Each bit in the *VFREQ* field is set when VF number (16*n+j) wrote a message in its mailbox. While 'n' is the register index, n=0...3 and 'j' is the index of the bits in the VFREQ, j=0...15.
VFACK	31:16	0x0	Each bit in the *VFACK* field is set when VF number (16*n+j) acknowledged a PF message. While 'n' is the register index, n=0...3 and '16+j' is the index of the bits in the VFACK, j=0...15.

8.2.3.27.4 PF Mailbox Interrupt Mask Register — PFMBIMR[n] (0x00720 + 4*n, n=0...1; RW)

Field	Bit(s)	Init Val	Description
VFIM	31:0	0xFF	Mailbox interrupt enable from VF # 32*n+j, while 'n' is the register index and 'j' is the bit number.

8.2.3.27.5 PF VFLR Events Indication — PFVFLRE[n] (0x00600, 0x001C0; RO)

Field	Bit(s)	Init Val	Description
VFLE	31:0	0x0	When set, bit 'i' in register 'n' reflects an FLR event on VF# 32*n+i. These bits are accessible only to the PF and are cleared by writing 0x1 to the matched bit in the PFVFLREC registers.

8.2.3.27.6 PF VFLR Events Clear — PFVFLREC[n] (0x00700 + 4*n, n=0...1; W1C)

Field	Bit(s)	Init Val	Description
Clear VFLE	31:0	X	Writing a 0x1 to bit 'i' in register 'n' clears the FLR event on VF# 32*n+i indicated in the PFVFLRE[n] registers.

8.2.3.27.7 PF VF Receive Enable — PFVFRE[n] (0x051E0 + 4*n, n=0...1; RW)

This register is reset on common reset cases and on per-function reset cases. Respective bits per VF are reset on VFLR, BME bit clear or on VF software reset. See Section 4.2.2.2 for more details.

Field	Bit(s)	Init Val	Description
VFRE	31:0	0x0	Bit j. Enables receiving packets to VF# (32*n+j). Each bit is cleared by the relevant VFLR.

8.2.3.27.8 PF VF Transmit Enable — PFVFTE[n] (0x08110 + 4*n, n=0...1; RW)

This register is reset on common reset cases and on per-function reset cases. Respective bits per VF are reset on VFLR, BME bit clear or on VF software reset. See Section 4.2.2.2 for more details.

Field	Bit(s)	Init Val	Description
VFTE	31:0	0x0	Bit j. Enables transmitting packets from VF# (32*n+j). Each bit is cleared by the relevant VFLR.

8.2.3.27.9 PF PF Queue Drop Enable Register — PFQDE (0x02F04; RW)

Field	Bit(s)	Init Val	Description
QDE	0	0b	Enable drop of packets from Rx queue Queue_Index. This bit overrides the SRRCTL.drop_en bit of each queue. For example, if either of the bits is set, a packet received when no descriptor is available is dropped.
Reserved	3:1	0x0	Reserved (see *WE* and *RE* bit descriptions).
Reserved	7:4	0x0	Reserved.
Queue Index	14:8	0x0	Indicates the queue referenced upon WE/RE commands.