4 Option byte description

There are six option bytes. They are configured by the end user depending on the application requirements. As a configuration example, the watchdog may be selected in hardware or software mode.

A 32-bit word is split up as follows in the option bytes.

Table 9. Option byte format

31-24	23-16	15 -8	7-0
Complemented option byte1	Option byte 1	Complemented option byte0	Option byte 0

The organization of these bytes inside the information block is as shown in *Table 10*.

The option bytes can be read from the memory locations listed in *Table 10* or from the Option byte register (FLASH_OBR).

Note: The new programmed option bytes (user, read/write protection) are loaded after a system reset.

Table 10. Option byte organization

Address	[31:24]	[23:16]	[15:8]	[7:0]
0x1FFF F800	nUSER	USER	nRDP	RDP
0x1FFF F804	nData1	Data1	nData0	Data0
0x1FFF F808	nWRP1	WRP1	nWRP0	WRP0

Table 11. Description of the option bytes

Flash memory address	Option bytes
0x1FFF F800	Bits [31:24]: **nUSER** Bits [23:16]: **USER:** User option byte (stored in FLASH_OBR[15:8]) This byte is used to configure the following features: - Select the watchdog event: Hardware or software - Reset event when entering Stop mode - Reset event when entering Standby mode Bit 23: Reserved Bit 22: **SRAM_PE** The SRAM hardware parity check is disabled by default. This bit allows the user to enable the SRAM hardware parity check. 0: Parity check enabled. 1: Parity check disabled. Bit 21: **VDDA_MONITOR** This bit selects the analog monitoring on the VDDA power source: 0: VDDA power supply supervisor disabled. 1: VDDA power supply supervisor enabled. Bit 20: **nBOOT1** Together with the BOOT0 pin, this bit selects Boot mode from the main Flash memory, SRAM or System memory. Refer to *Section 2.5 on page 52*. Bit 19: Reserved, must be kept at reset. Bit 18: **nRST_STDBY** 0: Reset generated when entering Standby mode. 1: No reset generated. Bit 17: **nRST_STOP** 0: Reset generated when entering Stop mode 1: No reset generated Bit 16: **WDG_SW** 0: Hardware watchdog 1: Software watchdog Bits [15:8]: **nRDP** Bits [7:0]: **RDP:** Read protection option byte The value of this byte defines the Flash memory protection level 0xAA: Level 0 0xXX (except 0xAA and 0xCC): Level 1 0xCC: Level 2 The protection levels are stored in the Flash_OBR Flash option bytes register (RDPRT bits).

Table 11. Description of the option bytes (continued)

Flash memory address	Option bytes
0x1FFF F804	**Datax**: Two bytes for user data storage. These addresses can be programmed using the option byte programming procedure. Bits [31:24]: **nData1** Bits [23:16]: **Data1** (stored in FLASH_OBR[31:24]) Bits [15:8]: **nData0** Bits [7:0]: **Data0** (stored in FLASH_OBR[23:16])
0x1FFF F808	**WRPx**: Flash memory write protection option bytes Bits [31:24]: **nWRP1** Bits [23:16]: **WRP1** (stored in FLASH_WRPR[15:8]) Bits [15:8]: **nWRP0** Bits [7:0]: **WRP0** (stored in FLASH_WRPR[7:0]) 0: Write protection active 1: Write protection not active Refer to *Section 3.3.2: Write protection* for more details. In total, 2 user option bytes are used to protect the whole main Flash memory. WRP0: Write-protects pages 0 to 15 WRP1: Write-protects pages 16 to 31 *Note: Even if WRP2 and WRP3 are not available, they must be kept at reset value.*

On every system reset, the option byte loader (OBL) reads the information block and stores the data into the Option byte register (FLASH_OBR) and the Write protection register (FLASH_WRPR). Each option byte also has its complement in the information block. During option loading, by verifying the option bit and its complement, it is possible to check that the loading has correctly taken place. If this is not the case, an option byte error (OPTERR) is generated. When a comparison error occurs, the corresponding option byte is forced to 0xFF. The comparator is disabled when the option byte and its complement are both equal to 0xFF (Electrical Erase state).