28 Revision history

Table 161. Document revision history

Date	Revision	Changes
26-Feb-2010	1	Initial release.
04-Jun-2010	2	Corrected description of TIMx_CCER register in *Section 12.4.9 on page 272* and *Section 13.4.9 on page 334* Updated *Section 14.3.5: Input capture mode on page 353* Added method 1 and 2 in *Section 22.3.3: I2C master mode* Updated note in POS bit description *Section 22.6: I^2C registers*
12-Oct-2010	3	Updated for high density value line devices Updated *Section 20.5.2: Supported memories and transactions* Added *Section 14: General-purpose timers (TIM12/13/14)* Added *Section 20: Flexible static memory controller (FSMC)*
21-Jul-2011	4	Corrected *Figure 2: High density value line system architecture on page 35* Updated SPI table in *Section 7.1.11: GPIO configurations for device peripherals on page 109* Updated bit descriptions in *Section 7.3.1: Clock control register (RCC_CR) on page 99* and *Section 8.3.1: Clock control register (RCC_CR) on page 132* EXTI: Updated *Figure 18: External interrupt/event controller block diagram* **ADC**: Corrected *Table 59: External trigger for regular channels for ADC1* and *Table 60: External trigger for injected channels for ADC1 on page 171* **TIMERS:** Removed wrong references to 32-bit counter in *Section 13.4: TIMx2 to TIM5 registers on page 321* TIM1&TIM8: Updated example and definition of DBL bits in *Section 12.4.19: TIM1 DMA control register (TIMx_DCR)*. Added example related to DMA burst feature and description of DMAB bits in *Section 12.4.20: TIM1 DMA address for full transfer (TIMx_DMAR)*. TIM2 to TIM5 and TIM15 to 17: added example and updated definition of DBL bits in *Section 13.4.17: TIMx DMA control register (TIMx_DCR)*. Added example related to DMA burst feature and description of DMAB bits in *Section 13.4.18: TIMx DMA address for full transfer (TIMx_DMAR)*. Updated definition of DBL bits in *Section 13.4.17: TIMx DMA control register (TIMx_DCR)*. In *Section 12.3.3: Repetition counter* Added paragraph “In Center aligned mode, for odd values of RCR, ...” Modified *Figure 167: Update rate examples depending on mode and TIMx_RCR register settings on page 398*. **WWDG** Updated *Section 19.2: WWDG main features*. Updated *Section 19.3: WWDG functional description* to remove paragraph related to counter reload using EWI interrupt.

Table 161. Document revision history (continued)

Date	Revision	Changes
21-Jul-2011	4 continued	**I2C:** Updated BERR bit description in *Section 22.6.6: I²C Status register 1 (I2C_SR1)*. Updated *Note:* in *Section 22.6.8: I²C Clock control register (I2C_CCR)*. Added note 3 below *Figure 235: Transfer sequence diagram for slave transmitter on page 570*. Added note below *Figure 236: Transfer sequence diagram for slave receiver on page 571*. Modified *Section : Closing slave communication on page 571*. Modified STOPF, ADDR, bit description in *Section 22.6.6: I²C Status register 1 (I2C_SR1) on page 591*. Modified *Section 22.6.7: I²C Status register 2 (I2C_SR2)*. **USART:** Updated *Figure 251: Mute mode using address mark detection* for Address =1.**SPI:** Modified *Slave select (NSS) pin management on page 539* and note on NSS in *Section 21.3.3: Configuring the SPI in master mode* **FSMC:** Updated description of DATLAT , DATAST , and ADDSET bits in *SRAM/NOR-Flash chip-select timing registers 1..4 (FSMC_BTR1..4)*. Updated byte select description in *Section 20.5.2: Supported memories and transactions on page 501*
10-Jun-2016	5	Added *SCL master clock generation* and *Note:* to *Entering Stop mode*. Added *Table 88: Minimum and maximum timeout values @24 MHz (f_{PCLK1})*. Updated *Table 74: TIMx Internal trigger connection*, *Table 79: TIMx Internal trigger connection*, *Table 92: Programmable NOR/PSRAM access parameters*, *Table 97: NOR flash/PSRAM controller: example of supported memories and transactions* and *Table 114: FSMC_BCRx bit fields*. Updated *Figure 5: Power on reset/power down reset waveform*, *Figure 6: PVD thresholds*, *Figure 7: Simplified diagram of the reset circuit*, *Figure 40: Advanced-control timer block diagram*, *Figure 68: Output stage of capture/compare channel (channel 1 to 3)*, *Figure 78: Clearing TIMx OCxREF*, *Figure 121: Clearing TIMx OCxREF*, *Figure 128: Master/Slave timer example*, *Figure 158: TIM16 and TIM17 block diagram*, *Figure 173: Output stage of capture/compare channel (channel 1)*, *Figure 200: Watchdog block diagram*, *Figure 201: Window watchdog timing diagram*, *Figure 202: FSMC block diagram*, *Figure 217: Asynchronous wait during a read access*, *Figure 218: Asynchronous wait during a write access* and *Figure 220: Synchronous multiplexed read mode - NOR, PSRAM (CRAM)*. Updated caption of *Figure 101: Counter timing diagram, Update event* and of *Figure 208: Mode2 and mode B read accesses*.

Table 161. Document revision history (continued)

Date	Revision	Changes
10-Jun-2016	5 continued	Updated: – *Introduction* – *Section 2.1: System architecture*, *Section 2.3: Memory map* – *Section 25.6.1: MCU device ID code*. – *Section 4.4.2: Power control/status register (PWR_CSR)*, – *Section 6.1.2: Power reset*, *Section 6.2.8: RTC clock* – *Section 7.2.3: Port input data register (GPIOx_IDR) (x=A..G)* and *Section 7.2.4: Port output data register (GPIOx_ODR) (x=A..G)* – *Section 8.2: External interrupt/event controller (EXTI)*, *Section 8.3.5: Software interrupt event register (EXTI_SWIER)* and *Section 8.3.6: Pending register (EXTI_PR)*. – *Section 10.11.7: ADC watchdog high threshold register (ADC_HTR)* and *Section 10.11.8: ADC watchdog low threshold register (ADC_LTR)*. Renumbered former *Section 14.3* into *Section 14.2.2*. Updated: – *Section 12.3.1: Time-base unit*, *Section 12.3.2: Counter modes*, *Section 12.3.6: Input capture mode*, *Section 12.3.11: Complementary outputs and dead-time insertion*, *Section 12.3.13: Clearing the OCxREF signal on an external event*, *Section 12.3.16: Encoder interface mode*, *Section 12.3.18: Interfacing with Hall sensors*, *Section 12.4.3: TIM1 slave mode control register (TIMx_SMCR)*, *Section 12.4.2: TIM1 control register 2 (TIMx_CR2)*, *Section 12.4.7: TIM1 capture/compare mode register 1 (TIMx_CCMR1)*, *Section 12.4.12: TIM1 auto-reload register (TIMx_ARR)*, *Section 13.3.5: Input capture mode*, *Section 13.3.9: PWM mode*, *Section 13.3.11: Clearing the OCxREF signal on an external event*, *Section 13.3.12: Encoder interface mode*, *Section 13.3.15: Timer synchronization*, *Section 13.4.2: TIMx control register 2 (TIMx_CR2)*, *Section 13.4.3: TIMx slave mode control register (TIMx_SMCR)*, *Section 13.4.7: TIMx capture/compare mode register 1 (TIMx_CCMR1)*, *Section 14.3.1: Time-base unit*, *Section 14.3.5: Input capture mode*, *Section 14.3.9: PWM mode*, *Section 14.4.7: TIM capture/compare mode register 1 (TIMx_CCMR1)*, *Section 14.5.5: TIM13/14 capture/compare mode register 1 (TIMx_CCMR1)*, *Section 15.2: TIM15 main features*, *Section 15.3: TIM16 and TIM17 main features*, *Section 15.4.1: Time-base unit*, *Section 15.4.2: Counter modes*, *Section 15.4.3: Repetition counter*, *Section 15.4.6: Input capture mode*, *Section 15.4.10: PWM mode*, *Section 15.4.11: Complementary outputs and dead-time insertion*, *Section 15.5.3: TIM15 slave mode control register (TIM15_SMCR)*, *Section 15.5.7: TIM15 capture/compare mode register 1 (TIM15_CCMR1)*, *Section 15.5.11: TIM15 auto-reload register (TIM15_ARR)*, *Section 15.5.15: TIM15 break and dead-time register (TIM15_BDTR)*, *Section 15.6.6: TIM16&TIM17 capture/compare mode register 1 (TIMx_CCMR1)*, *Section 15.6.10: TIM16&TIM17 auto-reload register (TIMx_ARR)* and *Section 15.6.13: TIM16&TIM17 break and dead-time register (TIMx_BDTR)*. Updated: – *Section 19.4: How to program the watchdog timeout*.

Table 161. Document revision history (continued)

Date	Revision	Changes
10-Jun-2016	5 continued	Updated: – *Mode 1 - SRAM/PSRAM (CRAM)*, *Asynchronous static memories (NOR flash memory, PSRAM, SRAM)*, , *Mode 2/B - NOR flash*, *SRAM/NOR-Flash chip-select timing registers 1..4 (FSMC_BTR1..4)*, *SRAM/NOR-Flash write timing registers 1..4 (FSMC_BWTR1..4)*, *SRAM/NOR-flash chip-select control registers 1..4 (FSMC_BCR1..4)*, *Section 20.5.4: NOR flash/PSRAM controller asynchronous transactions* and *Section 20.5.6: NOR/PSRAM control registers*. Replaced M/SL with MSL throughout *Section 22: Inter-integrated circuit (I2C) interface*, and updated *Section 22.6.1: I^2C Control register 1 (I2C_CR1)*, *Section 22.6.2: I^2C Control register 2 (I2C_CR2)* and *Section 22.6.9: I^2C TRISE register (I2C_TRISE)*. Replaced nCTS with CTS, nRTS with RTS and SCLK with CK throughout *Section 27: Universal synchronous asynchronous receiver transmitter (USART)*. Updated: – *Section 27.3.8: LIN (local interconnection network) mode*, *Selecting the proper oversampling method*, *How to derive USARTDIV from USART_BRR register values when OVER8=0* and *How to derive USARTDIV from USART_BRR register values when OVER8=1* and *Section 27.6.6: Control register 3 (USART_CR3)*.
12-Dec-2022	6	Updated *Introduction*, *Section 4.4.1: Power control register (PWR_CR)*, *Section 5.2: BKP main features*, *Section 5.4: BKP registers*, *Section 12.3.21: Debug mode*, *Section 12.4.7: TIM1 capture/compare mode register 1 (TIMx_CCMR1)*, *Section 12.4.14: TIM1 capture/compare register 1 (TIMx_CCR1)*, *Section 12.4.17: TIM1 capture/compare register 4 (TIMx_CCR4)*, *Section 12.4.20: TIM1 DMA address for full transfer (TIMx_DMAR)*, *Section 13.4.7: TIMx capture/compare mode register 1 (TIMx_CCMR1)*, sections *13.4.13* to *13.4.16*, *Section 14.4.7: TIM capture/compare mode register 1 (TIMx_CCMR1)*, sections *14.4.11* to *14.4.13*, *Section 14.5.9: TIM13/14 auto-reload register (TIMx_ARR)*, *Section 14.5.10: TIM13/14 capture/compare register 1 (TIMx_CCR1)*, *Section 15.5.5: TIM15 status register (TIM15_SR)*, *Section 15.6.12: TIM16&TIM17 capture/compare register 1 (TIMx_CCR1)*, and *Section 19.4: How to program the watchdog timeout*. Added *Section 1.4: General information* and *Section 27: Important security notice*. Updated *Table 14: BKP register map and reset values* and *Table 69: TIM1 register map and reset values*. Updated *Figure 6: PVD thresholds*, *Figure 40: Advanced-control timer block diagram*, *Figure 134: General-purpose timer block diagram (TIM12)*, and *Figure 259: Parity error detection using the 1.5 stop bits*. Minor text edits across the whole document.

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