

5 Power control (PWR)

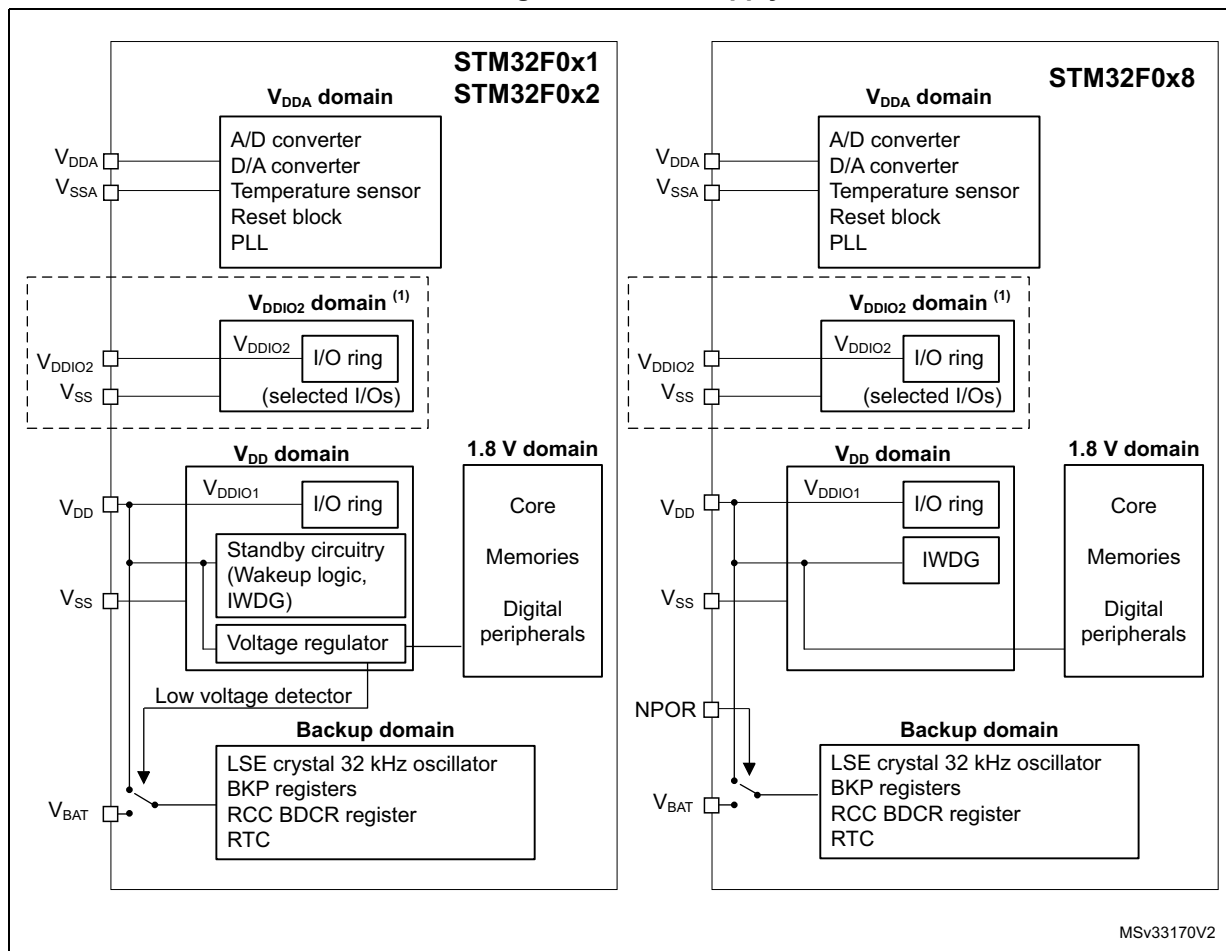
5.1 Power supplies

The STM32F0x1/F0x2 subfamily embeds a voltage regulator in order to supply the internal 1.8 V digital power domain, unlike the STM32F0x8 subfamily where the stable 1.8 V must be delivered by the application.

- The STM32F0x1/F0x2 devices require a 2.0 V - 3.6 V operating supply voltage (V_{DD}) and a 2.0 V - 3.6 V analog supply voltage (V_{DDA}).
- The STM32F0x8 devices require a 1.8 V \pm 8% operating supply voltage (V_{DD}), and a 1.65 V - 3.6 V analog supply voltage (V_{DDA}).

The real-time clock (RTC) and backup registers can be powered from the V_{BAT} voltage when the main V_{DD} supply is powered off.

Figure 6. Power supply overview



1. Available only on STM32F04x, STM32F07x and STM32F09x devices.

5.1.1 Independent A/D and D/A converter supply and reference voltage

To improve conversion accuracy and to extend the supply flexibility, the ADC and the DAC have an independent power supply that can be separately filtered and shielded from noise on the PCB.

- The ADC and DAC voltage supply input is available on a separate V_{DDA} pin.
- An isolated supply ground connection is provided on pin V_{SSA} .

The V_{DDA} supply/reference voltage must be equal or higher than V_{DD} .

When a single supply is used, V_{DDA} can be externally connected to V_{DD} , through the external filtering circuit in order to ensure a noise free V_{DDA} reference voltage.

When V_{DDA} is different from V_{DD} , V_{DDA} must always be higher or equal to V_{DD} . To keep safe potential difference in between V_{DDA} and V_{DD} during power-up/power-down, an external Schottky diode may be used between V_{DD} and V_{DDA} . Refer to the datasheet for the maximum allowed difference.

5.1.2 Independent I/O supply rail

For better supply flexibility on STM32F04x, STM32F07x and STM32F09x devices, portions of the I/Os are supplied from a separate supply rail. Power supply for this rail can range from 1.65 to 3.6 V and is provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA} , but it must not be provided without a valid operating supply on the V_{DD} pin. Refer to the pinout diagrams or tables in related device datasheets for concerned I/Os list.

The V_{DDIO2} supply is monitored and compared with the internal reference voltage (V_{REFINT}). When the V_{DDIO2} is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt.

5.1.3 Battery backup domain

To retain the content of the Backup registers and supply the whole RTC domain when V_{DD} is turned off, V_{BAT} pin can be connected to an optional standby voltage supplied by a battery or by another source.

The V_{BAT} pin powers the RTC unit, the LSE oscillator and the PC13 to PC15 I/Os, allowing the RTC to operate even when the main power supply is turned off. The switch to the V_{BAT} supply is controlled by the Power Down Reset embedded in the Reset block or (on STM32F0x8 devices) by the external NPOR signal.

Warning: During $t_{RSTTEMPO}$ (temporization at V_{DD} startup) or after a PDR is detected, the power switch between V_{BAT} and V_{DD} remains connected to V_{BAT} .

During the startup phase, if V_{DD} is established in less than $t_{RSTTEMPO}$ (Refer to the datasheet for the value of $t_{RSTTEMPO}$) and $V_{DD} > V_{BAT} + 0.6$ V, a current may be injected into V_{BAT} through an internal diode connected between V_{DD} and the power switch (V_{BAT}).

If the power supply/battery connected to the V_{BAT} pin cannot support

this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the V_{BAT} pin.

If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD} with a 100 nF external ceramic decoupling capacitor (for more details refer to AN4080).

When the RTC domain is supplied by V_{DD} (analog switch connected to V_{DD}), the following functions are available:

- PC13, PC14 and PC15 can be used as GPIO pins
- PC13, PC14 and PC15 can be configured by RTC or LSE (refer to [Section 25.4: RTC functional description on page 591](#))

Note: Due to the fact that the analog switch can transfer only a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is restricted: the speed has to be limited to 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

When the RTC domain is supplied by V_{BAT} (analog switch connected to V_{BAT} because V_{DD} is not present), the following functions are available:

- PC13, PC14 and PC15 can be controlled only by RTC or LSE (refer to [Section 25.4: RTC functional description on page 591](#))

5.1.4 Voltage regulator

The voltage regulator is always enabled after Reset. It works in three different modes depending on the application modes.

- In Run mode, the regulator supplies full power to the 1.8 V domain (core, memories and digital peripherals).
- In Stop mode the regulator supplies low-power to the 1.8 V domain, preserving contents of registers and SRAM
- In Standby Mode, the regulator is powered off. The contents of the registers and SRAM are lost except for the Standby circuitry and the RTC domain.

Note: In STM32F0x8 devices, the voltage regulator is bypassed and the microcontroller must be powered from a nominal $V_{DD} = 1.8 \text{ V} \pm 8\%$ supply.

5.2 Power supply supervisor

5.2.1 Power on reset (POR) / power down reset (PDR)

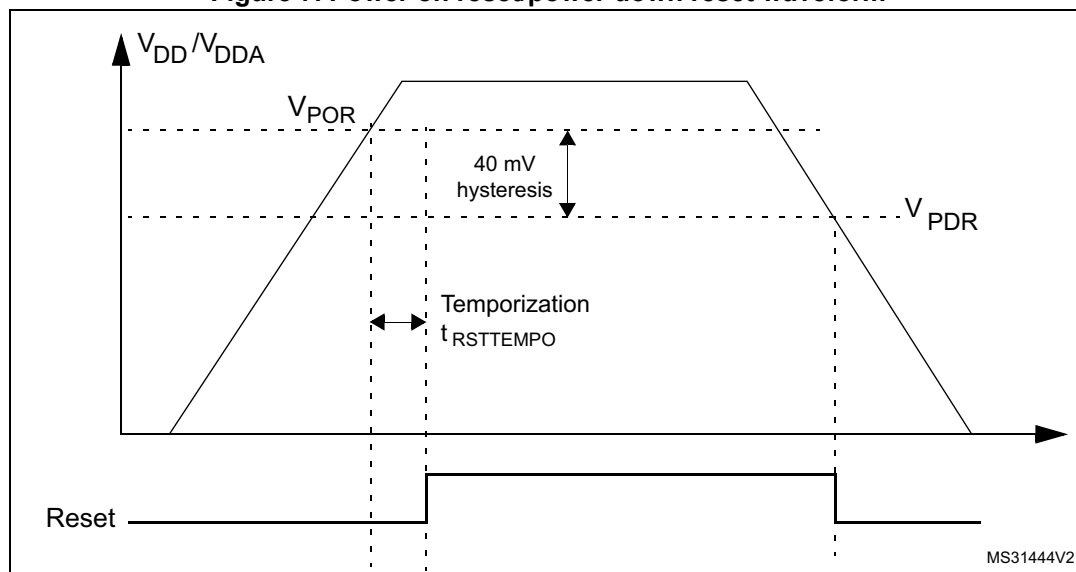
STM32F0x1xx and STM32F0x2xx devices feature integrated power-on reset (POR) and power-down reset (PDR) circuits, which are always active and ensure proper operation above a threshold of 2 V.

The devices remain in Reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase V_{DDA} must arrive first and be greater than or equal to V_{DD} .
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages. However, the V_{DDA} power supply supervisor can be disabled (by programming a dedicated option bit $V_{DDA_MONITOR}$) to reduce the power consumption if the application is designed to make sure that V_{DDA} is higher than or equal to V_{DD} .

For more details on the power on / power down reset threshold, refer to the electrical characteristics section in the datasheet.

Figure 7. Power on reset/power down reset waveform



External NPOR signal

In STM32F0x8 devices, the PB2 I/O (or PB1 on small packages) is not available and is replaced by the NPOR functionality used for power on reset.

To guarantee a proper power on and power down reset to the device, the NPOR pin must be held low until V_{DD} is stable or before turning off the supply. When V_{DD} is stable, the reset state can be exited by putting the NPOR pin in high impedance. The NPOR pin has an internal pull-up connected to V_{DDA} .

5.2.2 Programmable voltage detector (PVD)

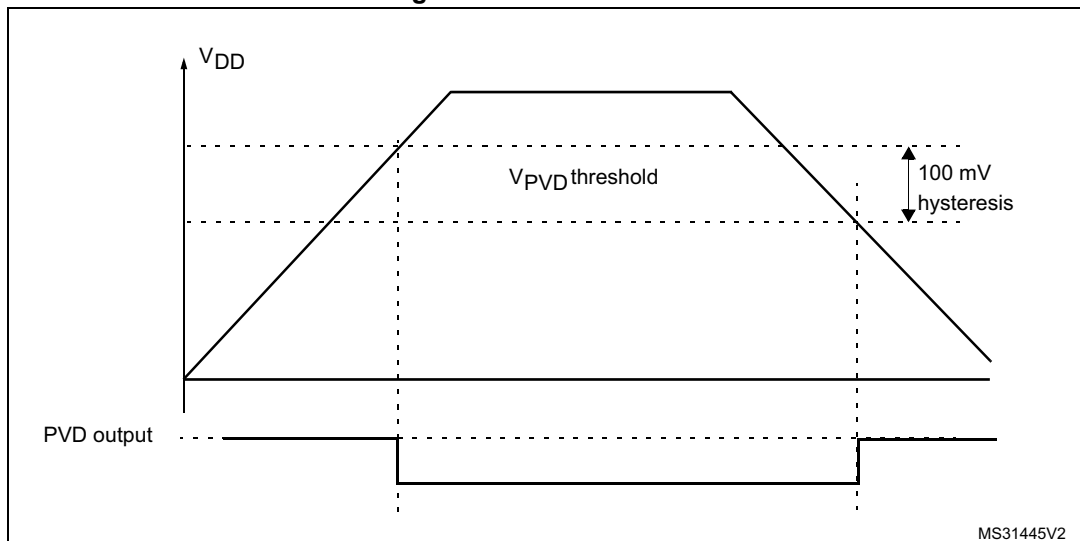
STM32F0x1xx and STM32F0x2xx can use the PVD to monitor the V_{DD} power supply by comparing it to a threshold selected by the PLS[2:0] bits in the [Power control register \(PWR_CR\)](#).

The PVD is enabled by setting the PVDE bit.

A PVDO flag is available, in the [Power control/status register \(PWR_CSR\)](#), to indicate if V_{DD} is higher or lower than the PVD threshold. This event is internally connected to the EXTI line16 and can generate an interrupt if enabled through the EXTI registers. The PVD output interrupt can be generated when V_{DD} drops below the PVD threshold and/or when V_{DD}

risers above the PVD threshold depending on EXTI line16 rising/falling edge configuration. As an example the service routine could perform emergency shutdown tasks.

Figure 8. PVD thresholds



5.3 Low-power modes

By default, the microcontroller is in Run mode after a system or a power Reset. Several low-power modes are available to save power when the CPU does not need to be kept running, for example when waiting for an external event. It is up to the user to select the mode that gives the best compromise between low-power consumption, short startup time and available wake-up sources.

The device features three low-power modes:

- Sleep mode (CPU clock off, all peripherals including Cortex®-M0 core peripherals like NVIC, SysTick, etc. are kept running)
- Stop mode (all clocks are stopped)
- Standby mode (1.8V domain powered-off)

In addition, the power consumption in Run mode can be reduced by one of the following means:

- Slowing down the system clocks
- Gating the clocks to the APB and AHB peripherals when they are unused.

Table 13. Low-power mode summary

| Mode name | Entry | Wake-up | Effect on 1.8 V domain clocks | Effect on V _{DD} domain clocks | Voltage regulator |
|---|---|--|--|---|---|
| Sleep (Sleep now or Sleep-on - exit) | WFI | Any interrupt | CPU clock OFF no effect on other clocks or analog clock sources | None | ON |
| | WFE | Wake-up event | | | |
| Stop | PDDS and LPDS bits + SLEEPDEEP bit + WFI or WFE | Any EXTI line (configured in the EXTI registers) Specific communication peripherals on reception events (CEC, USART, I2C) | All 1.8V domain clocks OFF | HSI and HSE oscillators OFF | ON or in low-power mode (depends on Power control register (PWR_CR)) |
| Standby | PDDS bit + SLEEPDEEP bit + WFI or WFE | WKUP pin rising edge, RTC alarm, external reset in NRST pin, IWDG reset | | | OFF |

Caution: On STM32F0x8 devices, the Stop mode is available, but it is meaningless to distinguish between voltage regulator in low-power mode and voltage regulator in Run mode because the regulator is not used and the core is supplied directly from an external source. Consequently, the Standby mode is not available on those devices.

5.3.1 Slowing down system clocks

In Run mode the speed of the system clocks (SYSCLK, HCLK, PCLK) can be reduced by programming the prescaler registers. These prescalers can also be used to slow down peripherals before entering Sleep mode.

For more details refer to [Section 6.4.2: Clock configuration register \(RCC_CFGR\)](#).

5.3.2 Peripheral clock gating

In Run mode, the AHB clock (HCLK) and the APB clock (PCLK) for individual peripherals and memories can be stopped at any time to reduce power consumption.

To further reduce power consumption in Sleep mode the peripheral clocks can be disabled prior to executing the WFI or WFE instructions.

Peripheral clock gating is controlled by the [AHB peripheral clock enable register \(RCC_AHBENR\)](#), the [APB peripheral clock enable register 2 \(RCC_APB2ENR\)](#) and the [APB peripheral clock enable register 1 \(RCC_APB1ENR\)](#).

5.3.3 Sleep mode

Entering Sleep mode

The Sleep mode is entered by executing the WFI (Wait For Interrupt) or WFE (Wait for Event) instructions. Two options are available to select the Sleep mode entry mechanism, depending on the SLEEPONEXIT bit in the Cortex[®]-M0 System Control register:

- Sleep-now: if the SLEEPONEXIT bit is cleared, the MCU enters Sleep mode as soon as WFI or WFE instruction is executed.
- Sleep-on-exit: if the SLEEPONEXIT bit is set, the MCU enters Sleep mode as soon as it exits the lowest priority ISR.

In the Sleep mode, all I/O pins keep the same state as in the Run mode.

Refer to [Table 14](#) and [Table 15](#) for details on how to enter Sleep mode.

Exiting Sleep mode

If the WFI instruction is used to enter Sleep mode, any peripheral interrupt acknowledged by the nested vectored interrupt controller (NVIC) can wake up the device from Sleep mode.

If the WFE instruction is used to enter Sleep mode, the MCU exits Sleep mode as soon as an event occurs. The wake-up event can be generated either by:

- enabling an interrupt in the peripheral control register but not in the NVIC, and enabling the SEVONPEND bit in the Cortex[®]-M0 System Control register. When the MCU resumes from WFE, the peripheral interrupt pending bit and the peripheral NVIC IRQ channel pending bit (in the NVIC interrupt clear pending register) must be cleared.
- or configuring an external or internal EXTI line in event mode. When the CPU resumes from WFE, it is not necessary to clear the peripheral interrupt pending bit or the NVIC IRQ channel pending bit as the pending bit corresponding to the event line is not set.

This mode offers the lowest wake-up time as no time is wasted in interrupt entry/exit.

Refer to [Table 14](#) and [Table 15](#) for more details on how to exit Sleep mode.

Table 14. Sleep-now

| Sleep-now mode | Description |
|------------------------|--|
| Mode entry | WFI (Wait for Interrupt) or WFE (Wait for Event) while: – SLEEPDEEP = 0 and – SLEEPONEXIT = 0 Refer to the Cortex®-M0 System Control register. |
| Mode exit | If WFI was used for entry: Interrupt: Refer to Table 36: Vector table If WFE was used for entry: Wake-up event: Refer to Section 11.2.3: Event management |
| Wake-up latency | None |

Table 15. Sleep-on-exit

| Sleep-on-exit | Description |
|------------------------|---|
| Mode entry | WFI (wait for interrupt) while: – SLEEPDEEP = 0 and – SLEEPONEXIT = 1 Refer to the Cortex®-M0 System Control register. |
| Mode exit | Interrupt: Refer to Table 36: Vector table . |
| Wake-up latency | None |

5.3.4 Stop mode

The Stop mode is based on the Cortex®-M0 deep sleep mode combined with peripheral clock gating. The voltage regulator can be configured either in normal or low-power mode. In Stop mode, all clocks in the 1.8 V domain are stopped, the PLL, the HSI and the HSE oscillators are disabled. SRAM and register contents are preserved.

In the Stop mode, all I/O pins keep the same state as in the Run mode.

Entering Stop mode

Refer to [Table 16](#) for details on how to enter the Stop mode.

To further reduce power consumption in Stop mode, the internal voltage regulator can be put in low-power mode. This is configured by the LPDS bit of the [Power control register \(PWR_CR\)](#).

If Flash memory programming is ongoing, the Stop mode entry is delayed until the memory access is finished.

If an access to the APB domain is ongoing, The Stop mode entry is delayed until the APB access is finished.

In Stop mode, the following features can be selected by programming individual control bits:

- Independent watchdog (IWDG): the IWDG is started by writing to its Key register or by hardware option. Once started it cannot be stopped except by a Reset. See [Section 23.3: IWDG functional description](#).

- real-time clock (RTC): this is configured by the RTCEN bit in the [RTC domain control register \(RCC_BDCR\)](#)
- Internal RC oscillator (LSI): this is configured by the LSION bit in the [Control/status register \(RCC_CSR\)](#).
- External 32.768 kHz oscillator (LSE): this is configured by the LSEON bit in the [RTC domain control register \(RCC_BDCR\)](#).

The ADC or DAC can also consume power during Stop mode, unless they are disabled before entering this mode. Refer to [ADC control register \(ADC_CR\)](#) and [DAC control register \(DAC_CR\)](#) for details on how to disable them.

Exiting Stop mode

Refer to [Table 16](#) for more details on how to exit Stop mode.

When exiting Stop mode by issuing an interrupt or a wake-up event, the HSI oscillator is selected as system clock.

When the voltage regulator operates in low-power mode, an additional startup delay is incurred when waking up from Stop mode. By keeping the internal regulator ON during Stop mode, the consumption is higher although the startup time is reduced.

Table 16. Stop mode

| Stop mode | Description |
|------------------------|---|
| Mode entry | <p>WFI (Wait for Interrupt) or WFE (Wait for Event) while:</p> <ul style="list-style-type: none"> – Set SLEEPDEEP bit in Cortex[®]-M0 System Control register – Clear PDDS bit in Power Control register (PWR_CR) – Select the voltage regulator mode by configuring LPDS bit in PWR_CR <p>Note: To enter Stop mode, all EXTI line pending bits (in Pending register (EXTI_PR)), all peripherals interrupt pending bits and RTC Alarm flag must be reset. Otherwise, the Stop mode entry procedure is ignored and program execution continues.</p> <p>If the application needs to disable the external oscillator (external clock) before entering Stop mode, the system clock source must be first switched to HSI and then clear the HSEON bit.</p> <p>Otherwise, if before entering Stop mode the HSEON bit is kept at 1, the security system (CSS) feature must be enabled to detect any external oscillator (external clock) failure and avoid a malfunction when entering Stop mode.</p> |
| Mode exit | <p>If WFI was used for entry:</p> <ul style="list-style-type: none"> – Any EXTI line configured in Interrupt mode (the corresponding EXTI Interrupt vector must be enabled in the NVIC). – Some specific communication peripherals (CEC, USART, I2C) interrupts, when programmed in wake-up mode (the peripheral must be programmed in wake-up mode and the corresponding interrupt vector must be enabled in the NVIC). <p>Refer to Table 36: Vector table.</p> <p>If WFE was used for entry:</p> <p>Any EXTI line configured in event mode. Refer to Section 11.2.3: Event management on page 218</p> |
| Wake-up latency | HSI wake-up time + regulator wake-up time from Low-power mode |

5.3.5 Standby mode

The Standby mode allows to achieve the lowest power consumption. It is based on the Cortex®-M0 deepsleep mode, with the voltage regulator disabled. The 1.8 V domain is consequently powered off. The PLL, the HSI oscillator and the HSE oscillator are also switched off. SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry (see [Figure 6](#)).

Caution: The Standby mode is not available on STM32F0x8 devices.

Entering Standby mode

Refer to [Table 17](#) for more details on how to enter Standby mode.

In Standby mode, the following features can be selected by programming individual control bits:

- Independent watchdog (IWDG): the IWDG is started by writing to its Key register or by hardware option. Once started it cannot be stopped except by a reset. See [Section 23.3: IWDG functional description](#).
- Real-time clock (RTC): this is configured by the RTCEN bit in the [RTC domain control register \(RCC_BDCR\)](#).
- Internal RC oscillator (LSI): this is configured by the LSION bit in the [Control/status register \(RCC_CSR\)](#).
- External 32.768 kHz oscillator (LSE): this is configured by the LSEON bit in the [RTC domain control register \(RCC_BDCR\)](#).

Exiting Standby mode

The microcontroller exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on one of the enabled WKUPx pins or an RTC event occurs. All registers are reset after wake-up from Standby except for [Power control/status register \(PWR_CSR\)](#).

After waking up from Standby mode, program execution restarts in the same way as after a Reset (boot pin sampling, option bytes loading, reset vector is fetched, etc.). The SBF status flag in the [Power control/status register \(PWR_CSR\)](#) indicates that the MCU was in Standby mode.

Refer to [Table 17](#) for more details on how to exit Standby mode.

Table 17. Standby mode

| Standby mode | Description |
|------------------------|--|
| Mode entry | WFI (Wait for Interrupt) or WFE (Wait for Event) while: <ul style="list-style-type: none"> – Set SLEEPDEEP in Cortex®-M0 System Control register – Set PDDS bit in Power Control register (PWR_CR) – Clear WUF bit in Power Control/Status register (PWR_CSR) |
| Mode exit | WKUP pin rising edge, RTC alarm event's rising edge, external Reset in NRST pin, IWDG Reset. |
| Wake-up latency | Reset phase |

I/O states in Standby mode

In Standby mode, all I/O pins are high impedance except:

- Reset pad (still available)
- PC13, PC14 and PC15 if configured by RTC or LSE
- WKUPx pins

Debug mode

By default, the debug connection is lost if the application puts the MCU in Stop or Standby mode while the debug features are used. This is due to the fact that the Cortex[®]-M0 core is no longer clocked.

However, by setting some configuration bits in the DBGMCU_CR register, the software can be debugged even when using the low-power modes extensively.

5.3.6 Auto-wake-up from low-power mode

The RTC can be used to wake-up the MCU from low-power mode by means of the RTC alarm from low-power mode without depending on an external interrupt (Auto-wake-up mode). The RTC provides a programmable time base for waking up from Stop or Standby mode at regular intervals. For this purpose, two of the three alternative RTC clock sources can be selected by programming the RTCSEL[1:0] bits in the [RTC domain control register \(RCC_BDCR\)](#):

- Low-power 32.768 kHz external crystal oscillator (LSE OSC)
This clock source provides a precise time base with very low-power consumption (less than 1 μ A added consumption in typical conditions)
- Low-power internal RC oscillator (LSI)
This clock source has the advantage of saving the cost of the 32.768 kHz crystal. This internal RC oscillator is designed to add minimum power consumption.

To wake-up from Stop mode with an RTC alarm event, it is necessary to:

- Configure the EXTI Line 17 to be sensitive to rising edge
- Configure the RTC to generate the RTC alarm

To wake-up from Standby mode, there is no need to configure the EXTI Line 17.

5.4 Power control registers

The peripheral registers can be accessed by half-words (16-bit) or words (32-bit).

5.4.1 Power control register (PWR_CR)

Address offset: 0x00

Reset value: 0x0000 0000 (reset by wake-up from Standby mode)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|-----|-----|-----|-----|----------|-----|-----|------|-------|-------|------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res |
| | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Res | Res | Res | Res | Res | Res | Res | DBP | PLS[2:0] | | | PVDE | CSBF | CWUF | PDDS | LPDS |
| | | | | | | | rw | rw | rw | rw | rw | rc_w1 | rc_w1 | rw | rw |

Bits 31:9 Reserved, must be kept at reset value.

Bit 8 **DBP**: Disable RTC domain write protection.

In reset state, the RTC and backup registers are protected against parasitic write access. This bit must be set to enable write access to these registers.

0: Access to RTC and Backup registers disabled

1: Access to RTC and Backup registers enabled

Bits 7:5 **PLS[2:0]**: PVD level selection.

These bits are written by software to select the voltage threshold detected by the Power Voltage Detector.

Once the PVD_LOCK is enabled in the [SYSCFG configuration register 2 \(SYSCFG_CFGR2\)](#), the PLS[2:0] bits cannot be programmed anymore.

000: PVD threshold 0

001: PVD threshold 1

010: PVD threshold 2

011: PVD threshold 3

100: PVD threshold 4

101: PVD threshold 5

110: PVD threshold 6

111: PVD threshold 7

Refer to the electrical characteristics of the datasheet for more details.

Bit 4 **PVDE**: Power voltage detector enable.

This bit is set and cleared by software. Once the PVD_LOCK is enabled in the [SYSCFG configuration register 2 \(SYSCFG_CFGR2\)](#) register, the PVDE bit cannot be programmed anymore.

0: PVD disabled

1: PVD enabled

Bit 3 **CSBF**: Clear standby flag.

This bit is always read as 0.

0: No effect

1: Clear the SBF standby flag (write).

Bit 2 **CWUF**: Clear wake-up flag.

This bit is always read as 0.

0: No effect

1: Clear the WUF wake-up Flag **after 2 System clock cycles**. (write)

Bit 1 **PDDS**: Power down deepsleep.

This bit is set and cleared by software. It works together with the LPDS bit.

0: Enter Stop mode when the CPU enters Deepsleep. The regulator status depends on the LPDS bit.

1: Enter Standby mode when the CPU enters Deepsleep.

Bit 0 **LPDS**: Low-power deepsleep.

This bit is set and cleared by software. It works together with the PDDS bit.

0: Voltage regulator on during Stop mode

1: Voltage regulator in low-power mode during Stop mode

Note: When a peripheral that can work in STOP mode requires a clock, the Power controller automatically switch the voltage regulator from Low-power mode to Normal mode and remains in this mode until the request disappears.

5.4.2 Power control/status register (PWR_CSR)

Address offset: 0x04

Reset value: 0x0000 000X (not reset by wake-up from Standby mode)

Additional APB cycles are needed to read this register versus a standard APB read.

| | | | | | | | | | | | | | | | |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----|-----|-----|-----|--------------------|------|-----|-----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res | Res |
| | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EWUP 8 | EWUP 7 | EWUP 6 | EWUP 5 | EWUP 4 | EWUP 3 | EWUP 2 | EWUP 1 | Res | Res | Res | Res | VREF INT RDY | PVDO | SBF | WUF |
| rw | rw | rw | rw | rw | rw | rw | rw | | | | | r | r | r | r |

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:8 **EWUPx**: Enable WKUPx pin

These bits are set and cleared by software.

0: WKUPx pin is used for general purpose I/O. An event on the WKUPx pin does not wake-up the device from Standby mode.

1: WKUPx pin is used for wake-up from Standby mode and forced in input pull down configuration (rising edge on WKUPx pin wakes-up the system from Standby mode).

Note: These bits are reset by a system Reset.

Bits 7:4 Reserved, must be kept at reset value.

Bit 3 **VREFINTRDY**: VREFINT reference voltage ready

This bit is set and cleared by hardware to indicate the state of the internal voltage reference VREFINT.

- 0: VREFINT is not ready
- 1: VREFINT is ready

Note: This flag is useful only for STM32F0x8 devices where POR is provided externally (through the NPOR pin). In STM32F0x1/F0x2 devices, the internal POR waits for VREFINT to stabilize before releasing the reset.

Bit 2 **PVDO**: PVD output

This bit is set and cleared by hardware. It is valid only if PVD is enabled by the PVDE bit.

- 0: V_{DD} is higher than the PVD threshold selected with the PLS[2:0] bits.
- 1: V_{DD} is lower than the PVD threshold selected with the PLS[2:0] bits.

Notes:

- The PVD is stopped by Standby mode. For this reason, this bit is equal to 0 after Standby or reset until the PVDE bit is set.
- Once the PVD is enabled and configured in the PWR_CR register, PVDO can be used to generate an interrupt through the external interrupt controller.

Bit 1 **SBF**: Standby flag

This bit is set by hardware when the device enters Standby mode and it is cleared only by a POR/PDR (power on reset/power down reset) or by setting the CSBF bit in the [Power control register \(PWR_CR\)](#)

- 0: Device has not been in Standby mode
- 1: Device has been in Standby mode

Bit 0 **WUF**: Wake-up flag

This bit is set by hardware to indicate that the device received a wake-up event. It is cleared by a system reset or by setting the CWUF bit in the [Power control register \(PWR_CR\)](#)

- 0: No wake-up event occurred
- 1: A wake-up event was received from one of the enabled WKUPx pins or from the RTC alarm.

Note: An additional wake-up event is detected if one WKUPx pin is enabled (by setting the EWUPx bit) when its pin level is already high.

5.4.3 PWR register map

The following table summarizes the PWR register map and reset values.

Table 18. PWR register map and reset values

| Offset | Register | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-------|-------|-------|-------|-------|-------|-------|----------|------|------|------|------|--------------|------|------|------|
| 0x000 | PWR_CR | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | DBP | PLS[2:0] | | | Res. | PVDE | CSBF | CWUF | PDDS | LPDS |
| | Reset value | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x004 | PWR_CSR | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | Res. | EWUP8 | EWUP7 | EWUP6 | EWUP5 | EWUP4 | EWUP3 | EWUP2 | EWUP1 | Res. | Res. | Res. | Res. | X VREFINTRDY | PVDO | SBF | WUF |
| | Reset value | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Res. | Res. | Res. | Res. | 0 | 0 | 0 | 0 |

Refer to [Section 2.2 on page 46](#) for the register boundary addresses.