33 Revision history

Table 179. Document revision history

Date	Revision	Changes
12-Apr-2022	1	Initial release.
21-Jul-2022	2	Section *Fast programming* - row size corrected. *Table 18: Organization of option bytes* now contains links to option registers and the duplicated description is removed. Format of reset values of option registers updated and/or corrected. Note in bit 16 of *FLASH security register (FLASH_SECR)* updated. Updated *Section 17.3.18: Clearing the OCxREF signal on an external event*. OC1M[3:0] bitfield description updated in *Section 17.4.8: TIM1 capture/compare mode register 1 [alternate] (TIM1_CCMR1)*, *Section 18.4.8: TIMx capture/compare mode register 1 [alternate] (TIMx_CCMR1) (x = 2 to 3)*, *Section 19.4.6: TIM14 capture/compare mode register 1 [alternate] (TIM14_CCMR1)*, and *Section 20.6.7: TIMx capture/compare mode register 1 [alternate] (TIMx_CCMR1)(x = 16 to 17)*. USART2 information in *Table 27: Device resources enabled in different operating modes* corrected. Spurious “TIM15” removed from *Section 6.2.7: Clock security system (CSS)*. Cross-reference to DBG added in WWDG *Section 23.3.5: Debug mode*. *Section 24.2: RTC main features* corrected (spurious “or by a tamper event” removed).
03-Dec-2022	3	First public release. *Section 5.3.2: Low-power modes*, bulleted point Standby mode. *Section 6.2: Clocks*, bulleted point TIMx. *Figure 9: Clock tree*. *Section 6.3: Low-power modes*, removal of “USART2”. Section *Converting a supply-relative ADC measurement to an absolute voltage value*. *Figure 100: Break and Break2 circuitry overview* - note under the figure corrected. *Section 17.3.25: Interfacing with Hall sensors* - removal of “TIM4”. *Figure 207: Break circuitry overview* - note under the figure corrected.
10-Jul-2024	4	Document device reference from “STM32C0x1” to “STM32C0 series”; Integration of the information relative to STM32C071xx. Cover page: added reference to the errata sheets. Added *Section 7: Clock recovery system (CRS)* and *Section 29: Universal serial bus full-speed host/device interface (USB)*. **Memory mapping:** Added *Table 1: Peripherals or functions versus products*. Updated *Figure 2: Memory map*, *Table 2: STM32C011xx and STM32C031xx boundary addresses*, and *Table 7: STM32C0 series peripheral register boundary addresses*; added *Table 4: STM32C071xx boundary addresses*. Promoted *Section 3: Boot modes* to the first level and updated. Demoted *Section 3.1: Boot configuration* as a subsection. Reworked *Section 3.1.4: Empty check*. In the table of boundary addresses, “Code” replaced with “FLASH” and “FLASH or SRAM”;