33 Revision history

Table 163. Document revision history

Date	Revision	Changes
29-Jun-2014	1	Initial release.
29-Sep-2015	2	Added *Section 9: Peripheral interconnect matrix* Updated Section 18.4.24: TIM1 option registers (TIM1_OR), Section 21: High Resolution Timer (HRTIM), *Section 5: Power control (PWR)*, *Section 14: Digital-to-analog converter (DAC1 and DAC2)*
06-Sep-2017	3	Bits 1,2,3,18,21,24,26,27,28,29,31 updated in the following sections: – *Section 11.2.6: External and internal interrupt/event line mapping* and note updated – *Section 11.3.1: Interrupt mask register (EXTI_IMR1)* and note updated – *Section 11.3.2: Event mask register (EXTI_EMR1)* – *Section 11.3.3: Rising trigger selection register (EXTI_RTSR1)* – *Section 11.3.4: Falling trigger selection register (EXTI_FTSR1)* – *Section 11.3.5: Software interrupt event register (EXTI_SWIER1)* – *Section 11.3.6: Pending register (EXTI_PR1)*,*Section 11.3.7: Interrupt mask register (EXTI_IMR2)* and note removed – *Section 11.3.8: Event mask register (EXTI_EMR2)* – *Section 11.3.9: Rising trigger selection register (EXTI_RTSR2)* – *Section 11.3.10: Falling trigger selection register (EXTI_FTSR2)* – *Section 11.3.11: Software interrupt event register (EXTI_SWIER2)* – *Section 11.3.12: Pending register (EXTI_PR2)* Updated *Section 26.6.16: RTC tamper and alternate function configuration register (RTC_TAFCR)* to modify bits 5 and 6.
16-Jun-2020	4	Updated: – Sections order (homogeneous STM32 reference manuals) – *Section 1: Documentation conventions* – *Section 2.2: Memory organization* – *Section 11: Direct memory access controller (DMA)* – *Section 17.6.10: TSC I/O group x counter register (TSC_IOGxCR)* – *Section 21.3.6: Set/reset events priorities and narrow pulses management* – *Section 18.4.7: TIM1 capture/compare mode register 1 [alternate] (TIM1_CCMR1)* – *Section 18.4.9: TIM1 capture/compare mode register 2 [alternate] (TIM1_CCMR2)* – *Figure 321: Watchdog block diagram* – *Section 26.3.4: Real-time clock and calendar* – *Section 27.4.1: I2C block diagram* – *Section 27.5: I2C low-power modes* – *Section 27.6: I2C interrupts*