ARM Bharat AI-SoC Student Challenge

Real-Time Object Detection Using Hardware-Accelerated CNN on Xilinx Zynq FPGA with Arm Processor

PROBLEM STATEMENT:5

COLLEGE NAME: EASWARI ENGINEERING COLLEGE

TEAM MEMBERS :

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Problem Statement

- Edge AI requires real-time object detection
- ARM processors alone are insufficient for high-resolution inference
- CNN inference is computationally intensive
- Need hardware/software co-design for performance improvement

Objective

- Design a multi-pipeline CNN inference system
- Implement MobileNet-based detection
- Accelerate compute-intensive layers in FPGA
- Achieve real-time performance on embedded hardware
- Demonstrate measurable performance improvement

Hardware Platform:

XC7Z020-CLG400-1 (PYNQ-Z2)

- Dual-core ARM Cortex-A9 (PS)
- AXI interconnect
- DDR memory controller
- USB webcam interface

SYSTEM ARCHITECTURE:

720p Webcam (USB

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Processing System (ARM)

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Pipeline Scheduler

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Programmable Logic (CNN Acceleration)

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Post Processing

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Browser Display

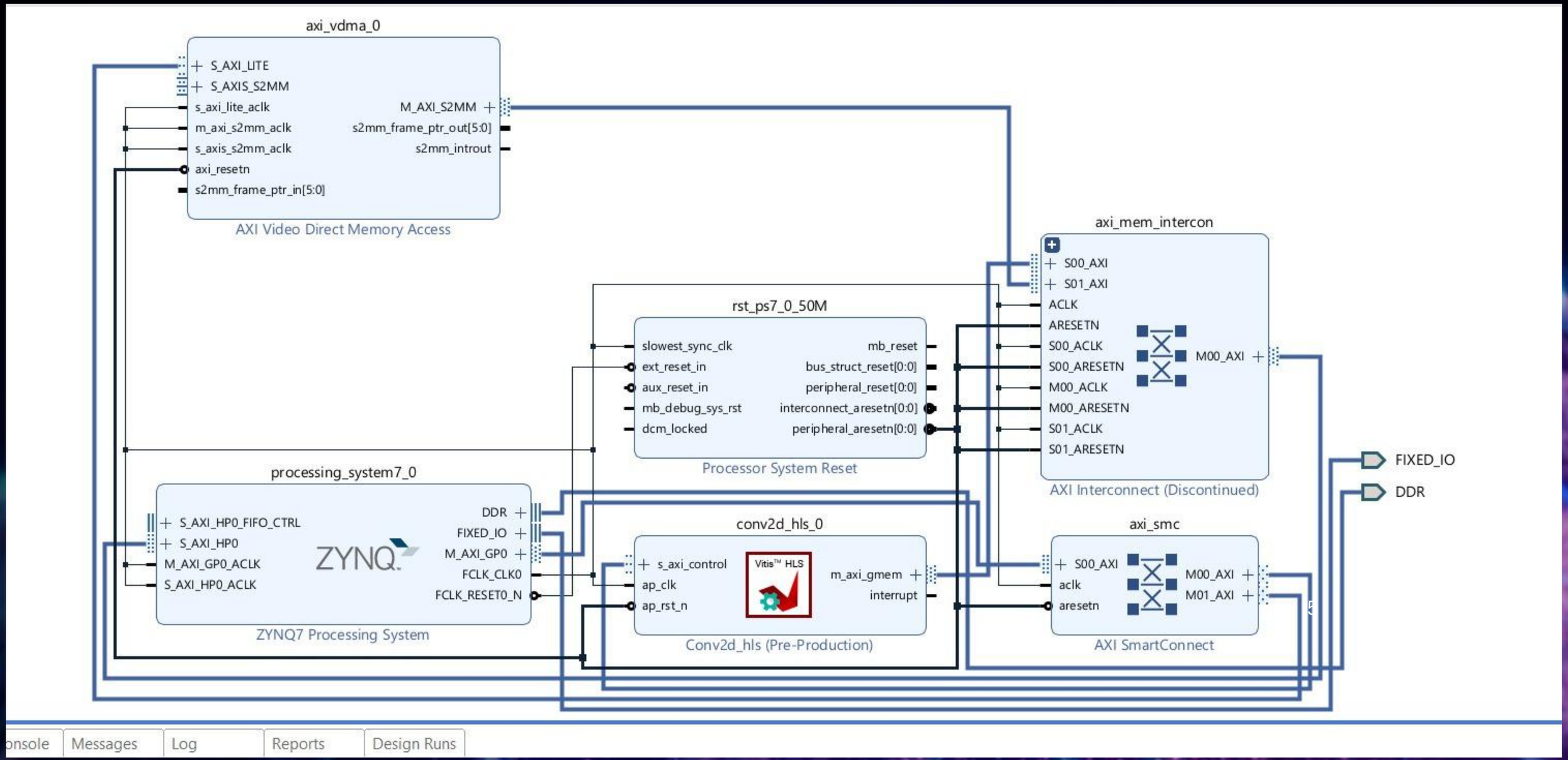
Pipeline Execution Flow:

- Frame captured at 720p
- Frame resized for MobileNet input
- Convolution layers offloaded to PL
- Feature maps returned to PS
- Classification & bounding boxes generated
- Display rendered

Par**allelism achieved through:**

- AXI DMA transfers
- Non-blocking processing
- Overlapping computation & data movement

BLOCK DESIGN :



FPGA Acceleration:

Accelerated operations:

- Convolution layers
- Multiply-Accumulate (MAC)
- Parallel DSP utilization

Benefits:

- Reduced convolution latency
- High parallel throughput
- Improved energy efficiency

Results:

Metric	CPU Only	Single Pipeline
FPS	3–5 FPS	17–20 FPS
Convolution Latency	5–10 ms	< 0.1 ms
Parallelism	Sequential	Parallel (DSP-based)


THANK
YOU!!!