Permanent Magnet Alternating Current Motor Controller

Alex Simon

October 30, 2021

Abstract

This document explores the design decisions for a Permanent Magnet Alternating Current (PMAC) motor controller. Specifically, the hardware component design choices and the commutation techniques used within the project.

1 Introduction

This paper will explore the process of designing a PMAC motor controller and the difficulties discovered along the way. Beginning with the printed circuit board (PCB) design stage, each of the major components used in the PCB will be evaluated. Once the PCB has been designed two different commutation techniques will be explored. Trapezoidal commutation will be evaluated first to validate the hardware design because it is less complex than Field Oriented Control (FOC). Field Oriented Control will be evaluated last because the software complexity introduces a lot of area for error, but the hardware will already be validated from trapezoidal control. The advantage of this order allows one problem to be solved at a time; hardware then control strategy.

2 Hardware Design

The hardware is divided into two sections: the power and control stage. Each stage is designed on a separate PCBs to minimize cost and for ease of testing. This modular design also allows for each stage to be tested independently of the other and eventually costs less because fewer components will need to be replaced when something goes wrong.

2.1 Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

To evaluate the advantages and disadvantages of each MOSFET a power calculation can be done. The power consumed by a MOSFET can be estimated using Equations 1, 2, 3, and 4.

$$P_{Total} = P_{On} + P_{Off} + P_{Sw} \tag{1}$$

$$P_{On} = (I_{Continuous})^2 * R_{ds(on)} * DutyCycle$$
 (2)

$$P_{Off} = (1 - DutyCycle) * V_{Off} * I_{Leakage}$$
(3)

$$P_{Sw} = \frac{V_{Off} * I_{Continuous} * (T_{Rise} + T_{Fall}) * F_{Sw}}{2}$$

$$\tag{4}$$

Using the given parameters for each MOSFET and Equations 1, 2, 3, and 4 it becomes easier to compare each MOSFET. For this project 8 different MOSFETs were chosen for evaluation. As shown in Table 1, Infineous BSC016N06 consumes the least power, but due to the rated voltage, rated current and solderability Infineous IPB017N10N5 was chosen instead.

MOSFET	P_{On}	P_{Off}	P_{Sw}	P_{Total}
BSC047N08NS3	0.94	24μ	0.1344	1.07
CSD18540Q5B	0.44	24μ	0.0576	0.50
BSC014N06NS	0.29	24μ	0.1008	0.39
BSC016N06NS	0.32	24μ	0.0864	0.41
IPT012N08N5	0.24	2μ	0.2928	0.53
CSD18531Q5A	0.70	24μ	0.0504	0.75
IPB017N10N5	0.34	24μ	0.2400	0.58
IPB044N15N5	0.88	24μ	0.0528	0.93

Table 1: Power Consumption for each MOSFET assuming: $V_{Off} = 48v$, $f_{Sw} = 10kHz$, $I_{Continuous} = 20$, DutyCycle = 50%. Note: Equation 4 uses rectangular commutation to estimate P_{Sw} .

2.2 Gate Driver

A MOSFET is only as good as the gate driver behind it. If the gate driver has slow rise and fall times, the MOSFET will have slow rise and fall times irregardless of its own rise and fall times. In addition if the driver does not provide enough current fast the gate of the MOSFET will have slow rise and fall times, again irregardless of its own rise and fall times. When choosing the gate driver a voltage rating of 150v $\geq V_{rated} \geq 100v$ was desired. The 150v upper bound is for monetary and complexity reasons while the 100v lower bound is needed to withstand voltage transients.

After the voltage rating rise and fall times of the gate driver are most important. The goal is to have faster rise and fall times than the chosen MOSFET; $23\mu s$ and $27\mu s$ respectively for *Infineons* IPB017N10N5. The amount of peak current of the gate driver can also play a factor in rise and fall times as it needs to charge the MOSFET gate.

With these three constraints it came down to 2 different Gate Drivers, *Texas Instruments* UCC27201 and UCC27211, with UCC27211 being a revision later than UCC27201. Table 2 shows a comparison between several key characteristics of the drivers.

Characteristic	UCC27201A	UCC27211
Rated Voltage (V)	110	110
Rise Time (μ s)	8.0	8.0
Fall Time (μs)	7.0	7.0
Peak Current (A)	3.0	4.0
Negative voltage handling at HS pin (V)	-15.0	-12.0
Cost (\$)	3.12	3.60
Footprint	SOIC-8	SOIC-8

Table 2: With four of the seven highlighted characteristics being the same both driver would work, but for the added peak current UCC27211 has an edge. In the event that more neggative voltage handling is needed UCC27201A can be a drop in replacement for the UCC27211.

2.2.1 Bootstrap Capacitor

The bootstrap capacitor is one of the most important components besides the driver itself. This capacitor ensures the gate has sufficient voltage during operation, especially at high duty cycles.

To determine the size of Bootstrap Capacitor we must first find the gate charge of the MOSFET. For the IPB017N10N5 MOSFET, we can see from the data sheet that Q_G is 168nC. Using the formulas from Texas Instruments [1], we can calculate the bootstrap capacitance for this system.

Given the following parameters from the Gate Driver and MOSFET:

$$\begin{array}{lll} V_{DD} = 12V & I_{DDO} = 2.6mA & F_{SW} = 10kHz \\ V_{DH} = 0.85V & I_{HBS} = 0.5nA & D_{MAX} = 0.99 \\ V_{HBL} = 5.5V & I_{HB} = 65\mu A & Q_G = 168nC \end{array}$$

Using Equation 3 from Bootstrap Circuitry Selection for Half-Bridge Configurations [1].

$$Q_{Total} = Q_G + I_{HBS} * \frac{D_{MAX}}{F_{SW}} + \frac{I_{HB}}{F_{SW}}$$

$$Q_{Total} = 168 * 10^{-9} + 0.5 * 10^{-9} (\frac{0.99}{10^4}) + \frac{65 * 10^{-6}}{10^4} = 174.5nC$$

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL}$$

$$\Delta V_{HB} = 12 - 0.85 - 5.5 = 5.65V$$

$$C_{Boot} \ge 10 * \frac{Q_{Total}}{\Delta V_{HB}}$$

$$C_{Boot} \ge 771nF$$

When comparing the calculations to Silicon Labs [2], the boot strap capacitor values are within $\pm 63nF$ of each other, as shown in Figure 1.

Isolation Bootstrap Calculator

The web-based bootstrap calculator helps you determine the required CB recharge current at MAX and MIN duty cycle, and provides the information required to determine the best fit bootstrap module.



Figure 1: Bootstrap capacitor calculator provided by Silicon Labs [2].

2.3 DC-DC Converter

To convert 48v into a usable 12v and 5v for the Microcontroller, Gate Driver, etc... I needed a high voltage regulator. The two types of regulators are linear and switching, and based on the large voltage conversion a switching regulator is the better choice. *Texas Instruments* TL2575HV switching regulator had

the specifications for the job [3]. In addition it has an adjustable regulator so that I could use the same Integrated Circuit (IC) for both of the conversions.

2.3.1 5 Volts

The 48v to 5v conversion is the harder of the two due do the extensive voltage difference, but running though the calculations given by [3] it is possible.

Known:

$$\begin{aligned} V_{in} &= 48v & V_{out} &= 5v & R_1 &= 2k\Omega \\ I_{load} &= 1A & V_{ref} &= 1.23v & F_{sw} &= 52kHz \end{aligned}$$

Following the sizing steps given by the TL2575HV data sheet [3]:

$$R_{2} = R_{1}(\frac{V_{out}}{V_{ref}} - 1) = 6.13k\Omega$$

$$\epsilon * \tau = (V_{in} - V_{out}) * t_{on} = (V_{in} - V_{out}) * \frac{V_{out}}{V_{in}} * \frac{1000}{f_{sw}} = 86.14V * \mu s$$

$$86.14V * \mu s \to L1 = 330\mu H$$

$$I_{L_{1}(pk)} = I_{load} + (V_{in} - V_{out}) * \frac{\frac{V_{out}}{V_{in}} * \frac{1}{J_{sw}}}{2*L_{1}} = 1.13A$$

$$C_{out} \ge 7758 * \frac{V_{in}}{V_{out}*L_{1}} \to C_{out} \ge 235.1\mu F \to C_{out} \approx 1mF$$

2.3.2 12 Volts

Write your subsection text here.

2.4 Microcontroller

The STM32F407VG microcontroller was chosen for this project because it contains several key features that make PMAC control easier. The first feature this microcontroller has is automatic dead time insertion [4]. The second feature is complementary (low side) wave generation [4]. In addition to these features the high clock frequency (168MHz) and built in digital signal processor (DSP) [4] also make this microcontroller a prime choice for this project.

2.4.1 Pulse Width Modulation (PWM) Strategy

One method to reduce electromagnetic noise and voltage transients within the system is to stagger the set/reset events in the timing module of the microntroller. As shown in Figure 2 when the timer is set to up counting in set/reset mode all of the MOSFETs turn off at the same time it generates an unnecessary amount of electromagnetic noise and transients. To combat this issue I decided to stagger the events by setting the timer to up/down counting in reset/set/reset mode. As shown in Figure 3 this staggers the transition events which helps reduce electromagnetic noise and voltage transients which in turn increases the longevity of the electrical components.

3 Commutation Techniques

Write your section text here.

3.1 Trapezoidal Control

Write your subsection text here.

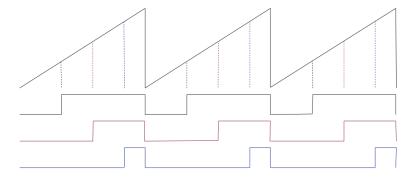


Figure 2: Up counting mode for phases A, B, and C. Turning off all the phases at the same time will induce a transient in voltage and reduce the device's overall electromagnetic compatibility.

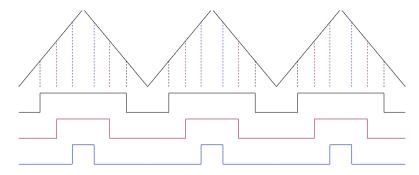


Figure 3: Up/down counting mode for phases A, B, and C. This method of PWM reduces electromagnetic interference and voltage transients by staggering when the MOSFETs turn on and off.

3.2 Field Oriented Control

Write your subsection text here.

4 Conclusion

Write your conclusion here.

5 Lessons Learned

Write your lessons learned here.

References

- [1] Texas Instruments. Bootstrap Circuitry Selection for Half-Bridge Configurations. http://www.ti.com/lit/an/slua887/slua887.pdf
- [2] Silicon Labs. *Isolation Bootstrap Calculator*. https://www.silabs.com/support/isolation-bootstrap-calculator
- [3] Texas Instruments. TL2575, TL2575HV 1-A Simple Step-Down Switching Voltage Regulators http://www.ti.com/lit/ds/symlink/tl2575-12.pdf

[4] RM0090 Reference Manual STM32F405/415, STM32F407/417, STM32F427/437 and STM32F429/439 advanced Arm-based 32-bit MCUs

 $\label{lem:manual} $$ $$ https://www.st.com/resource/en/reference_manual/dm00031020-stm32f405-415-stm32f407-417-stm32f427-437-and-stm32f429-439-advanced-arm-based-32-bit-mcus-stmicroelectronics.pdf$