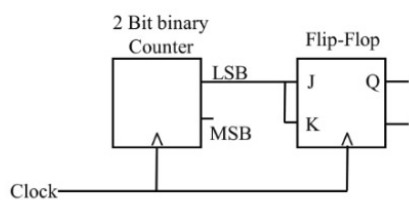


GATE

NIKHIL

November 23, 2023

1. For the circuit shown, the clock frequency is f_0 and the duty cycle is 25%.
For the signal at the Q output of the Flip-Flop,_____.



- (a) frequency is $\frac{f_0}{4}$ and duty cycle is 50%
- (b) frequency is $\frac{f_0}{4}$ and duty cycle is 25%
- (c) frequency is $\frac{f_0}{2}$ and duty cycle is 50%
- (d) frequency is f_0 and duty cycle is 25%