Yasmeen Osama

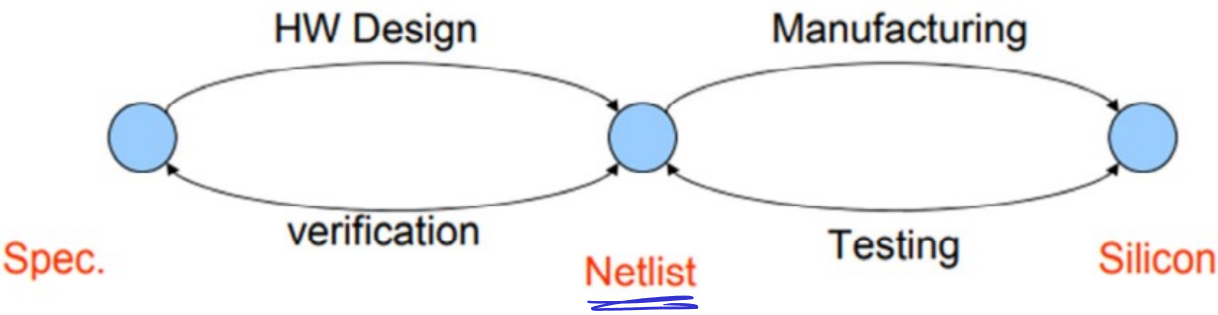
Lec 1 : Introduction

verification : is the Process used to demonstrate that the intent of design is Preserved in its implementation. (70 % of design effort goes behind verification)

1 – It helps ensuring that design meets specifications and makes sure that SOC has less bugs.

2 - verification is always on the critical path for any Product design

3 - verification is not a test bench.



group of gates

10% system Design   20% Implementation   70 % verification

re-spin : the bugs was discovered after sending the design for manufacturing

system verilog : is the most commonly used hardware description language for verification in industry

why do Companies pay less attention to verification?

1- To save money   2- To save time   3- To hide the inefficiencies

0.10		0.5
0.01		0.25
0.001		0.125
0.0001101	(8 bits)	0.09765625 ≠ 0.1
0.0001100110011001	(16 bits)	0.0999984423 ≠ 0.1
0.00011 0011 ----	(24 bits)	0.09999999643 ≠ 0.1

we can never reach 0.1 ⟹ after 100 hour work (error = 0.1287 sec)

Main Sources of Bugs :-

[1] Design Errors :

1- This mainly Comes due to misinterpretation of the specification

2- wrong component

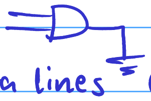
3- Incorrect wiring

[2] Fabrication Defects :

1- Due to problems in the fabrication process

Ex: • Contaminating particle : dust Particle falling on the chip destroying thousands of transistors

• Break in a meta line

2 - Stuck at faults : stuck at Zero or one  or

3 - Bridging faults : metal between two meta lines (shorts between signal lines)

[3] Physical failures :

Due to aging through the Chip life cycle

Defects : Occure during manufacturing detected by tests performed after the end of manufacturing.

Failures : Occure during service, after the chip has been sold and used

Type of verification :-

[1] functional verification : 1- Simulation 2- formal

[2] Performance verification : make sure that the design will meet its targeted bandwidth and latency levels.

Bandwidth : the number of bits you Can send Per second

Latency : the amount of time needed for the data to travel from one point to another

PDL : Performance Description Language provides a compact notations for the specification of non-functional attributes of VLSI system

[3] Power Aware verification : verify the operation of a design under active Power management (required to ensure energy efficiency)

4] Clocking & CDC verification : Dealing with multiple clock domains in a single SoC

CDC : Clock Domain Crossing

Types of Problems

1- Data loss in fast to slow Clock domain

2- Improper data enabling : the data is enable while it's still changing

توفر بيانات غير مناسبة لتغيرها لازم تثبت الأول وبعدها يبقى متاحة

3- Convergence of synched signals : make glitches

4- Reset synchronization : when a transmitting flip flop in a clock domain is reset and the receiving flip flop in a different clock domain has no reset , this results in glitches and loss of functional Correlation.

The approaches for CDC verification

1- flat SoC verification :

- we run verification on the whole design as one entity.
- need the whole design is avilable and well integrated.
- Find any critical bug very late in the design cycle.
- Difficult to Scale it because of huge number of violations and huge run time.

2- Black Boxing :

- verify inputs and outputs only without block analysis.
- Save runtime
- Can be done Selectively for bulky blocks

3- Gray Boxing : Check only inter block violations and not those that are totally within an block

5] DFT / DFM verification : ensure that inserted Cells are Correctly implemented.

DFT : Design for Testing (group of flip flops that act as shift registers)

Its importance 1- Can save time and Cost by detecting and fixing DFT errors early
2- Can improve the test quality and reliability of the Chip

DFM : Design for Manufacturing

6 Hardware - Accelerated Simulation

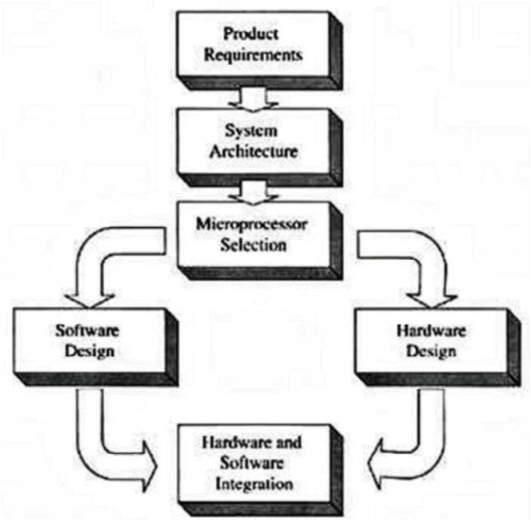
- used at the higher levels of verification like → a system verification
  → a full chip verification
- we try to move the time consuming Part of the design to the hard ware by taking those time consuming modules, and synthesize and compile them into real hardware FPGAs, so they can run on a real hardware much faster.

Challenges : 1- Generally improves speed but degrades on HW-SW communication (testbench)
2- Abstracting HW-SW communication at transaction level rather than cycle level desired for better speeds

7 HW/SW Coverification

Verifying embedded systems

It means running the Software on the hardware to make sure there are no hardware bugs before the design is committed to fabrication.



اللهم إني أستودعك ما قرأت وما حفظت وما تعلمت، فرده لي عند حاجتي إليه إنك على كل شيء قدير، وحسبنا الله ونعم الوكيل.

- ربّ ادخلنى مدخل صدق وأخرجنى مخرج صدق واجعل لى من لدنك سلطاناً نصيراً.

- ربّ اشرح لى صدري، ويسّر لى أمري، واحلل عقدة من لساني يفقه قولي، باسم الله الفتاح، اللهم لا سهل إلا ما جعلته سهلاً، فإنك إن شئت تجعل الصعب سهلاً يا أرحم الراحمين.