



Department of Computer and Systems Engineering
Senior 1, and Senior 2 Level Students

2nd Semester, 2023/2024

Course Code: CSE 313s

Time allowed: 1 Hr.

Digital Verification

The Exam Consists of six Questions in two Pages.

Maximum Marks: 30 Marks

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تعليمات هامة

- حيازة التليفون المحمول مفتوحا داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب.
- لا يسمح بدخول سماعة الأذن أو البلوتوث.
- لا يسمح بدخول أي كتب أو ملازم أو أوراق داخل اللجنة والمخالفة تعتبر حالة غش.

Question 1:

[5 marks]

Show the value of x, y, and z on the timeline.

```
initial begin
  x=5;y=6;z=7;
  x<=#4z;
  #1;
  z<=y;
  y=y+1;
  #1
  y<=x;
  x=9;
  #1;
  z<=#2x;
end
```

Question 2:

[5 marks]

Calculate the following code coverage items

- statement coverage
- Branch coverage
- toggle coverage for x and y

```
initial begin
  x=1;
  y=0;
end
always @(a or b)begin
  if(a==1)
    x=0;
  else if(b=1)
    y=1;
end
```

Question 3:

[5 marks]

- 1) What is the difference between static and dynamic verification ?
- 2) If we have a high functional coverage but low code coverage, what is most likely to be the problem in real life development ?
- 3) What is the difference between these 3 expressions: **verification**, **post-silicon validation** and **testing**
- 4) What is the main disadvantage of pure random testing ?
- 5) Hardware acceleration is usually used to speed up verification closure and gain more trust in the design, however it has a couple of drawbacks, what are they ?

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Question 4:

[5 marks]

Draw the logic diagram for the circuit that represents this module

```

module module_a(input x,y,clk,rst, output reg z);

    wire w1, w2;

    assign w1 = x & y;
    assign w2 = w1 & y;

    always @(posedge clk)
        if(y==1)
            z <= ! w2;
        else
            z <= x || w1;
    always @(posedge rst)
        z <= 0;

endmodule

```

Question 5:

[5 marks]

Write a verification plan for the given binary_counter in the following form.

Feature	Checkers list	Stimulus	Priority

```

module binary_counter(input clk,rst, output reg [3:0] count);

    always @(posedge clk or posedge rst) begin
        if (rst) begin
            count <= 4'b0000;
        end else begin
            count <= count + 1;
        end
    end

endmodule

```

Question 6:

[5 marks]

- 1) Write a systemverilog code that declares a dynamic array of integers named "my_arr" that have 8 elements
- 2) Fill the array with values from 1 to 8 using literals.
- 3) Using one of array manipulation functions print number of elements greater than 5
- 4) What is the data structure that will be returned by the function you used in (3)
- 5) What is the data type of my_arr[9] ?