Ain Shams University
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CSE 313s
Selected Topics in Computer Engineering
Sheet 8

1. Which of the following is not supported inside a System Verilog interface?
   a. Functions
   b. Tasks
   c. Modules
   d. always blocks

2. What is the difference between program block and module?

3. Why always block is not allowed in program block?

4. What are the ways to avoid race condition between testbench and RTL using System Verilog?

5. Which of the following are true?
   a. Program can contain always blocks
   b. Module can contain Class
   c. Interface can contain module instance
   d. Program can contain Class

6. What is the difference between $display, $write, $monitor, and $strobe in SystemVerilog?

7. What is *final* block, and how it differs from an *initial* block?