AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING

Department of Electrical Engineering
4th Year, Computer & Systems Engineering

2nd Semester, 2021/2022	**Course Code: *CSE 412***	***Time allowed: 2 Hrs.***

Selected Topics in Computer Engineering

The Exam Consists of **Four** Questions in **Three** Pages. ***Maximum Marks: 90 Marks*** **1 / 3**

تعليمات هامة

- حيازة التيلفون المحمول مفتوحا داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب وإذا كان من الضرورى الدخول بالمحمول فيوضع مغلقاً فى الحقائب.
- لا يسمح بدخول سماعة الأذن أو البلوتوث.
- لايسمح بدخول أي كتب أو ملازم أو أوراق داخل اللجنة والمخالفة تعتبر حالة غش.

Question 1: **[ILO: a1, a2, a3] [35 Marks]**

A. State briefly what is the difference between *testing* and *verification*?
B. Make a comparison between *code coverage* and *functional coverage*.
C. Comment briefly on the following two statements (agree or disagree and why):
- 100% functional coverage ensures that the design can have no bugs.
- 100% code coverage guarantees that the test bench is very well written.

D. One of the practical problems in simulation-based verification is the large input space. State briefly how the problem is tackled in real life.
E. State the differences between *formal verification* and *simulation-based verification*
F. What are the two main types of formal verification?
G. What is the difference between *rand* and *randc* in System Verilog?

Question 2: **[ILO: c1, c2] [10 marks]**

1. Logic variables can have multiple drivers
   a. True b. False

2. Target to the completion of Verification process is
   a. Functional coverage 100% and code coverage is 100%
   b. If all the test cases ran
   c. Functional coverage 100% and code coverage is not considered
   d. Code coverage should be 100% and functional coverage is not considered

3. *array [4][8]*. This array declaration type is:
   a. Compact declaration
   b. Verbose declaration
   c. Single dimension array declaration
   d. None of the above

4. *modport* is used to
   a. declare input and output skew
   b. declare direction of signals
   c. synchronize signals
   d. make interface complex

5. Randomization of any random variable can be disabled
   a. by overriding in post_randomize function
   b. by setting rand_mode of particular variable to ‘0’
   c. by setting constraint_mode to ‘0’
   d. by constraining particular variable to ‘0’

Question 3: **[ILO: b2, b3] [25 marks]**

A. Write constraints into the following class to create a random array of integers such that array size is between 10 and 20 and the values of the array are in descending order, and the elements of the array are less than 30.

```
class dynamic_array;
  rand int unsigned abc[];
endclass
```

B. What is wrong with following SystemVerilog constraint? Write it correctly.

```
class packet;
  rand bit [15:0] a, b, c;
  constraint pkt_c { 0 < a < b < c; }
endclass
```

C. How many bins are created in following example for coverpoint cp_x ?

```
bit[3:0] var_x;
covergroup test_cg @(posedge clk);
  cp_x : coverpoint var_x {
  bins low_bins[] = {[0:3]};
  bins med_bins = {[4:12]};
}
```

D. What are the transitions covered by following coverpoint?

```
coverpoint my_variable {
  bins trans_bin[] = ( a,b,c => x, y);
}
```

E. Is this a correct code? State the reason.

```
module test();
  enum {a=0, b=7, c, d=8} alphabet;
endmodule
```

Question 4: **[ILO: b1, b2, c1, c2] [20 marks]**

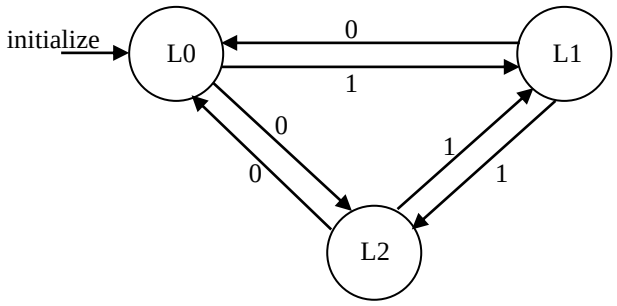
A. Write *concurrent* SVA to express the following:

- Every time a request signal *req* is high (at the rising edge of the clock), an acknowledgement signal *ack* becomes high exactly 3 clocks later.
- Every time (at the rising edge of the clock) the valid signal *vld* is high, the *cnt* signal is incremented by 1.

B. Two signal lines *r1* and *r2* are mutually exclusive (i,e both of them cannot be high at the same time). The following assertion is used to take care of that. State whether this assertion is right or wrong with justification.

```
assert (tr.r1 ^ tr.r2 );
```

C. A finite state machine is described by the following state diagram. It has one input *pi*, a clock signal *clk*, and one signal called *initialize*, which puts the machine in the state L0 whenever it is active. Write a coverage group to check whether all the transitions have been exercised.



D. What is the maximum coverage you can get from the following coverage group? How to increase the maximum coverage in this case?

```
class Transaction;
  rand bit [2:0] p;
  rand bit [3:0] k;
endclass

Transaction tr;

covergroup CovPort;
  CP1 : coverpoint (tr.p + tr.k);
endgroup
```

END of Exam, Good Luck