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Faculty of Engineering
Computer and Systems Department
Spring 2022

CSE412
Selected Topics in Computer Engineering
Sheet 1

1. Why is Verification important in the SOC design flow?
    a. It helps the designer to don't care about what he does during design process
    b. It helps ensuring that design meets specification and makes sure that SOC has less bugs.
    c. It is just fun to do
    d. It makes the whole design flow looks complete.

2. What is the most commonly used Hardware description language for Verification in industry?
    a. C++
    b. VHDL
    c. System Verilog
    d. Vera
    e. System C

3. What happens if a critical functional bug escapes the chip design flow into silicon?
    a. It is easy to just fix the bug in silicon just like fixing a software code
    b. A re-spin of chip must be done to fix the bug and fabricate again
    c. Just ignore and continue using the chip

4. What is meant by inheritance in object-oriented programming?
    a. It is the concept that allows a class to instantiate another class as its member
    b. It is a way in which a class can hide all its properties and attributes being accessed from outside
    c. It is a concept in which same object can exist in multiple forms
    d. It is a way in which a class can extend all properties and methods of a base class

5. Which of the Following is not captured in a verification plan?
    a. Scenarios to be verified for ensuring design correctness
    b. Methodology for stimulus generation for exercising design
    c. Verification effort to complete Verification

d. Design implementation details like Flip Flops, State machines etc

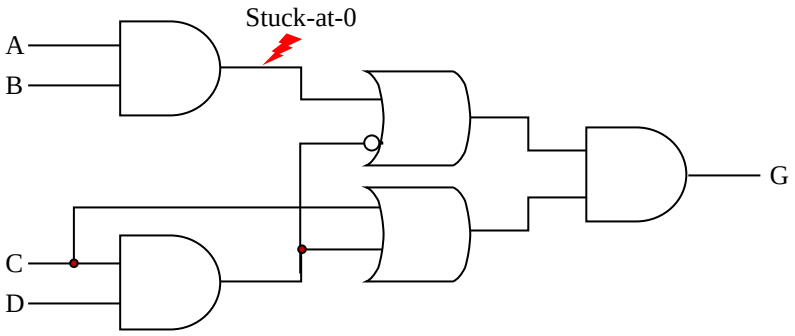
6. Which of the following statement related to assertions is not correct?
   a. Assertions are a way to generate stimulus for verification
   b. Assertions helps in debugging and checking of design correctness
   c. Assertions are useful in both Simulation and Formal Verificaiton
   d. Assertions are useful to judge quality of stimulus used for verification

7. Which of the following is not correct with respect to formal verification?
   a. Formal Verification uses mathematical models and algorithms to exhaustively verify design intent
   b. Formal Verification needs effort in creating stimulus generator for verifying design
   c. Formal Verification on FSM based models to prove FSM state transitions and behavior is known as model checking
   d. Formal Verification can use assertions to capture design intent

8. What is meant by constrained random verification approach?
   a. It is a method of creating random tests for verifying a design by hoping that random seeds will cover all design state space verification
   b. It is a method of creating intelligent stimulus using constraints around interesting design points that allows faster and thorough testing of design features under different conditions
   c. It is a method in which we create tests for each design feature and working conditions and use those for design verification

9. Which of the following is not true with respect to HW accelerated simulation or emulation?
   a. It improves the simulation speed and allows to run long tests in shorter time during verification
   b. It improves the overall debug capability and observability in the design
   c. It helps to gain higher confidence in system level verification
   d. It can help in early SW validation and reduce risks of finding bugs after chip is manufactured.

10. The following circuit has a stuck-at-0 fault as shown. Find a testing pattern for ABCD such that we can observe the fault at the output G.



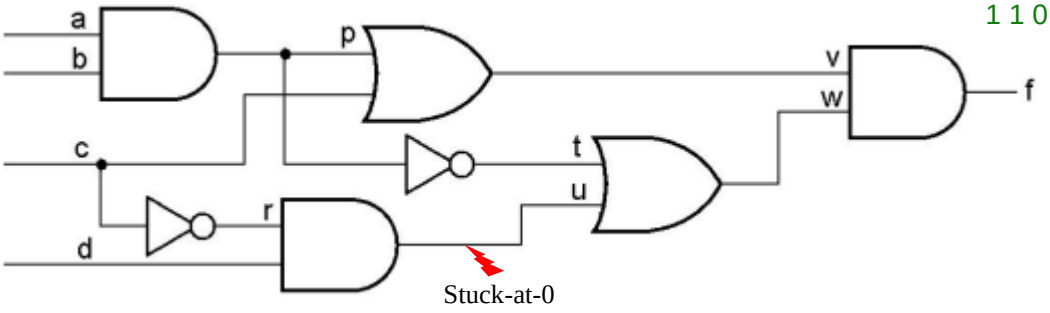
A B C D
1 1 1 1

11. For a circuit with k lines _____ single stuck-at faults are possible.
    a. k b. 2k c. k/2 d. k^2

12. The quality of the test set is measured by
    a. fault margin b. fault detection c. fault correction d. fault coverage

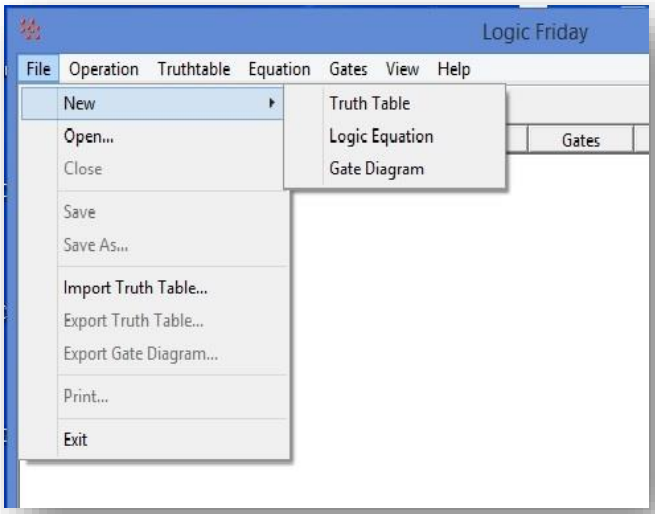
13. The following circuit has a stuck-at-0 fault as shown. Find a testing pattern for ABCD such that we can observe the fault at the output F.

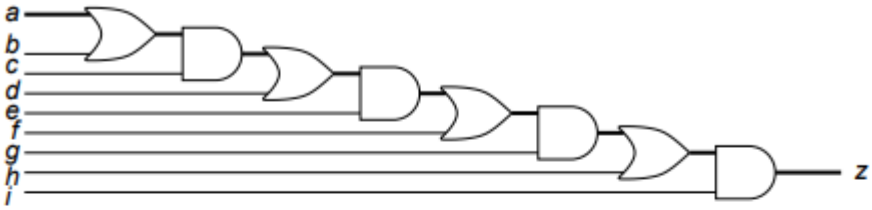
A B C D
1 1 0 1



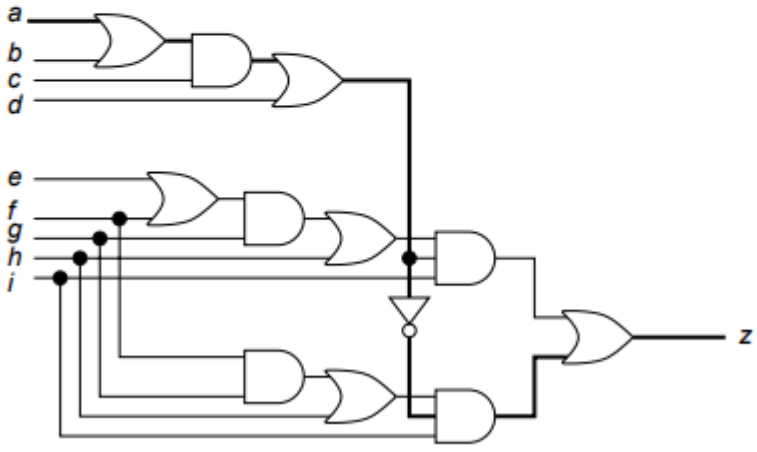
CSE 313s: Digital Design Verification
ASSIGNMENT 1

1. Visit the following site: https://download.cnet.com/Logic-Friday/3000-20415_4-75848245.html
2. Download the Logic Friday tool (file: lf114_setup.exe (859 KB))
3. Get acquainted with the tool.
4. From the file menu, select a new to enter a design in the form of your choice.
5. After you enter the function press on the minimize icon, to minimize your design.
6. The figure below shows two versions of the same design. The second version was designed to reduce the critical path delay of the first version. You are required to prove that both versions are equivalent, by constructing a miter circuit, and showing that its output is 0.





(i) Original circuit.



(ii) Redesigned circuit.