



Department of Computer and Systems Engineering

Senior 1, and Senior 2 Level Students

2nd Semester, 2022/2023

Course Code: CSE 313

Time allowed: 1 Hr.

Digital Verification

Model: A

The Exam Consists of Five Questions in five Pages.

Maximum Marks: 25 Marks

1 / 5

تعليمات هامة

- حيازة التيلفون المحمول مفتوحا داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب.
- لا يسمح بدخول سماعة الأذن أو البلوتوث.
- لا يسمح بدخول أي كتب أو ملازم أو أوراق داخل اللجنة والمختلفة تعتبر حالة غش.

Question 1:

[12 marks]

Select only one answer in the following questions:

- 1) Coverage is used to measure the quality and progress of
 - a) RTL development
 - b) Specs extraction
 - c) verification process
 - d) fabrication process
- 2) Which of the following is done on mass production to verify against fabrication faults
 - a) Pre-silicon verification
 - b) Post-silicon validation
 - c) Structural testing
 - d) HW accelerated verification
- 3) To verify that a certain property in the design holds, we can use
 - a) Model checking as a static analysis technique or assertions during simulation
 - b) assertions as a static analysis technique or Model checking during simulation
 - c) Model checking during simulation or assertions during simulation
 - d) All of the above
- 4) In coverage-driven verification what may happen when coverage-time curve flattens
 - a) Randomization Constraints may be tightened
 - b) Direct tests may be ran
 - c) Verification process ends because coverage goals are achieved
 - d) All the above
- 5) If we have a high functional coverage but low code coverage, which of the following is most likely to be the problem in real life development
 - a) RTL have useless code
 - b) RTL have Missing features
 - c) Verification Plan is not complete (missing some features)
 - d) Testing process is not complete (more tests need to be ran)

Digital Verification

The Exam Consists of Five Questions in five Pages.

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2 / 5

6) Equivalency checking is considered

- a) Formal verification technique
- b) Simulation based technique
- c) Both (a) and (b)
- d) None of the above

7) For the module Q7, which of the following is correct ?

- a) $(x < y)$ evaluates to 1 and path1 is executed
- b) $(x < y)$ evaluates to 0 and path2 is executed
- c) $(x < y)$ evaluates to x and path2 is executed
- d) $(x < y)$ evaluates to x and path1 is executed

8) $\{1,2\{3\}4\},5,6\}$ is equivalent to

- a) $\{1,2,3,4,5,6\}$
- b) $\{1,4,4,4,4,4,5,6\}$
- c) $\{1,2,4,4,4,5,6\}$
- d) $\{1,3,3,4,5,6\}$

```
module Q7 ;
  reg[3:0] x,y;

  initial begin
    x=5;

    if(x<y)
      $display("path1")
    else
      $display("path2")

  end
endmodule
```

9) For module Q9, Which of the following is correct

- a) X is assigned at time step 3 and y assigned at time step 0
- b) Both x and y are assigned at time stem 0
- c) Both x and y are assigned at time stem 3
- d) X is assigned at time step 0 and y assigned at time step 3

```
module Q9 ;
  reg[3:0] x,y;

  initial begin
    x<= #3 5;
    y=6;

  end
endmodule
```

10) Which of the following data structures can use non-integer indexing

- a) Static arrays
- b) Dynamic arrays
- c) Associative arrays
- d) Queue

11) Which of the following is a valid declaration in SystemVerilog ?

- a) * my_array [string]
- b) String my_array [*][string]
- c) Reg [3:0] my_que[\$][\$]
- d) String [3:0] my_dynamic_array[]

12) What is the returned value from this statement ?

- a) 1
- b) 7
- c) {7,12}
- d) 19

```
int my_array [4]={3,4,7,12};
my_array.sum() with( (item>5)?item:0 )
```

Digital Verification

The Exam Consists of Five Questions in five Pages.

Maximum Marks: 25 Marks

3 / 5

Question 2:

[4 marks]

Draw the logic diagram for the circuit that represents this module

```
module exam (input x,y,c1k, output reg z1,z2);

wire w1,w2;

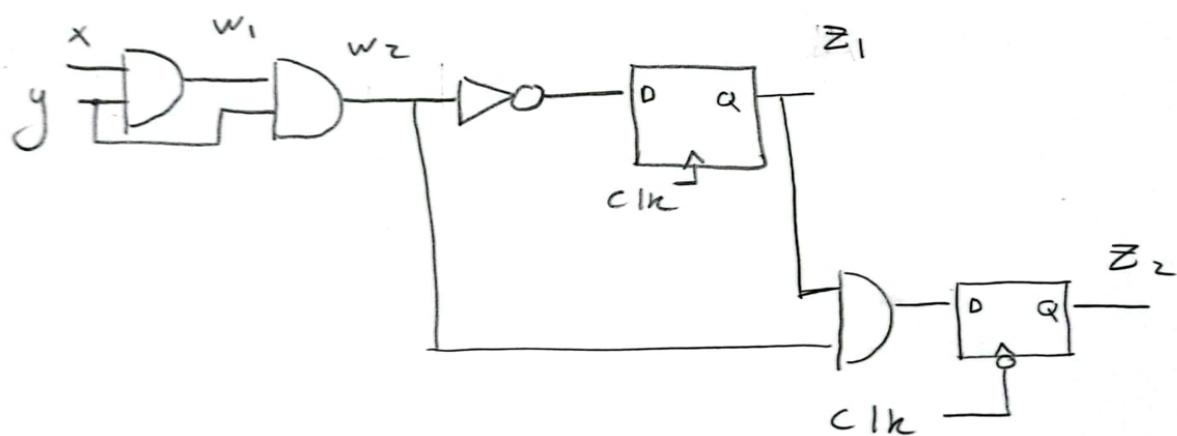
assign w1 = x & y;
assign w2 = w1 & y;

always @(posedge c1k)
z1 <= ! w2;

always @(negedge c1k)
z2 <= z1 & w2;

endmodule
```

Answer :



Digital Verification

The Exam Consists of Five Questions in five Pages.

Maximum Marks: 25 Marks

4 / 5

Question 3 :

[4 marks]

It is required to store this matrix and perform some operations on it.

1	12	5
3	7	14

- 1) Declare a dynamic array of integers with the same size as the matrix

```
int matrix [][] = new[2];
foreach (matrix[i]) matrix[i]=new[3];
```

- 2) Assign the declared array with the values in the matrix using array literal

```
matrix = '{1,12,5},{3,7,14};
```

- 3) Write a foreach loop that loops only on rows of this array, and prints each row elements

```
foreach(matrix[i])begin
    $display(matrix[i]);
end
```

- 4) Edit the above code using the array locator function “**find()**” to print only elements greater than or equal to 5

```
foreach(matrix[i])begin
    $display(matrix[i].find with(item >=5));
end
```

Digital Verification

The Exam Consists of Five Questions in five Pages.

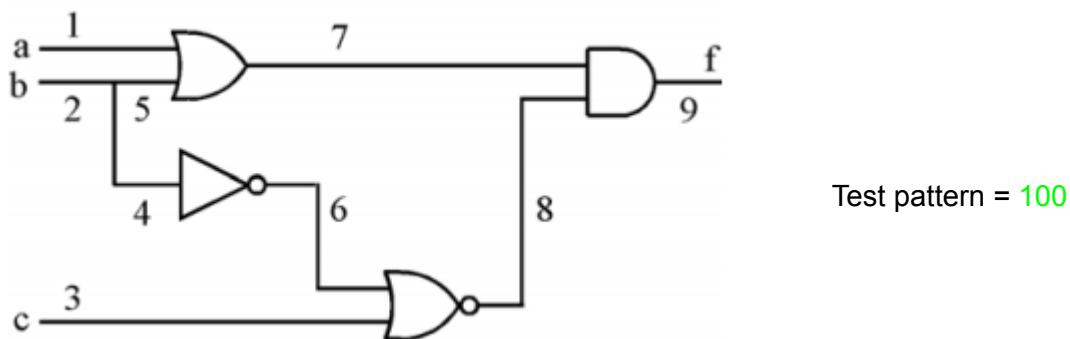
Maximum Marks: 25 Marks

5 / 5

Question 4 :

[2 marks]

The following circuit has a stuck-at-0 fault at wire 6 . Find a testing pattern for ABC such that we can observe the fault at the output F.

**Question 5 :**

[3 marks]

Consider the following function: $F(a,b,c) = ac + bc + a'b'c'$. Draw the BDD to represent this function (use order a,b,c from top to bottom). Remember to mark the edge with '0' or '1' to indicate 0 and 1 cofactors. Please draw the '0' edges on the left and the '1' edges on the right

Answer :

