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## CSE313s

### Selected Topics in Computer Engineering

### Sheet 9

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1. In System Verilog, class can be defined inside
  - a. Program
  - b. Module
  - c. Package
  - d. All of the above

2. What will be the output of below the code?

```
module test;
  class abc;
    function void display(input int a, input int b=0);
      $display("Value of a = %0d, b = %0d", a, b);
    endfunction
  endclass

  initial begin
    abc obj;
    obj = new();
    obj.display(3);
  end
endmodule
```

- a. Compilation error
  - b. Value of a = 3, b = 0
  - c. Value of a = 3
  - d. Value of a = 3, b = X
3. Randomization of any random variable can be disabled
  - a. by overriding in post\_randomize function
  - b. by setting rand\_mode of particular variable to '0'
  - c. by setting constraint\_mode to '0'
  - d. by constraining particular variable to '0'

4. What will be the output of below the code?

```
module test;

  class abc;
    static int sum;
    function int calc(input int a, input int b);
      this.sum = a+b;
      return sum;
    endfunction
  endclass

  initial begin
    abc obj1, obj2;
    obj1 = new();
    obj2 = new();

    obj1.sum = obj1.calc(10,20);
    obj2.sum = obj2.calc(30,40);

    $display("obj1.sum = %0d, obj2.sum = %0d", obj1.sum, obj2.sum);
  end
endmodule
```

- a. obj1 sum = 0, obj2 sum = 0
- b. obj1 sum = 30, obj2 sum = 70
- c. obj1 sum = 70, obj2 sum = 70
- d. obj1 sum = 70, obj2 sum = 30

5. What will be the value of *var* after randomization?

```
module test;

  class abc;
    rand bit [7:0] xyz;
    constraint xyz_valid {!(xyz inside {[20:40]})};
  endclass

  initial begin
    abc obj1=new();
    obj1.randomize();
    $display(obj1.xyz);
  end
endmodule
```

- a. between 20 and 40
- b. less than 20 or greater than 40
- c. less than 20
- d. greater than 40

6. What is the difference between rand and randc?

7. What is the difference between new( ) and new[ ] in SystemVerilog?

8. What is a *unique* constraint in SystemVerilog?

9. How can we disable or enable constraints selectively in a class?

10. Given a Packet class with following constraints, how can we generate a packet object with address value greater than 200?

```
class Packet;
  rand bit[31:0] addr;
  constraint c_addr { addr inside [0:100];}
endclass
```

11. Write constraints to generate elements of a dynamic array (abc as shown in code below) such that each element of the array is less than 10 and the array size is less than 10.

```
class dynamic_array;
  rand int unsigned abc[];
endclass
```

12. Write constraints to create a random array of integers such that array size is between 10 and 20 and the values of the array are in descending order, and the elements of the array are less than 30.

13. How can we use constraints to generate a dynamic array with random but unique values? Refer the code below:

```
class TestClass;
  rand bit[3:0] my_array[]; //dynamic array of bit[3:0]
endclass
```

14. Given a 32 bit address field as a class member, write a constraint to generate a random value such that it always has 10 bits as 1 and no two bits next to each other should be 1

15. What is the difference between hard and soft constraints?

16. What is wrong with following SystemVerilog constraint?

```
class packet;
  rand bit [15:0] a, b, c;
  constraint pkt_c { 0 < a < b < c; }
endclass
```

17. How to randomize a real data type variable?

18. Write code for the below specs:

- You have 2 variables  $a$ , and  $b$ .
- Generate random values for  $a$ ,  $b$  such that  $a > b$
- Don't use \$random nor \$urandom

19. How to generate random numbers between a range of values?

20. What is the difference between \$random and \$urandom?

21. List the predefined randomization methods.
22. What are bi-directional constraints?
23. Without using *randomize* method nor *randc*, generate an array of unique values?
24. How do you use classes to randomize?
25. How to check whether randomization is successful or not?
26. How to randomize a dynamic array of objects?
27. How to select an element randomly from a queue?