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CSE 313s
Selected Topics in Computer Engineering
Sheet 4

1. Which of the following are true with respect to System Verilog arrays?
   a. Associative arrays can be used when size of an array is not known as it can be built as key/value pairs.
   b. Dynamic arrays are useful for contiguous collection of variables whose number keeps varying.
   c. Dynamic arrays can be re-sized after size is allocated.
   d. All of the above

2. What will be the output of the code below?

```
1 module test;
2   bit [31:0] xyz[*];
3
4   initial begin
5     xyz["a"] = 40;
6     $display(xyz.num());
7   end
8 endmodule
```

   a. a b. 1 c. 40 d. 41

3. Logic variables can have multiple drivers.
   a. True
   b. False

4. 'bit' is two state
   a. True
   b. False

5. Testbench functionality is to:
   a. Generate stimulus and apply to DUT
   b. Capture response and check for correctness
   c. Measure progress against verification goals
   d. All of the above

6. 'wire' variables can have multiple drivers
    a. True
    b. False

7. The declaration of the array shown in the following code is:

```
{{6,7,8},default:4};
```

    a. array_m[3][2]
    b. array_m[1][2]
    c. array_m[2][3]
    d. array_m[3][3]

8. What will be the output of the below code:

```
module test;
  int array[8] = '{5,10,7,4,3,5,7,8};
  int que[$];

  initial begin
    que = array.unique;
    $display(que);
  end
endmodule
```

    a. Compilation error
    b. '{{5, 10, 7, 4, 3, 8}
    c. '{3, 4, 5, 5, 7, 7, 8, 10}
    d. '{5, 10, 7, 4, 3, 5, 7, 8}

9. With respect to dynamic array, which of the following are true (select all those apply)
    a. During runtime, array can be extended and retaining the old values
    b. Can add and remove array elements from anywhere of the array
    c. Array can grow and shrink at runtime
    d. Array is initially empty and space is allocated when new[ ] is called

10. Array [4][8]. This array declaration type is:
    a. Compact declaration
    b. Verbose declaration
    c. Single dimension array declaration
    d. None of the above

11. Which of the following is queue declaration?
    a. int a[ ];
    b. int a[$];
    c. int a;
    d. int a[*];

12. What will be the output of the below code?

```
module test;
  int que[$];

  initial begin
    foreach(que[i]) begin
      $display("que element at index %0d = %0d", i, que[i]);
    end
  end

endmodule
```

a. Fatal error
b. Que element at index 0 = 0
c. Simulation ends without displaying display statement
d. Compilation error

13. Does SystemVerilog support multidimensional arrays?
    a. True
    b. False

14. Is there any method to append one dynamic array to another?

15. Given a is an array defined as follows:

```
int a[] = '{1,4,8,3,7,0,23,2,5,6};
```

What is the difference between the following statements?

```
a.sum() with (item <5)
a.sum() with (int'(item <5))
a.find() with (item < 5)
```

16. What is the difference between Associative array and Dynamic array?

17. What's the difference between data type logic, reg and wire?

18. How many array types in SystemVerilog? How do you use them? Show examples.

19. What is the difference between a bit and logic data type?

20. What is the difference between logic[7:0] and byte variable in SystemVerilog?

21. Which of the array types: dynamic array or associative array, are good to model really large arrays, say: a huge memory array of 32KB?

22. Suppose a dynamic array of integers (myvalues) is initialized to values as shown below. Write a code to find all elements greater than 3 in the array using array locator method *find*

    int myvalues[ ] = '{9, 1, 8, 3, 2, 4, 6};

23. Given a dynamic array of size 20, how can the array be re-sized to hold 40 elements while the lower 20 elements are preserved as original?

24. Given the following code sample:

```
module test;
  byte dt_byte;
  integer dt_integer = 32'b0000_1111_xxxx_zzzz;
  int dt_int = dt_integer;
  bit[15:0] dt_bit = 16'h8000;
  shortint dt_short_int1 = dt_bit;
  shortint dt_short_int2 = dt_short_int1-1;
endmodule
```

a. What is the range of values dt_byte can take?

b. What is the value of dt_int in hex?

c. What is the value of dt_bit in decimal?

d. What is the value of dt_short_int1 in decimal?

e. What is the value of dt_short_int2 in decimal?

25. Write the System Verilog code to:
    a. Declare a 2-state array, dt_array, that holds four 12-bit values
    b. Initialize dt_array so that:
       dt_array[0] = 12'h012;
       dt_array[1] = 12'h345;
       dt_array[2] = 12'h678;
       dt_array[3] = 12'h9AB;
    c. Traverse dt_array and print out bits [5:4] of each12-bit element
       Using a for loop
       Using a foreach loop

26. Write a System Verilog code to:
    a. Declare a 2-state integer dynamic array, dt_array, and allocate the size of 10 elements.
    b. Perform the following operations:
    - Initialize the elements of the array with random values.
    - Print the size of the array and its elements.
    - Copy the dynamic array dt_array into another dynamic array dt_array_copy[]
    - Double the size of the dynamic array dt_array while keeping the content of the initial 10 locations the same as before.

27. Put 50 integer values at random locations (between 1 and 100) into an integer associative array.
    - Check whether there are values at index 2 and index 45.
    - Print the value at first index along with index