



Digital Systems Testing and Verification

The Exam Consists of **Five** Questions in **Four** Pages.

Maximum Marks: 60 Marks

1 / 4

تعليمات هامة

- حيازة التيلفون المحمول مقتوفها داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب وإذا كان ضروري الدخول بال محمول فيوضع مغلق في الحقائب.
 - لا يسمح بدخول سماعة الأذن أو البلوتوث.
 - لا يسمح بدخول أي كتب أو ملزام أو أوراق داخل اللجنة والمخالفة تعتبر حالة غش.

Question 1:

LO2, LO3 [16 Marks]

A novice designer wrote a design for a counter with the following specs:

1. Its 4-bit output Q counts from 0 to 9, in the normal cases, when *Enable* is active. The count is incremented with the rising edge of the clock signal CLK .
 2. It has an asynchronous reset signal MR (Master Reset).
 3. It can be loaded by any 4-bit value P , using the synchronous *Load* line.

You simulated the design and while investigating the generated waveforms (shown below), you realized that there is a bug.

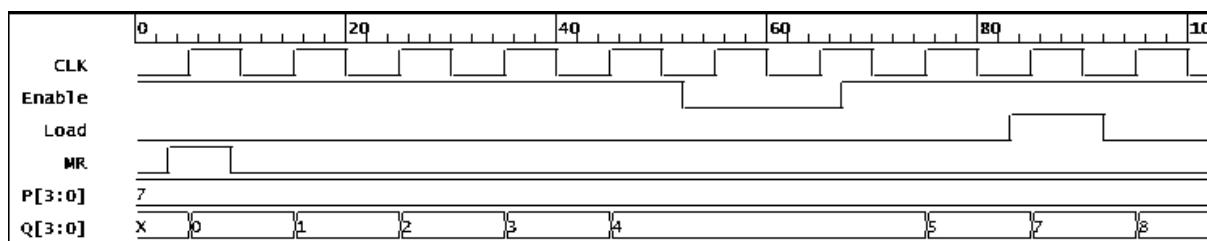
```
module decade_counter(P,Load,Enable,MR,CLK,Q);

    input P,Load,Enable,MR,CLK;
    output Q;

    bit [3:0] P,Q;
    bit Load,Enable,MR,CLK;

    always @(posedge CLK) begin
        if (MR)
            Q = 4'b0000;
        else if (Load)
            Q = P;
        else if (Enable)
            Q = (Q+1) % 10;
    end

endmodule
```



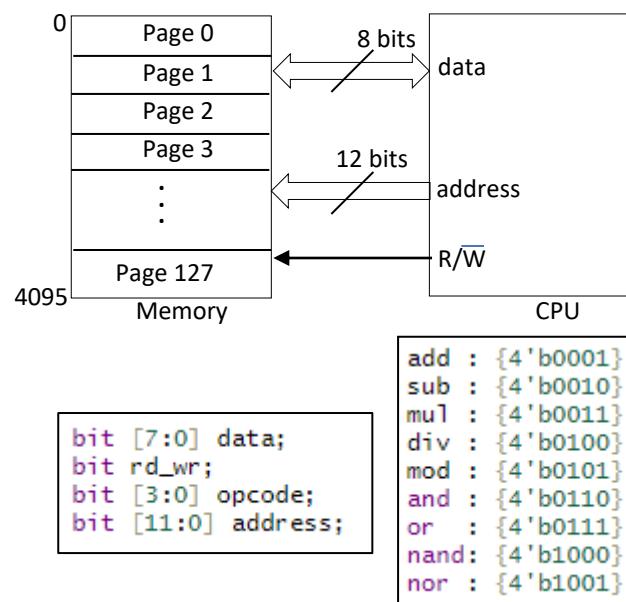
- A. Identify the bug. [3 marks]
B. Modify the code to correct the bug. [4 marks]
C. System Verilog assertions are used to reveal errors without the need for investigating waveforms. Write 3 concurrent assertions to ensure the correct implementation of the counter specifications. [9 marks]

Question 2:

LO3, LO4 [10 Marks]

Assume that you are modelling a processor. It reads data and instructions from memory, performs an operation, specified by an opcode, and writes back the result into the memory. The verification plan requires the following:

1. Both Read & Write operations should be tested.
2. You should try different values for data such that you get at least one value in the range from 1 to 64, and at least one value in the range 65 to 128, and at least one value in the range 129 to 254. The value 0 should be used at least once, and the value 255 should also be used at least once.
3. All operations should be tried. The different opcodes are shown to the right.
4. The memory space is divided into 128 pages. An address falling on each of the pages should be used at least once.



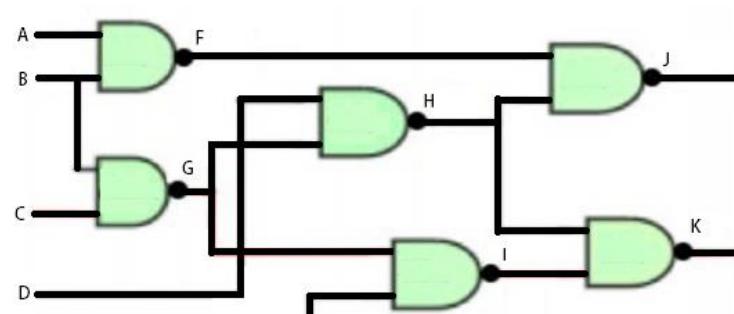
Write a coverage group to measure the coverage when using random testing. **You are NOT asked to write the processor model.** You are only asked to write the coverage group, illustrating the used cover points. Specify the appropriate bins, and the illegal bins. Use whatever options in your cover group.

Question 3:

LO1 [14 Marks]

A. Generate test patterns capable of detecting the following faults:

- G stuck at 1
- C stuck at 0
- K stuck at 1
- F stuck at 1



B. What is the difference between testing and verification.

C. State the reasonable values for the percentage of effort spent in design and in verification, commonly used in industry.

D. What is the verification technique most commonly used in the industry?

E. What is meant by Re-spin in the context of IC design?

F. What is meant by corner cases? Give an example.

G. State the names of 3 verification methodologies other than UVM

Spring 2023	Course Code: CSE 313s Digital Systems Testing and Verification	Time Allowed: 2 Hrs.
The Exam Consists of Five Questions in Four Pages.		3 / 4

Question 4:

LO4 [10 Marks]

A. Given the following assertion:

[3 marks]

- ```
assert property (@(posedge clk) Req |-> ##[1:2] Ack);
```
- What is the type of the above assertion?
  - What is the type of the implication operator?
  - Draw a wave diagram showing *clk*, *Req* and *Ack* in two succeeding scenarios, and one failing scenario.

B. What is wrong with the following assertion?

[2 marks]

```
assert (P |-> Q);
```

C. The following code has a problem.

[5 marks]

Determine the problem and write a modified code to solve this problem.

```
logic [4:0] addr;
logic [3:0] data;

covergroup c_group;
 cp0: coverpoint (addr + data);
endgroup
```

### **Question 5:**

**LO1 [10 Marks]**

Choose the right answer

1. An event is triggered by symbol
 

|         |          |        |         |
|---------|----------|--------|---------|
| a. $=>$ | b. $---$ | c. $@$ | d. None |
|---------|----------|--------|---------|
2. Which construct is used to execute a loop for a fixed number of times?
 

|           |          |            |         |
|-----------|----------|------------|---------|
| a. repeat | b. while | c. forever | d. None |
|-----------|----------|------------|---------|
3. Analyze the code below and choose the right answer

```
reg clock;
initial
begin
 clock = 1'b0;
 forever #10 clock = ~clock;
end
```

- a. The forever loop will execute the statement infinitely without advancing simulation time.
- b. Forever loop will execute the statement infinitely and rest of the design is executed in simulation time
- c. Timing control construct is optional in forever
- d. None
4. Verilog functions have
  - a. Input, output and inout port as argument
  - b. Have one input argument only
  - c. Can have more than one input arguments
  - d. Can have both input or output as argument.

5. Verilog functions have
- a. Registers
  - b. Time variables
  - c. Local variables
  - d. Wires
6. Which is true about task and function
- a. Task and function contain always and initial blocks
  - b. Task and function do not contain always and initial blocks and called from initial and always blocks or other tasks
  - c. Task and function do not contain behavioral statement
  - d. Done
7. Random number is generated by
- a. \$random
  - b. \$rand
  - c. \$strobe
  - d. None
8. If A=1'b1, B=2'b01, C=2'b00, then y = {4{A}, 2{B}, C} equals
- a. 10'b1111010100
  - b. 9'b111101010
  - c. 8'b11110100
  - d. None
9. <= is used in
- a. Blocking
  - b. Non Blocking
  - c. Both
  - d. None
10. Asynchronous reset is
- a. Clock dependent
  - b. Clock independent
  - c. Either
  - d. None

**END of Exam, Good Luck**

**Examination Committee**

*Prof. Dr. Ayman Wahba, Prof. Dr. M. Watheq El-Kharashy*

**Exam Date : 9<sup>th</sup> of June, 2023**

**Question/ILO matrix**

|                   | <b>LO1</b> | <b>LO2</b> | <b>LO3</b> | <b>LO4</b> |
|-------------------|------------|------------|------------|------------|
| <b>Question 1</b> |            | ✓          | ✓          |            |
| <b>Question 2</b> |            |            | ✓          | ✓          |
| <b>Question 3</b> | ✓          |            |            |            |
| <b>Question 4</b> |            |            |            | ✓          |
| <b>Question 5</b> | ✓          |            |            |            |