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**Spring 2024**

# CSE 313s
# Selected Topics in Computer Engineering
# Sheet 6

1. If a clocking block definition has timing specified as follows - what does it mean?

```
default input #2ns output #3ns
```

   a. All input signals in the clocking block are sampled 2ns before clocking event and all output signals are driven 3ns before clocking event
   b. All input signals in the clocking block are sampled 2ns after clocking event and all output signals are driven 3ns before clocking event
   c. All input signals in the clocking block are sampled 2ns after clocking event and all output signals are driven 3ns after clocking event
   d. All input signals in the clocking block are sampled 2ns before clocking event and all output signals are driven 3ns after clocking event

2. A single System Verilog “interface” can have multiple modports and multiple clocking blocks inside
   a. True
   b. False

3. Modport is used to
   a. declare input and output skew
   b. declare direction of signals
   c. synchronize signals
   d. make interface complex

4. What is the use of modports?

5. What is the need of clocking blocks?

6. What are interfaces in SystemVerilog?

7. What is a modport construct in an interface?

8. Are interfaces synthesizable?

9. What is the difference between the following two ways of specifying skews in a clocking block?

```
input #1 step req1;
input #1ns req1;
```

10. Write code for the below requirement
    DUT has data bus of 64 bit which is driven on positive edge of clock.
    TESTBENCH has data bus of 32 bit which can sample on both positive edge and negative edge.
    On positive edge, drive [0 to 31] bits of DUT to TESTBENCH bus and on negative edge drive [32 to 63] bits of DUT to TESTBENCH bus. All the above logic should be done inside the interface itself.

11. If clocking block is not used, then what happens?