King Saud University College of Computer and Information Sciences Computer Engineering Department



Semester II, 1443 H
CEN 415, Introduction to VLSI Design
Class Project
Due Date: Check LMS

Class Project (1 to 4 students)

Problem:

Design and Implement a circuit that has two 8-bit inputs and one 16-bit output to perform the following tasks based on the user choice determined by C_0 and C_1 .

Case 00:

the circuit generate the complement of the first input and show the result in the 8 least significant bits of the output

Case 01:

the circuit perform a modulo 256 count down with the ability to hold the result if (H) is asserted. The result is shown in the 8 most significant bits of the output.

Case 10:

the circuit multiply both inputs using shift and add method.

Case 11

the circuit generates the even parity of the second input and show the result in the most significant bit of the output.

Assume all nMOS and pMOS has (W= 4λ , L= 2λ) unless it is nessesary to change sizing. The inputs and outputs of your design are as follows:

Inputs:

An unsigned 8-bit first input $A(a_7: a_0)$

An unsigned 8-bit second input B (b_7 : b_0)

User choice bits C_0 and C_1 .

Clocking signals Phi1, Phi1 b, Phi2, Phi2 b.

Counter holder H.

A common VDD and common GND lines

Any other necessary inputs

Outputs:

An unsigned 16-bit output Q (q_{15} : q_0)

Any other necessary outputs

Requirement:

Phase 1:

- Part 1: Verify the design using a logic design tool <u>and</u> an HDL tool (VHDL or Verilog) using structural method
- Part 2: List in a table the required components with their respective input and output labels.

Phase 2:

- Part 3: Implement your design using Magic VLSI layout tool to generate your project layout http://opencircuitdesign.com/magic/
- Part 4: Test your design using *irsim* to simulate your project. http://opencircuitdesign.com/irsim/

Deliverables:

- **1- One PDF** that contains the following sections:
 - Introduction
 - Problem statement and specifications

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- Motivation
- Solution design using a logic design tool that you studied in the previous logic design courses and HDL tool
- Stick diagram for each component of your design. The building blocks components are enough.
- Testing strategy and results: they should show instructions to simulate and verify your design, by including Linux terminal commands for Magic and Irsim used to run your project with few different inputs.

2- A compressed folder containing:

• Source code and layout.