TP 2 Ordonnancement Temps Réel

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Systèmes et Ordonnancement Temps Réel

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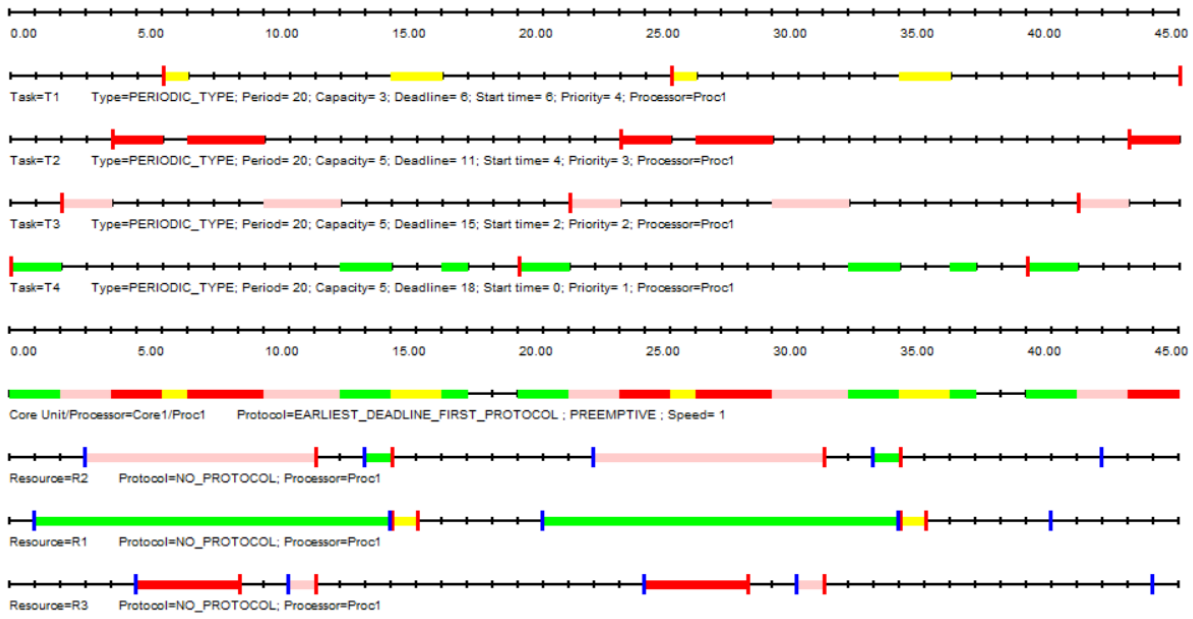
Exercise 1

1.1



Scheduling simulation, Processor Proc1 :

- Number of context switches : 18
- Number of preemptions : 10

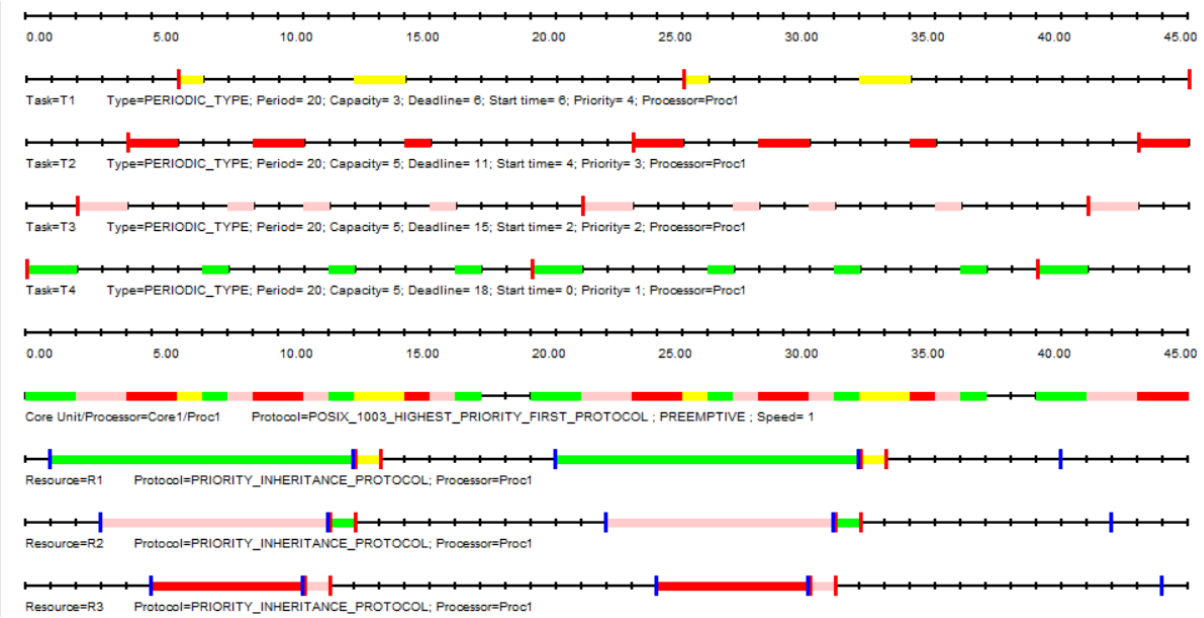
Task response time computed from simulation :

- T1 $\Rightarrow$ 11/worst, missed its deadline (absolute deadline = 12 ; completion time = 17), missed its deadline (absolute deadline = 32 ; completion time = 37)
- T2 $\Rightarrow$ 6/worst
- T3 $\Rightarrow$ 11/worst
- T4$\Rightarrow$ 18/worst

Some task deadlines will be missed : the task set is not schedulable.

Based on the simulation results, the task set is not schedulable on the given system. This is primarily due to missed deadlines for task T1.

1.2



Scheduling simulation, Processor Proc1 :

- Number of context switches : 26
- Number of preemptions : 18

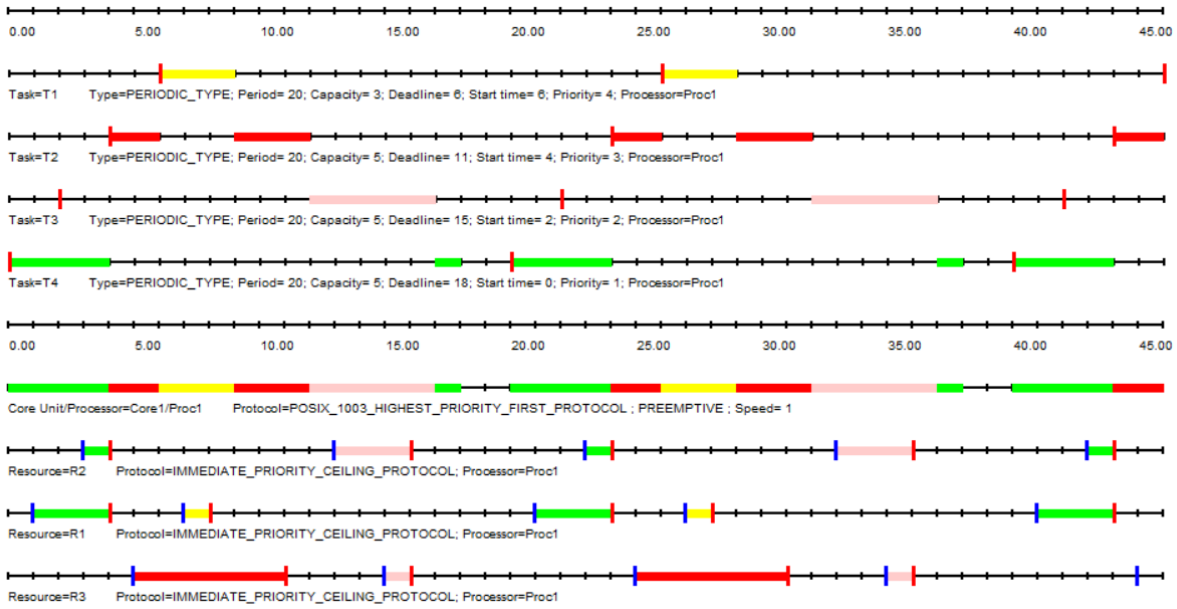
Task response time computed from simulation :

- T1 ⇒ 9/worst, mmissed its deadline (absolute deadline = 12 ; completion time = 15), missed its deadline (absolute deadline = 32 ; completion time = 35)
- T2 ⇒ 12/worst, missed its deadline (absolute deadline = 15 ; completion time = 16), missed its deadline (absolute deadline = 35 ; completion time = 36)
- T3 ⇒ 11/worst
- T4⇒ 18/worst

Some task deadlines will be missed : the task set is not schedulable.

Based on the simulation results, the task set is not schedulable on the given system. This is primarily due to missed deadlines for taskS T1 and T2.

1.3



Scheduling simulation, Processor Proc1 :

- Number of context switches : 11
- Number of preemptions : 4

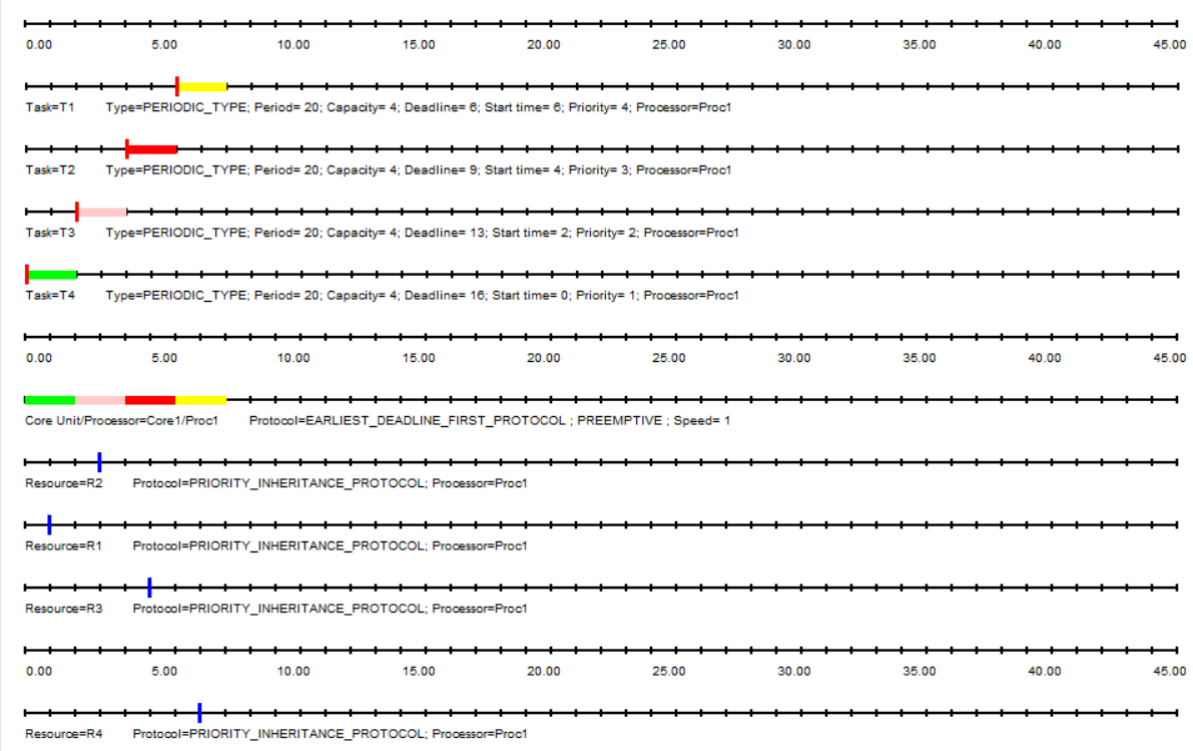
Task response time computed from simulation :

- T1 ⇒ 3/worst
- T2 ⇒ 8/worst,
- T3 ⇒ 15/worst
- T4⇒ 18/worst

Some task deadlines will be missed : the task set is not schedulable.

The schedulability of the tasks can be confirmed by the results.

Exercise 2



Scheduling simulation, Processor Proc1 :

- Number of context switches : 3
- Number of preemptions : 0

Task response time computed from simulation :

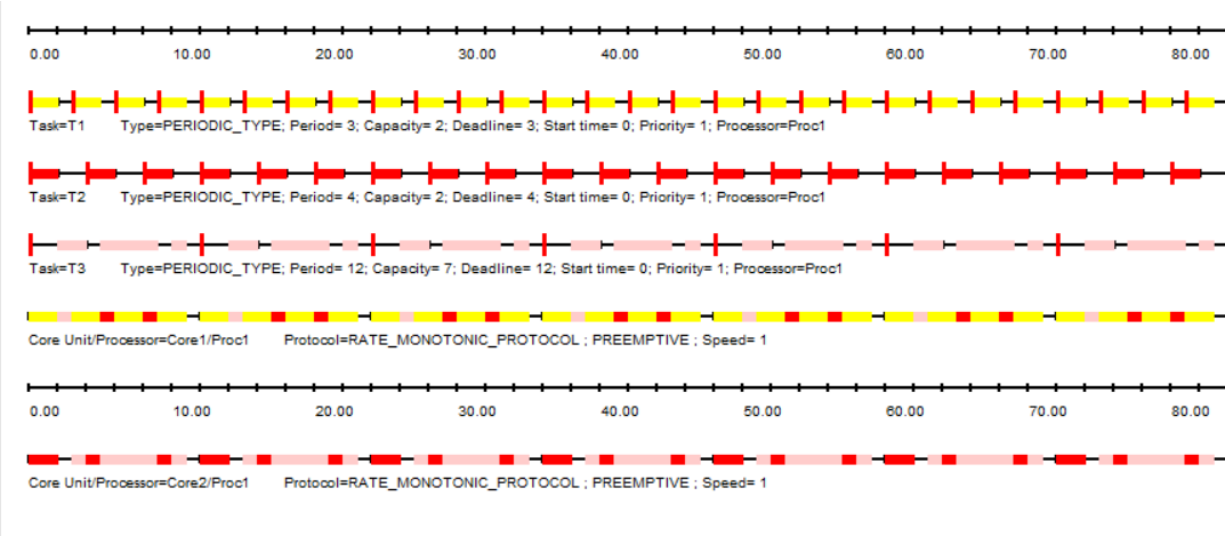
- T1⇒ 0/worst , response time not computed since the task did not run all its capacity
- T2⇒ 0/worst , response time not computed since the task did not run all its capacity
- T3⇒ 0/worst , response time not computed since the task did not run all its capacity
- T4⇒ 0/worst , response time not computed since the task did not run all its capacity

- One or several tasks did not complete their execution.

One or more tasks did not complete their execution. This indicates a scheduling or resource allocation issue that prevented these tasks from running to completion, so it's not schedulable

Exercise 3

3.1



Scheduling simulation, Processor Proc1 :

— Number of context switches : 1439
— Number of preemptions : 720

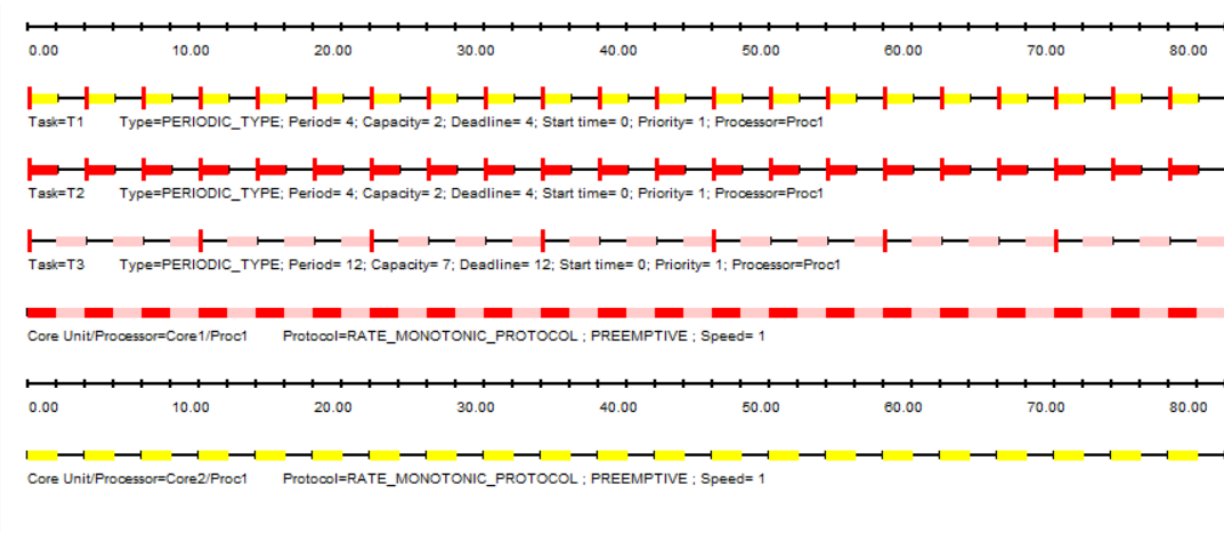
Task response time computed from simulation :

— T1⇒ 2/worst
— T2⇒ 2/worst
— T3⇒ 11/worst

- No deadline missed in the computed scheduling : the task set is schedulable if you computed the scheduling on the feasibility interval.

The schedulability of the tasks can be confirmed by the results.

3.2



Scheduling simulation, Processor Proc1 :

- Number of context switches : 1079
- Number of preemptions : 401

Task response time computed from simulation :

- T1 ⇒ 2/worst
- T2 ⇒ 2/worst
- T3 ⇒ 11/worst , missed its deadline (absolute deadline = 12 ; completion time = 15), missed its deadline (absolute deadline = 24 ; completion time = 28)

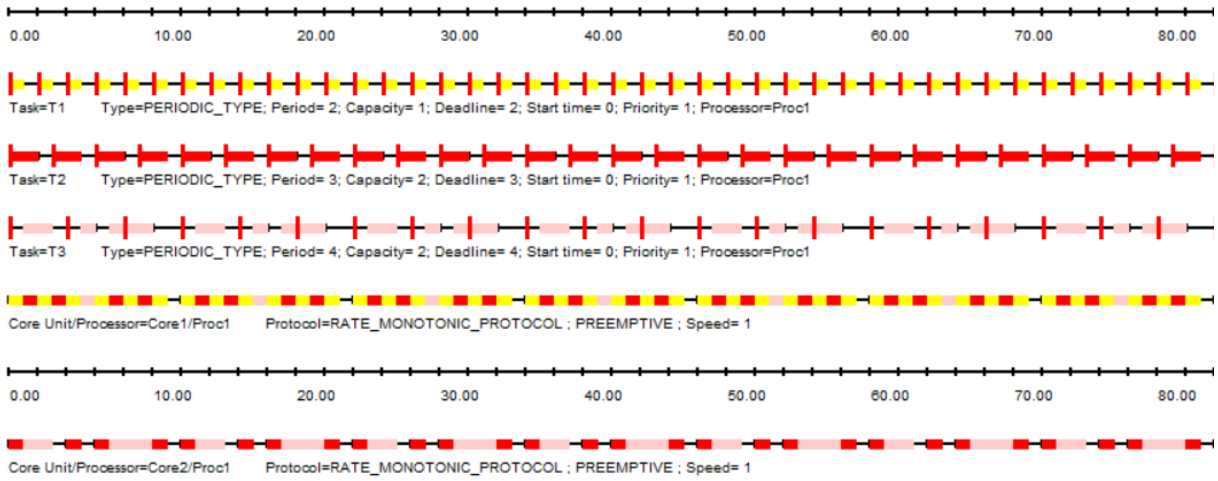
Some task deadlines will be missed : the task set is not schedulable.

Based on the simulation results, the task set is not schedulable on the given system. This is primarily due to missed deadlines for task T1.

3.3

When two tasks have identical periods and are synchronized on a dual-core processor, both tasks will be executed concurrently by the two cores. However, the performance of the third task, T3, was less satisfactory. Compared to the second simulation, the first simulation demonstrated superior performance for task T3.

Exercise 4



Scheduling simulation, Processor Proc1 :

- Number of context switches : 323
- Number of preemptions : 54

Task response time computed from simulation :

- T1⇒ 1/worst
- T2⇒ 2/worst
- T3⇒ 4/worst

- No deadline missed in the computed scheduling : the task set is schedulable if you computed the scheduling on the feasibility interval.

The schedulability of the tasks can be confirmed by the results. And fot T_3 the worst case happens during its first job, because based in the simulation the response time of T_3 is 4 units and its finishes just at its deadline.
In conclusion the first job of T_3 experiences its worst-case scenario due to the high priority of tasks T_1 and T_2, despite there is no deadline missed, meaning the task set is schedulable under RM on dual-core processor.

Exercise 5

First thing first, let's calculate the utilization of each task by $U_i = \frac{C_i}{P_i}$

Task	U
T1	U1 = 2÷6 = 0.333
T2	U2 = 4÷8 = 0.5
T3	U3 = 3÷10 = 0.3
T4	U4 = 12÷20 = 0.5
T5	U5 = 1÷50 = 0.02
T6	U6 = 20÷50 = 0.4
T7	U7 = 5÷100 = 0.05
T8	U8 = 1÷100 = 0.01

2And then we need to assign each task to 3 processor based on the sum if utilization which should be lower than 1. For exemple we can give to :
P_1, T_1 and T_2 $(0.6 + 0.3 = 0.833)$
P_2, T_3, T_4 and T_5 $(0.3 + 0.6 + 0.02 = 0.92)$
P_3, T_1, T_5 and T_7 $(0.4 + 0.05 + 0.01 = 0.46)$

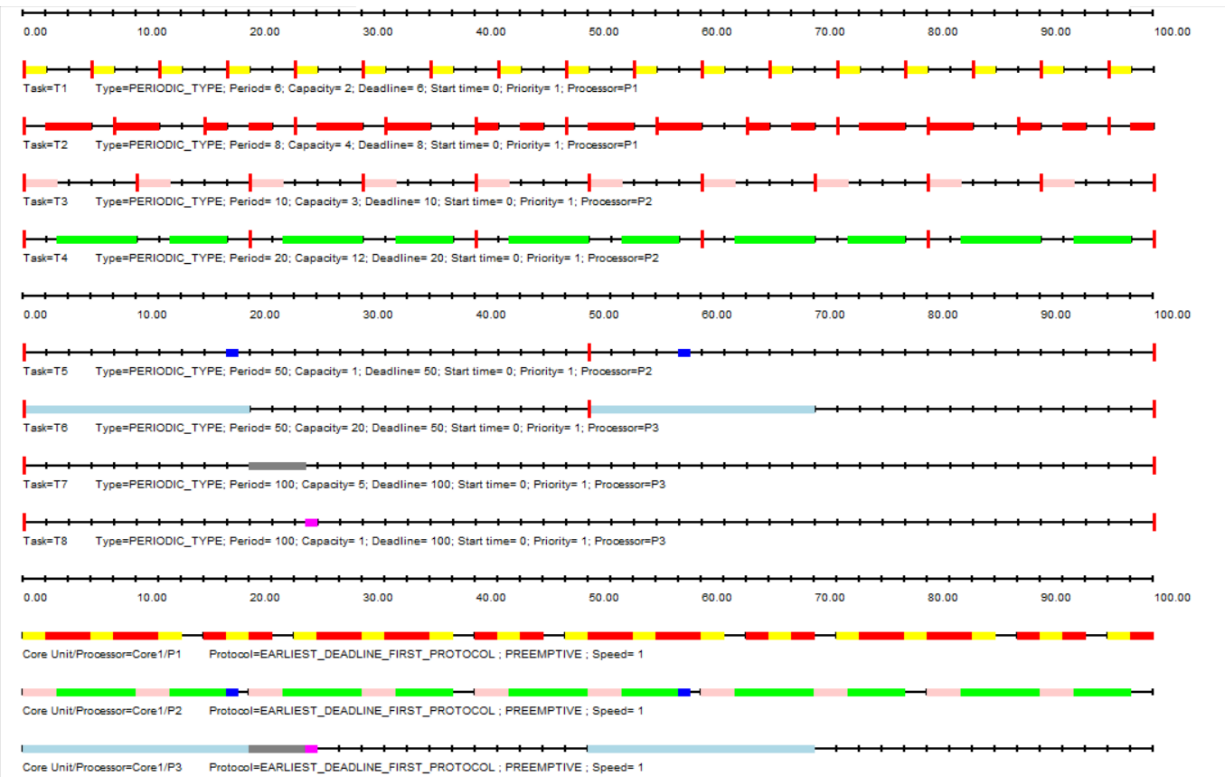
Processors	**P1**	**P2**	**P3**
Tasks	T1	T3	T6
	T2	T4	T7
		T5	T8
Utilization	**U_{P1}= 0.8**	**U_{P2} = 0.92**	**U_{P3} = 0.46**

First-Fit Rate Monotonic

UP	$n(2^{1/n}-1)$	UTi Total	Condition Uti $<n(2^{1/n}-1)$
UP1	0.82	0.833	✗
UP2	0.77	0.92	✗
UP3	0.77	0.46	✓

As we can see in the table, P1 and P2 do not meet the condition of $U_P \leq U_T i$, so we can say that the system is not schedulable using RM on three processors, so we should add at least one processor.

First-Fit Earliest Deadline First



Scheduling simulation, Processor P1 :

— Number of context switches : 33
— Number of preemptions : 4

Task response time computed from simulation :

— T1 ⇒ 2/worst
— T2 ⇒ 6/worst

No deadline missed in the computed scheduling : the task set is schedulable if you computed the scheduling on the feasibility interval.

Scheduling simulation, Processor P2 :

— Number of context switches : 21
— Number of preemptions : 5

Task response time computed from simulation :

— T3 ⇒ 3/worst
— T4 ⇒ 18/worst
— T5 ⇒ 19/worst

No deadline missed in the computed scheduling : the task set is schedulable if you computed the scheduling on the feasibility interval.

Scheduling simulation, Processor P3 :

— Number of context switches : 3
— Number of preemptions : 0

Task response time computed from simulation :

— T6 ⇒ 20/worst
— T7 ⇒ 25/worst
— T8 ⇒ 26/worst

No deadline missed in the computed scheduling : the task set is schedulable if you computed the scheduling on the feasibility interval.

The schedulability of the tasks on the 3 processors can be confirmed by the results.