Design of 4-bit Ring Counter

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***Abstract*—A ring counter is a digital sequential circuit that recirculates the same data throughout the circuit. It is one of the applications of shift register. In this paper, a 4-bit ring counter is designed and simulated using Xilinx ISE Tool.**

Keywords—counter, shift register

I. INTRODUCTION

In this digital world, counters are the most important sequential logic circuits which are used widely in many day-to-day life applications such as microwave ovens, washing machines, digital clocks, timers and in many electronic devices such as frequency dividers, analog to digital converters, triangular waveform generators, etc. Any digital circuit which is used to count the number of occurrences of the input is called counter. The purpose of counters is not only for counting but also for measuring frequency and time.

Basically, counters are of 2 types: synchronous and asynchronous counters. If the change in transition occurs based on the clock input of the counter, then it is called synchronous counter. If not, then, it is called asynchronous counter. There are many other types of counters, such as decade counter, mod counter, binary counter, ring counter, etc. This paper mainly focuses on the ring counter only.

II. DESIGN OF 4-BIT RING COUNTER

A. Circuit Diagram

A ring counter is a synchronous counter which transfers the same data throughout it. It is a typical application of shift register and can be designed using either D or JK flip-flops (FFs). In this paper, a 4-bit ring counter is designed by a series of 4 D-FFs connected together in feedback manner [1]. That means the output of the last FF is connected to the input of the first FF. The clock signal is applied to all the FFs simultaneously as shown in Fig.1.

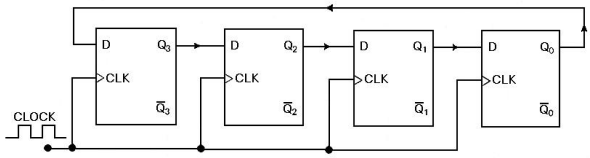

Fig. 1. Circuit Diagram of 4-bit ring counter

B. Operation

Initially all the FFs are at RESET state. When the PRESET is applied, the input of the ring counter becomes 1. Now the output of the first FF (Q_3) is 1 and other FF outputs (Q_2, Q_1 and Q0) will be low. Then for the next clock signal, Q_2 becomes 1 and others outputs will be low. In this way, as the clock input changes, the outputs change and the data sequence rotates in the ring counter. Table I shows the truth table of the ring counter.

TABLE I. TRUTH TABLE OF 4-BIT RING COUNTER

Clock	Q_3	Q_2	Q_1	Q_0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0

C. State Diagram

State diagram is used to describe the behaviour of the digital sequential circuits. It shows the transitions of states from one state to the next as well as the output for a given input [2]. Fig.2 shows the state diagram of ring counter.

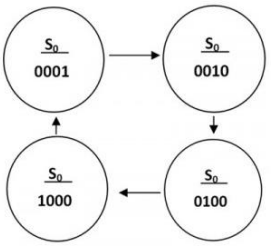

Fig. 2. State Diagram of 4-bit ring counter

The number of states decides the number of FFs to be used to design any counter [3]. For a n-bit ring counter,

Number of states = Number of FFs used = n

III. SIMULATION RESULTS

The 4-bit ring counter is designed using Verilog code and simulated using Xilinx ISE tool [4]. Fig. shows the simulation results.

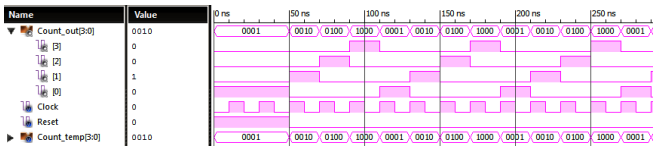

Fig. 3. Simulation Results of 4-bit ring counter

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