PARALLEL COMPUTING ARCHITECTURE – ASSIGNMENT 1

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INTEL SKYLAKE

Intel SkyLake is a 6th Gen Core processor microarchitecture launched in August of 2015. SkyLake's OutOfOrder window is 224 uops, which allows greater scope for parallelism. It is designed to allow a dispatch of 6 uops at once, which leads to queues being quicker and also the number of maximum dispatches from queues to execution units is 6, which can be taken advantage of by efficient reordering of the micro-ops. SkyLake uses a 4-way associative L2 cache as opposed to the earlier 8-way models. This move might increase the cache miss-rate, which is countered by increasing the bandwidth of L2 cache and improved cache-miss handling. The lower associativity results in lesser power consumption. The eDRAM placement in SkyLake: It becomes a DRAM buffer and since it is visible to all softwares that requires DRAM access, it need not be flushed to maintain coherency. For some tasks it can bypass the L3 cache level when required in a standard DRAM access scenario. Intel has introduced SGX (Security Guard Extensions) and MPX (Memory Protection Extensions) to SkyLake to reduce buffer flow errors which is a common source of security breaches which allows programs to run in a private environment unaccessible to any other program. SkyLake has an improved branch predictor, faster divider, improved load and store bandwidth, more execution units, better page-miss handling and deeper buffers. SkyLake allows micro-op retirement: each thread in a core can retire 4 uops in 1 cycle. SkyLake (6700) consists of 4 cores with 8 threads per core. It has a 8 MB cache with the clock speed ranging from 2.8GHz to 4GHz. It has a 14nm manufacturing process and supports both DDR3L SDRAM and DDR4 SDRAM. On different variants L4 eDRAM cache can be of a size from 64MB to 128MB. Modern processors change their operating frequency depending on the voltage which is usually managed by the operating system. With SkyLake's Speed Shift technology the processor regulates its own frequency which results in faster frequency changes. Also, it allows the processor a finer control over its states, leading to lesser power consumption from that processor.

IBM Power8

Power8 (POWER – Performance Optimization With Enhanced RISC) is a family of superscalar symmetric multiprocessors based on the Power Architecture (Reduced Instruction Set Computing Architecture). The Power8 processor features a 16 execution pipeline, 64K data cache per-core and 32K instruction cache. It has 512KB SRAM L2 cache per core, 96MB eDRAM shared L3 cache and 128MB eDRAM L4 cache that is situated off-die. It also uses Coherent Accelerator Processor Interface (CAPI) for coherent memory addressing in CPUs and external co-processors. Power8 is the first implementation of Power ISA v2.07. Power8 is a highly multithreaded chip: each of its 12 core can handle eight hardware threads simultaneously, for a total of 96 threads executing simultaneously. This allows for massive parallelism. Some of the other features that enhance

parallelism: there are 8 decoders, 8 dispatches per cycle, 4 load units, data cache can process four 128-bit transactions per cycle, and the bus width between L2 and data cache is 512 bits. Power8 is capable of clock speeds around 4.5GHz. An on-chip power management micro-controller (OCC – On-Chip Controller) is used for regulating operating frequency, voltage, memory bandwidth, and thermal control of both the chip and the memory. The OCC can be programmed to overclock the processor. The memory controllers on the Power8 chips are specified to use either DDR3 or DDR4 memory but are designed to be future-proof by being generic memory controllers paired to an external component called Centaur that acts as a memory buffer, L4 cache chip and the actual memory controllers. Centaur contains 16MB of eDRAM which can be used as L4 cache by the processor and each chip can be linked up to eight Centaur chips allowing for up to 1TB of memory per socket. Each Power8 core can issue 10 instructions to 16 execution units, 2 fixed-point units, 2 load-store units, 2 instruction fetch units, 4 floating point units, 2 VMX units, 1 cryptographic unit, 1 decimal floating unit, 1 conditional register unit and 1 branch register unit. The 12-core chip is designed on a 22nm die. This poweful processor is mainly used in big data and cloud computing applications.

Source:

1. Wikipedia
2. http://wccftech.com/ibm-power8-processor-architecture-detailed/
3. http://www.anandtech.com/show/9582/intel-skylake-mobile-desktop-launch-architecture-analysis/5