Wed Apr 27 22:33:19 2016

```
1
                                                      timescale 1ns / 1ps
          2
                                               3
                                               // Company:
                                              // Engineer:
          4
          5
                                              //
          6
                                              // Create Date:
                                                                                                                                                                                                                              11:31:44 04/17/2016
          7
                                               // Design Name:
                                              // Module Name:
          8
                                                                                                                                                                                                                            hex7seq
          9
                                              // Project Name:
10
                                              // Target Devices:
11
                                               // Tool versions:
12
                                              // Description:
13
                                              //
                                               // Dependencies:
14
15
                                               // Revision:
16
17
                                               // Revision 0.01 - File Created
18
                                               // Additional Comments:
19
20
                                              21
                                              module hex7seq(
22
                                                                                    input [3:0] n,
                                                                                    output a,
23
24
                                                                                   output b,
25
                                                                                   output c,
26
                                                                                   output d,
27
                                                                                   output e,
28
                                                                                   output f,
29
                                                                                   output q
30
                                                                                   );
31
32
                                                                           assign a = (\n[3] \& \n[2] \& \n[1] \& \n[0]) \ | \ (\n[3] \& \n[2] \& \n[1] \& \n[0]) \ | \ (\n[3] \& \n[2] \& \n[1] \& \n[0]) \ | \ (\n[3] \& \n[2] 
                                               0]) | (n[3] & n[2] & n[1] & n[0]);
33
                                                                          assign b = (\n [3] & n[2] & \n [1] & n[0]) + (\n [3] & n[2] & n[1] & \n [0]) + (\n [3] & \n [2] & n[1] & \n [2] & \n [
                                               0]) | (n[3] & n[2] & \sim n[1] & \sim n[0]) | (n[3] & n[2] & n[1] & \sim n[0]) | (n[3] & n[2] & n[1] & n[0]);
34
                                                                           assign c = (\sim n[3] \& \sim n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& \sim n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& n[1] \& \sim n[0]) | (n[3] \& n[2] \& 
                                                 [0]) | (n[3] & n[2] & n[1] & n[0]);
35
                                                                           assign d = (\n[3] \& \n[2] \& \n[1] \& \n[0]) | (\n[3] \& \n[2] \& \n[1] \& \n[0]) | (\n[3] \& \n[2] \& \n[1] \& \n[2] \& \n[2
                                               n[0]) + (n[3] \& \neg n[2] \& \neg n[1] \& n[0]) + (n[3] \& \neg n[2] \& n[1] \& \neg n[0]) + (n[3] \& n[2] \& n[1] \& n[0]);
36
                                                                           assign e = (\n[3] \& \n[2] \& \n[1] \& \n[0]) | (\n[3] \& \n[2] \& \n[1] \& \n[0]) | (\n[3] \& \n[2] \& \n[1] \& \n[0])
                                               ] \& n[0]  | (n[3] \& n[2] \& n[1] \& n[0]) | (n[3] \& n[2] \& n[1] \& n[0]) | (n[3] \& n[2] \& n[1] \& n[0])
                                               1);
37
                                                                           assign f = (\sim n[3] \& \sim n[2] \& \sim n[1] \& n[0]) | (\sim n[3] \& \sim n[2] \& n[1] \& \sim n[0]) | (\sim n[3] \& \sim n[2] \& n[1] | (\sim n[3] \& \sim n[2] \& n[1] | (\sim n[3] \& \sim n[2] \& \sim n[2] | (\sim n[3] | (\sim n[3
                                               ] &n[0]) | (~n[3]&n[2]&n[1]&n[0]) | (n[3]&n[2]&~n[1]&n[0]);
38
                                                                            assign g = (\n [3] \& \n [2] \& \n [1] \& \n [0]) | (\n [3] \& \n [2] \& \n [1] \& \n [0]) | (\n [3] \& \n [2] \& \n [1] \& \n [0]) | (\n [3] \& \n [2] \& \n [1] \& \n [2] \& \
                                               ] \&n[0]) | (n[3] \&n[2] \& \sim n[1] \& \sim n[0]);
39
40
                                               endmodule
41
```