```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Company:
4   // Engineer:
5   //
6   // Create Date:    12:55:58 05/07/2016
7   // Design Name:
8   // Module Name:    FSM
9   // Project Name:
10  // Target Devices:
11  // Tool versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  module FSM(
22      input pb2,
23      input pb0,
24      input [7:0] Q,
25      output counterRL,
26      output counterLR,
27      output [7:0] D,
28      output resetTimer
29      );
30
31     assign D[0] = (Q[0]+Q[1]+Q[2]+Q[4]+Q[5])&(~pb0&~pb2);//
32     assign D[1] = (Q[0]+Q[1]+Q[2]+Q[7])&(~pb0&pb2);//
33     assign D[2] = (Q[1]+Q[2]+Q[3])&(pb0&pb2);//
34     assign D[3] = (Q[2]+Q[3])&(pb0&~pb2);//
35     assign D[4] = (Q[0]+Q[4]+Q[5]+Q[7])&(pb0&~pb2);//
36     assign D[5] = (Q[4]+Q[5]+Q[6])&(pb0&pb2);
37     assign D[6] = (Q[5]+Q[6])&(~pb0&pb2);//
38     assign D[7] = (Q[6]+Q[3]+Q[7])&(~pb0&~pb2);// done
39
40     assign counterRL = Q[6]&(~pb0&~pb2);
41     assign counterLR = Q[3]&(~pb0&~pb2);
42
43     assign resetTimer = ~pb0&~pb2 | (Q[0]+Q[2]+Q[7])&(~pb0&pb2) | (Q[1]+Q[3])&(pb0&pb2)
    | Q[2]&pb0&~pb2 | (Q[0]+Q[5]+Q[7])&(pb0&~pb2) | (Q[4]+Q[6])&(pb0&pb2) | Q[5]&~pb0&pb2;
44  endmodule
45
```