```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Company:
4   // Engineer:
5   //
6   // Create Date:    16:10:25 05/14/2016
7   // Design Name:
8   // Module Name:    Sync
9   // Project Name:
10  // Target DeV[9:0]ices:
11  // Tool V[9:0]ersions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // ReV[9:0]ision:
17  // ReV[9:0]ision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  module Sync(
22      input [9:0] H,
23      input [9:0] V,
24      output HS,
25      output VS,
26      output R2,
27      output R1,
28      output R0,
29      output G2,
30      output G1,
31      output G0,
32      output B1,
33      output B0
34      );
35
36      wire ActiveRegion = ((H <= 639) & (V <= 479));
37      wire RightEdge = ((H >= 632) & (H <= 639));
38      wire LeftEdge = ((H >= 0) & (H <= 7));
39      wire TopEdge = ((V >= 0) & (V <= 7));
40      wire BottomEdge = ((V >= 472) & (V <= 479));
41
42      assign HS = ~((H < 655) | (H > 751)); // 655 751
43      assign VS = ~((V < 490) | (V > 491)); //good
44
45      assign G2 = ActiveRegion & (RightEdge | LeftEdge | TopEdge | BottomEdge);
46      assign G1 = ActiveRegion & (RightEdge | LeftEdge | TopEdge | BottomEdge);
47      assign G0 = ActiveRegion & (RightEdge | LeftEdge | TopEdge | BottomEdge);
48      assign R2 = ActiveRegion & (RightEdge | LeftEdge | TopEdge | BottomEdge);
49      assign R1 = ActiveRegion & (RightEdge | LeftEdge | TopEdge | BottomEdge);
50      assign R0 = ActiveRegion & (RightEdge | LeftEdge | TopEdge | BottomEdge);
51
52
53  endmodule
54
```