

```
1  `timescale 1ns / 1ps
2  ///////////////////////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date:    19:55:37 04/30/2016
7  // Design Name:
8  // Module Name:    hex7seg
9  // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module hex7seg(
22     input [3:0] n,
23     output [6:0] y
24 );
25
26     assign y[0] = (~n[3]&n[2]&n[1]&n[0]) | (~n[3]&n[2]&n[1]&~n[0]) | (n[3]&~n[2]&n[1]
&n[0]) | (n[3]&n[2]&~n[1]&n[0]);
27     assign y[1] = (~n[3]&n[2]&n[1]&n[0]) | (~n[3]&n[2]&n[1]&~n[0]) | (n[3]&~n[2]&n[1]
&n[0]) | (n[3]&n[2]&~n[1]&~n[0]) | (n[3]&n[2]&n[1]&~n[0]) | (n[3]&n[2]&n[1]&n[0]);
28     assign y[2] = (~n[3]&~n[2]&n[1]&~n[0]) | (n[3]&n[2]&~n[1]&~n[0]) | (n[3]&n[2]&n[1]
&~n[0]) | (n[3]&n[2]&n[1]&n[0]);
29     assign y[3] = (~n[3]&~n[2]&n[1]&n[0]) | (~n[3]&n[2]&~n[1]&~n[0]) | (~n[3]&n[2]&n[1]
&n[0]) | (n[3]&~n[2]&~n[1]&n[0]) | (n[3]&~n[2]&n[1]&~n[0]) | (n[3]&n[2]&n[1]&n[0]);
30     assign y[4] = (~n[3]&~n[2]&n[1]&n[0]) | (~n[3]&~n[2]&n[1]&n[0]) | (~n[3]&n[2]&~n[1]
&~n[0]) | (~n[3]&n[2]&~n[1]&n[0]) | (~n[3]&n[2]&n[1]&n[0]) | (n[3]&~n[2]&~n[1]&n[0]
&~n[0]);
31     assign y[5] = (~n[3]&~n[2]&n[1]&n[0]) | (~n[3]&~n[2]&n[1]&~n[0]) | (~n[3]&~n[2]&n[1]
&n[0]) | (~n[3]&n[2]&n[1]&n[0]) | (n[3]&n[2]&~n[1]&n[0]);
32     assign y[6] = (~n[3]&~n[2]&n[1]&~n[0]) | (~n[3]&~n[2]&~n[1]&n[0]) | (~n[3]&n[2]&n[1]
&n[0]) | (n[3]&n[2]&~n[1]&~n[0]);
33
34 endmodule
35
```