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Lab Write-Up

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Description

The purpose of this lab was to learn how to use the ISE simulator along with the Bysas2 board's 7-Segment display. The objective of this lab was to create a 3-bit adder with switches as inputs, and display the result in the 7-Segment display. To do this I learned how to use a hierarchy in my schematic by creating symbols for lower-level schematics. Once the adder was complete, the next task was to map the output to the display.

Methods

Adder

The first part of the lab was to create a 3-bit adder. I first created a truth table with inputs Cin, a, and b. There were two outputs: the sum and the carry out. Once I created the truth table, I then created two equations, one for the sum and one for the carry out. The truth table can be seen in Table 1:

C _{in}	B	A		S	C _{out}
0	0	0		0	0
0	0	1		1	0
0	1	0		1	0
0	1	1		0	1
1	0	0		1	0
1	0	1		0	1
1	1	0		0	1
1	1	1		1	1

Table 1: A truth table for a 3-bit adder (Carry in, B, and A)

The minimized equations were:

$$\text{Sum } (S) = A \oplus B \oplus C$$

$$C_{\text{out}} (C) = (A \oplus B)C + AB$$

From here I created the schematic diagram that can be see here in figure 1:

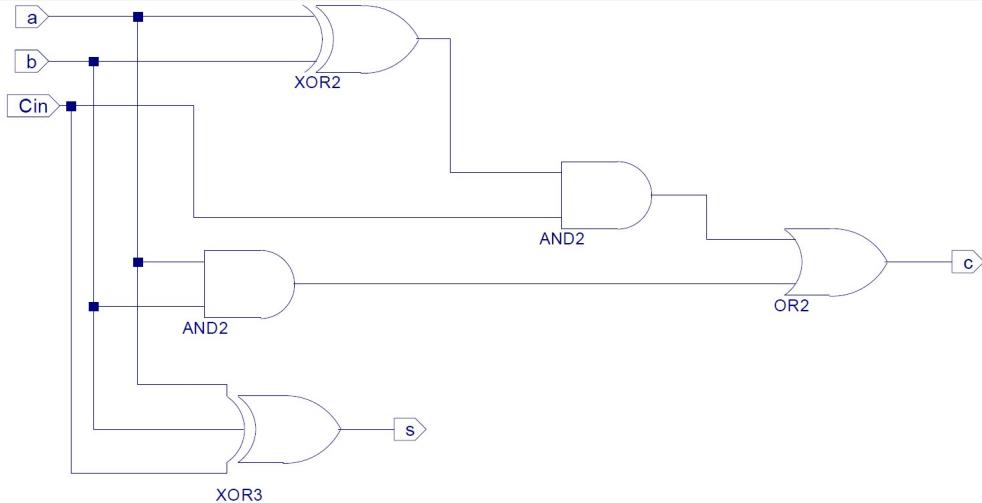


Figure 1: A single-bit adder implementation based on the equations above.

Full Adder

Once this adder was created, I created a symbol for a full adder, and implemented three symbols to create the full 3-bit adder. Since each adder adds one bit, I needed 3 Adders. Implementing this full adder resulted in a hierarchy where my full adder was above my schematic in Figure 1.

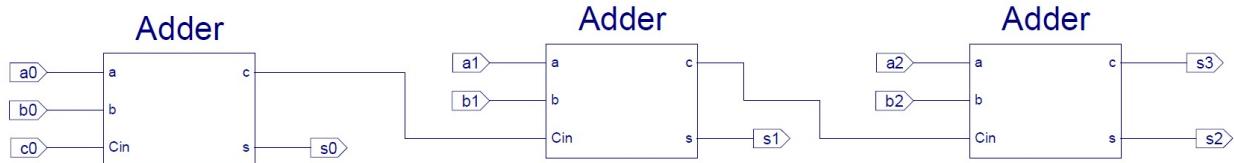


Figure 2: Full Adder (3-bits) implemented with symbols of Figure 1.

*A*0 and *b*0 corresponds to the first bit, *a*1 and *b*1 correspond to the second bit, and *a*2 and *b*2 correspond to the third bits being added. A final sum comes from each Adder. The last Adder (right most adder) contains a second sum for the final carry out bit.

7-Segment Display

My next step was to make the adder's output go to the 7-Segment display. To do this I first created a truth table with every LED on the 7-Segment display to tell whether it will be lit (1) or not (0). I had an equation for each LED: CA, CB, CC, CD, CE, CF, CG, AN0, AN1, AN2, AN3. I came up with twelve logic equations in total. I checked the Reference Manual to determine the name of the LEDs (CA-CG) as well as the names of each digit (AN0-AN3). It took me a while to

realize how 0 means on and 1 means off. Since I did not want to redo my truth table I simply put a bar on top all of my equations. Once I minimized all my equations I began creating a schematic for all the LEDs (CA – CG).

N 3	N 2	N 1	N 0	C A	C B	C C	C D	C E	C F	C G	DP	AN 0	AN 1	AN 2	AN 3
0	0	0	0	1	1	1	1	1	1	0	0	1	0	0	0
0	0	0	1	0	1	1	0	0	0	0	0	1	0	0	0
0	0	1	0	1	1	0	1	1	0	1	0	1	0	0	0
0	0	1	1	1	1	1	1	0	0	1	0	1	0	0	0
0	1	0	0	0	1	1	0	0	1	1	0	1	0	0	0
0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	0
0	1	1	0	1	0	1	1	1	1	1	0	1	0	0	0
0	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0
1	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0
1	0	0	1	1	1	1	0	0	1	1	0	1	0	0	0
1	0	1	0	1	1	1	0	1	1	1	0	1	0	0	0
1	0	1	1	0	0	1	1	1	1	1	0	1	0	0	0
1	1	0	0	1	0	0	1	1	1	0	0	1	0	0	0
1	1	0	1	0	1	1	1	1	0	1	0	1	0	0	0
1	1	1	0	1	0	0	1	1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	0	1	1	1	0	1	0	0	0

Table 2: Truth table for 7-segment display outputs (For outputs, 0 = off, 1 = on)

Since I realized later in the lab how 0 means the LED's are on and 1 means they are off, I simply inverted the entire equation for each LED, and simplified with De' Morgan's law. The minimized equations are as follows:

$$CA = \bar{n}_3\bar{n}_2\bar{n}_1\bar{n}_0 + \bar{n}_3n_2\bar{n}_1\bar{n}_0 + n_3\bar{n}_2n_1n_0 + n_3n_2\bar{n}_1n_0$$

$$CB = \bar{n}_3n_2\bar{n}_1n_0 + \bar{n}_3n_2n_1\bar{n}_0 + n_3\bar{n}_2n_1n_0 + n_3n_2\bar{n}_1\bar{n}_0 + n_3n_2n_1\bar{n}_0 + n_3n_2n_1n_0$$

$$CC = \bar{n}_3\bar{n}_2n_1\bar{n}_0 + n_3n_2\bar{n}_1\bar{n}_0 + n_3n_2n_1\bar{n}_0 + n_3n_2n_1n_0$$

$$CD = \bar{n}_3\bar{n}_2\bar{n}_1n_0 + \bar{n}_3n_2\bar{n}_1\bar{n}_0 + \bar{n}_3n_2n_1n_0 + n_3\bar{n}_2\bar{n}_1n_0 + n_3\bar{n}_2n_1\bar{n}_0 + n_3n_2n_1n_0$$

$$CE = \bar{n}_3\bar{n}_2\bar{n}_1n_0 + \bar{n}_3\bar{n}_2n_1n_0 + \bar{n}_3n_2\bar{n}_1\bar{n}_0 + \bar{n}_3n_2\bar{n}_1n_0 + \bar{n}_3n_2n_1n_0 + n_3\bar{n}_2\bar{n}_1n_0$$

$$CF = \bar{n}_3\bar{n}_2\bar{n}_1n_0 + \bar{n}_3\bar{n}_2n_1\bar{n}_0 + \bar{n}_3\bar{n}_2n_1n_0 + \bar{n}_3n_2n_1n_0 + n_3\bar{n}_2\bar{n}_1n_0$$

$$CG = \bar{n}_3\bar{n}_2\bar{n}_1\bar{n}_0 + \bar{n}_3\bar{n}_2\bar{n}_1n_0 + \bar{n}_3n_2n_1n_0 + n_3n_2\bar{n}_1\bar{n}_0$$

The next step was to implement these sum of products equations with logic gates on my schematic.

Once my low-level logic for the 7-Segment display was complete I then created a top hierarchy schematic which contained a symbol for the 3 bit adder (Figure 2) and the 7-Segment display. I then connect each bit from sum of the full adder to the input of each bit of the 7-Segment display. The table below shows my findings of mapping of inputs to pins on the Bysas2 board.

Control	Pin		Control	Pin
CA	L14		SW2	K3
CB	H12		SW3	B4
CC	N14		SW4	G3
CD	N11		SW5	F3
CE	P12		SW6	E2
CF	L13		AN0	F12
CG	M12		AN1	J12
SW1	L3		AN2	M13
DP	N13		AN3	K14

Table 3: Pin mappings to LED's and switches

Top Level Schematic

Once all my inputs and outputs (I/O) was mapped to I/O BUFS, Symbols for the full adder and 7 segment display were created. Next I connected the switches to the proper inputs of the Full Adder, and the outputs of the Full Adder were sent to the appropriate signal on the 7-Segment display. The final result of my top layer schematic can be seen in Figure 3 on the next page.

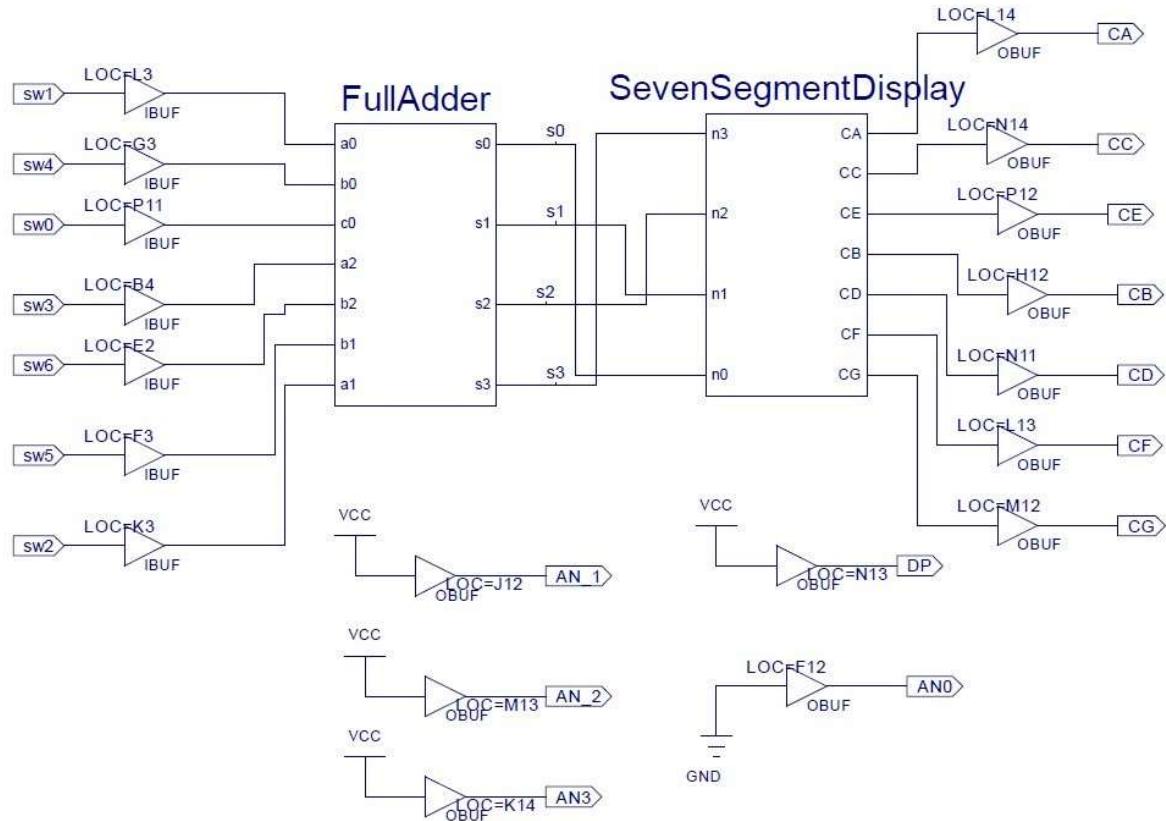


Figure 3: The Top schematic connects the 3-bit adder to the 7-Segment display

Simulator

My next task was to test my design in the simulator. I created a Verilog text fixture and pasted the provide code. This code would run in the simulator and it was my job to check to see if I was getting the correct 1 and 0 inputs and outputs for the LED's and switches. The code I had was not complete. I had to map out which switches were left on and continue to simulate flipping switches to test the next few characters that were not in the given Verilog code. I continued the provided code to make switches output hex numbers b-f. Once this was complete I ran the simulator and verified my results were the desired output.

Results

I was correct. I did not encounter any errors. My final step was to load my schematic to the board and run it on the board, and when I did my project ran perfectly. The first switch was a 1, which represented Cin, while the next three switches represented a's 3-bit input, and the next three switches represented b's 3-bit inputs.

From my schematic, the longest path for any input to any output in my 3-bit adder is 3 gates for the first adder + 2 gates x 2 remaining adders = 7 gates total.

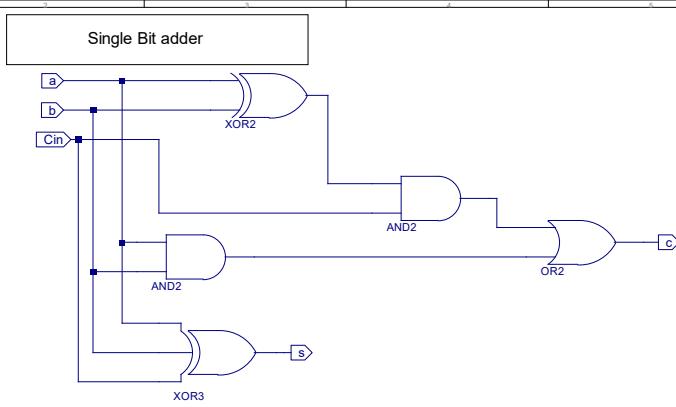
For an n-bit adder it will take a total of $3 + 2(n-1)$ gates total for a n-bit adder.

The number of possible input values for my adder is $2^7 = 128$ values. We tested 16 values which is $16/128 = 12.5\%$ of all possible inputs.

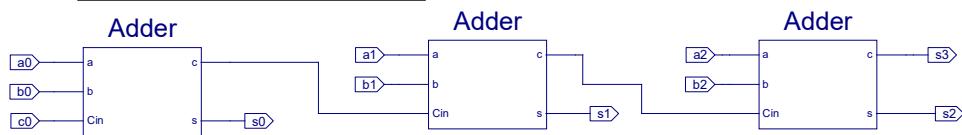
Conclusion

In this lab, I learned how to use LEDs for output schematic hierarchy, and how to use the simulator. In this process, I became familiar with mapping binary output to the 7-segment display. I learned how for this display, 0 means on and 1 means off. I was also able to become more familiar with the ISE design suite programs by learning a little bit of Verilog code. This will come in handy when stimulating future labs. If I could do this assignment again I would try to make sure I do not mix up my 0's and 1's when regarding the 7-segment display

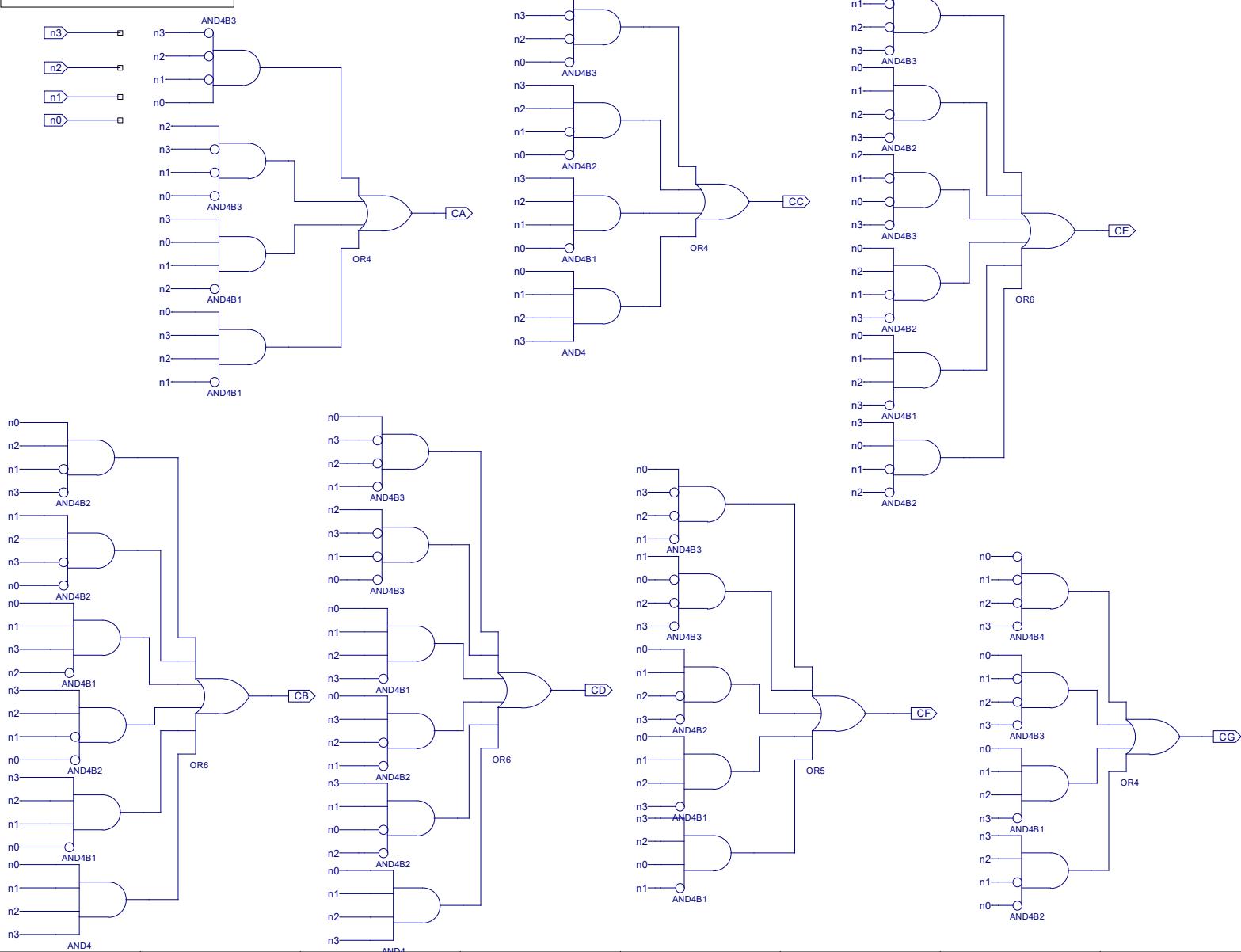
Appendices start on the next page

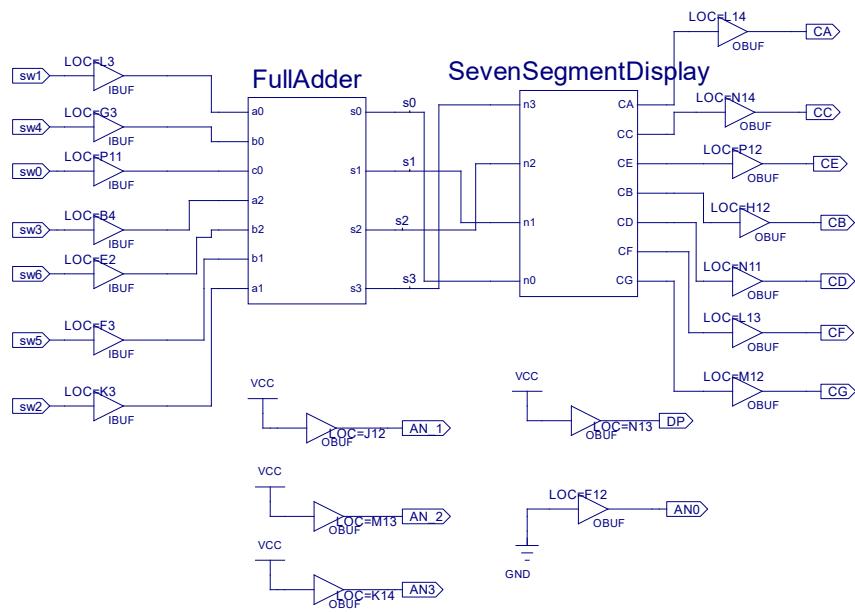


3-Bit Adder

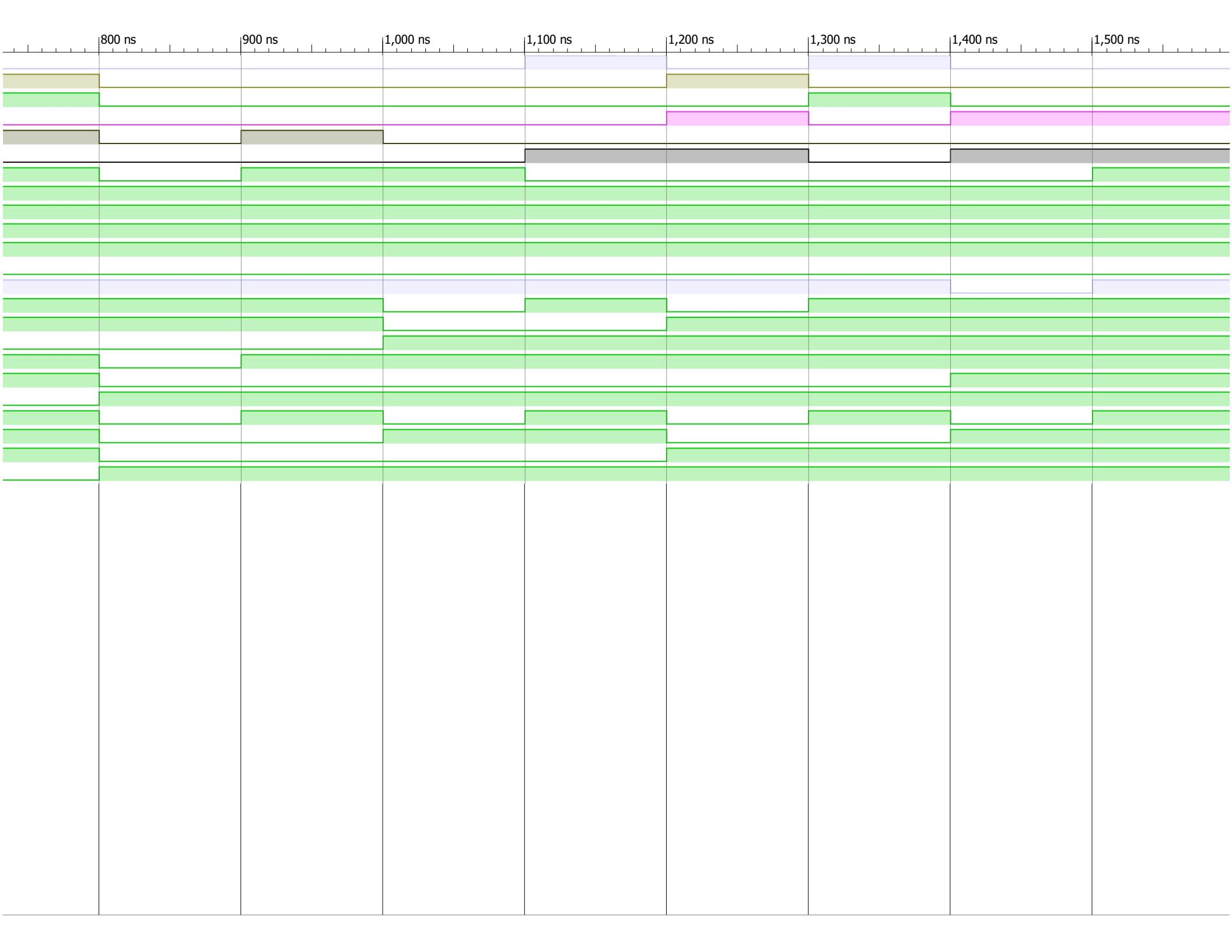


7-Segment Display LEDs CA - CG









Lab 2

3-bit full adder

3-bit full adder				
Input	Output			
C	B	A	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean Expression: $A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + A\bar{B}C = \text{sum}(S)$

$$\begin{aligned}
 & A\bar{A} + A\bar{B}\bar{C} + A\bar{B} + \\
 & \bar{A}A + \bar{A}B\bar{C} + \bar{A}\bar{B} + \\
 & \bar{A}A\bar{C} + A\bar{B}C + \bar{A}\bar{B}C + \bar{B}BC + A\bar{B}C \\
 & (A\bar{A} + AB + \bar{A}\bar{B} + B\bar{B})C + (\bar{A}B + A\bar{B})\bar{C} \\
 & ((A + \bar{B})(\bar{A} + B))C + (\bar{A}B + A\bar{B})\bar{C} \\
 & (A + \bar{B} + \bar{A} + B)C + (\bar{A}B + A\bar{B})\bar{C}
 \end{aligned}$$

DeMorgan: $(A\bar{B} + \bar{A}B)C + (\bar{A}B + A\bar{B})\bar{C}$

XOR Identity:

$$(A\bar{B} + \bar{A}B) \oplus C$$

XOR Identity:

$$\boxed{A \oplus B \oplus C = \text{sum}(S)}$$

$$\begin{aligned}
 \text{Cout} &= \bar{C}AB + C\bar{B}A + CBA\bar{C} + CBA \\
 & (A\bar{B} + \bar{A}B)C + CBA + \bar{C}AB
 \end{aligned}$$

$$(A\bar{B} + \bar{A}B)C + AB(C + \bar{C})$$

$$\boxed{\text{Cout} = (A \oplus B)C + AB}$$

Input			Truth Table ($1 = \text{on}$, $0 = \text{off}$)												
			Output												
n_3	n_2	n_1	n_0	C_A	C_B	C_C	C_D	C_E	C_F	C_G	ANO	AN1	AN2	AN3	DP
0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0
0	0	0	1	0	1	1	0	0	0	0	1	0	0	0	0
0	0	0	0	1	0	0	1	0	0	1	1	0	0	0	0
0	0	0	1	1	1	1	1	0	0	1	1	0	0	0	0
0	0	0	0	0	0	1	0	0	1	1	1	1	0	0	0
0	0	1	0	1	0	0	0	0	1	1	1	0	0	0	0
0	1	0	1	0	1	0	0	0	1	1	1	0	0	0	0
0	0	1	1	1	1	1	1	1	1	0	0	1	0	0	0
1	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0
1	0	0	1	1	1	1	0	0	1	1	1	0	0	0	0
1	0	1	0	0	1	0	1	1	1	1	1	0	0	0	0
1	1	0	0	1	0	0	0	1	1	1	0	0	0	0	0
1	1	0	1	0	1	1	1	0	1	1	1	0	0	0	0
1	1	1	0	1	0	0	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	0	0	1	1	1	0	0	0	0

$$\overline{C_A} = (n_3 + n_2 + n_1 + \bar{n}_0) (\bar{n}_3 + \bar{n}_2 + \bar{n}_1 + n_0) (\bar{n}_3 + n_2 + \bar{n}_1 + \bar{n}_0) (\bar{n}_3 + \bar{n}_2 + \bar{n}_1 + n_0)$$

- The cathode means $0 = 1$ and $1 = 0$ so I just invert my equations for the LEDs

$$C_A = \overline{(n_3 + n_2 + n_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + \bar{n}_1 + n_0)} \cdot \overline{(n_3 + n_2 + \bar{n}_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + \bar{n}_1 + n_0)}$$

$$\overline{n_3 n_2 n_1 \bar{n}_0} + \overline{n_3 \bar{n}_2 n_1 n_0} + \overline{n_3 n_2 \bar{n}_1 \bar{n}_0} + \overline{\bar{n}_3 \bar{n}_2 \bar{n}_1 n_0}$$

$$C_A = \overline{n_3 \bar{n}_2 \bar{n}_1 n_0} + \overline{\bar{n}_3 n_2 \bar{n}_1 \bar{n}_0} + \overline{n_3 \bar{n}_2 n_1 n_0} + \overline{n_3 n_2 \bar{n}_1 n_0}$$

$$C_B = \overline{(n_3 + \bar{n}_2 + n_1 + \bar{n}_0)} (\bar{n}_3 + \bar{n}_2 + \bar{n}_1 + n_0) (\bar{n}_3 + n_2 + \bar{n}_1 + \bar{n}_0) (\bar{n}_3 + \bar{n}_2 + n_1 + n_0) \cdot (\bar{n}_3 + \bar{n}_2 + \bar{n}_1 + n_0)$$

$$C_B = \overline{n_3 n_2 \bar{n}_1 n_0} + \overline{\bar{n}_3 n_2 n_1 \bar{n}_0} + \overline{n_3 \bar{n}_2 n_1 n_0} + \overline{n_3 n_2 \bar{n}_1 \bar{n}_0}$$

$$CC = \overline{(n_3 + n_2 + \bar{n}_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + n_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + \bar{n}_1 + n_0)} \cdot \overline{(n_3 + \bar{n}_2 + \bar{n}_1 + \bar{n}_0)}$$

$$CC = \bar{n}_3 \bar{n}_2 n_1 \bar{n}_0 + n_3 n_2 \bar{n}_1 \bar{n}_0 + n_3 n_2 n_1 \bar{n}_0 + n_3 n_2 n_1 n_0$$

$$CD = \overline{(n_3 + n_2 + n_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + n_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + \bar{n}_1 + \bar{n}_0)} \cdot \overline{(n_3 + n_2 + \bar{n}_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + \bar{n}_1 + \bar{n}_0)}$$

$$CD = \bar{n}_3 \bar{n}_2 \bar{n}_1 n_0 + \bar{n}_3 n_2 \bar{n}_1 \bar{n}_0 + \bar{n}_3 n_2 n_1 \bar{n}_0 + n_3 \bar{n}_2 \bar{n}_1 n_0 + n_3 \bar{n}_2 n_1 \bar{n}_0 + n_3 n_2 n_1 n_0$$

$$CE = \overline{(n_3 + n_2 + n_1 + \bar{n}_0)} \cdot \overline{(n_3 + n_2 + \bar{n}_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + n_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + \bar{n}_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + \bar{n}_1 + \bar{n}_0)}$$

$$CE = \bar{n}_3 \bar{n}_2 \bar{n}_1 n_0 + \bar{n}_3 \bar{n}_2 n_1 \bar{n}_0 + \bar{n}_3 n_2 \bar{n}_1 \bar{n}_0 + \bar{n}_3 n_2 \bar{n}_1 n_0 + \bar{n}_3 n_2 n_1 \bar{n}_0 + n_3 \bar{n}_2 \bar{n}_1 \bar{n}_0$$

$$CF = \overline{(n_3 + n_2 + \bar{n}_1 + \bar{n}_0)} \cdot \overline{(n_3 + n_2 + \bar{n}_1 + \bar{n}_0)}$$

$$CF = \overline{(n_3 + n_2 + n_1 + \bar{n}_0)} \cdot \overline{(n_3 + n_2 + \bar{n}_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + \bar{n}_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + n_1 + \bar{n}_0)}$$

$$CF = \bar{n}_3 \bar{n}_2 \bar{n}_1 n_0 + \bar{n}_3 \bar{n}_2 n_1 \bar{n}_0 + \bar{n}_3 \bar{n}_2 n_1 n_0 + \bar{n}_3 n_2 \bar{n}_1 \bar{n}_0 + \bar{n}_3 n_2 \bar{n}_1 n_0 + n_3 n_2 n_1 \bar{n}_0$$

$$CG = \overline{(n_3 + n_2 + n_1 + \bar{n}_0)} \cdot \overline{(n_3 + n_2 + \bar{n}_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + \bar{n}_1 + \bar{n}_0)} \cdot \overline{(n_3 + \bar{n}_2 + n_1 + \bar{n}_0)}$$

$$CG = \bar{n}_3 \bar{n}_2 \bar{n}_1 \bar{n}_0 + \bar{n}_3 \bar{n}_2 \bar{n}_1 n_0 + \bar{n}_3 \bar{n}_2 n_1 \bar{n}_0 + \bar{n}_3 n_2 \bar{n}_1 \bar{n}_0 + n_3 n_2 \bar{n}_1 \bar{n}_0$$

$$\boxed{AN\ 0 = 0} \quad (0 = ON)$$

$$\boxed{AN\ 1 = 1} \quad (1 = OFF)$$

$$\boxed{AN\ 2 = 1}$$

$$\boxed{AN\ 3 = 1}$$

$$\boxed{DP = 1}$$

$$\begin{array}{c} A \\ \hline F \mid G \mid B \\ E \mid \overline{D} \mid C \end{array}$$

Verilog code

Switches	0	1	2	3	4	5	6	Value, letter of switch	
0	0	0	0	0	0	0	0		
1	1	0	0	0	0	0	0	1c	
2	1	1	0	0	0	0	0	1a + 1c	
3	1	1	0	0	1	0	0	1a + 1c + 1L	
4	0	1	0	0	1	1	0	3b + 1a	
5	1	1	0	0	1	1	0	3b + 1a + 1c	
6	1	0	1	0	1	1	0	3b + 2a + 1c	
7	1	1	1	0	1	1	0	3b + 3a + 1c	
8	1	1	1	0	0	0	1	4b + 3a + 1c	
9	1	1	1	0	1	0	1	5b + 3a + 1c	
10	A	1	0	0	1	1	0	1	5b + 4a + 1c
11	B	1	1	0	1	1	0	1	5b + 5a + 1c
12	C	1	0	1	0	1	0	1	+ 1c
13	D	1	1	0	1	0	1		
14	E	0	1	1	1	1	1		
15	F	1	1	1	1	1	1		

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