

```
1  `timescale 1ns / 1ps
2  ///////////////////////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date:      18:15:00 04/30/2016
7  // Design Name:
8  // Module Name:      FSM
9  // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21 module FSM(Q,D,sec2,sec8,pb1,pb0,Match,swoff, resetTimer, LEDcontrols, Inc, Dec, Flash,
    Load, sec12, FlashLED, start, Vsec2, undertime, check);
22 input [6:0] Q;
23 input sec2;
24 input sec8;
25 input pb1;
26 input pb0;
27 input Match;
28 input swoff;
29 input sec12;
30 input Vsec2;
31
32 output [6:0] D;
33 output resetTimer;
34 output [1:0] LEDcontrols;
35 output Dec;
36 output Inc;
37 output Flash;
38 output Load;
39 output FlashLED;
40 output start;
41 output undertime;
42 output check;
43
44
45 assign D[0] = Q[0]&(~swoff | ~pb0) | Q[4]&Vsec2;
46 assign D[1] = Q[0]&pb0&swoff | ~sec2&Q[1]&swoff&~Match | pb0&swoff&Q[6] | pb0&swoff&Q[4]
    | pb0&swoff&Q[3] | pb0&swoff&Q[5]; // | pb0&swoff&Q[5]
47 assign D[2] = ~pb1&~sec8&Q[2] | sec2&swoff&Q[1]&~Match;
48 assign D[3] = (Q[1]&~swoff&~sec2) | (Q[3]&~swoff | Q[3]&swoff&~pb0) ;// EDIT LOGIC
49 assign D[4] = Q[2]&pb1&Match&~sec8 | Q[4]&~pb0 | Q[4]&~swoff | Q[4]&~Vsec2;
50 assign D[5] = Q[2]&~Match&pb1 | Q[5]&~swoff | Q[5]&~Match&~pb0;
51 assign D[6] = sec8&Q[2] | Q[6]&sec8;
52
53 assign resetTimer = pb0&swoff&Q[6] | pb0&swoff&Q[5] | pb0&swoff&Q[4] | pb0&swoff&Q[3] |
    Q[2]&~Match&pb1 | Q[0]&pb0&swoff | Q[1]&~swoff&~sec2;
54 assign LEDcontrols [0] = Q[0] | Q[2] | Q[4];
55 assign LEDcontrols [1] = Q[5] | Q[6] | Q[0] | Q[2];
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56 assign Dec = Q[2]&~Match&pb1 | Q[1]&~swoff&~sec2 | sec8&Q[2];
57 assign Inc = Q[2]&pb1&Match&~sec8;
58 assign Flash = Q[3]&~sec2; // | Q[5]&~sec2;
59 assign FlashLED = Q[5]&~Match&~sec2 | Q[6]&~sec12;
60 assign Load = (pb0&swoff)&(Q[6] | Q[5] | Q[4] | Q[3] | Q[0] | Q[4]) ;// add q[0] to
whiteboard
61 assign start = Q[2];
62 assign undertime = Q[3];
63 assign check = Q[4];
64 endmodule
```