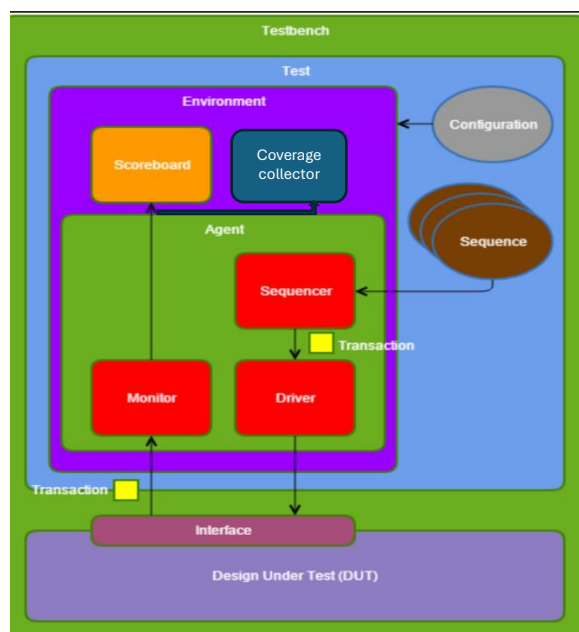


Test plane:

- I use UVM hierarchy to check FIFO design
- I do virtual interface to communicate with DUT as classes do not have ports
- I made sequences that are intended to be sent to the DUT
- Sequences delivering multiple sequence items through the sequencer to the driver
- Test start the sequence, build the env and passes the virtual interface
- Env build agent, scoreboard and coverage it also connects scoreboard and coverage with agent
- Agent builds sequencer, driver and monitor it also connect sequencer with driver and monitor with agent and virtual interface for driver and monitor
- Driver drives the interface signals
- Monitor monitors the activity of the interface and translate the pin level signals into sequence items to broadcast them to scoreboard and coverage
- Coverage checks on the functional coverage of the DUT
- Scoreboard checks for the DUT outputs



```

=====
Branch Coverage:
  Enabled Coverage      Bins    Hits    Misses  Coverage
  -----
  Branches              24      24      0    100.00%
=====Branch Details=====

```

```

Statement Coverage:
  Enabled Coverage      Bins    Hits    Misses  Coverage
  -----
  Statements            25      25      0    100.00%
=====Statement Details=====

```

```

Toggle Coverage:
  Enabled Coverage      Bins    Hits    Misses  Coverage
  -----
  Toggles              20      20      0    100.00%
=====Toggle Details=====

```

```

TOTAL COVERGROUP COVERAGE: 98.43%  COVERGROUP TYPES: 1
DIRECTIVE COVERAGE:

```

The coverage isn't 100% Bec. Cross coverage between wr_en , rd_en and full when wr is 0 or 1 and rd is 1 and full is 1 happen only at negedge of the clk

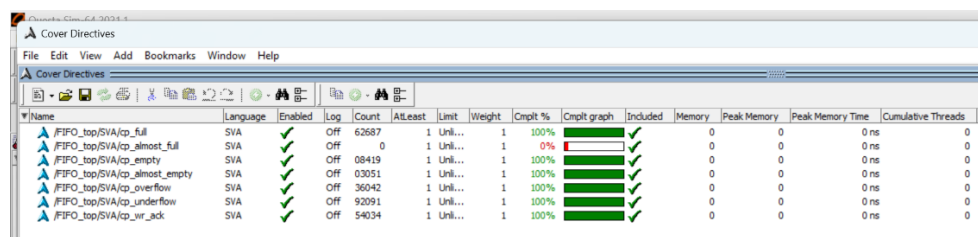
```

Assertion Coverage:
  Assertions            8      8      0    100.00%
-----
Name                  File(Line)                  Failure Count    Pass Count
-----
/FIFO_top/DUT/inst/ap_full
  FIFO_sva.sv(4)                  0      1
/FIFO_top/DUT/inst/ap_almost_full
  FIFO_sva.sv(11)                 0      1
/FIFO_top/DUT/inst/ap_empty
  FIFO_sva.sv(17)                  0      1
/FIFO_top/DUT/inst/ap_almost_empty
  FIFO_sva.sv(23)                  0      1
/FIFO_top/DUT/inst/ap_overflow
  FIFO_sva.sv(29)                  0      1
/FIFO_top/DUT/inst/ap_underflow
  FIFO_sva.sv(35)                  0      1
/FIFO_top/DUT/inst/ap_wr_ack
  FIFO_sva.sv(41)                  0      1
/FIFO_top/DUT/inst/assert_rst
  FIFO_sva.sv(48)                  0      1

Directive Coverage:
  Directives           7      7      0    100.00%
DIRECTIVE COVERAGE:
-----
Name                  Design Design Lang File(Line)    Hits Status
Unit UnitType
-----
/FIFO_top/DUT/inst/cp_full
  FIFO_sva Verilog SVA FIFO_sva.sv(6) 122676 Covered
/FIFO_top/DUT/inst/cp_almost_full
  FIFO_sva Verilog SVA FIFO_sva.sv(13) 27540 Covered
/FIFO_top/DUT/inst/cp_empty
  FIFO_sva Verilog SVA FIFO_sva.sv(19) 105192 Covered
/FIFO_top/DUT/inst/cp_almost_empty
  FIFO_sva Verilog SVA FIFO_sva.sv(25) 102566 Covered
/FIFO_top/DUT/inst/cp_overflow
  FIFO_sva Verilog SVA FIFO_sva.sv(31) 108499 Covered
/FIFO_top/DUT/inst/cp_underflow
  FIFO_sva Verilog SVA FIFO_sva.sv(37) 98864 Covered
/FIFO_top/DUT/inst/cp_wr_ack
  FIFO_sva Verilog SVA FIFO_sva.sv(43) 133514 Covered

```

Before correcting the errors:



Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads
▲ FIFO_top/SVA/cp_full	SVA	✓	Off	62687	1	Unli...	1	100%		✓	0	0	0 ns	0
▲ FIFO_top/SVA/cp_almost_full	SVA	✓	Off	0	1	Unli...	1	0%		✓	0	0	0 ns	0
▲ FIFO_top/SVA/cp_empty	SVA	✓	Off	08419	1	Unli...	1	100%		✓	0	0	0 ns	0
▲ FIFO_top/SVA/cp_almost_empty	SVA	✓	Off	03051	1	Unli...	1	100%		✓	0	0	0 ns	0
▲ FIFO_top/SVA/cp_overflow	SVA	✓	Off	36942	1	Unli...	1	100%		✓	0	0	0 ns	0
▲ FIFO_top/SVA/cp_underflow	SVA	✓	Off	92091	1	Unli...	1	100%		✓	0	0	0 ns	0
▲ FIFO_top/SVA/cp_wr_ack	SVA	✓	Off	54034	1	Unli...	1	100%		✓	0	0	0 ns	0

Assertions												
File Edit View Add Bookmarks Window Help												
Assertions												
Name	Assertion Type	Language	Enable	Failure Count	Pass Count	Active Count	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	ATV	Assertion Expression
uvm_pkg_uvm_reg_map_do_write/#ubk#215181159#17...	Immediate	SVA	on	0	0	-	-	-	-	-	-	off assert (kact1seq,0)
uvm_pkg_uvm_reg_map_do_read/#ubk#215181159#17...	Immediate	SVA	on	0	0	-	-	-	-	-	-	off assert (kact1seq,0)
FIFO_random_seq_pkg:FIFO_random_sequence:body/#...	Immediate	SVA	on	0	1	-	-	-	-	-	-	off assert (randomize(...))
FIFO_read_write_seq_pkg:FIFO_read_write_sequence:b...	Immediate	SVA	on	0	1	-	-	-	-	-	-	off assert (randomize(...))
FIFO_write_seq_pkg:FIFO_write_sequence:body/#ubk#...	Immediate	SVA	on	0	1	-	-	-	-	-	-	off assert (randomize(...))
FIFO_read_seq_pkg:FIFO_read_sequence:body/#ubk#2...	Immediate	SVA	on	0	1	-	-	-	-	-	-	off assert (randomize(...))
FIFO_top/SVA/ap_full	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_empty	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_almost_empty	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_overflow	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_underflow	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_ack	Concurrent	SVA	on	5664	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_almost_full	Concurrent	SVA	on	53545	0	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...

The errors was Bec. Of

- Almost full signal was implemented logically in correct
- Underflow signal was combinational and the spec want it sequential output
- The data out when reset asserted doesn't take zero
- The count signal not handle all its case

After correcting the errors:

```

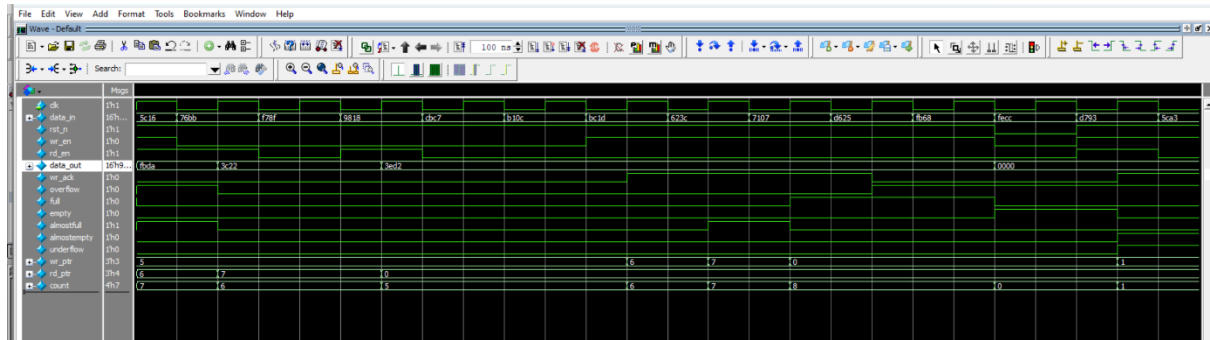
Transcript
# uvm_config_db{uvm_bitstream_t}::set(null, "", "recording_detail", 0);
# uvm_info FIFO_test.av(51) @ 2: uvm_test_top [run_phase] reset deasserted
# uvm_info FIFO_test.av(53) @ 2: uvm_test_top [run_phase] stimulus generation started
# uvm_info FIFO_test.av(55) @ 200002: uvm_test_top [run_phase] stimulus generation ended
# uvm_info FIFO_test.av(57) @ 200002: uvm_test_top [run_phase] stimulus generation started
# uvm_info FIFO_test.av(59) @ 400002: uvm_test_top [run_phase] stimulus generation started
# uvm_info FIFO_test.av(61) @ 400002: uvm_test_top [run_phase] stimulus generation started
# uvm_info FIFO_test.av(63) @ 600002: uvm_test_top [run_phase] stimulus generation started
# uvm_info FIFO_test.av(65) @ 600002: uvm_test_top [run_phase] stimulus generation started
# uvm_info FIFO_test.av(67) @ 800002: uvm_test_top [run_phase] stimulus generation ended
# uvm_info verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1367) @ 800002: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
# uvm_info FIFO_scoreboard.av(102) @ 800002: uvm_test_top.env.sb [report_phase] total successful transactions:400001
# uvm_info FIFO_scoreboard.av(103) @ 800002: uvm_test_top.env.sb [report_phase] total failed transactions:0

--- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO : 16
# UVM_WARNING : 0
# UVM_ERROR : 0
# UVM_FATAL : 0
#
# ** Report counts by id
# [Questa UVM] 2
# [RNTST] 1
# [TEST_DONE] 1
# [report_phase] 2
# [run_phase] 10
#
# ** Note: $finish : C:/questasim64_2021.1/win64/./verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
# Time: 800002 ns Iteration: 61 Instance: /FIFO_top
# Break in Task uvm_pkg/uvm_root::run_test at C:/questasim64_2021.1/win64/./verilog_src/uvm-1.1d/src/base/uvm_root.svh line 430
# QuestaSim-64 vcover 2021.1 Coverage Utility 2021.01 Jan 19 2021
# Start time: 12:46:47 on Oct 09, 2024
# vcover report FIFO_test.ucdb -details -all -annotate -output FIFO_cvr.txt
# End time: 12:46:47 on Oct 09, 2024, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0

```

Assertions												
File Edit View Add Bookmarks Window Help												
Assertions												
Name	Assertion Type	Language	Enable	Failure Count	Pass Count	Active Count	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	ATV	Assertion Expression
uvm_pkg_uvm_reg_map_do_write/#ubk#215181159#17...	Immediate	SVA	on	0	0	-	-	-	-	-	-	off assert (kact1seq,0)
uvm_pkg_uvm_reg_map_do_read/#ubk#215181159#17...	Immediate	SVA	on	0	0	-	-	-	-	-	-	off assert (kact1seq,0)
FIFO_random_seq_pkg:FIFO_random_sequence:body/#...	Immediate	SVA	on	0	1	-	-	-	-	-	-	off assert (randomize(...))
FIFO_read_write_seq_pkg:FIFO_read_write_sequence:b...	Immediate	SVA	on	0	1	-	-	-	-	-	-	off assert (randomize(...))
FIFO_write_seq_pkg:FIFO_write_sequence:body/#ubk#...	Immediate	SVA	on	0	1	-	-	-	-	-	-	off assert (randomize(...))
FIFO_read_seq_pkg:FIFO_read_sequence:body/#ubk#2...	Immediate	SVA	on	0	1	-	-	-	-	-	-	off assert (randomize(...))
FIFO_top/SVA/ap_full	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_almost_full	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_empty	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_almost_empty	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_overflow	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_underflow	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_ack	Concurrent	SVA	on	0	1	-	0B	0B	0ns	0	off	assert(@posedge tfs_f.clk) disa...
FIFO_top/SVA/ap_almost_full	Immediate	SVA	on	0	1	-	-	-	-	-	-	off assert (DUT.count==0BOUT.wr...

Cover Directives												
File Edit View Add Bookmarks Window Help												
Cover Directives												
Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmpnt %	Cmpnt graph	Included	Memory	Peak Memory
FIFO_top/SVA/ap_full	SVA	Off	22676	1	Unli...	1	100%	100%	100%	0	0	0
FIFO_top/SVA/ap_almost_full	SVA	Off	27540	1	Unli...	1	100%	100%	100%	0	0	0
FIFO_top/SVA/ap_empty	SVA	Off	05192	1	Unli...	1	100%	100%	100%	0	0	0
FIFO_top/SVA/ap_almost_empty	SVA	Off	02566	1	Unli...	1	100%	100%	100%	0	0	0
FIFO_top/SVA/ap_overflow	SVA	Off	08499	1	Unli...	1	100%	100%	100%	0	0	0
FIFO_top/SVA/ap_underflow	SVA	Off	98864	1	Unli...	1	100%	100%	100%	0	0	0
FIFO_top/SVA/ap_ack	SVA	Off	33514	1	Unli...	1	100%	100%	100%	0	0	0



feature	assertion
When counter=fifo depth, full=1	<code>(@(posedge fifo_if.clk) disable iff(!fifo_if.rst_n) DUT.count===fifo_if.FIFO_DEPTH -> fifo_if.full);</code>
When counter=fifo depth-1 ,almost full=1	<code>(@(posedge fifo_if.clk) disable iff(!fifo_if.rst_n) DUT.count==(fifo_if.FIFO_DEPTH-1) -> fifo_if.almostfull);</code>
When counter=0, empty signal=1	<code>(@(posedge fifo_if.clk) disable iff(!fifo_if.rst_n) DUT.count===0 -> fifo_if.empty);</code>
When counter=1, almost empty=1	<code>(@(posedge fifo_if.clk) disable iff(!fifo_if.rst_n) DUT.count===1 -> fifo_if.almostempty);</code>
When full=1 and write enable =1, overflow=1	<code>(@(posedge fifo_if.clk) disable iff(!fifo_if.rst_n) fifo_if.full&&fifo_if.wr_en => fifo_if.overflow);</code>
When empty=1 and read enable=1, underflow=1	<code>(@(posedge fifo_if.clk) disable iff(!fifo_if.rst_n) fifo_if.empty&&fifo_if.rd_en => fifo_if.underflow);</code>
When write pointer value increased by one , wr_ack=1	<code>(@(posedge fifo_if.clk) disable iff(!fifo_if.rst_n) DUT.wr_ptr===\$past(DUT.wr_ptr)+1 -> fifo_if.wr_ack);</code>
When reset asserted then counter , write pointer and read pointer =0	<code>assert_rst: assert final(DUT.count===0 && DUT.wr_ptr===0 && DUT.rd_ptr===0);</code>