Project 2

Digital Calculator

The American University in Cairo

School of Science and Engineering

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Digital Design 1

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Project Report

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Introduction:

This project represents a simple digital calculator which performs the basic arithmetic operations addition (+), multiplication (*), subtraction (-), and division (/) of two numbers N1 and N2, then it displays their output on the seven-segment display using FPGA (Basys 3) and VHDL (Verilog).

Program Design:

The program has four buttons where the user uses each button to adjust a single digit on the FPGA. The two numbers are separated with a decimal point between them. Each digit ranges from 0 : 9, and each two digits represents the tenths and the unites of a single number from the two that are used in the calculations. The program gets the digit in the tenths place and multiply it by ten the add it to the other digit in the units' place to get the numbers that will be used in the arithmetic operations. Consequently, each number of them is restricted between $0 \leq N1 \leq 99$, $0 \leq N2 \leq 99$. The two numbers are of max 7 bits and after doing any one of the calculations (addition, multiplication, division, subtraction) the maximum output we could get is 9801 which is 99 multiply 99. This number is represented by 14 bits. Thus, the size of the output reg in the program is 14 bits. Then the program takes this number and keeps getting the modulus of it until it gets the four digits separated in four different wires. Then each number is transformed through a decoder that will get the code equivalents for the desired digit that will be displayed on a specific location on the FPGA. In case of division the program checks whether the second number is zero or not. If it is zero, the output on the screen will be "EEEE" as an indicator that there is an error in the input numbers. Otherwise, it will output the number resulted from the calculation, and it will even show if it is negative or not. Since it is impossible to display

different four numbers at the 7-segment display at the same time. I used the famous trick of displaying each digit on a different location then use a 2-bit counter and a fast clock to make them look as if they are all are present at the same time which is a known trick on the eye. The whole sequential circuit is synchronized with each other using a clock f 1 KHz and an asynchronized reset.

Instructions:

The user should use:

Buttons:

- Button U17: to adjust the tenth of the first number.
- Button T17: to adjust the unit of the first number.
- Button T18: to adjust the tenth of the second number.
- Button W19: to adjust the unit of the second number.

Switches:

Level Triggered

- Switch R2: to reset the circuit.
    - 0: The calculator works.
    - 1: The calculator resets and does not work.
- Switch T1: to show the answer of the calculation.
    - 0: It displays the original numbers used for the calculation.
    - 1: It displays the output of the arithmetic operations.

Positive Edge Triggered

- Switch W2: to perform addition.

- Switch R3: to perform subtraction
- Switch T2: to perform multiplication.
- Switch T3: to perform division.

All the required test cases are done on the FPGA in the videos on this drive.

https://drive.google.com/drive/folders/13QgOYz580w19VscJFpZnKRFrVafiMshN?usp=sharing