
**Digital Design using Verilog by Karim
Wassem**

**Combinational Circuit Design &
Sequential Logic Design
Project (2)**

SPI Slave with Single Port RAM

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Group: 1

• QuestaSim Snippets

```

VSIM 109> do run_spi.do
# ** Warning: (vlib-34) Library already exists at "work".
# Errors: 0, Warnings: 1
# QuestaSim-64 vlog 2021.1 Compiler 2021.01 Jan 19 2021
# Start time: 14:43:25 on Aug 05,2025
# vlog -reportprogress 300 SPI_Slave.v RAM.v TopModule.v SPI_Slave_tb.v
# -- Compiling module SPI_Slave
# -- Compiling module SPI_RAM
# -- Compiling module TopModule
# -- Compiling module SPI_Slave_tb
#
# Top level modules:
#   SPI_Slave_tb
# End time: 14:43:25 on Aug 05,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# ** Error: 指定した名前でファイルが既に存在します。
#
#       Unable to replace existing ini file (F:/Downloads Backup/test - Copy/test - Copy/spi.mpf). File can not be renamed.
# ** Error: 指定した名前でファイルが既に存在します。
#
#       Unable to replace existing ini file (F:/Downloads Backup/test - Copy/test - Copy/spi.mpf). File can not be renamed.

```

Transcript

```

# Errors: 0, Warnings: 0
# ** Error: 指定した名前でファイルが既に存在します。

#
#       Unable to replace existing ini file (F:/Downloads Backup/test - Copy/test - Copy/spi.mpf). File can not be renamed.
# ** Error: 指定した名前でファイルが既に存在します.

#
#       Unable to replace existing ini file (F:/Downloads Backup/test - Copy/test - Copy/spi.mpf). File can not be renamed.
# End time: 14:43:31 on Aug 05,2025, Elapsed time: 0:02:53
# Errors: 3, Warnings: 3
# vsim -voptargs="+acc" work.SPI_Slave_tb
# Start time: 14:43:31 on Aug 05,2025
# ** Note: (vsim-8009) Loading existing optimized design _opt1
# Loading work.SPI_Slave_tb(fast)
# Loading work.TopModule(fast)
# Loading work.SPI_Slave(fast)
# Loading work.SPI_RAM(fast)
# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf
#           File in use by: lenovo Hostname: DESKTOP-C3FPSSER ProcessID: 11308
#           Attempting to use alternate WLF file "./wlft9fk9t".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
#           Using alternate file: ./wlft9fk9t
# Test 1 : Write Address Command
# Test 2 : Write Data Command
# Verify RAM Content
# Test 3 : Read Address Command
# Test 4 : Read Data Command
# Done
# ** Note: $stop : SPI_Slave_tb.v(125)
# Time: 156 ns Iteration: 1 Instance: /SPI_Slave_tb
# Break in Module SPI_Slave_tb at SPI_Slave_tb.v line 125

VSIM 109> ]

```



• QuestaLint Snippets

The screenshot shows the QuestaLogic interface with several windows open:

- Design View:** Shows the project structure and the code for `TopModule.v`. The code defines a module `TopModule` with an SPI slave and a SPI RAM component.
- Schematic View:** Shows the internal logic of the `TopModule`. It includes an `spi_slave` component connected to an `SPI_SLAVE` and an `SPI_RAM` component. The `spi_slave` component has connections for `MOSI`, `SS_n`, `clk`, `rst_n`, `rx_data`, `tx_data`, `rx_valid`, and `tx_valid`.
- Lint Checks View:** Displays a table of lint errors found in the design. The table includes columns for Severity, Status, Check, Alias, Message, Module, and Category.

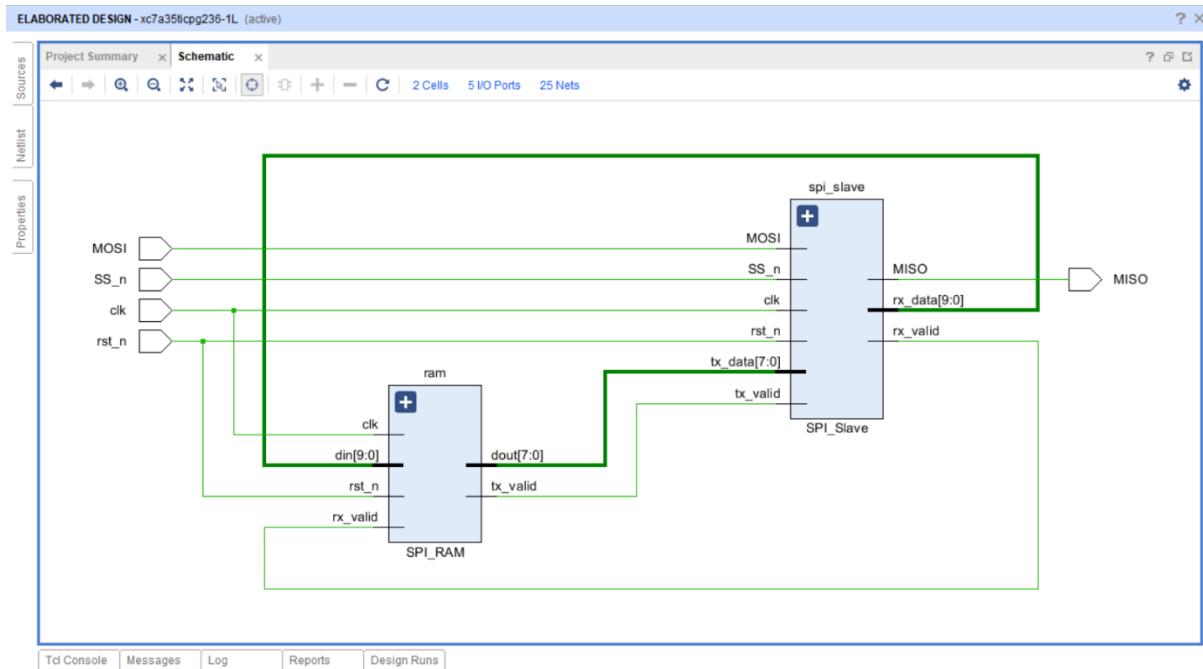
Severity	Status	Check	Alias	Message	Module	Category
?	?	always_signal_assign_large		Always block has more signal assignments than the specified limit. T...	SPI_Slave	Rtl Design Style
?	?	multi_ports_in_single_line		Multiple ports are declared in one line. Module SPI_RAM, File G:/kar...	SPI_RAM	Rtl Design Style
?	?	multi_ports_in_single_line		Multiple ports are declared in one line. Module SPI_Slave, File G:/kar...	SPI_Slave	Rtl Design Style
?	?	multi_ports_in_single_line		Multiple ports are declared in one line. Module TopModule, File G:/kar...	TopModule	Rtl Design Style

• Vivado Snippets

1. Sequential encoding

-Elaborated Design

Schematic

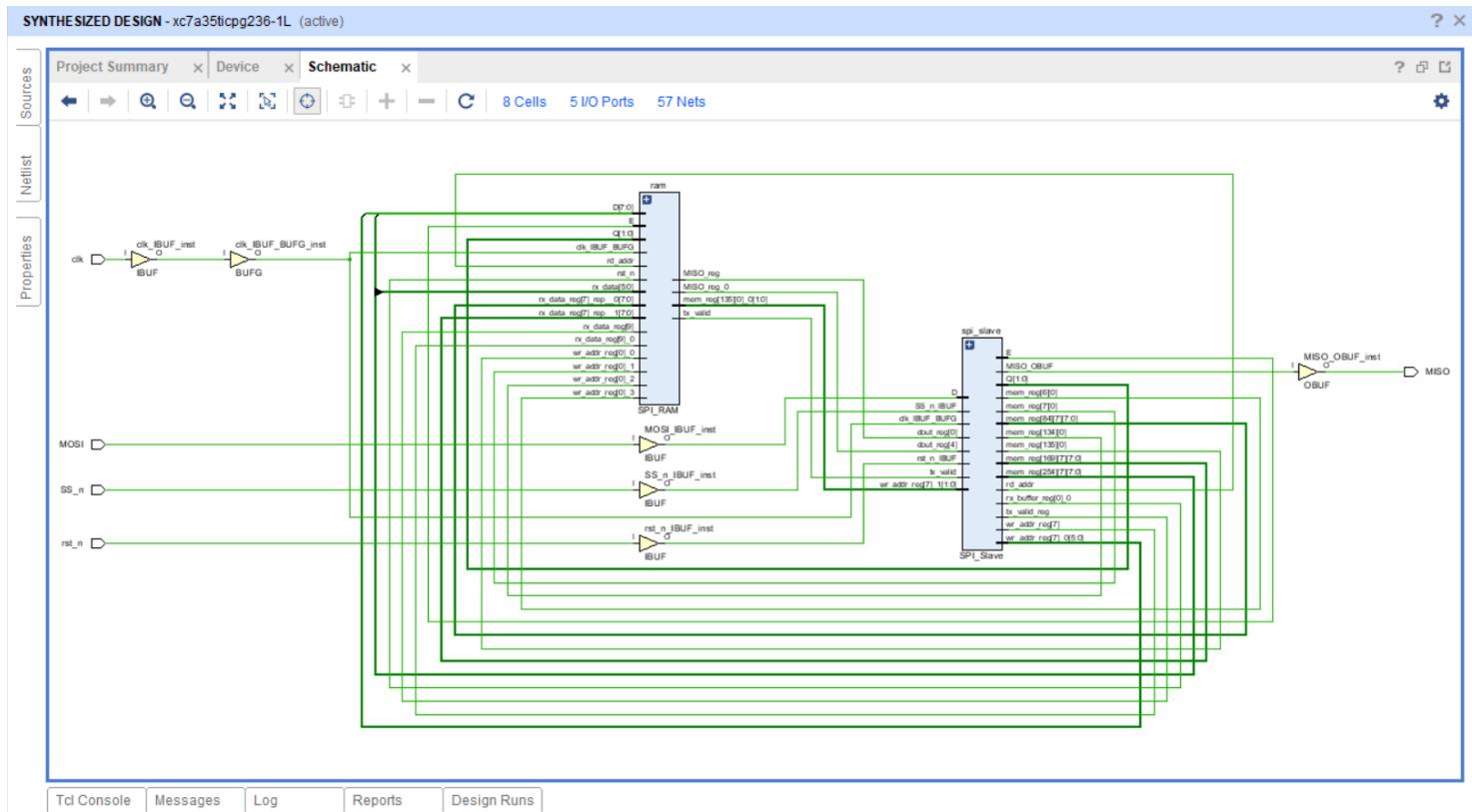


Message Tab

- ✓ Elaborated Design (2 warnings, 10 infos)
 - ✓ General Messages (2 warnings, 10 infos)
 - > ⓘ [Synth 8-6157] synthesizing module 'TopModule' [[TopModule.v:1](#)] (2 more like this)
 - ⓘ [Synth 8-155] case statement is not full and has no default [[SPI_Slave.v:97](#)]
 - ⓘ [Synth 8-5788] Register mem_reg in module SPI_RAM is has both Set and reset with same priority. This may cause simulation mismatches. Consider rewriting code
 - ⓘ [Synth 8-4767] Trying to implement RAM 'mem_reg' in registers. Block RAM or DRAM implementation is not possible; see log for reasons.
 - > ⓘ [Synth 8-6155] done synthesizing module 'SPI_Slave' (#1) [[SPI_Slave.v:1](#)] (2 more like this)
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - ⓘ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

-Synthesis Design

Schematic



Message Tab

- ✓ **Synthesis** (4 warnings, 130 infos)
- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'.
 - [Synth 8-6157] synthesizing module 'TopModule' [**TopModule.v1**] (2 more like this)
 - [Synth 8-115] case statement is not full and has no default [SPI_Slave.v97]
 - [Synth 8-5788] Register mem_Reg in module SPI_RAM has both Set and reset with same priority. This may cause simulation mismatches. Consider rewriting code.
 - [Synth 8-4767] Trying to implement RAM 'mem_Reg' in registers. Block RAM or DRAM implementation is not possible; see log for reasons.
 - [Synth 8-6155] done synthesizing module 'SPI_Slave' (1#1) [**SPI_Slave.v1**] (2 more like this)
 - [Device 21-403] Loading part xc7a35tcpg236-1L
 - [Project 1-236] Implementation specific constraints were found while reading constraint file [E:/Digital_Design/Project2/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xil/TopModule_propimpl.xdc].
Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
 - [Synth 8-802] inferred ROM for state register 'cs_Reg' in module 'SPI_Slave'
 - [Synth 8-5541] ROM 'rx_valid' won't be mapped to Block RAM because address size (4) smaller than threshold (5) (4 more like this)
 - [Synth 8-3354] encoded FSM with state register 'cs_Reg' using encoding 'sequential' in module 'SPI_Slave'
 - [Synth 8-5546] ROM 'p_0_out' won't be mapped to RAM because it is too sparse (99 more like this)
 - [Common 17-14] Message 'Synth 8-5546' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set_msg_config to change the current settings.
 - [Project 1-571] Translating synthesized netlist
 - [Netlist 29-17] Analyzing 412 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Netlist 29-101] Netlist 'TopModule' is not ideal for floorplanning, since the cellview 'SPI_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
 - [Project 1-570] Preparing netlist for logic optimization (1 more like this)
 - [Opt 31-138] Pushed 0 inverter(s) to load pin(s).
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
 - [Common 17-83] Releasing license: Synthesis
 - [Constraints 18-5210] No constraint will be written out.
 - [Common 17-1381] The checkpoint 'E:/Digital_Design/IVADO/Assignment4/project_16/runs/synth_1/TopModule.dcp' has been generated.
 - [runlcl-4] Executing :report_utilization -file TopModule_utilization_synth.rpt -pb TopModule_utilization_synth.pb
 - [Common 17-206] Exiting Vivado at Tue Aug 5 15:32:25 2025...
- ✓ **Synthesized Design** (1 warning, 6 infos)
- ✓ **General Messages** (1 warning, 6 infos)
- [Netlist 29-17] Analyzing 412 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Netlist 29-101] Netlist 'TopModule' is not ideal for floorplanning, since the cellview 'SPI_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to load pin(s).
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

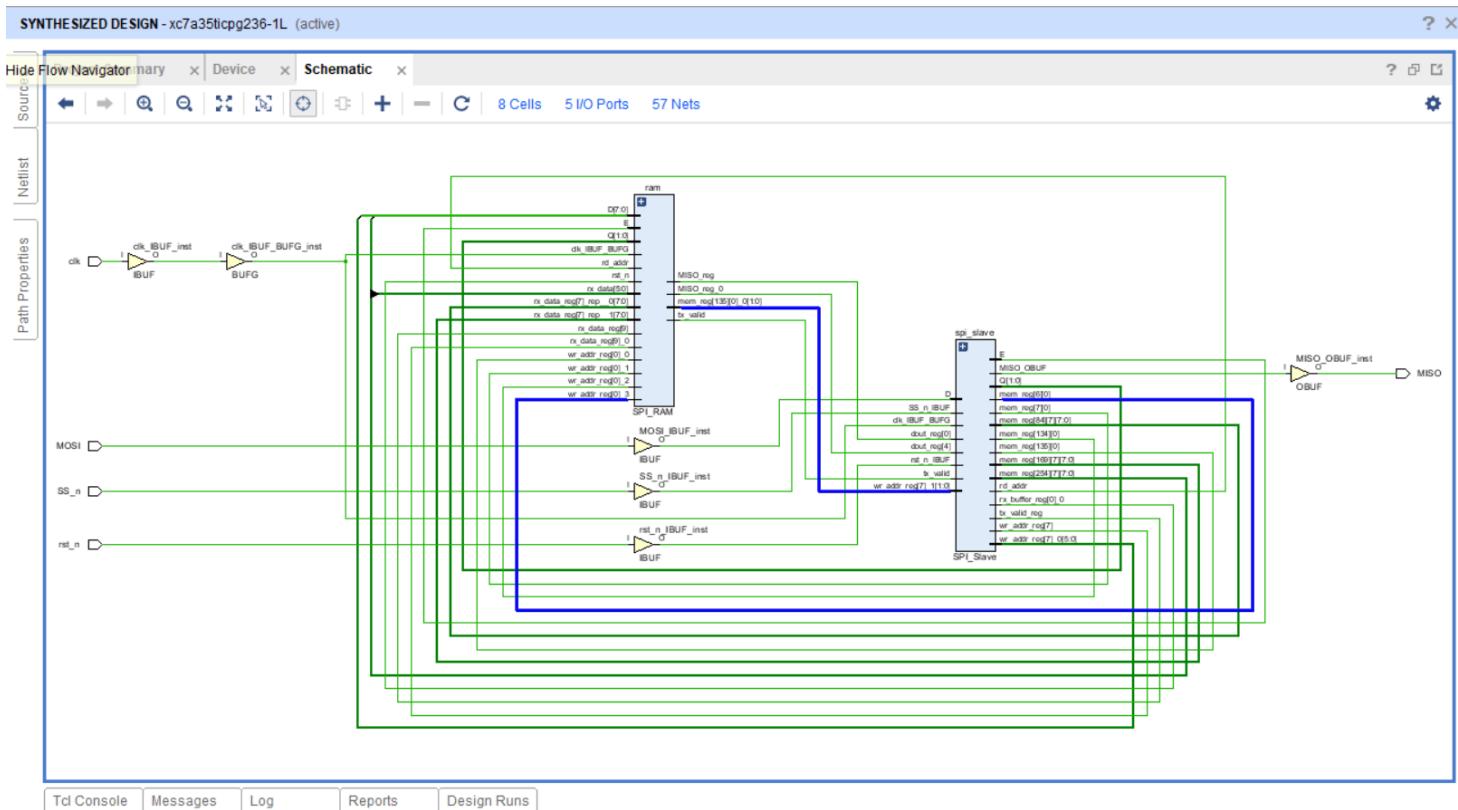
Utilization Report

	Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Bonded IOB (106)	BUFGCTRL (32)
Hierarchy							
Summary							
Slice Logic							
Slice LUTs (4%)	TopModule	894	2154	272	136	5	1
LUT as Logic (4%)	ram (SPI_RAM)	810	2100	272	136	0	0
Slice Registers (5%)	spi_slave (SPI_Slave)	84	54	0	0	0	0
Register as Flip Flop (5%)							
F8 Muxes (2%)							

Timing Report

Tcl Console	Messages	Log	Reports	Design Runs	Utilization	Timing	
Q	☰	☰	C	H		Design Timing Summary	
General Information							
Timer Settings							
Design Timing Summary							
Clock Summary (1)							
> Check Timing (4)							
> Intra-Clock Paths							
Inter-Clock Paths							
Other Path Groups							
User Ignored Paths							
> Unconstrained Paths							

Critical Synthesized Path



Synthesis Report

SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active) ? x

Project Summary x Device x Schematic x synth_1_synth_synthesis_report_0 - synth_1 x

E:/Digital_Design/VIVADO/Assignment4/project_16/project_16.runs/synth_1/TopModule.vds

Read-only |

Sources | Netlist | Path Properties

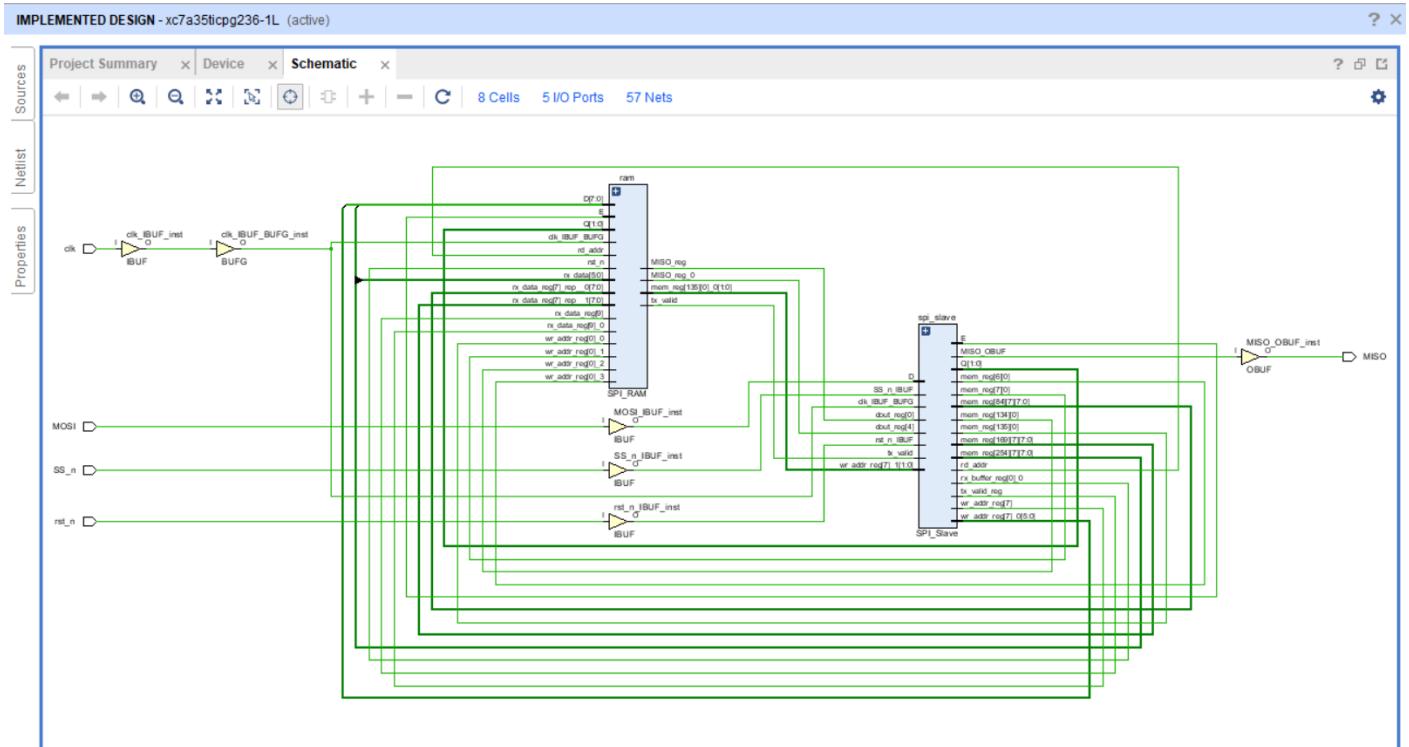
sequential | Next | Previous | Highlight | Match Case | Whole Words | 1 Match(es)

```
83 Finished Loading Part and Timing Information : Time (s): cpu = 00:00:20 ; elapsed = 00:00:23 . Memory (MB): peak = 845.289 ; gain = 525.363
84 -----
85 -----
86 Start Applying 'set_property' XDC Constraints
87 -----
88 -----
89 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:20 ; elapsed = 00:00:24 . Memory (MB): peak = 845.289 ; gain = 525.363
90 -----
91 INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_Slave'
92 INFO: [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
93 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
94 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
95 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
96 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
97 -----
98 State | New Encoding | Previous Encoding
99 -----
100 IDLE | 000 | 000
101 CHK_CMD | 001 | 001
102 READ_ADD | 010 | 100
103 READ_DATA | 011 | 011
104 WRITE | 100 | 010
105 -----
106 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_Slave'
107 -----
108 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:21 ; elapsed = 00:00:25 . Memory (MB): peak = 845.289 ; gain = 525.363
109 -----
110 -----
111 Report RTL Partitions:
<-----
```

Tcl Console | Messages | Log | Reports | Design Runs

-Implementation Design

Schematic



Message Tab

Implemented Design (1 warning, 9 infos)
General Messages (1 warning, 9 infos)
[Netlist 29-17] Analyzing 412 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Netlist 29-101] Netlist 'TopModule' is not ideal for floorplanning, since the cellview 'SPI_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
[Project 1-479] Netlist was created with Vivado 2018.2
[Project 1-570] Preparing netlist for logic optimization
[Timing 38-478] Restoring timing data from binary archive.
[Timing 38-479] Binary timing data restore complete.
[Project 1-856] Restoring constraints from binary archive.
[Project 1-853] Binary constraint restore complete.
[Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.

Utilization Report

Tcl Console	Messages	Log	Reports	Design Runs	Power	Methodology	Timing	Utilization	x	?	—	⊕	⚙
Q	☰	☰	Q	☰	☰	☰	%	Hierarchy					
Hierarchy													
Summary													
Slice Logic													
Slice LUTs (4%)													
LUT as Logic (4%)													
F8 Muxes (2%)													
F7 Muxes (2%)													
Slice Registers (5%)													
Register as Flip Flop ()
Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)			
TopModule		893	2154	272	136	775	893	52	5	1			
ram (SPI_RAM)		810	2100	272	136	744	810	8	0	0			
spi_slave (SPI_Slave)		83	54	0	0	34	83	43	0	0			

Timing Report

Tcl Console Messages Log Reports Design Runs Power Methodology **Timing** Utilization ? _ < >

General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
> Check Timing (4)
> Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
> Unconstrained Paths

Design Timing Summary

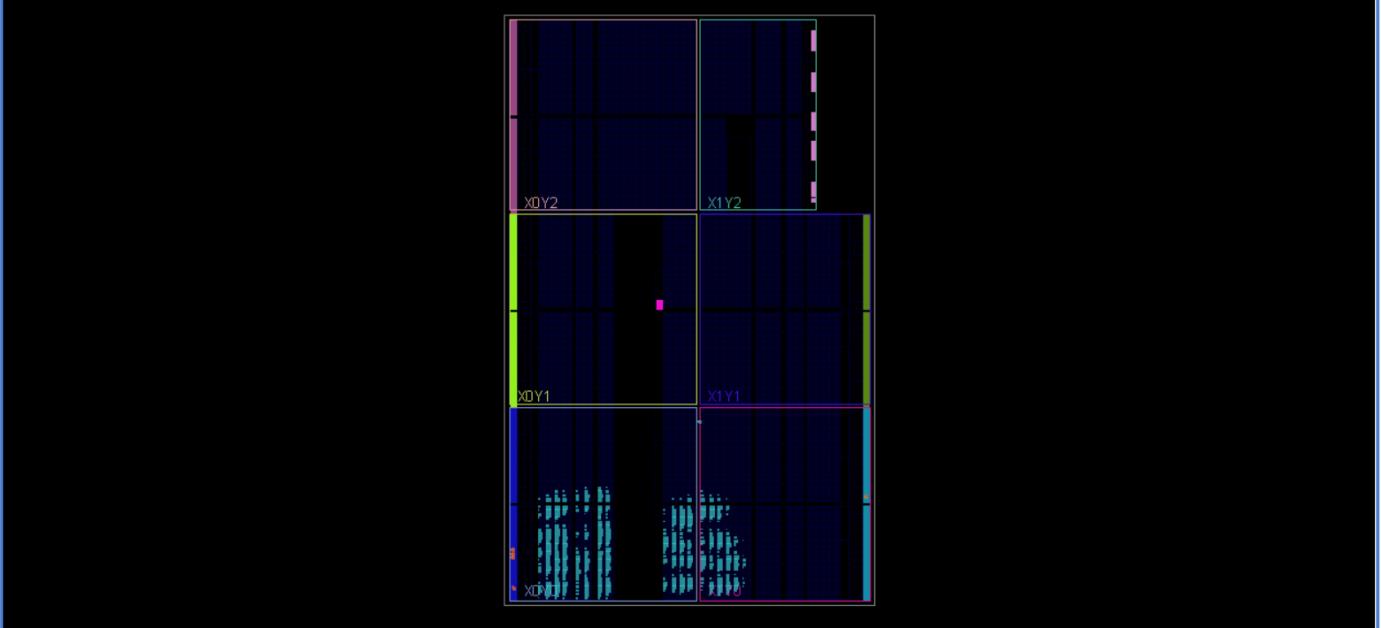
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.590 ns	Worst Hold Slack (WHS): 0.202 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4258	Total Number of Endpoints: 4258	Total Number of Endpoints: 2155

All user specified timing constraints are met.

FPGA Device

IMPLEMENTED DESIGN - xc7a35tci236-1L (active)

Project Summary Device TopModule.v SPI_Slave.v ? & < > Sources Netlist Source File Properties

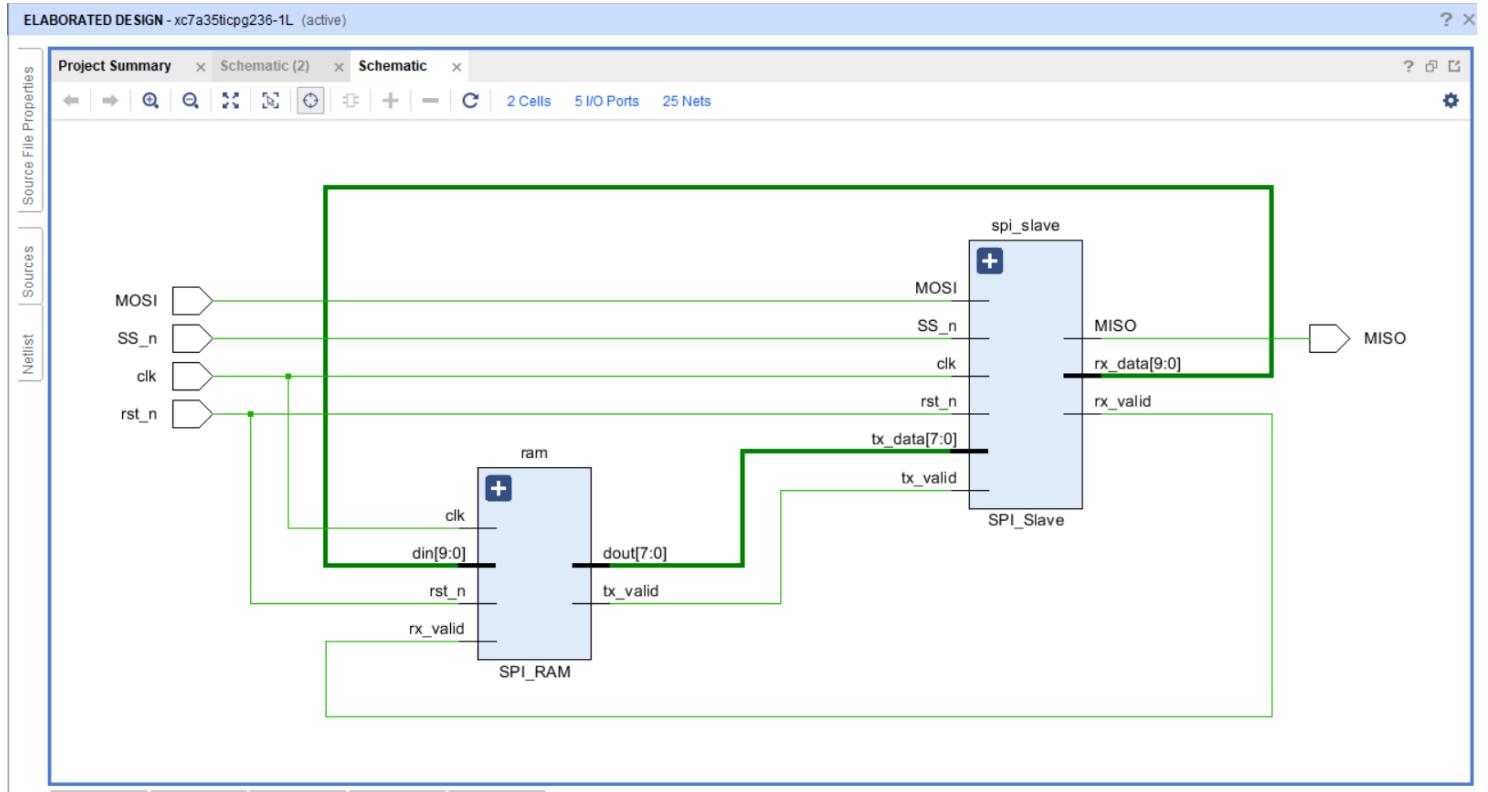


Tcl Console Messages Log Reports Design Runs Power Methodology Timing ? _ < >

2. Gray coded encoding

-Elaborated Design

Schematic

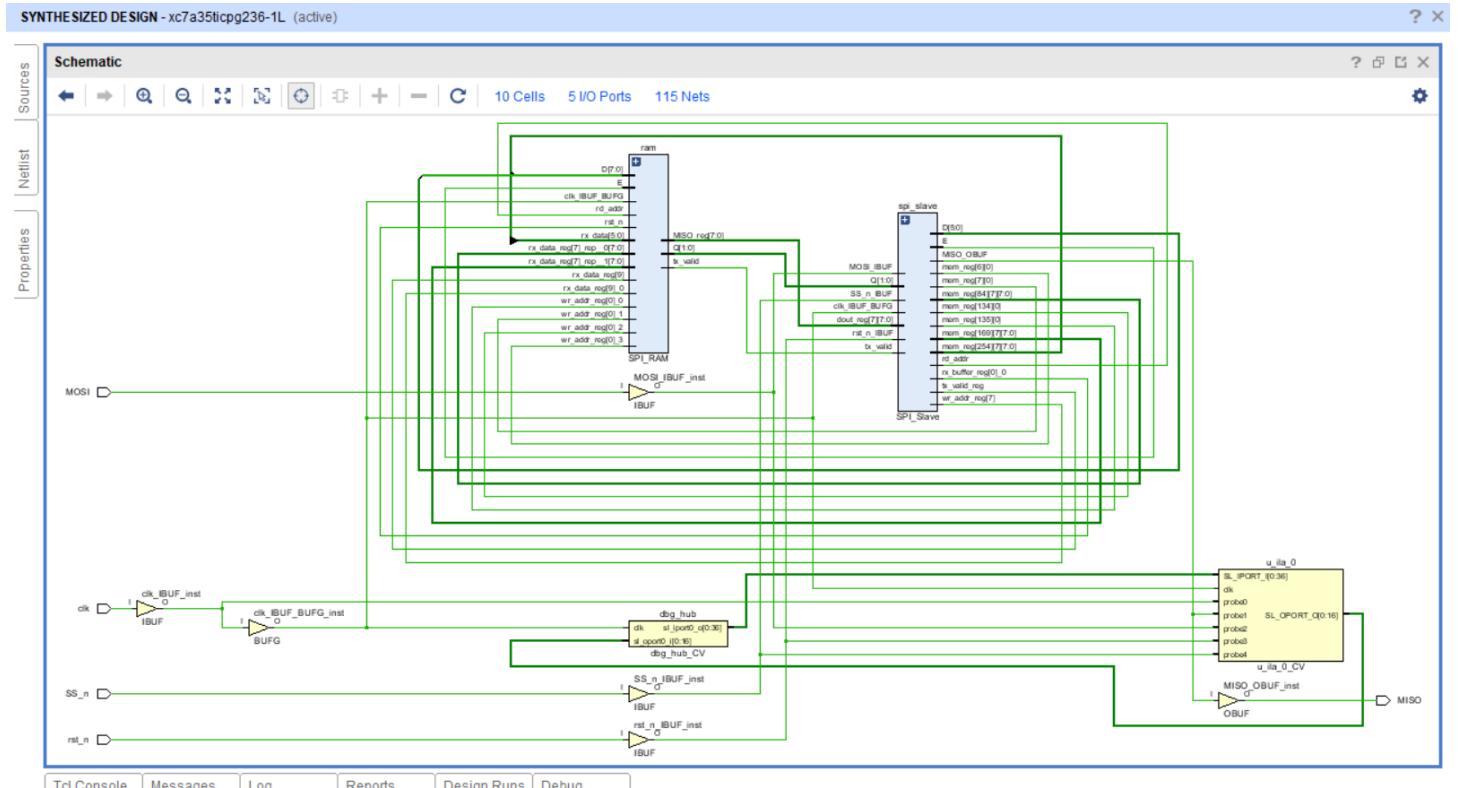


Message Tab

- ✓ Elaborated Design (3 infos)
 - ✓ General Messages (3 infos)
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - ⓘ [Project 1-236] Implementation specific constraints were found while reading constraint file [E:/Digital_Design/Project2/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xil/TopModule_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in [Xil/TopModule_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
 - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

-Synthesis Design

Schematic



Message Tab

- ✓ **Synthesized Design** (1 warning, 6 infos)
 - ✓ **General Messages** (1 warning, 6 infos)
 - ⓘ [Netlist 29-17] Analyzing 412 Unisim elements for replacement
 - ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - ⓘ [Netlist 29-101] Netlist 'TopModule' is not ideal for floorplanning, since the cellview 'SPI_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do
 - ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - ⓘ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Utilization Report

Tcl Console | Messages | Log | Reports | Design Runs | Utilization | Debug | ? | □ | X | Hierarchy

Hierarchy

Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Bonded IOB (106)	BUFGCTRL (32)
TopModule	897	2154	272	136	5	1	
dbg_hub (dbg_hub_CV)	0	0	0	0	0	0	
ram (SPI_RAM)	808	2100	272	136	0	0	
spi_slave (SPI_Slave)	89	54	0	0	0	0	
u_il_0 (u_il_0_CV)	0	0	0	0	0	0	

utilization_1

Timing Report

Tcl Console | Messages | Log | Reports | Timing | Utilization | Debug | ? | □ | X | Design Timing Summary

General Information

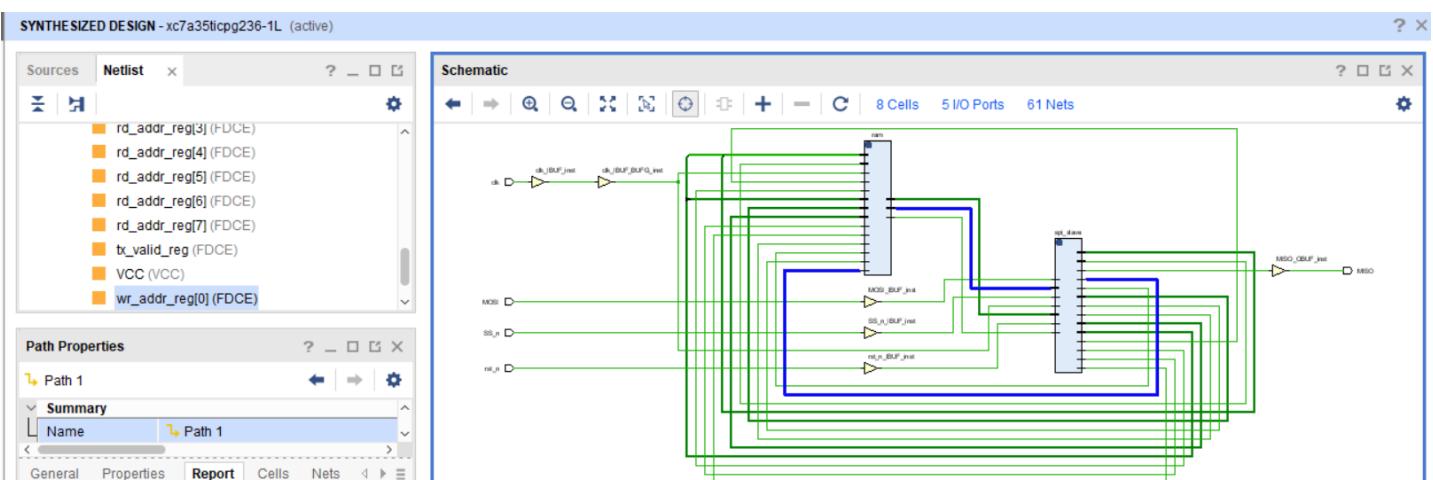
Timer Settings

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.143 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4258	Total Number of Endpoints: 4258	Total Number of Endpoints: 2155

All user specified timing constraints are met.

Critical Synthesized Path



Tcl Console | Messages | Log | Reports | Design Runs | Timing | Debug | ? | □ | X | Intra-Clock Paths - sys_clk_pin - Setup

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (4)

Intra-Clock Paths

- sys_clk_pin
- Setup 6.143 ns (10)

Name	Slack	^1	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	6.143	3	16	ram/wr_addr_reg[0]/C	ram/mem_reg[102][0]/CE	3.475	0.999	2.476	10.000	sys_clk_pin	
Path 2	6.143	3	16	ram/wr_addr_reg[0]/C	ram/mem_reg[102][1]/CE	3.475	0.999	2.476	10.000	sys_clk_pin	
Path 3	6.143	3	16	ram/wr_addr_reg[0]/C	ram/mem_reg[102][2]/CE	3.475	0.999	2.476	10.000	sys_clk_pin	
Path 4	6.143	3	16	ram/wr_addr_reg[0]/C	ram/mem_reg[102][3]/CE	3.475	0.999	2.476	10.000	sys_clk_pin	
Path 5	6.143	3	16	ram/wr_addr_reg[0]/C	ram/mem_reg[102][4]/CE	3.475	0.999	2.476	10.000	sys_clk_pin	
Path 6	6.143	3	16	ram/wr_addr_reg[0]/C	ram/mem_reg[102][5]/CE	3.475	0.999	2.476	10.000	sys_clk_pin	

Timing Summary - timing_1

Synthesis Report

SYNTHEZIZED DESIGN - xc7a35ticpg236-1L (active) ?

Schematic × synth_1_synth_synthesis_report_0 - synth_1 ×

E:/Digital_Design/VIVADO/Assignment4/project_16/project_16.rns/synth_1/TopModule.vds

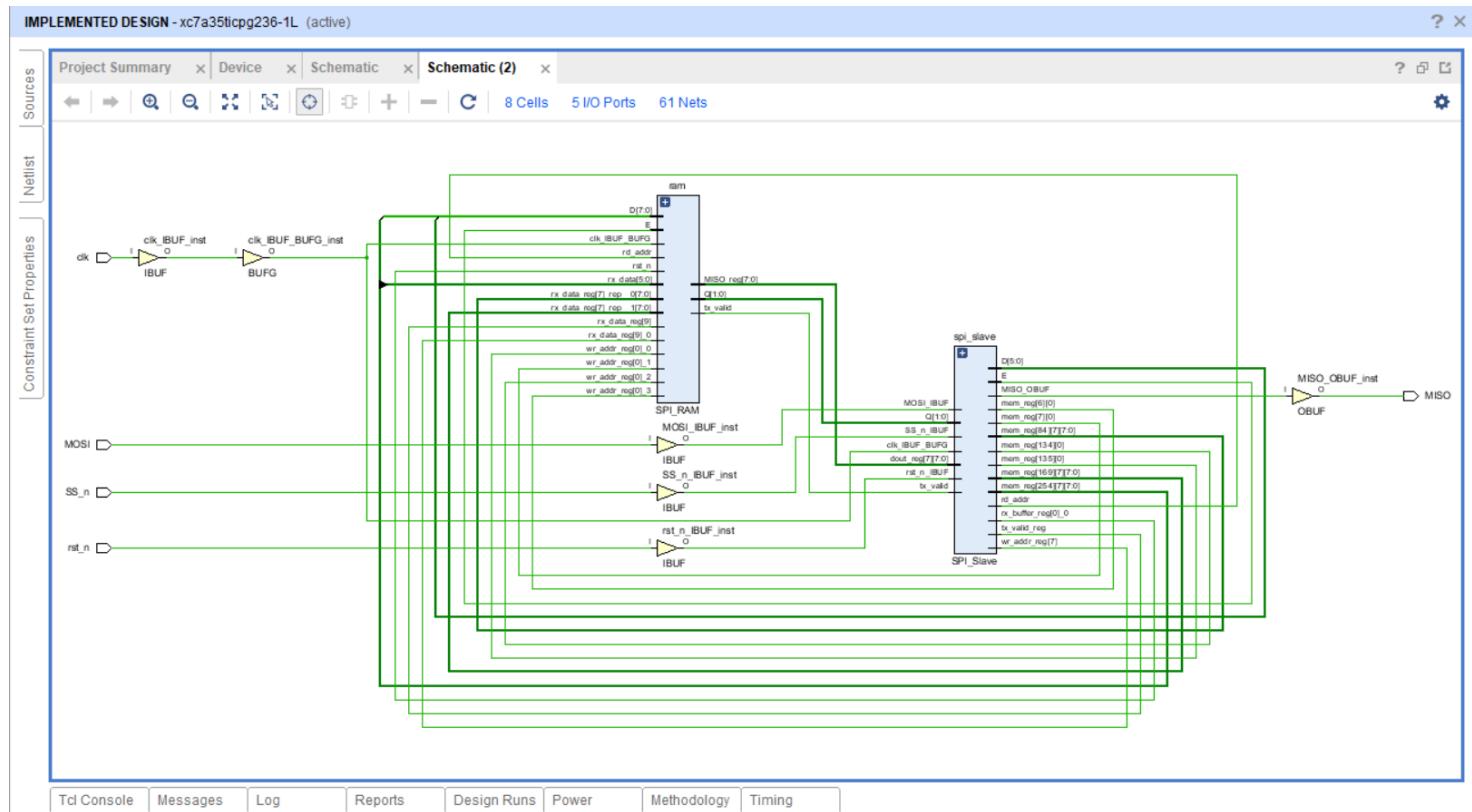
Sources | Neillist | Path Properties

gray Next Previous Highlight Match Case Whole Words 2 Match(es)

83 -----
84 Finished Loading Part and Timing Information : Time (s): cpu = 00:00:15 ; elapsed = 00:00:17 . Memory (MB): peak = 845.102 ; gain = 527.238
85 -----
86 -----
87 Start Applying 'set_property' XDC Constraints
88 -----
89 -----
90 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:15 ; elapsed = 00:00:17 . Memory (MB): peak = 845.102 ; gain = 527.238
91 -----
92 INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_Slave'
93 INFO: [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
94 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
95 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
96 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
97 INFO: [Synth 8-5544] ROM "ns0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
98 -----
99 State | New Encoding | Previous Encoding
100 -----
101 IDLE | 000 | 000
102 CHK_CMD | 001 | 001
103 READ_ADD | 011 | 100
104 READ_DATA | 010 | 011
105 WRITE | 111 | 010
106 -----
107 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_Slave'
108 -----
109 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:16 ; elapsed = 00:00:18 . Memory (MB): peak = 845.102 ; gain = 527.238
110 -----
111 -----
112 -----

-Implementation Design

Schematic



Message Tab

- ✓ Implementation (1 warning, 87 infos)
 - ✓ Design Initialization (1 warning, 7 infos)
 - ⓘ [Netlist 29-17] Analyzing 412 Unisim elements for replacement
 - ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - ⓘ [Netlist 29-101] Netlist 'TopModule' is not ideal for floorplanning, since the cellview 'SPI_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
 - ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
 - ⓘ [Device 21-403] Loading part xc7a35tci236-1L
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - ⓘ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Utilization Report

Hierarchy										
	Name	1 Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
Hierarchy										
Summary										
slice logic										
slice lut (4%)	TopModule	897	2154	272	136	782	897	50	5	1
lut as logic (4%)	ram (SPL_RAM)	808	2100	272	136	752	808	8	0	0
f8 muxes (2%)	spi_slave (SPL_Slave)	89	54	0	0	32	89	42	0	0

Timing Report

Tcl Console | Messages | Log | Reports | Design Runs | Power | Methodology | **Timing** × Utilization | ? — □

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

> Check Timing (4)

> Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

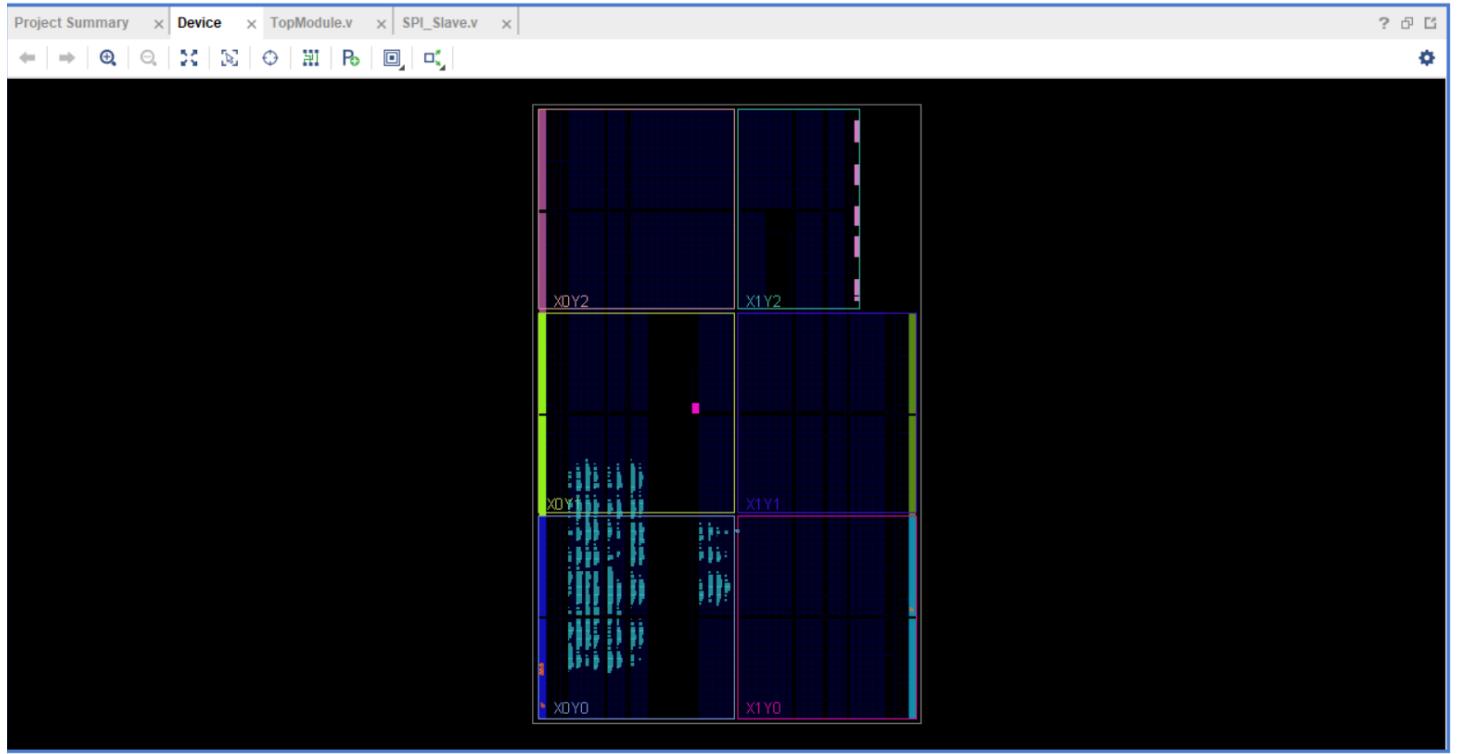
User Ignored Paths

> Unconstrained Paths

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.461 ns	Worst Hold Slack (WHS): 0.176 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 4258	Total Number of Endpoints: 4258	Total Number of Endpoints: 2155

All user specified timing constraints are met.

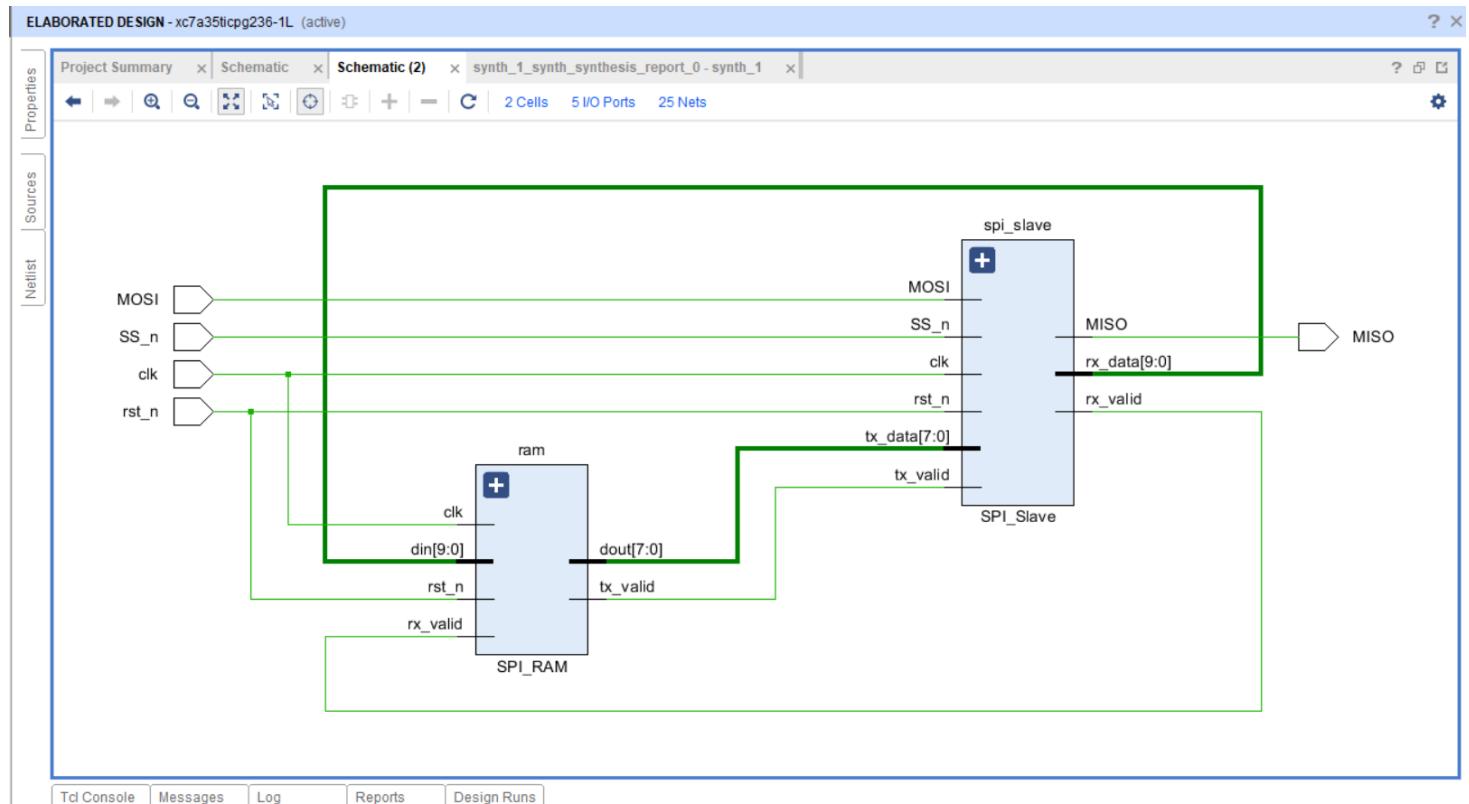
FPGA Device



3. One_hot encoding

Elaborated Design

Schematic

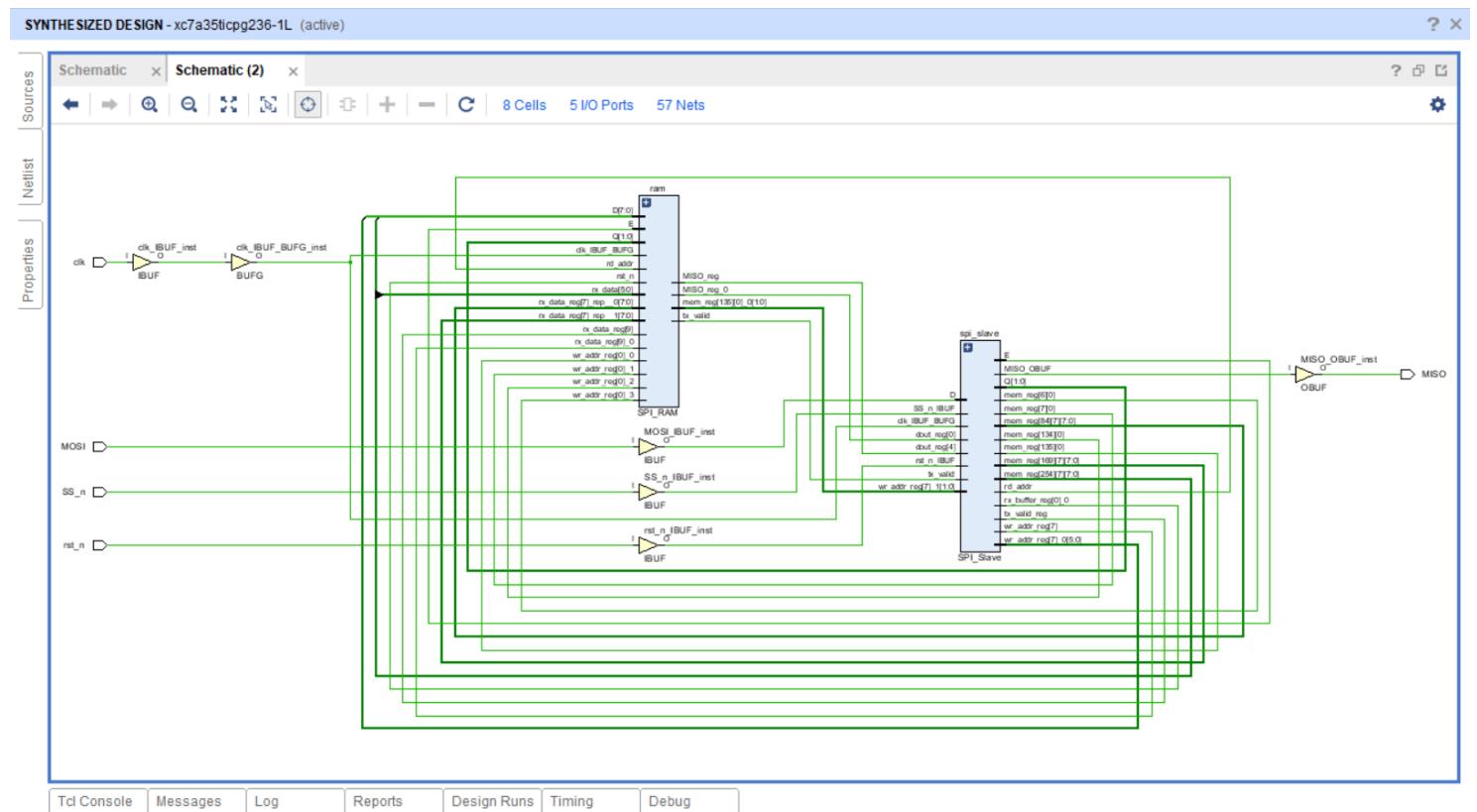


Message Tab

- ▼ Elaborated Design (2 infos)
 - ▼ General Messages (2 infos)
 - ➊ [Project 1-570] Preparing netlist for logic optimization
 - ➋ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Synthesis Design

Schematic



Message Tab

SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)

Tcl Console | **Messages** | Log | Reports | Design Runs | Timing | Debug | ? | _ | □ | X | Sources | Netlist | Properties

Search | Filter | Show All | Warning (9) | Info (323) | Status (474) | Show All | Settings

Synthesis (4 warnings, 131 infos)

- ⓘ [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
- > ⓘ [Synth 8-6157] synthesizing module 'TopModule' [[TopModule.v:1](#)] (2 more like this)
- ⓘ [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [[SPI_Slave.v:15](#)]
- ⓘ [Synth 8-155] case statement is not full and has no default [[SPI_Slave.v:97](#)]
- ⓘ [Synth 8-5788] Register mem_reg in module SPI_RAM is has both Set and reset with same priority. This may cause simulation mismatches. Consider rewriting code
- ⓘ [Synth 8-4767] Trying to implement RAM 'mem_reg' in registers. Block RAM or DRAM implementation is not possible; see log for reasons.
- > ⓘ [Synth 8-6155] done synthesizing module 'SPI_Slave' (#1) [[SPI_Slave.v:1](#)] (2 more like this)
- ⓘ [Device 21-403] Loading part xc7a35ticpg236-1L
- ⓘ [Project 1-236] Implementation specific constraints were found while reading constraint file [E:/Digital_Design/Project2/Constraints_basys3_1.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [xil/TopModule_dpropimpl.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- ⓘ [Synth 8-802] Inferred FSM for state register 'cs_reg' in module 'SPI_Slave'
- > ⓘ [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (4) smaller than threshold (5) (4 more like this)
- ⓘ [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_Slave'
- > ⓘ [Synth 8-5546] ROM "p_0_out" won't be mapped to RAM because it is too sparse (99 more like this)
- ⓘ [Common 17-14] Message 'Synth 8-5546' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set_msg_config to change the current settings.
- ⓘ [Project 1-571] Translating synthesized netlist
- ⓘ [Netlist 29-17] Analyzing 412 Unisim elements for replacement
- ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- ⓘ [Netlist 29-101] Netlist 'TopModule' is not ideal for floorplanning, since the cellview 'SPI_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
- > ⓘ [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- > ⓘ [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed. (1 more like this)
- ⓘ [Common 17-83] Releasing license: Synthesis
- ⓘ [Constraints 18-5210] No constraint will be written out.
- ⓘ [Common 17-1381] The checkpoint 'E:/Digital_Design/VIVADO/Assignment4/project_16/project_16.runs/synth_1/TopModule.dcp' has been generated.

Synthesized Design (1 warning, 5 infos)

General Messages (1 warning, 5 infos)

- ⓘ [Netlist 29-17] Analyzing 412 Unisim elements for replacement
- ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- ⓘ [Netlist 29-101] Netlist 'TopModule' is not ideal for floorplanning, since the cellview 'SPI_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
- > ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
- ⓘ [Project 1-570] Preparing netlist for logic optimization
- ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Utilization Report

Tcl Console | Messages | Log | Reports | Design Runs | **Utilization** | Timing | Debug | ? | _ | □ | X | Hierarchy

Search | Filter | **Hierarchy** | %

Name	1 Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Bonded IOB (106)	BUFGCTRL (32)
TopModule	892	2156	272	136	5	1
ram (SPI_RAM)	810	2100	272	136	0	0
spi_slave (SPI_Slave)	82	56	0	0	0	0

utilization_1

Timing Report

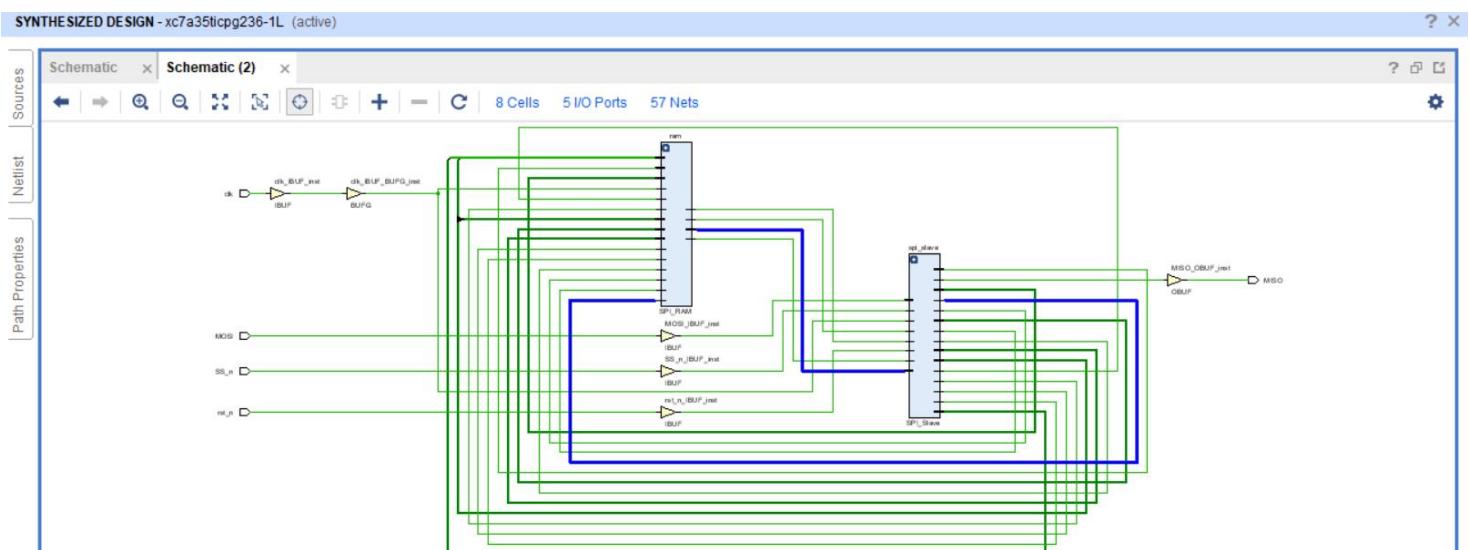
Tcl Console Messages Log Reports Design Runs Utilization Timing Debug ? - ×

Design Timing Summary

Setup			Hold			Pulse Width		
Worst Negative Slack (WNS):	6.143 ns		Worst Hold Slack (WHS):	0.142 ns		Worst Pulse Width Slack (WPWS):	4.500 ns	
Total Negative Slack (TNS):	0.000 ns		Total Hold Slack (THS):	0.000 ns		Total Pulse Width Negative Slack (TPWS):	0.000 ns	
Number of Failing Endpoints:	0		Number of Failing Endpoints:	0		Number of Failing Endpoints:	0	
Total Number of Endpoints:	4260		Total Number of Endpoints:	4260		Total Number of Endpoints:	2157	

All user specified timing constraints are met.

Critical Synthesized Path



Tcl Console Messages Log Reports Design Runs Utilization Timing Debug ? - ×

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source CI
Path 1	6.143	3	16	ram/wr_addr_reg[0]/C	ram/mem_reg[102][0]/CE	3.475	0.999	2.476	10.000	sys_clk_r
Path 2	6.143	3	16	ram/wr_addr_reg[0]/C	ram/mem_reg[102][1]/CE	3.475	0.999	2.476	10.000	sys_clk_r
Path 3	6.143	3	16	ram/wr_addr_reg[0]/C	ram/mem_reg[102][2]/CE	3.475	0.999	2.476	10.000	sys_clk_r

Synthesis Report

SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)

Schematic Sources Path Properties

synth_1_synth_synthesis_report_0 - synth_1

```

E:/Digital_Design/MIVADebug/Assignment4/project_16/project_16.runs/synth_1/TopModule.vds

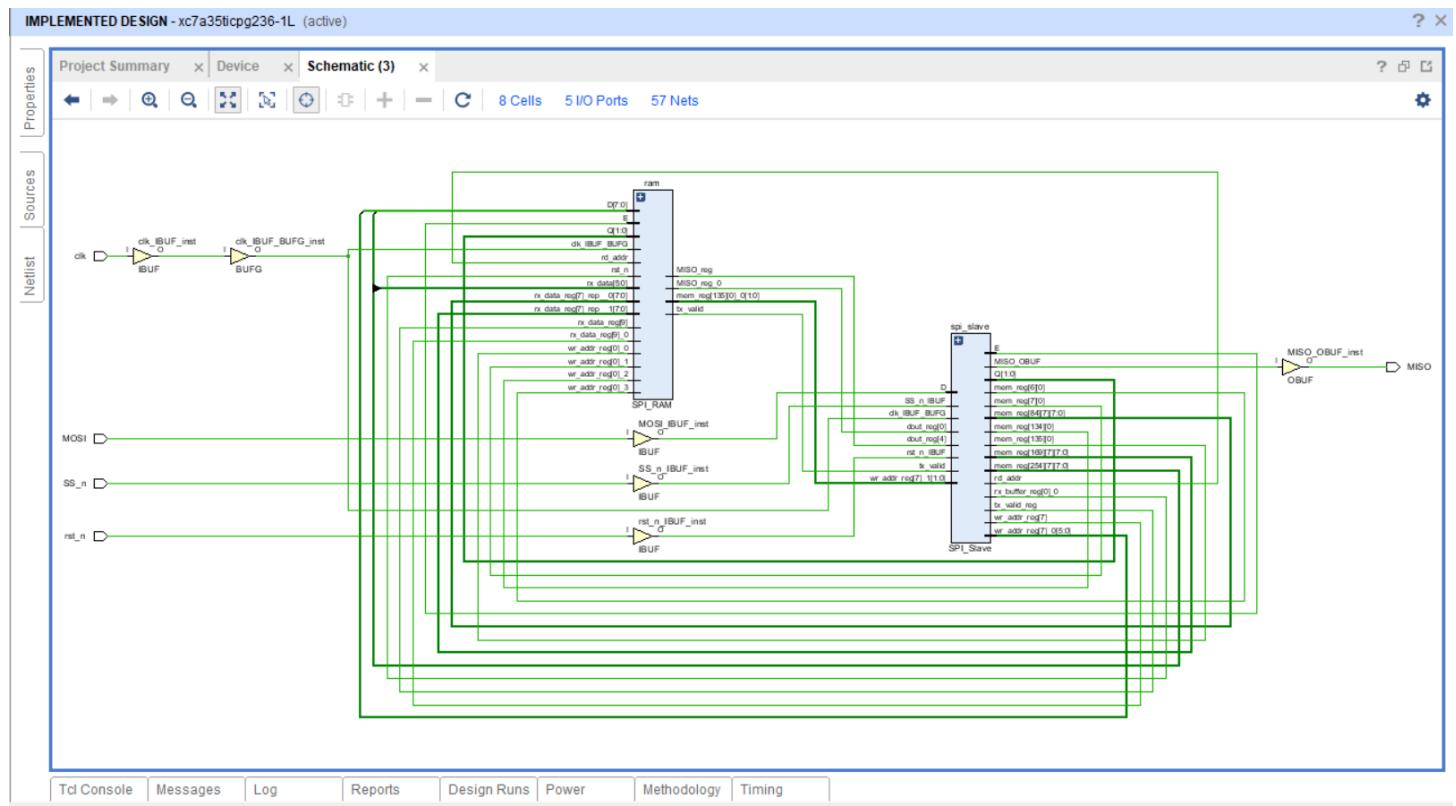
one-hot Next Previous Highlight Match Case Whole Words 1 Match(es) Read-only

85 -----
86 -----
87 Start Applying 'set_property' XDC Constraints
88 -----
89 -----
90 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:14 ; elapsed = 00:00:17 . Memory (MB): peak = 845.488 ; gain = 526.211
91 -----
92 INFO: [Synth 8-802] inferred FSR for state register 'cs_reg' in module 'SPI_Slave'
93 INFO: [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
94 INFO: [Synth 8-5544] ROM "nso" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
95 INFO: [Synth 8-5544] ROM "ne" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
96 INFO: [Synth 8-5544] ROM "ne" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
97 INFO: [Synth 8-5544] ROM "ne0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
98 -----
99 State | New Encoding | Previous Encoding
100 -----
101 IDLE | 00001 | 000
102 CHK_CMD | 00010 | 001
103 READ_ADD | 00100 | 100
104 READ_DATA | 01000 | 011
105 WRITE | 10000 | 010
106 -----
107 INFO: [Synth 8-3354] encoded FSR with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_Slave'
108 -----
109 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:15 ; elapsed = 00:00:18 . Memory (MB): peak = 845.488 ; gain = 526.211
110 -----
111 -----
112 Report RTL Partitions:
113 +-----+
<----+-----+

```

-Implementation Design

Schematic



Message Tab

- ✓ Implementation (1 warning, 90 infos)
 - ✓ Design Initialization (1 warning, 11 infos)
 - ⓘ [Netlist 29-17] Analyzing 412 Unisim elements for replacement
 - ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - ⓘ [Netlist 29-101] Netlist 'TopModule' is not ideal for floorplanning, since the cellview 'SPI_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
 - ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
 - ⓘ [Device 21-403] Loading part xc7a35tci236-1L
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - ⓘ [Timing 38-478] Restoring timing data from binary archive.
 - ⓘ [Timing 38-479] Binary timing data restore complete.
 - ⓘ [Project 1-856] Restoring constraints from binary archive.
 - ⓘ [Project 1-853] Binary constraint restore complete.
 - ⓘ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
 - ⓘ [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

- ✓ Implemented Design (1 warning, 8 infos)
 - ✓ General Messages (1 warning, 8 infos)
 - ⓘ [Netlist 29-17] Analyzing 412 Unisim elements for replacement
 - ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - ⓘ [Netlist 29-101] Netlist 'TopModule' is not ideal for floorplanning, since the cellview 'SPI_RAM' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.
 - ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - ⓘ [Timing 38-478] Restoring timing data from binary archive.
 - ⓘ [Timing 38-479] Binary timing data restore complete.
 - ⓘ [Project 1-856] Restoring constraints from binary archive.
 - ⓘ [Project 1-853] Binary constraint restore complete.

Utilization Report

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

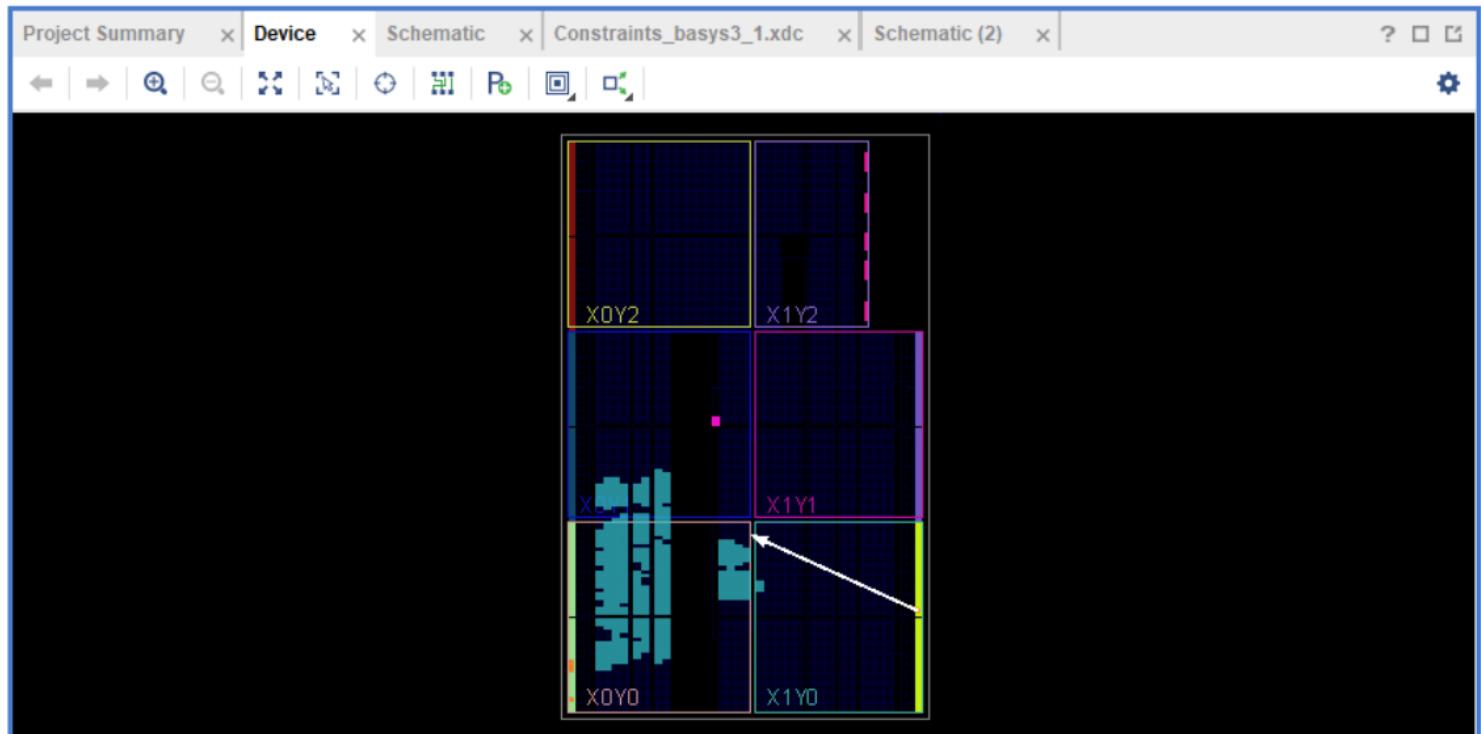
Tcl Console	Messages	Log	Reports	Design Runs	Power	Methodology	Timing	Utilization	x	?	...	Properties																																												
Hierarchy												Netlist																																												
<table border="1"> <thead> <tr> <th>Name</th><th>1</th><th>Slice LUTs (20800)</th><th>Slice Registers (41600)</th><th>F7 Muxes (16300)</th><th>F8 Muxes (8150)</th><th>Slice (8150)</th><th>LUT as Logic (20800)</th><th>LUT Flip Flop Pairs (20800)</th><th>Bonded IOB (106)</th><th>BUFGCTRL (32)</th></tr> </thead> <tbody> <tr> <td>TopModule</td><td></td><td>892</td><td>2156</td><td>272</td><td>136</td><td>754</td><td>892</td><td>54</td><td>5</td><td>1</td></tr> <tr> <td>ram (SPI_RAM)</td><td></td><td>810</td><td>2100</td><td>272</td><td>136</td><td>724</td><td>810</td><td>8</td><td>0</td><td>0</td></tr> <tr> <td>spi_slave (SPI_Slave)</td><td></td><td>82</td><td>56</td><td>0</td><td>0</td><td>34</td><td>82</td><td>45</td><td>0</td><td>0</td></tr> </tbody> </table>												Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)	TopModule		892	2156	272	136	754	892	54	5	1	ram (SPI_RAM)		810	2100	272	136	724	810	8	0	0	spi_slave (SPI_Slave)		82	56	0	0	34	82	45	0	0	
Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)																																														
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ram (SPI_RAM)		810	2100	272	136	724	810	8	0	0																																														
spi_slave (SPI_Slave)		82	56	0	0	34	82	45	0	0																																														

Timing Report

Tcl Console Messages Log Reports Design Runs Power Methodology Timing Utilization

Design Timing Summary															
General Information				Setup				Hold				Pulse Width			
Timer Settings				Worst Negative Slack (WNS): 2.847 ns				Worst Hold Slack (WHS): 0.151 ns				Worst Pulse Width Slack (WPWS): 4.500 ns			
Design Timing Summary				Total Negative Slack (TNS): 0.000 ns				Total Hold Slack (THS): 0.000 ns				Total Pulse Width Negative Slack (TPWS): 0.000 ns			
Clock Summary (1)				Number of Failing Endpoints: 0				Number of Failing Endpoints: 0				Number of Failing Endpoints: 0			
> Check Timing (4)				Total Number of Endpoints: 4260				Total Number of Endpoints: 4260				Total Number of Endpoints: 2157			
All user specified timing constraints are met.															

FPGA Device



After Comparing Setup/Hold time Slack We concluded that “One-hot” encoding is the best choice for Maximum frequency.

Successful Bitstream Generation

The screenshot displays two windows from the Vivado Design Suite. The top window is titled "Design Runs" and shows a table of completed design runs. The bottom window is titled "Messages" and shows a list of build logs.

Design Runs Table:

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Status
synth_1	constrs_1	synth_design Complete!								892	2156	0.00	0	0	8/5/25 5:35 PM	00:00:31	Vivado Syn
impl_1	constrs_1	write_bitstream Complete!	2.847	0.000	0.151	0.000	0.000	0.066	0	892	2156	0.00	0	0	8/5/25 5:36 PM	00:01:19	Vivado Imp

Messages Window:

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

- > Vivado Commands (3 infos)
- > Synthesis (4 warnings, 131 infos)
- < Implementation (2 warnings, 109 infos)
 - > Design Initialization (1 warning, 7 infos)
 - > Opt Design (24 infos)
 - > Place Design (21 infos)
 - > Route Design (35 infos)
 - > Write Bitstream (1 warning, 22 infos)
- > Implemented Design (1 warning, 9 infos)