[Year]

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Project 1

RTL Design

```
module
DSP48A1(A,B,C,D,CLK,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMO
DE,CEA,CEB,CEM,CEP,CEC,CECARRYIN,CED,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
input [17:0]A,B,D,BCIN;
input[47:0]C,PCIN;
input [7:0]OPMODE;
input
CLK,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CECAR
RYIN,CED,CEOPMODE;
output [17:0]BCOUT ;
output [47:0]PCOUT;
output reg [47:0] P;
output [35:0]M;
output reg CARRYOUT;
output  CARRYOUTF;
parameter RSTTYPE="SYNC";
parameter BINPUT="DIRECT";
parameter CARRYINSEL="OPMODE5";
parameter A0REG =0;
parameter A1REG =1;
parameter B0REG=0;
 parameter B1REG=1;
 parameter CREG=1;
 parameter DREG=1;
 parameter MREG=1;
 parameter PREG=1;
 parameter CARRYINREG=1;
 parameter CARRYOUTREG =1;
 parameter OPMODEREG=1;

reg [17:0]A0_reg,B0_reg,D_reg;
reg [47:0]C_reg ;
reg [17:0]A1_reg,B1_reg;
wire[17:0] pre_add_sub,B1;
wire [35:0] Mul_out;
reg [35:0] M_reg;
reg CYI;
wire [47:0] D_A_B_CONCATENATED,X, Z;
wire[48:0] post_add_sub;




generate
    if  (A0REG) begin
```

```
      if(RSTTYPE=="ASYNC") begin
       always@(posedge CLK, posedge RSTA)begin
       if (RSTA)
         A0_reg <=0;
       else if(CEA)
         A0_reg <=A;
       end
      end
      else
      always@(posedge CLK)begin
         if (RSTA)
         A0_reg <=0;
       else if(CEA)
         A0_reg <=A;
      end
      end
    else begin
        always@(*)begin
        A0_reg=A;
        end
     end


endgenerate

generate
    if  (B0REG)begin
      if(RSTTYPE=="ASYNC") begin
       always@(posedge CLK, posedge RSTB)begin
       if (RSTB)
         B0_reg <=0;
       else if(CEB)
         B0_reg <= (BINPUT=="CASCADE")? BCIN: B;
       end
      end
      else begin
      always@(posedge CLK)begin
         if (RSTB)
         B0_reg <=0;
       else if(CEB)
         B0_reg <= (BINPUT=="CASCADE")? BCIN: B;
      end
      end
    end
    else begin
        always@(*)begin
        B0_reg = (BINPUT=="CASCADE")? BCIN: B;
        end
     end

endgenerate

generate
    if  (CREG)begin
      if(RSTTYPE=="ASYNC") begin
```

```
       always@(posedge CLK, posedge RSTC)begin
       if (RSTC)
        C_reg <=0;
       else if(CEC)
         C_reg <=C;
       end
      end
      else begin
      always@(posedge CLK)begin
         if (RSTC)
        C_reg <=0;
       else if(CEC)
         C_reg <=C;
      end
      end
    end

    else begin
        always@(*)begin
        C_reg=C;
        end
    end


endgenerate

generate
    if  (DREG)begin
      if(RSTTYPE=="ASYNC") begin
       always@(posedge CLK, posedge RSTD)begin
       if (RSTD)
         D_reg <=0;
       else if(CED)
         D_reg <=D;
       end
      end
      else begin
      always@(posedge CLK)begin
         if (RSTD)
        D_reg <=0;
       else if(CED)
         D_reg <=D;
      end
      end
    end
    else begin
        always@(*)begin
        D_reg=D;
        end
     end
endgenerate

assign pre_add_sub = (OPMODE[6]==0)? D_reg + B0_reg : D_reg - B0_reg ;
assign B1 = (OPMODE[4]==0)? B0_reg : pre_add_sub;
assign BCOUT = B1_reg;
```

```
assign Mul_out= A1_reg * B1_reg;
assign M = M_reg;
assign D_A_B_CONCATENATED = {D[11:0],A[17:0],B[17:0]};
assign post_add_sub = (OPMODE[7]==0)? (Z+X+CYI) : (Z-(X+CYI)) ;
assign CARRYOUTF = CARRYOUT;
assign PCOUT = P;


generate
    if  (B1REG)begin
      if(RSTTYPE=="ASYNC") begin
       always@(posedge CLK, posedge RSTB)begin
       if (RSTB)
         B1_reg <=0;
       else if(CEB)
         B1_reg <= B1;
       end
      end
      else begin
      always@(posedge CLK)begin
         if (RSTB)
         B1_reg <=0;
       else if(CEB)
         B1_reg <= B1;
      end
      end
    end
    else begin
        always@(*)begin
        B1_reg = B1;
        end
     end
endgenerate

generate
    if  (A1REG)begin
      if(RSTTYPE=="ASYNC") begin
       always@(posedge CLK, posedge RSTA)begin
       if (RSTA)
         A1_reg <=0;
       else if(CEA)
         A1_reg <=A0_reg;
       end
      end
      else begin
      always@(posedge CLK)begin
         if (RSTA)
         A1_reg <=0;
       else if(CEA)
         A1_reg <=A0_reg;
      end
      end
    end
    else begin
        always@(*)begin
```

```
        A1_reg = A0_reg;
     end
    end

endgenerate


generate
    if  (MREG)begin
      if(RSTTYPE=="ASYNC") begin
       always@(posedge CLK, posedge RSTM)begin
       if (RSTM)
         M_reg <=0;
       else if(CEM)
         M_reg <= Mul_out;
       end
      end
      else begin
      always@(posedge CLK)begin
         if (RSTM)
         M_reg <=0;
       else if(CEM)
         M_reg <= Mul_out;
      end
      end
    end
    else begin
        always@(*)begin
        M_reg = Mul_out;
        end
     end
endgenerate

generate
    if  (CARRYINREG)begin
      if(RSTTYPE=="ASYNC") begin
       always@(posedge CLK, posedge RSTCARRYIN)begin
       if (RSTCARRYIN)
        CYI <=0;
       else if(CECARRYIN)
         CYI <= (CARRYINSEL=="CARRYIN")? CARRYIN: OPMODE[5];
       end
      end
      else begin
      always@(posedge CLK)begin
         if (RSTCARRYIN)
         CYI <=0;
       else if(CECARRYIN)
         CYI <= (CARRYINSEL=="CARRYIN")? CARRYIN: OPMODE[5];
      end
      end
    end
    else begin
        always@(*)begin
        CYI = (CARRYINSEL=="CARRYIN")? CARRYIN: OPMODE[5];
```

```
        end
     end
endgenerate

assign X =(OPMODE[1:0]==2'b0)? 48'b0:
          (OPMODE[1:0]==2'b01)?  M_reg:
          (OPMODE[1:0]==2'b10)?  P:
          (OPMODE[1:0]==2'b11)?  D_A_B_CONCATENATED:48'b0;

assign Z =(OPMODE[3:2]==2'b0)? 48'b0:
          (OPMODE[3:2]==2'b01)?  PCIN:
          (OPMODE[3:2]==2'b10)?  P:
          (OPMODE[3:2]==2'b11)?  C_reg:48'b0;
generate
    if  (PREG)begin
      if(RSTTYPE=="ASYNC") begin
       always@(posedge CLK, posedge RSTP)begin
       if (RSTP)
         P<=0;
       else if(CEP)
         P <= post_add_sub;
       end
      end
      else begin
      always@(posedge CLK)begin
         if (RSTP)
         P <=0;
       else if(CEP)
         P <= post_add_sub;
      end
      end
    end
    else begin
        always@(*)begin
        P = post_add_sub;
        end
     end
endgenerate

generate
    if  (CARRYOUTREG)begin
      if(RSTTYPE=="ASYNC") begin
       always@(posedge CLK, posedge RSTCARRYIN)begin
       if (RSTCARRYIN)
         CARRYOUT<=0;
       else if(CECARRYIN)
         CARRYOUT <= post_add_sub[48];
       end
      end
      else begin
      always@(posedge CLK)begin
         if (RSTCARRYIN)
         CARRYOUT <=0;
       else if(CECARRYIN)
         CARRYOUT <= post_add_sub[48];
```

```
      end
      end
    end
    else begin
        always@(*)begin
        CARRYOUT = post_add_sub[48];
        end
     end
endgenerate
endmodule
```

Testbench code

```
module DSP48A1_tb();

reg  [17:0]A,B,D,BCIN;
reg  [47:0]C,PCIN;
reg  [7:0]OPMODE;
reg
CLK,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CECAR
RYIN,CED,CEOPMODE;
wire  [17:0]BCOUT ;
wire  [47:0]PCOUT;
wire [47:0] P;
wire [35:0]M;
wire CARRYOUT;
wire  CARRYOUTF;

DSP48A1
dut(A,B,C,D,CLK,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,C
EA,CEB,CEM,CEP,CEC,CECARRYIN,CED,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);

initial begin
    CLK=0;
    forever
    #1 CLK=~CLK;
end
initial begin
    //reset
    RSTA = 1;RSTB = 1;RSTC = 1;RSTCARRYIN = 1;
    RSTD = 1;RSTM = 1; RSTOPMODE = 1;RSTP = 1;

    A=$random; B=$random; D=$random;
    BCIN=$random; C=$random;PCIN=$random;CARRYIN=$random;

    CEA=$random;CEB=$random;CEM=$random; CEP=$random;CEC=$random;
    CECARRYIN=$random;CED=$random;CEOPMODE=$random;

@(negedge CLK);
  if (P!=0 || M!=0 || CARRYOUT!=0 || PCOUT!=0 || BCOUT!=0 || CARRYOUTF!=0) begin
   $display("reset test failed" );
   $stop;
```

```
  end

    RSTA =0; RSTB = 0; RSTC = 0; RSTCARRYIN = 0;
    RSTD = 0;RSTM = 0;RSTOPMODE = 0;RSTP = 0;

    CEA=1;CEB=1;CEM=1;CEP=1;
    CEC=1; CECARRYIN=1; CED=1; CEOPMODE=1;

//path1
OPMODE=8'b11011101;
A=20; B=10; C=350; D=25;
BCIN=$random; PCIN=$random; CARRYIN=$random;

repeat(4)@(negedge CLK);
if ( P!='h32 || PCOUT!='h32 || BCOUT!='hf || M!='h12c || CARRYOUT!=0 || CARRYOUTF != 0 )
begin
   $display("pre/post-subtractor test failed" );
   $stop;
end

//path2
OPMODE=8'b00010000;
A=20; B=10; C=350; D=25;
BCIN=$random; PCIN=$random; CARRYIN=$random;

repeat(3)@(negedge CLK);
if(BCOUT!='h23 || M!='h2bc || P!=0 || PCOUT!=0)begin
   $display("pre/post-adition test failed" );
   $stop;
end

//path3
OPMODE=8'b00001010;

repeat(3)@(negedge CLK);
if(BCOUT!='ha || M!='hc8 || P!=0 || PCOUT!=0)begin
   $display("post-adition test failed" );
   $stop;
end

//path4
OPMODE=8'b00001010;
A=5; B=6; C=350; D=25; PCIN=3000;
BCIN=$random; CARRYIN=$random;

repeat(3)@(negedge CLK);
if(BCOUT!='h6 || M!='h1e || P!='hfe6fffec0bb1 || PCOUT!='hfe6fffec0bb1 || CARRYOUT!=1 ||
CARRYOUTF=1)begin
   $display("post-subtraction test failed" );
   $stop;
end

$stop;

end
```

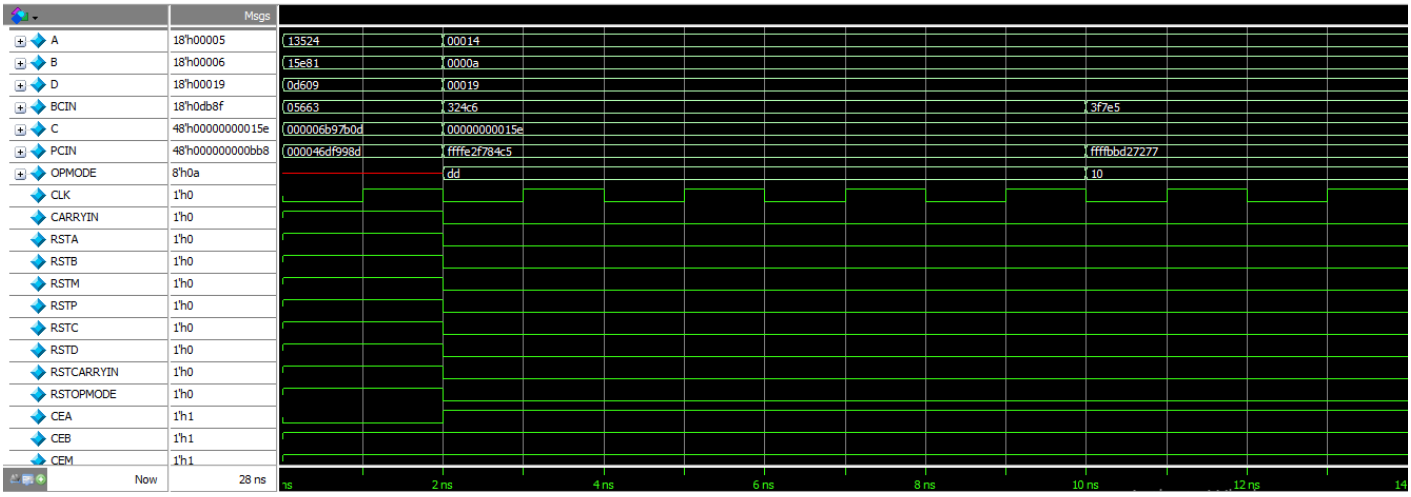
```
endmodule
```

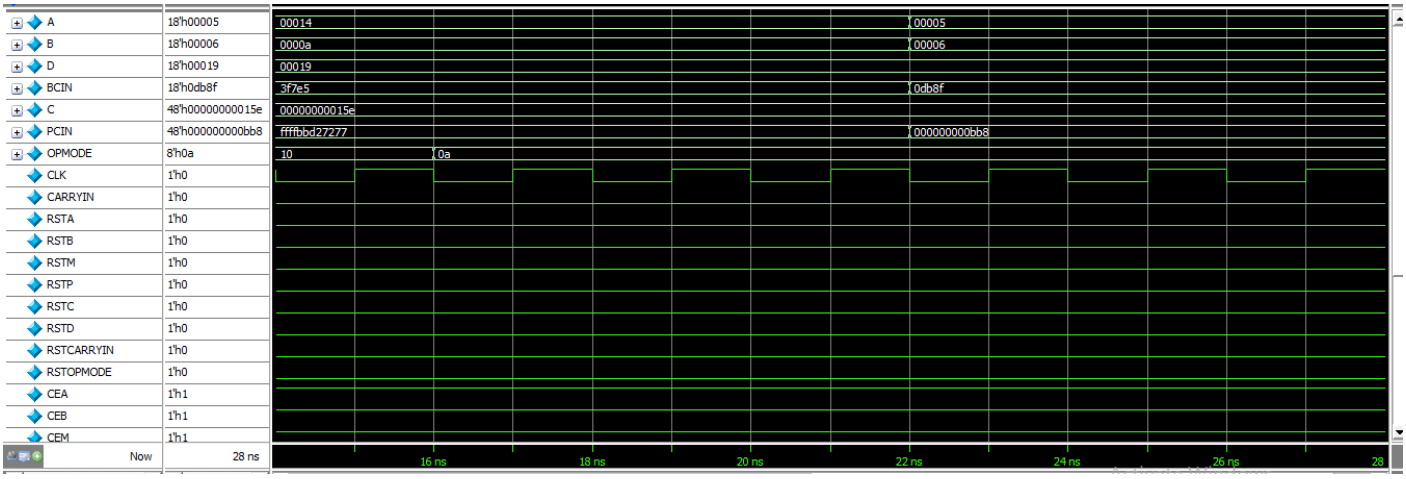
DO file

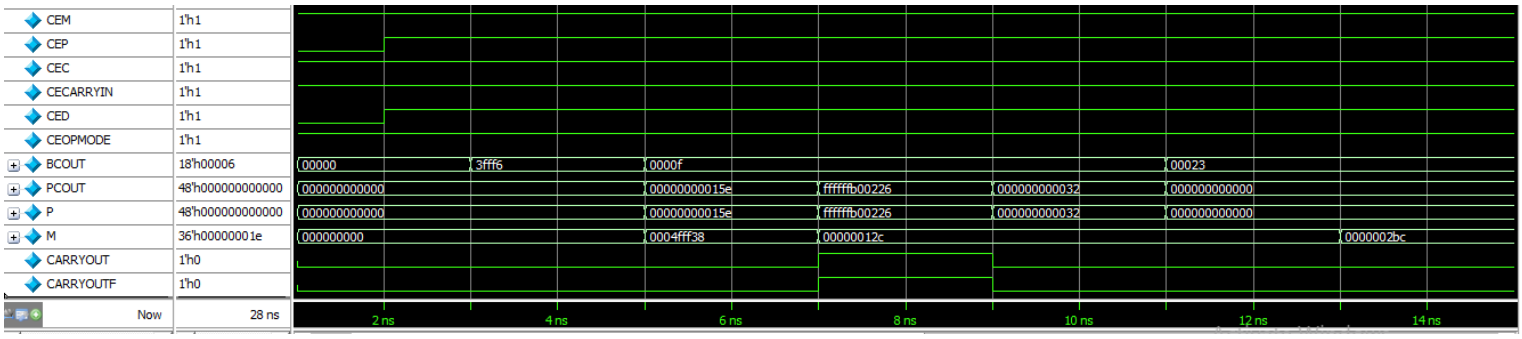
run.do

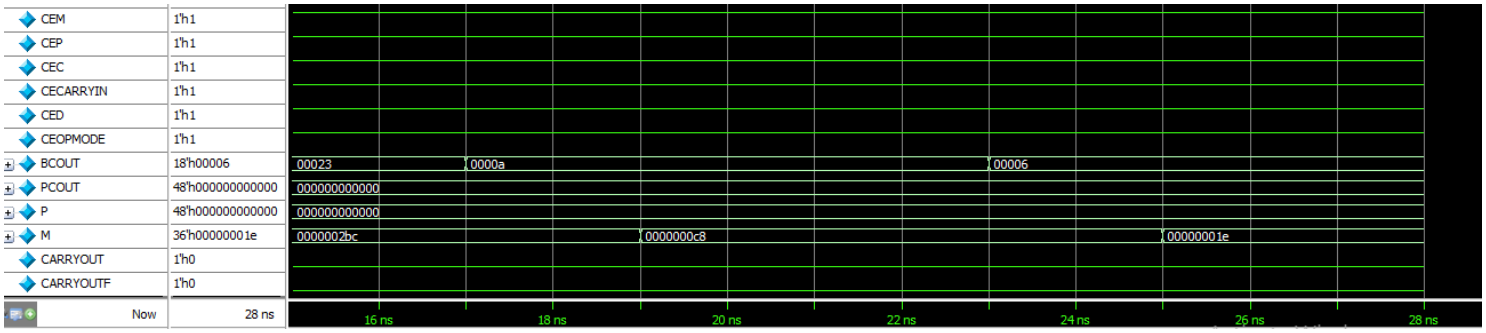
```
vlib work
vlog p1.v p1_tb.v
vsim -voptargs=+acc work.DSP48A1_tb
add wave *
run -all
#quit -simS
```

Questasim snippets









Constraints file

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level
signal names in the project

## Clock signal
set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports CLK]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports
CLK]


## Switches
#set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports {sw[0]}]
#set_property -dict { PACKAGE_PIN V16   IOSTANDARD LVCMOS33 } [get_ports {sw[1]}]
#set_property -dict { PACKAGE_PIN W16   IOSTANDARD LVCMOS33 } [get_ports {sw[2]}]
#set_property -dict { PACKAGE_PIN W17   IOSTANDARD LVCMOS33 } [get_ports {sw[3]}]
#set_property -dict { PACKAGE_PIN W15   IOSTANDARD LVCMOS33 } [get_ports {sw[4]}]
#set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 } [get_ports {sw[5]}]
#set_property -dict { PACKAGE_PIN W14   IOSTANDARD LVCMOS33 } [get_ports {sw[6]}]
#set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCMOS33 } [get_ports {sw[7]}]
#set_property -dict { PACKAGE_PIN V2    IOSTANDARD LVCMOS33 } [get_ports {sw[8]}]
#set_property -dict { PACKAGE_PIN T3    IOSTANDARD LVCMOS33 } [get_ports {sw[9]}]
#set_property -dict { PACKAGE_PIN T2    IOSTANDARD LVCMOS33 } [get_ports {sw[10]}]
#set_property -dict { PACKAGE_PIN R3    IOSTANDARD LVCMOS33 } [get_ports {sw[11]}]
#set_property -dict { PACKAGE_PIN W2    IOSTANDARD LVCMOS33 } [get_ports {sw[12]}]
```

```
#set_property -dict { PACKAGE_PIN U1    IOSTANDARD LVCMOS33 } [get_ports {sw[13]}]
#set_property -dict { PACKAGE_PIN T1    IOSTANDARD LVCMOS33 } [get_ports {sw[14]}]
#set_property -dict { PACKAGE_PIN R2    IOSTANDARD LVCMOS33 } [get_ports {sw[15]}]


## LEDs
#set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports {led[0]}]
#set_property -dict { PACKAGE_PIN E19   IOSTANDARD LVCMOS33 } [get_ports {led[1]}]
#set_property -dict { PACKAGE_PIN U19   IOSTANDARD LVCMOS33 } [get_ports {led[2]}]
#set_property -dict { PACKAGE_PIN V19   IOSTANDARD LVCMOS33 } [get_ports {led[3]}]
#set_property -dict { PACKAGE_PIN W18   IOSTANDARD LVCMOS33 } [get_ports {led[4]}]
#set_property -dict { PACKAGE_PIN U15   IOSTANDARD LVCMOS33 } [get_ports {led[5]}]
#set_property -dict { PACKAGE_PIN U14   IOSTANDARD LVCMOS33 } [get_ports {led[6]}]
#set_property -dict { PACKAGE_PIN V14   IOSTANDARD LVCMOS33 } [get_ports {led[7]}]
#set_property -dict { PACKAGE_PIN V13   IOSTANDARD LVCMOS33 } [get_ports {led[8]}]
#set_property -dict { PACKAGE_PIN V3    IOSTANDARD LVCMOS33 } [get_ports {led[9]}]
#set_property -dict { PACKAGE_PIN W3    IOSTANDARD LVCMOS33 } [get_ports {led[10]}]
#set_property -dict { PACKAGE_PIN U3    IOSTANDARD LVCMOS33 } [get_ports {led[11]}]
#set_property -dict { PACKAGE_PIN P3    IOSTANDARD LVCMOS33 } [get_ports {led[12]}]
#set_property -dict { PACKAGE_PIN N3    IOSTANDARD LVCMOS33 } [get_ports {led[13]}]
#set_property -dict { PACKAGE_PIN P1    IOSTANDARD LVCMOS33 } [get_ports {led[14]}]
#set_property -dict { PACKAGE_PIN L1    IOSTANDARD LVCMOS33 } [get_ports {led[15]}]


##7 Segment Display
#set_property -dict { PACKAGE_PIN W7   IOSTANDARD LVCMOS33 } [get_ports {seg[0]}]
#set_property -dict { PACKAGE_PIN W6   IOSTANDARD LVCMOS33 } [get_ports {seg[1]}]
#set_property -dict { PACKAGE_PIN U8   IOSTANDARD LVCMOS33 } [get_ports {seg[2]}]
#set_property -dict { PACKAGE_PIN V8   IOSTANDARD LVCMOS33 } [get_ports {seg[3]}]
#set_property -dict { PACKAGE_PIN U5   IOSTANDARD LVCMOS33 } [get_ports {seg[4]}]
#set_property -dict { PACKAGE_PIN V5   IOSTANDARD LVCMOS33 } [get_ports {seg[5]}]
#set_property -dict { PACKAGE_PIN U7   IOSTANDARD LVCMOS33 } [get_ports {seg[6]}]

#set_property -dict { PACKAGE_PIN V7   IOSTANDARD LVCMOS33 } [get_ports dp]

#set_property -dict { PACKAGE_PIN U2   IOSTANDARD LVCMOS33 } [get_ports {an[0]}]
#set_property -dict { PACKAGE_PIN U4   IOSTANDARD LVCMOS33 } [get_ports {an[1]}]
#set_property -dict { PACKAGE_PIN V4   IOSTANDARD LVCMOS33 } [get_ports {an[2]}]
#set_property -dict { PACKAGE_PIN W4   IOSTANDARD LVCMOS33 } [get_ports {an[3]}]


##Buttons
# set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports rst]
#set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports btnU]
#set_property -dict { PACKAGE_PIN W19   IOSTANDARD LVCMOS33 } [get_ports btnL]
#set_property -dict { PACKAGE_PIN T17   IOSTANDARD LVCMOS33 } [get_ports btnR]
#set_property -dict { PACKAGE_PIN U17   IOSTANDARD LVCMOS33 } [get_ports btnD]


##Pmod Header JA
#set_property -dict { PACKAGE_PIN J1   IOSTANDARD LVCMOS33 } [get_ports {JA[0]}];#Sch
name = JA1
#set_property -dict { PACKAGE_PIN L2   IOSTANDARD LVCMOS33 } [get_ports {JA[1]}];#Sch
name = JA2
```

```
#set_property -dict { PACKAGE_PIN J2   IOSTANDARD LVCMOS33 } [get_ports {JA[2]}];#Sch
name = JA3
#set_property -dict { PACKAGE_PIN G2   IOSTANDARD LVCMOS33 } [get_ports {JA[3]}];#Sch
name = JA4
#set_property -dict { PACKAGE_PIN H1   IOSTANDARD LVCMOS33 } [get_ports {JA[4]}];#Sch
name = JA7
#set_property -dict { PACKAGE_PIN K2   IOSTANDARD LVCMOS33 } [get_ports {JA[5]}];#Sch
name = JA8
#set_property -dict { PACKAGE_PIN H2   IOSTANDARD LVCMOS33 } [get_ports {JA[6]}];#Sch
name = JA9
#set_property -dict { PACKAGE_PIN G3   IOSTANDARD LVCMOS33 } [get_ports {JA[7]}];#Sch
name = JA10

##Pmod Header JB
#set_property -dict { PACKAGE_PIN A14   IOSTANDARD LVCMOS33 } [get_ports {JB[0]}];#Sch
name = JB1
#set_property -dict { PACKAGE_PIN A16   IOSTANDARD LVCMOS33 } [get_ports {JB[1]}];#Sch
name = JB2
#set_property -dict { PACKAGE_PIN B15   IOSTANDARD LVCMOS33 } [get_ports {JB[2]}];#Sch
name = JB3
#set_property -dict { PACKAGE_PIN B16   IOSTANDARD LVCMOS33 } [get_ports {JB[3]}];#Sch
name = JB4
#set_property -dict { PACKAGE_PIN A15   IOSTANDARD LVCMOS33 } [get_ports {JB[4]}];#Sch
name = JB7
#set_property -dict { PACKAGE_PIN A17   IOSTANDARD LVCMOS33 } [get_ports {JB[5]}];#Sch
name = JB8
#set_property -dict { PACKAGE_PIN C15   IOSTANDARD LVCMOS33 } [get_ports {JB[6]}];#Sch
name = JB9
#set_property -dict { PACKAGE_PIN C16   IOSTANDARD LVCMOS33 } [get_ports {JB[7]}];#Sch
name = JB10

##Pmod Header JC
#set_property -dict { PACKAGE_PIN K17   IOSTANDARD LVCMOS33 } [get_ports {JC[0]}];#Sch
name = JC1
#set_property -dict { PACKAGE_PIN M18   IOSTANDARD LVCMOS33 } [get_ports {JC[1]}];#Sch
name = JC2
#set_property -dict { PACKAGE_PIN N17   IOSTANDARD LVCMOS33 } [get_ports {JC[2]}];#Sch
name = JC3
#set_property -dict { PACKAGE_PIN P18   IOSTANDARD LVCMOS33 } [get_ports {JC[3]}];#Sch
name = JC4
#set_property -dict { PACKAGE_PIN L17   IOSTANDARD LVCMOS33 } [get_ports {JC[4]}];#Sch
name = JC7
#set_property -dict { PACKAGE_PIN M19   IOSTANDARD LVCMOS33 } [get_ports {JC[5]}];#Sch
name = JC8
#set_property -dict { PACKAGE_PIN P17   IOSTANDARD LVCMOS33 } [get_ports {JC[6]}];#Sch
name = JC9
#set_property -dict { PACKAGE_PIN R18   IOSTANDARD LVCMOS33 } [get_ports {JC[7]}];#Sch
name = JC10

##Pmod Header JXADC
#set_property -dict { PACKAGE_PIN J3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[0]}];#Sch
name = XA1_P
#set_property -dict { PACKAGE_PIN L3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[1]}];#Sch
name = XA2_P
```

```
#set_property -dict { PACKAGE_PIN M2   IOSTANDARD LVCMOS33 } [get_ports {JXADC[2]}];#Sch
name = XA3_P
#set_property -dict { PACKAGE_PIN N2   IOSTANDARD LVCMOS33 } [get_ports {JXADC[3]}];#Sch
name = XA4_P
#set_property -dict { PACKAGE_PIN K3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[4]}];#Sch
name = XA1_N
#set_property -dict { PACKAGE_PIN M3   IOSTANDARD LVCMOS33 } [get_ports {JXADC[5]}];#Sch
name = XA2_N
#set_property -dict { PACKAGE_PIN M1   IOSTANDARD LVCMOS33 } [get_ports {JXADC[6]}];#Sch
name = XA3_N
#set_property -dict { PACKAGE_PIN N1   IOSTANDARD LVCMOS33 } [get_ports {JXADC[7]}];#Sch
name = XA4_N


##VGA Connector
#set_property -dict { PACKAGE_PIN G19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[0]}]
#set_property -dict { PACKAGE_PIN H19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[1]}]
#set_property -dict { PACKAGE_PIN J19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[2]}]
#set_property -dict { PACKAGE_PIN N19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[3]}]
#set_property -dict { PACKAGE_PIN N18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[0]}]
#set_property -dict { PACKAGE_PIN L18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[1]}]
#set_property -dict { PACKAGE_PIN K18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[2]}]
#set_property -dict { PACKAGE_PIN J18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[3]}]
#set_property -dict { PACKAGE_PIN J17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[0]}]
#set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[1]}]
#set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[2]}]
#set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [get_ports {vgaGreen[3]}]
#set_property -dict { PACKAGE_PIN P19   IOSTANDARD LVCMOS33 } [get_ports Hsync]
#set_property -dict { PACKAGE_PIN R19   IOSTANDARD LVCMOS33 } [get_ports Vsync]


##USB-RS232 Interface
#set_property -dict { PACKAGE_PIN B18   IOSTANDARD LVCMOS33 } [get_ports RsRx]
#set_property -dict { PACKAGE_PIN A18   IOSTANDARD LVCMOS33 } [get_ports RsTx]


##USB HID (PS/2)
#set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33   PULLUP true } [get_ports
PS2Clk]
#set_property -dict { PACKAGE_PIN B17   IOSTANDARD LVCMOS33   PULLUP true } [get_ports
PS2Data]


##Quad SPI Flash
##Note that CCLK_0 cannot be placed in 7 series devices. You can access it using the
##STARTUPE2 primitive.
#set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[0]}]
#set_property -dict { PACKAGE_PIN D19   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[1]}]
#set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[2]}]
#set_property -dict { PACKAGE_PIN F18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[3]}]
#set_property -dict { PACKAGE_PIN K19   IOSTANDARD LVCMOS33 } [get_ports QspiCSn]


## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
```

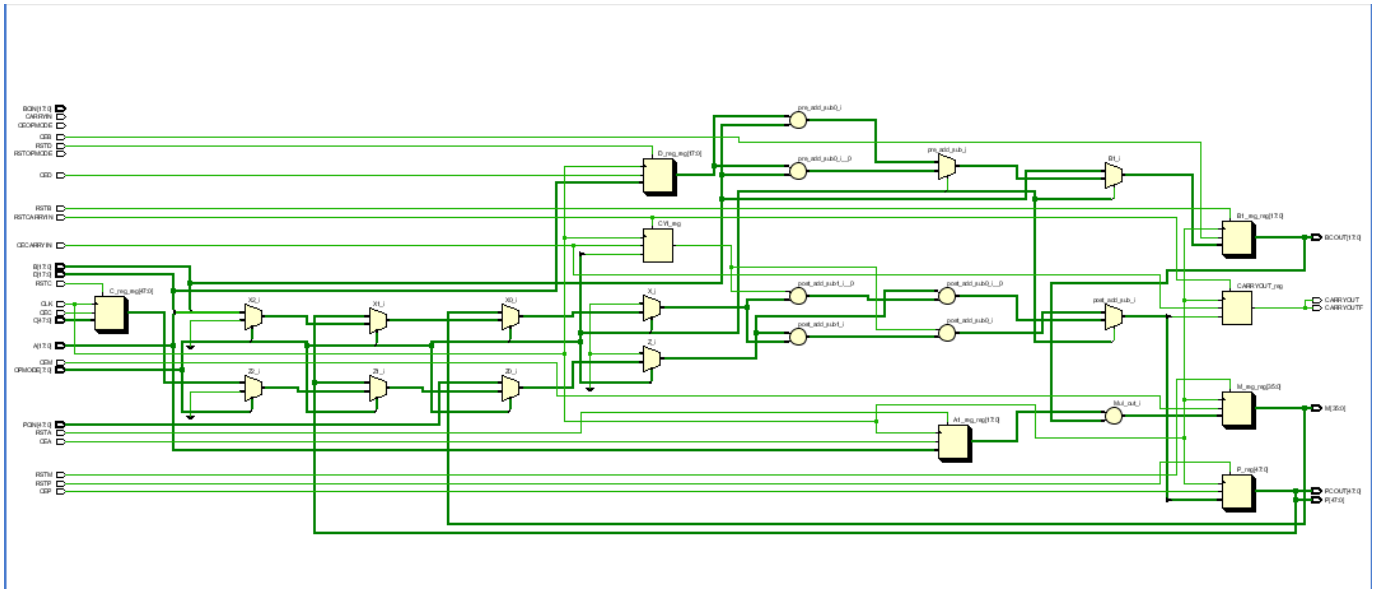
```
set_property CFGBVS VCCO [current_design]

## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]

create_debug_core u_ila_0 ila
set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
set_property C_TRIGIN_EN false [get_debug_cores u_ila_0]
set_property C_TRIGOUT_EN false [get_debug_cores u_ila_0]
set_property port_width 1 [get_debug_ports u_ila_0/clk]
connect_debug_port u_ila_0/clk [get_nets [list CLK_IBUF_BUFG]]
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
set_property port_width 18 [get_debug_ports u_ila_0/probe0]
connect_debug_port u_ila_0/probe0 [get_nets [list {A_IBUF[0]} {A_IBUF[1]} {A_IBUF[2]}
{A_IBUF[3]} {A_IBUF[4]} {A_IBUF[5]} {A_IBUF[6]} {A_IBUF[7]} {A_IBUF[8]} {A_IBUF[9]}
{A_IBUF[10]} {A_IBUF[11]} {A_IBUF[12]} {A_IBUF[13]} {A_IBUF[14]} {A_IBUF[15]}
{A_IBUF[16]} {A_IBUF[17]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
set_property port_width 48 [get_debug_ports u_ila_0/probe1]
connect_debug_port u_ila_0/probe1 [get_nets [list {P_OBUF[0]} {P_OBUF[1]} {P_OBUF[2]}
{P_OBUF[3]} {P_OBUF[4]} {P_OBUF[5]} {P_OBUF[6]} {P_OBUF[7]} {P_OBUF[8]} {P_OBUF[9]}
{P_OBUF[10]} {P_OBUF[11]} {P_OBUF[12]} {P_OBUF[13]} {P_OBUF[14]} {P_OBUF[15]}
{P_OBUF[16]} {P_OBUF[17]} {P_OBUF[18]} {P_OBUF[19]} {P_OBUF[20]} {P_OBUF[21]}
{P_OBUF[22]} {P_OBUF[23]} {P_OBUF[24]} {P_OBUF[25]} {P_OBUF[26]} {P_OBUF[27]}
{P_OBUF[28]} {P_OBUF[29]} {P_OBUF[30]} {P_OBUF[31]} {P_OBUF[32]} {P_OBUF[33]}
{P_OBUF[34]} {P_OBUF[35]} {P_OBUF[36]} {P_OBUF[37]} {P_OBUF[38]} {P_OBUF[39]}
{P_OBUF[40]} {P_OBUF[41]} {P_OBUF[42]} {P_OBUF[43]} {P_OBUF[44]} {P_OBUF[45]}
{P_OBUF[46]} {P_OBUF[47]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
set_property port_width 48 [get_debug_ports u_ila_0/probe2]
connect_debug_port u_ila_0/probe2 [get_nets [list {C_IBUF[0]} {C_IBUF[1]} {C_IBUF[2]}
{C_IBUF[3]} {C_IBUF[4]} {C_IBUF[5]} {C_IBUF[6]} {C_IBUF[7]} {C_IBUF[8]} {C_IBUF[9]}
{C_IBUF[10]} {C_IBUF[11]} {C_IBUF[12]} {C_IBUF[13]} {C_IBUF[14]} {C_IBUF[15]}
{C_IBUF[16]} {C_IBUF[17]} {C_IBUF[18]} {C_IBUF[19]} {C_IBUF[20]} {C_IBUF[21]}
{C_IBUF[22]} {C_IBUF[23]} {C_IBUF[24]} {C_IBUF[25]} {C_IBUF[26]} {C_IBUF[27]}
{C_IBUF[28]} {C_IBUF[29]} {C_IBUF[30]} {C_IBUF[31]} {C_IBUF[32]} {C_IBUF[33]}
{C_IBUF[34]} {C_IBUF[35]} {C_IBUF[36]} {C_IBUF[37]} {C_IBUF[38]} {C_IBUF[39]}
{C_IBUF[40]} {C_IBUF[41]} {C_IBUF[42]} {C_IBUF[43]} {C_IBUF[44]} {C_IBUF[45]}
{C_IBUF[46]} {C_IBUF[47]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
set_property port_width 18 [get_debug_ports u_ila_0/probe3]
connect_debug_port u_ila_0/probe3 [get_nets [list {D_IBUF[0]} {D_IBUF[1]} {D_IBUF[2]}
{D_IBUF[3]} {D_IBUF[4]} {D_IBUF[5]} {D_IBUF[6]} {D_IBUF[7]} {D_IBUF[8]} {D_IBUF[9]}
{D_IBUF[10]} {D_IBUF[11]} {D_IBUF[12]} {D_IBUF[13]} {D_IBUF[14]} {D_IBUF[15]}
{D_IBUF[16]} {D_IBUF[17]}]]
```

```
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
set_property port_width 36 [get_debug_ports u_ila_0/probe4]
connect_debug_port u_ila_0/probe4 [get_nets [list {M_OBUF[0]} {M_OBUF[1]} {M_OBUF[2]}
{M_OBUF[3]} {M_OBUF[4]} {M_OBUF[5]} {M_OBUF[6]} {M_OBUF[7]} {M_OBUF[8]} {M_OBUF[9]}
{M_OBUF[10]} {M_OBUF[11]} {M_OBUF[12]} {M_OBUF[13]} {M_OBUF[14]} {M_OBUF[15]}
{M_OBUF[16]} {M_OBUF[17]} {M_OBUF[18]} {M_OBUF[19]} {M_OBUF[20]} {M_OBUF[21]}
{M_OBUF[22]} {M_OBUF[23]} {M_OBUF[24]} {M_OBUF[25]} {M_OBUF[26]} {M_OBUF[27]}
{M_OBUF[28]} {M_OBUF[29]} {M_OBUF[30]} {M_OBUF[31]} {M_OBUF[32]} {M_OBUF[33]}
{M_OBUF[34]} {M_OBUF[35]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe5]
set_property port_width 48 [get_debug_ports u_ila_0/probe5]
connect_debug_port u_ila_0/probe5 [get_nets [list {PCIN_IBUF[0]} {PCIN_IBUF[1]}
{PCIN_IBUF[2]} {PCIN_IBUF[3]} {PCIN_IBUF[4]} {PCIN_IBUF[5]} {PCIN_IBUF[6]}
{PCIN_IBUF[7]} {PCIN_IBUF[8]} {PCIN_IBUF[9]} {PCIN_IBUF[10]} {PCIN_IBUF[11]}
{PCIN_IBUF[12]} {PCIN_IBUF[13]} {PCIN_IBUF[14]} {PCIN_IBUF[15]} {PCIN_IBUF[16]}
{PCIN_IBUF[17]} {PCIN_IBUF[18]} {PCIN_IBUF[19]} {PCIN_IBUF[20]} {PCIN_IBUF[21]}
{PCIN_IBUF[22]} {PCIN_IBUF[23]} {PCIN_IBUF[24]} {PCIN_IBUF[25]} {PCIN_IBUF[26]}
{PCIN_IBUF[27]} {PCIN_IBUF[28]} {PCIN_IBUF[29]} {PCIN_IBUF[30]} {PCIN_IBUF[31]}
{PCIN_IBUF[32]} {PCIN_IBUF[33]} {PCIN_IBUF[34]} {PCIN_IBUF[35]} {PCIN_IBUF[36]}
{PCIN_IBUF[37]} {PCIN_IBUF[38]} {PCIN_IBUF[39]} {PCIN_IBUF[40]} {PCIN_IBUF[41]}
{PCIN_IBUF[42]} {PCIN_IBUF[43]} {PCIN_IBUF[44]} {PCIN_IBUF[45]} {PCIN_IBUF[46]}
{PCIN_IBUF[47]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe6]
set_property port_width 18 [get_debug_ports u_ila_0/probe6]
connect_debug_port u_ila_0/probe6 [get_nets [list {B_IBUF[0]} {B_IBUF[1]} {B_IBUF[2]}
{B_IBUF[3]} {B_IBUF[4]} {B_IBUF[5]} {B_IBUF[6]} {B_IBUF[7]} {B_IBUF[8]} {B_IBUF[9]}
{B_IBUF[10]} {B_IBUF[11]} {B_IBUF[12]} {B_IBUF[13]} {B_IBUF[14]} {B_IBUF[15]}
{B_IBUF[16]} {B_IBUF[17]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe7]
set_property port_width 8 [get_debug_ports u_ila_0/probe7]
connect_debug_port u_ila_0/probe7 [get_nets [list {OPMODE_IBUF[0]} {OPMODE_IBUF[1]}
{OPMODE_IBUF[2]} {OPMODE_IBUF[3]} {OPMODE_IBUF[4]} {OPMODE_IBUF[5]} {OPMODE_IBUF[6]}
{OPMODE_IBUF[7]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe8]
set_property port_width 18 [get_debug_ports u_ila_0/probe8]
connect_debug_port u_ila_0/probe8 [get_nets [list {BCOUT_OBUF[0]} {BCOUT_OBUF[1]}
{BCOUT_OBUF[2]} {BCOUT_OBUF[3]} {BCOUT_OBUF[4]} {BCOUT_OBUF[5]} {BCOUT_OBUF[6]}
{BCOUT_OBUF[7]} {BCOUT_OBUF[8]} {BCOUT_OBUF[9]} {BCOUT_OBUF[10]} {BCOUT_OBUF[11]}
{BCOUT_OBUF[12]} {BCOUT_OBUF[13]} {BCOUT_OBUF[14]} {BCOUT_OBUF[15]} {BCOUT_OBUF[16]}
{BCOUT_OBUF[17]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe9]
set_property port_width 1 [get_debug_ports u_ila_0/probe9]
connect_debug_port u_ila_0/probe9 [get_nets [list CARRYOUTF_OBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe10]
set_property port_width 1 [get_debug_ports u_ila_0/probe10]
connect_debug_port u_ila_0/probe10 [get_nets [list CEA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe11]
```

```
set_property port_width 1 [get_debug_ports u_ila_0/probe11]
connect_debug_port u_ila_0/probe11 [get_nets [list CEB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
set_property port_width 1 [get_debug_ports u_ila_0/probe12]
connect_debug_port u_ila_0/probe12 [get_nets [list CEC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe13]
set_property port_width 1 [get_debug_ports u_ila_0/probe13]
connect_debug_port u_ila_0/probe13 [get_nets [list CECARRYIN_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe14]
set_property port_width 1 [get_debug_ports u_ila_0/probe14]
connect_debug_port u_ila_0/probe14 [get_nets [list CED_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe15]
set_property port_width 1 [get_debug_ports u_ila_0/probe15]
connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe16]
set_property port_width 1 [get_debug_ports u_ila_0/probe16]
connect_debug_port u_ila_0/probe16 [get_nets [list CEP_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe17]
set_property port_width 1 [get_debug_ports u_ila_0/probe17]
connect_debug_port u_ila_0/probe17 [get_nets [list CLK_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe18]
set_property port_width 1 [get_debug_ports u_ila_0/probe18]
connect_debug_port u_ila_0/probe18 [get_nets [list RSTA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe19]
set_property port_width 1 [get_debug_ports u_ila_0/probe19]
connect_debug_port u_ila_0/probe19 [get_nets [list RSTB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
set_property port_width 1 [get_debug_ports u_ila_0/probe20]
connect_debug_port u_ila_0/probe20 [get_nets [list RSTC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
set_property port_width 1 [get_debug_ports u_ila_0/probe21]
connect_debug_port u_ila_0/probe21 [get_nets [list RSTCARRYIN_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe22]
set_property port_width 1 [get_debug_ports u_ila_0/probe22]
connect_debug_port u_ila_0/probe22 [get_nets [list RSTD_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe23]
set_property port_width 1 [get_debug_ports u_ila_0/probe23]
connect_debug_port u_ila_0/probe23 [get_nets [list RSTM_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe24]
set_property port_width 1 [get_debug_ports u_ila_0/probe24]
connect_debug_port u_ila_0/probe24 [get_nets [list RSTP_IBUF]]
set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
```

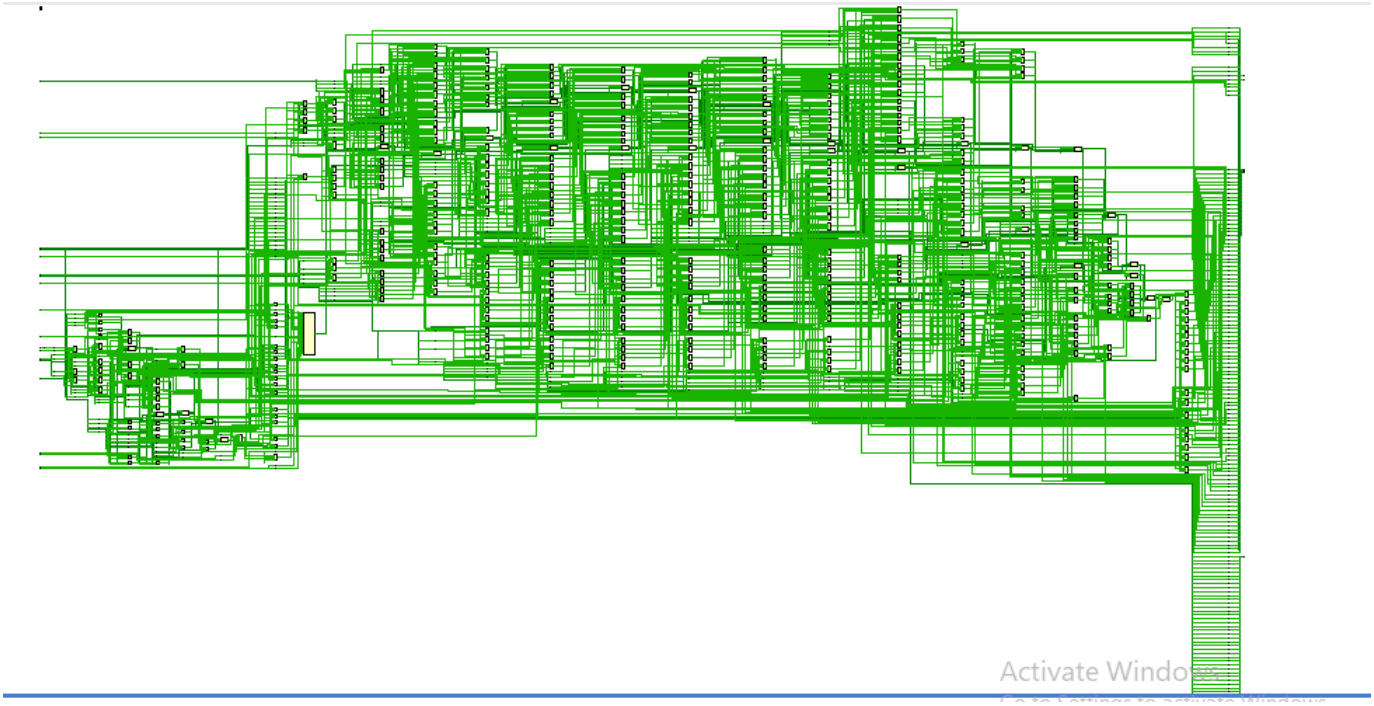
```
set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
connect_debug_port dbg_hub/clk [get_nets CLK_IBUF_BUFG]
```

Elaboration



- Elaborated Design (22 warnings, 6 infos, 7 status messages)
  - General Messages (22 warnings, 6 infos, 7 status messages)
    - [Synth 8-2490] overwriting previous definition of module DSP48A1 [p1.v:1]
    - [Synth 8-6157] synthesizing module 'DSP48A1' [p1.v:1]
    - [Synth 8-6155] done synthesizing module 'DSP48A1' (1#1) [p1.v:1]
    - [Synth 8-3331] design DSP48A1 has unconnected port CARRYIN (20 more like this)
    - [Project 1-570] Preparing netlist for logic optimization
    - Processing XDC Constraints (6 more like this)
    - [Project 1-236] Implementation specific constraints were found while reading constraint file [G:/kareem_waseem/p1/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/DSP48A1_propImpl.xdc].
      Resolution: To avoid this warning, move constraints listed in [.Xil/DSP48A1_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.

synthesis



Synthesis (46 warnings, 22 infos, 11 status messages)

- Command: synth_design -top DSP48A1 -part xc7a200tffg1156-3 (10 more like this)
- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
- [Synth 8-2490] overwriting previous definition of module DSP48A1 [p1.v:1]
- [Synth 8-6157] synthesizing module 'DSP48A1' [p1.v:1]
- [Synth 8-6155] done synthesizing module 'DSP48A1' (1#1) [p1.v:1]
- [Synth 8-3331] design DSP48A1 has unconnected port CARRYIN (41 more like this)
- [Device 21-403] Loading part xc7a200tffg1156-3
- [Project 1-236] Implementation specific constraints were found while reading constraint file [G:/kareem_waseem/p1/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/DSP48A1_propImpl.xdc].
  Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [p1.v:152] (1 more like this)
- [Synth 8-4471] merging register 'B1_reg_reg[17:0]' into 'B1_reg_reg[17:0]' [p1.v:176] (1 more like this)
- [Synth 8-6014] Unused sequential element B1_reg_reg was removed. [p1.v:176] (1 more like this)
- [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [p1.v:155]
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 205 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out

- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'G:/kareem_waseem/p1/project_1/project_1.runs/synth_1/DSP48A1.dcp' has been generated.
- [runtcl-4] Executing : report_utilization -file DSP48A1_utilization_synth.rpt -pb DSP48A1_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Thu Jul 31 19:44:23 2025...

Synthesized Design (7 infos, 2 status messages)

Design Timing Summary

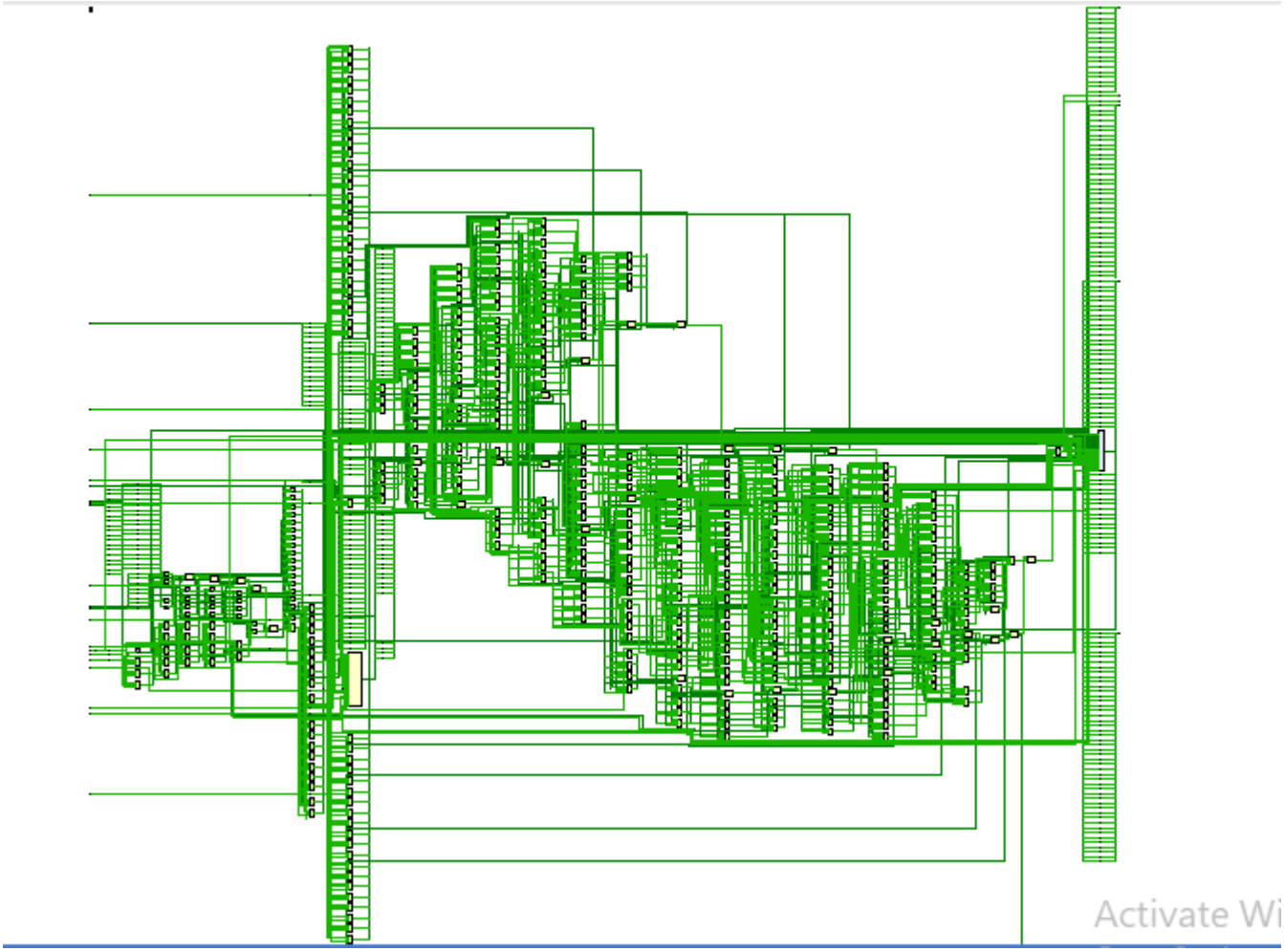
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.168 ns	Worst Hold Slack (WHS):	0.341 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	86	Total Number of Endpoints:	86	Total Number of Endpoints:	136

All user specified timing constraints are met.

Hierarchy

Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
N DSP48A1	229	134	1	325	1

Implementation



- Implementation (2 warnings, 104 infos, 234 status messages)
  - Design Initialization (7 infos, 7 status messages)
    - Command: link_design -top DSP48A1 -part xc7a200tffg1156-3 (6 more like this)
    - [Netlist 29-17] Analyzing 205 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Device 21-403] Loading part xc7a200tffg1156-3
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
  - Opt Design (37 infos, 54 status messages)
    - Command: opt_design (53 more like this)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
    - [Project 1-461] DRC finished with 0 Errors
    - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'F:/vivado/Vivado/2018.2/data/ip'.
    - [Chipscope 16-329] Generating Script for core instance : dbg_hub (1 more like this)
    - [IP_Flow 19-3806] Processing IP xilinx.com:ip:xsdbm:3.0 for cell dbg_hub_CV. (1 more like this)
    - [Chipscope 16-220] Re-using generated and synthesized IP, "xilinx.com:ip:xsdbm:3.0", from Vivado IP cache entry "9c4ae1ee9885a9c0". (1 m
    - [Opt 31-49] Retargeted 0 cell(s).
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)

    - [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
    - [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
    - [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
    - [Pwropt 34-9] Applying IDT optimizations ...
    - [Pwropt 34-10] Applying ODC optimizations ...
    - [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
    - [Physopt 32-619] Estimated Timing Summary | WNS=4.870 | TNS=0.000 |
    - [Pwropt 34-162] WRITE_MODE attribute of 0 BRAM(s) out of a total of 8 has been updated to save power. Run report_power_opt to get a complete listing of the BRAMs updated.
    - [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports
    - [Common 17-83] Releasing license: Implementation
    - [Timing 38-480] Writing timing data to binary archive.
    - [Common 17-1381] The checkpoint 'G:/kareem_waseem/p1/project_1/project_1.runs/impl_1/DSP48A1_opt.dcp' has been generated.
    - [runtcl-4] Executing : report_drc -file DSP48A1_drc_opted.rpt -pb DSP48A1_drc_opted.pb -rpx DSP48A1_drc_opted.rpx
    - [IP_Flow 19-1839] IP Catalog is up to date.
    - [DRC 23-27] Running DRC with 2 threads (1 more like this)
    - [Coretcl 2-168] The results of DRC are in file DSP48A1_drc_opted.rpt.
  - Place Design (24 infos, 90 status messages)
    - [Chipscope 16-240] Debug cores have already been implemented
    - Command: place_design (89 more like this)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
    - [DRC 23-27] Running DRC with 2 threads (1 more like this)
    - [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
    - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
    - [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs

[Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Timing 38-35] Done setting XDC timing constraints. (2 more like this)
[Physopt 32-65] No nets found for high-fanout optimization.
[Physopt 32-232] Optimized 0 net. Created 0 new instance.
[Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
[Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
[Place 30-746] Post Placement Timing Summary WNS=4.182. For the most accurate timing information please run report_timing.
[Common 17-83] Releasing license: Implementation
[Timing 38-480] Writing timing data to binary archive.
[Common 17-1381] The checkpoint 'G:/kareem_waseem/p1/project_1/project_1.runs/impl_1/DSP48A1_placed.dcp' has been generated.
[runtcl-4] Executing : report_io -file DSP48A1_io_placed.rpt (2 more like this)
Route Design (2 warnings, 36 infos, 83 status messages)
Command: route_design (82 more like this)
[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
DRC (1 warning)
Pin Planning (1 warning)
[DRC CFGBVS-7] CONFIG_VOLTAGE with Config Bank VCCO: The CONFIG_MODE property of current_design specifies a configuration mode (SPIx4) that uses pins in bank 14. I/O standards used in this bank have a voltage requirement of 1.80. However, the CONFIG_VOLTAGE for current_design is set to 3.3. Ensure that your configuration voltage is compatible with the I/O standards in banks used by your configuration mode. Refer to device configuration user guide for more information. Pins used by config mode: V28 (IO_L1P_T0_D00_MOSI_14), V29 (IO_L1N_T0_D01_DIN_14), V26 (IO_L2P_T0_D02_14), V27 (IO_L2N_T0_D03_14), W26 (IO_L3P_T0_DQS_PUDC_B_14), and Y27 (IO_L6P_T0_FCS_B_14)
[Vivado_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings
[Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

mode: V28 (IO_L1P_T0_D00_MOSI_14), V29 (IO_L1N_T0_D01_DIN_14), V26 (IO_L2P_T0_D02_14), V27 (IO_L2N_T0_D03_14), W26 (IO_L3P_T0_DQS_PUDC_B_14), Y27 (IO_L6P_T0_FCS_B_14)
[Vivado_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings
[Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
[Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
[Route 35-416] Intermediate Timing Summary | WNS=4.192 | TNS=0.000 | WHS=-0.698 | THS=-319.237| (3 more like this)
[Route 35-57] Estimated Timing Summary | WNS=2.963 | TNS=0.000 | WHS=0.057 | THS=0.000 |
[Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report_timing_summary.
[Route 35-16] Router Completed Successfully
[Common 17-83] Releasing license: Implementation
[Timing 38-480] Writing timing data to binary archive.
[Common 17-1381] The checkpoint 'G:/kareem_waseem/p1/project_1/project_1.runs/impl_1/DSP48A1_routed.dcp' has been generated.
[IP_Flow 19-1839] IP Catalog is up to date.
[DRC 23-27] Running DRC with 2 threads (1 more like this)
[Coretcl 2-168] The results of DRC are in file DSP48A1_drc_routed.rpt.
[runtcl-4] Executing : report_drc -file DSP48A1_drc_routed.rpt -pb DSP48A1_drc_routed.pb -rpx DSP48A1_drc_routed.rpx (7 more like this)
[Timing 38-35] Done setting XDC timing constraints. (2 more like this)
[DRC 23-133] Running Methodology with 2 threads
[Coretcl 2-1520] The results of Report Methodology are in file DSP48A1_methodology_drc_routed.rpt.
[Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.
[Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
[Timing 38-91] UpdateTimingParams: Speed grade: -3, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.965 ns	Worst Hold Slack (WHS):	0.059 ns	Worst Pulse Width Slack (WPWS):	3.950 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0

Name 1	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	E
DSP48A1	2619	4099	96	8	1301	2155	464	1510	
dbg_hub (dbg_hub)	476	727	0	0	253	452	24	296	
u_ila_0 (u_ila_0)	1914	3238	96	8	988	1474	440	1155	

Block RAM Tile (365)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	BSCANE2 (4)
8	1	325	2	1
0	0	0	1	1
8	0	0	0	0

Linting no errors