

Institute of Engineering & Management
Department of Computer Science & Engineering
Computer Architecture Laboratory for 2nd year 4th semester 2018
Code: CS 493

Date: 17/02/18

WEEK-3

Assignment-1: Implementation of 8 bit Adder, 8 bit Subtractor, 8 bit Parallel Adder, 8 bit Parallel Subtractor, 4 bit Multiplier & 8 bit Comparator using Xilinx ISE.

Objective: To implement 8 bit Adder

Software used:

<u>Property Name</u>	<u>Value</u>
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:




- i. Make VHDL with required port specification.
- ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
- iii. Make test bench waveform and check for the given inputs.

Data flow Model:

Data flow Model Code:

```
entity a1 is
  Port ( a : in STD_LOGIC_VECTOR (7 downto 0);
        b : in STD_LOGIC_VECTOR (7 downto 0);
        c : out STD_LOGIC_VECTOR (7 downto 0));
end a1;
architecture Behavioral of a1 is
begin
  c<=a+b;
end Behavioral;
```

Output:

Current Simulation Time: 1000 ns		829.1 ns									
		100 ns	200 ns	300 ns	400 ns	500 ns	600 ns	700 ns	800 ns	900 ns	1000 ns
 a[7:0]	20	175	113	205	30	187	97	220		20	134
 b[7:0]	75	136	118	221	10	176	101	158		75	97
 c[7:0]	95	55	231	170	40	107	198	122		95	231

Objective: To implement 8 bit subtractor

Software used:

<u>Property Name</u>	<u>Value</u>
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

- i. Make VHDL with required port specification.
- ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
- iii. Make test bench waveform and check for the given inputs.

Data flow Model:

Data flow Model Code:




```
entity a1 is
  Port ( a : in  STD_LOGIC_VECTOR (7 downto 0);
        b : in  STD_LOGIC_VECTOR (7 downto 0);
        c : out STD_LOGIC_VECTOR (7 downto 0));
end a1;
```

```

architecture Behavioral of a1 is
begin
c<=ab;
end Behavioral;

```

Output:

Current Simulation Time: 1000 ns		100 ns	200 ns	300 ns	400 ns	500 ns	600 ns	700 ns	800 ns	900 ns
 a[7:0]	134	175	113	205	30	187	97	220	20	
 b[7:0]	97	136	118	221	10	176	101	158	75	
 c[7:0]	37	39	251	240	20	11	252	62	201	

Objective: To implement 8 bit Comparator

Software used:

<u>Property Name</u>	<u>Value</u>
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

- Make VHDL with required port specification.
- Calculate the value c for both data flow and behavioral model using if and else statement with required condition.

- iii. Make test bench waveform and check for the given inputs.

Data flow Model:

Data flow Model Code:

```
entity a3 is
  Port ( a : in
        STD_LOGIC_VECTOR (7
        downto 0);
        b : in
        STD_LOGIC_VECTOR (7
        downto 0);
        low : out STD_LOGIC;
        high : out STD_LOGIC;
        equal : out STD_LOGIC);
end a3;
```

architecture Behavioral of a3 is

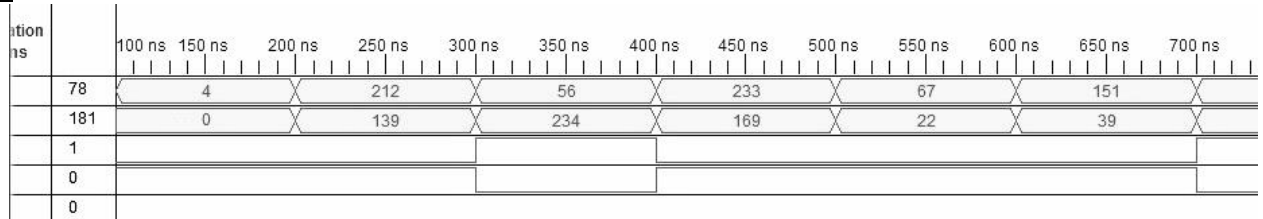
```
begin process(a,b)
begin
if (a<b) then
low<='1';
high<='0';
equal<='0';
elsif (a>b) then
low<='0';
high<='1';
equal<='0';
elsif (a=b) then
low<='0';
high<='0';
```

```

equal<='1';
end if;
end process;
end Behavioral;

```

Output:



Objective: To implement 8 bit Parallel Adder

Software used:

<u>Property Name</u>	<u>Value</u>
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

- Make VHDL with required port specification.
- Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
- Make test bench waveform and check for the given inputs.

Data flow Model:








Data flow Model Code:

```
entity a2 is
  Port ( a : in  STD_LOGIC_VECTOR (7 downto 0);
        b : in  STD_LOGIC_VECTOR (7 downto 0);
        cin : in  STD_LOGIC;
        s : out STD_LOGIC_VECTOR (7 downto 0));
end a2;

architecture Behavioral of a2 is

  begin process(a,b,cin)
    variable ct:std_logic_vector(7 downto 0);
    begin
      ct(0):=cin;
      for i in 0 to 7 loop
        s(i)<=a(i) xor b(i) xor ct(i);
        ct(i+1):=( a(i) and b(i)) or (b(i) and ct(i)) or (a(i) and ct(i));
      end loop;
    end process;
  end Behavioral;
```

Output:

Current Simulation Time: 1000 ns		100 ns	150 ns	200 ns	250 ns	300 ns	350 ns	400 ns	450 ns	500 ns	550 ns	600 ns	650 ns	700 ns
  a[7:0]	0	148		118		160		1		215		51		
  b[7:0]	210	4		81		213		116		168		33		
 cin	0													
  s[7:0]	210	152		199		117				127		84		

Objective: To implement 8bit Parallel Subtractor

Software used:

<u>Property Name</u>	<u>Value</u>
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

- i. Make VHDL with required port specification.
- ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
- iii. Make test bench waveform and check for the given inputs.

Data flow Model:

Data flow Model Code:

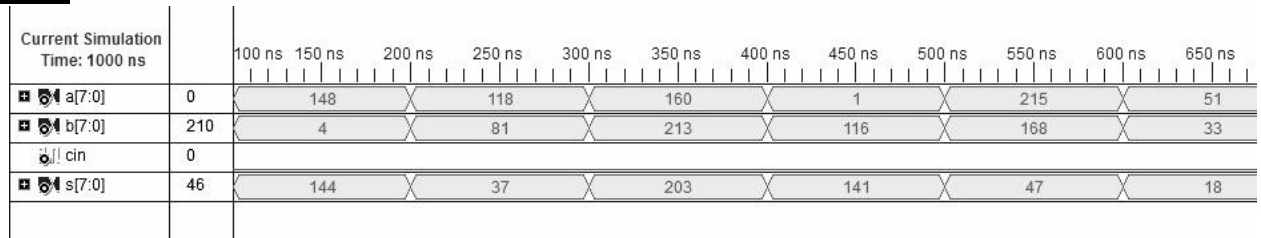
```
entity a2 is
  Port ( a : in  STD_LOGIC_VECTOR (7 downto 0);
        b : in  STD_LOGIC_VECTOR (7 downto 0);
        cin : in  STD_LOGIC;
        s : out STD_LOGIC_VECTOR (7 downto 0));
```


end a2;

architecture Behavioral of a2 is

```
begin process(a,b,cin)
variable ct:std_logic_vector(7 downto 0);
begin
ct(0):=cin;
for i in 0 to 7 loop
s(i)<=a(i) xor b(i) xor ct(i);
ct(i+1):=((not a(i)) and b(i)) or (b(i) and ct(i)) or ((not a(i)) and ct(i));
end loop;
end process;
end Behavioral;
```

Output:



Objective: To implement 4bit Multiplier

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

- i. Make VHDL with required port specification.
- ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
- iii. Make test bench waveform and check for the given inputs.

Data flow Model:

Data flow Model Code:







```
entity a4 is
  Port ( a : in STD_LOGIC_VECTOR (3 downto 0);
        b : in STD_LOGIC_VECTOR (3 downto 0);
        c : out STD_LOGIC_VECTOR (7 downto 0));
end a4;
```

architecture Behavioral of a4 is

```
begin process(a,b)
begin
  c<=a*b;
```

```
end process;
end Behavioral;
```

Output:

Current Simulation Time: 1000 ns		100 ns	150 ns	200 ns	250 ns	300 ns	350 ns	400 ns	450 ns	500 ns	550 ns	600 ns	650 ns
  a[3:0]	2	0		9		5		12		2		11	
  b[3:0]	5	0		14		13		5		0		10	
  c[7:0]	10	0		126		65		60		0		110	