Institute of Engineering & Management
Department of Computer Science & Engineering
Computer Architecture Laboratory for 2nd year 4th semester 2018
Code: CS 493

Date: 21/04/18

WEEK-8

Assignment-1: Implementation of SR, JK, D & T Flipflops using Xilinx ISE.

Objective: To implement SR Flipflop

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

i. Make VHDL with required port specification.
ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
iii. Make test bench waveform and check for the given inputs.

Truth Table:

CLK	S	R	Q_{n+1}	$Q_{n+1}{}^{c}$
0	1	0	Q_n	$Q_n{}^{c}$
1	0	0	Q_n	$Q_n{}^{c}$
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid	Invalid

Code:

```
entity srff1 is
   Port ( S : in  STD_LOGIC;
          R : in  STD_LOGIC;
          CLK : in  STD_LOGIC;
          Q : inout  STD_LOGIC;
          NQ : inout  STD_LOGIC);
end srff1;
```

```
architecture Behavioral of srff1 is
begin
process(S,R,CLK)
begin
NQ<=not Q;
if CLK='0' then
Q<=Q;
NQ<= not Q;
else
if(R='0' and S='0') then
Q<=Q;
NQ<=not Q;
elsif(R='1' and S='0') then
Q<='0';
NQ<='1';
elsif(R='0' and S='1') then
Q<='1';
NQ<='0';
elsif(R='1' and S='1') then
Q<='X';
NQ<='X';
end if;
end if;
end process;
end Behavioral;
```

Model:

Output:

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Objective: To implement JK Flipflop

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

i. Make VHDL with required port specification.
ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
iii. Make test bench waveform and check for the given inputs.

Truth Table:

CLK	S	R	Q_{n+1}	$\underline{Q_{n+1}}^c$
0	1	0	Q_n	$\underline{Qn}^c$
1	0	0	Q_n	$\underline{Q_n}^c$
1	0	1	0	1
1	1	0	1	0
1	1	1	$\underline{Q_n}^c$	Q_n

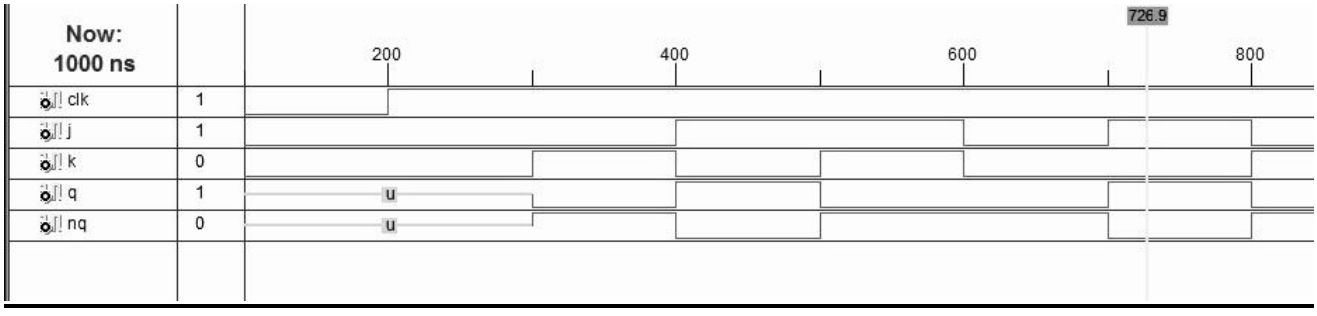
Code:

```
entity jkff is
   Port ( clk : in  STD_LOGIC;
          j : in  STD_LOGIC;
          k : in  STD_LOGIC;
          q : inout  STD_LOGIC;
          nq : inout  STD_LOGIC);
end jkff;

architecture Behavioral of jkff is
begin
process(j,k,clk)
begin

if clk='0' then
q<=q;
nq<=not q;
else
if (j='0' and k='0') then
```

```
        q<=q;
        nq<=not q;
        elsif (j='0' and k='1') then
        q<='0';
        nq<='1';
        elsif (j='1' and k='0') then
        q<='1';
        nq<='0';
        else
        q<=nq;
        nq<= not nq;
end if;
end if;
end process;
end Behavioral;
```

Model:

Output:



Objective: To implement D Flipflop

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

i. Make VHDL with required port specification.
ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
iii. Make test bench waveform and check for the given inputs.

Truth Table:

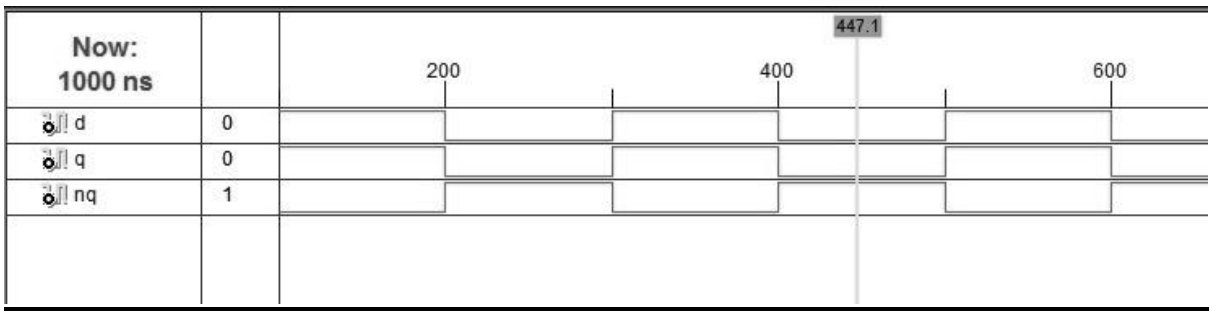
D	Q_{n+1}	Q_{n+1}^c
1	1	0
0	0	1

Code:

```
entity dff1 is
   Port ( D : in  STD_LOGIC;
          Q : inout  STD_LOGIC;
          NQ : inout  STD_LOGIC);
end dff1;

architecture Behavioral of dff1 is
begin
process(D)
begin
if D='0' then
Q<='0';
NQ<='1';
else
Q<='1';
NQ<='0';
end if;
end process;
end Behavioral;
```

Model:

Output:



Objective: To implement T Flipflop

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

i. Make VHDL with required port specification.
ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
iii. Make test bench waveform and check for the given inputs.

Truth Table:

T	$\mathbf{Q_{n+1}}$	$\mathbf{\underline{Q_{n+1}}^{c}}$
1	$\underline{Q_n}^{c}$	$\underline{Q_n}$
0	Q_n	$\underline{Q_n}^{c}$

Code:

```
entity tff1 is
   Port ( T : in  STD_LOGIC;
          Q : inout  STD_LOGIC:='1';
          NQ : inout  STD_LOGIC:='0');
end tff1;

architecture Behavioral of tff1 is
begin
process(T)
variable x : STD_LOGIC := '1';
begin
if T='1' then
Q<= not Q;
NQ<= not NQ;
end if;
end process;
end Behavioral;
```

Model:

Output: