Institute of Engineering & Management Department of Computer Science & Engineering Computer Architecture Laboratory for 2nd year 4th semester 2018 Code: CS 493

Date: 24/02/2018

WEEK-4

Assignment-1: Conversion from Binary to Grey number & Grey to Binary using Xilinx ISE.

Objective: Convert 4bit binary to grey

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

- i. Make VHDL with required port specification.
- ii. Calculate the value c for both data flow and behavioural model using if and else statement with required condition.
- iii. Make test bench waveform and check for the given inputs.

Truth Table:

BINARY	GREY	BINARY	GREY
0000	0000	0010	0011
0001	0001	1010	1111
1111	1000	0111	0100
1011	1110	0100	0110

Behavioural Model:

Data flow Model:

Code:

Behavioural Model Code:

```
entity abcd is

Port ( b : in STD_LOGIC_VECTOR (3 downto 0);
g : out STD_LOGIC_VECTOR (3 downto 0));
end abcd;
architecture Behavioral of abcd is

begin process(b)
Begin
g(3)<=b(3);
for i in 2 downto 0 loop
if b(i)=b(i+1) then
g(i)<='0';
```

```
else
g(i) <= '1';
end if;
end loop;
end process;
end Behavioral;
Data Flow Model Code:
entity abcd is
  Port ( g: in STD_LOGIC_VECTOR (3 downto 0);
      b: out STD_LOGIC_VECTOR (3 downto 0));
end abcd;
architecture Behavioral of abcd is
begin process(b)
begin
g(3) <= b(3);
g(2) <= b(3) \text{ xor } b(2);
g(1) <= b(2) \text{ xor } b(1);
```

Output:

g(0) <= b(1) xor b(0);

end process;
end Behavioral;

Current Simulation Time: 1000 ns							540	.6 ns		
		100 ns 150 ns 200	ns 250 ns 300	ns 350 ns 4	100 ns	450 ns 50	0 ns 5	550 ns	600 ns	650 ns
■ ⑤ ∮ b[3:0]	4	(8)	1)	10	X	11	X	4	X	5
b[3] اِلْ	0							10:		
₀[] b[2]	1									
o [! b[1]	0						1			
o [i p[0]	0							No.		
■ ⑤ 4 g[3:0]	6	(12)	1	15	X	14	X	6	X	7
[3] و[3]	0			V						
g[2] و ن	1									
o .[! g[1]	1									
g[0] وال م	0		17					(0):		

Objective: Convert 4 - bit grey to binary

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

- i. Make VHDL with required port specification.
- ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
- iii. Make test bench waveform and check for the given inputs.

Truth Table:

GREY	BINARY	GREY	BINARY
0000	0000	0011	0010
0001	0001	1111	1010
1000	1111	0100	0111
1110	1011	0110	0100

Data Flow Model:

Behavioural Model:

Code:

Behavioural Model Code:

```
entity abcd is
 Port (g: in STD_LOGIC_VECTOR (3 downto 0);
       b: inout \ STD\_LOGIC\_VECTOR \ (3 \ downto \ 0));
end abcd;
architecture Behavioral of abcd is
begin process(g,b)
begin
b(3) <= g(3);
for i in 2 downto 0 loop
if g(i)=b(i+1) then
b(i) < = '0';
else
b(i) <= '1';
end if;
end loop;
end process;
end Behavioral;
```

Data Flow Model Code:

```
entity abcd is

Port (g: in STD_LOGIC_VECTOR (3 downto 0);
b: out STD_LOGIC_VECTOR (3 downto 0));
end abcd;
architecture Behavioral of abcd is
begin process(g)
begin
b(3)<=g(3);
b(2)<=g(3) xor g(2);
b(1)<=g(3) xor g(2) xor g(1);
b(0)<=g(3) xor g(2) xor g(1) xor g(0);
end process;
end Behavioral;
```

Output:

				969	3 ns			
Current Simulation Time: 1000 ns		100 ns 150 ns 200	ns 250 ns 300	ns 350 ns	400 ns 4	450 ns 500	ns 550 ns 600	ns 650 ns 700
■ ⑤ ∮ g[3:0]	2	0	9	2	X	3	12	(5
[3]و اِلرَّ	0							
[2]و اِلْ	0							
[1]و اِلرَّ	1							
[0]و اِلْ	0	8	5)		88			
■ ⑤ ∮ b[3:0]	3	0	(14)	3	<u> </u>	2	8	(6)
p[3] وأرق	0	51						
[2] إلى	0							
b[1] إِنْ	1	(c) (c) (d) (d) (d) (d) (d) (d) (d) (d) (d) (d				01		
p [*] [i p[0]	1	W			**			

Assignment-2: Implementation of 4:2 encoder using Xilinx ISE.

Objective: Implement a 4:2 encoder with behavioural code.

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

- i. Make VHDL with required port specification.
- ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
- iii. Make test bench waveform and check for the given inputs.

Truth Table:

Input	Output
0001	00
0010	01
0100	10
1000	11

Behavioural Model:

Behavioural Model Code:

```
entity a1 is
 Port (a: in STD_LOGIC_VECTOR (3 downto 0);
       b: out STD_LOGIC_VECTOR(1 downto 0));
end a1;
architecture Behavioral of a1 is
begin
process(a)
begin
if a(3)='1' then
b<="11";
elsif a(2)='1' then
b<="10";
elsif a(1)='1' then
b<="01";
elsif a(0)='1' then
b<="00";
end if;
end process;
end Behavioral;
```

Output:

		(A		372	9 ns							
Current Simulation Time: 1000 ns		200 ns 250 ns 3	00 ns	350 ns	400 I I	ns 	450 ns	5 1 1 1	00 ns 	550 ns	600 ns	650 n
■ 🗖 a[3:0]	4	2	X	4	$ \longrightarrow $		8	*****	X	0	Х	1
o ∭ a[3]	0	2		-								
a[2]	1		k ·									
[a[1] وأو	0											
a[0] غياً a	0	G:	58.7									
■ 🗖 b[1:0]	2	1	X	2	$\overline{}$				3		X	0
₀ [b[1]	1		8									
j ∭ b[0]	0		_									
	-		- 50			_						