Institute of Engineering & Management
Department of Computer Science & Engineering
Computer Architecture Laboratory for 2nd year 4th semester 2018
Code: CS 493

Date: 24/03/18

WEEK-6

Assignment-1: Implementation of 4:1 MUX and 2:1 MUX using Xilinx ISE.

Objective: To implement a 2:1 mux

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

i. Make VHDL with required port specification.
ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
iii. Make test bench waveform and check for the given inputs.

Truth Table:

S	B(0)	B(1)	O
0	1	1	1
0	0	1	1
0	1	0	0
1	1	1	1
1	0	1	0

Data Flow Code:

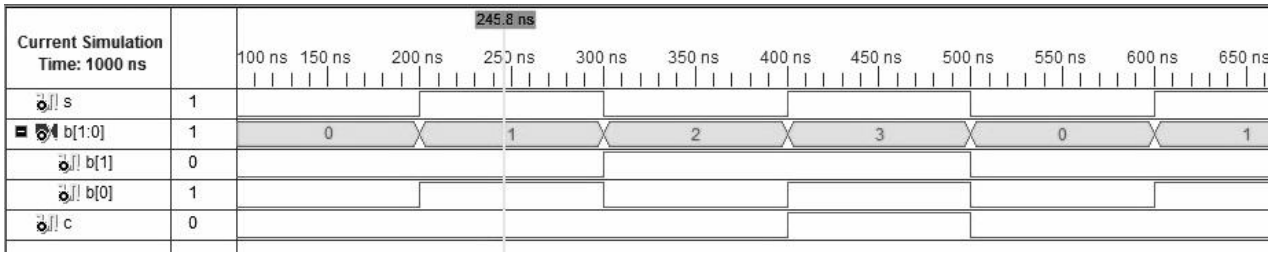
```
entity a1 is
   Port ( s : in  STD_LOGIC;
          b : in  STD_LOGIC_VECTOR(1 downto 0);
                  c : out  STD_LOGIC );
end a1;

architecture Behavioral of a1 is

begin
c<= (s and b(1)) or ((not s) and b(0));
end Behavioral;
```

Data Flow Model:

Output:



Objective: To implement a 4:1 mux

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

i. Make VHDL with required port specification.
ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
iii. Make test bench waveform and check for the given inputs.

Truth Table:

S(0)	S(1)	B(3)	B(2)	B(1)	B(0)	O
0	0	0	1	1	0	0
0	1	1	0	1	1	1
0	0	1	0	0	0	0
1	1	1	1	0	0	1
1	1	1	0	0	1	1
1	0	1	1	1	0	1
1	0	0	0	1	0	0

Data Flow Code:

```
entity a1 is
   Port ( s : in  STD_LOGIC_VECTOR (1 downto 0);
          b : in  STD_LOGIC_VECTOR(3 downto 0);
                              c : out  STD_LOGIC );
end a1;
architecture Behavioral of a1 is


begin
c<= (s(1) and s(0) and b(3)) or (s(1) and (not s(0)) and b(3)) or ((not s(1)) and s(0) and b(1)) or
((not s(1)) and (not s(0)) and b(0));
```

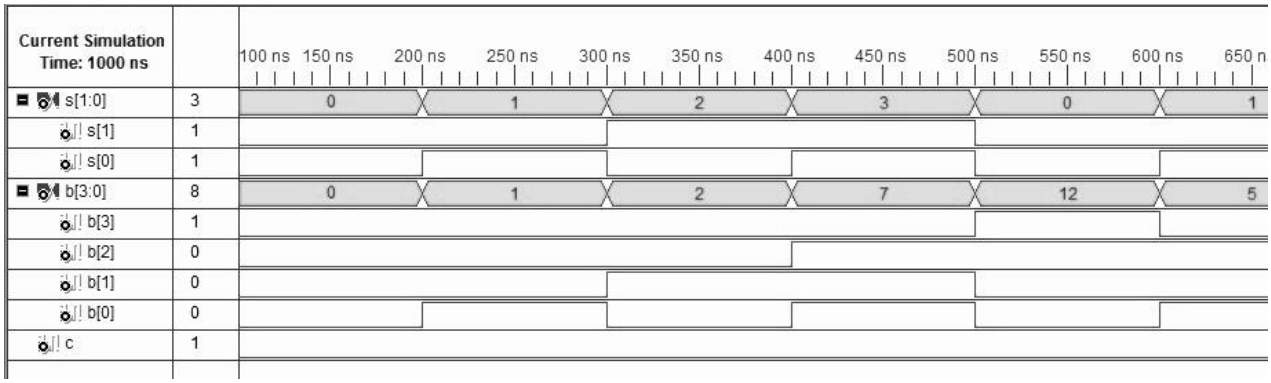
```
end Behavioral;
```

Case Code:

```
entity a1 is
   Port ( s : in  STD_LOGIC_VECTOR (1 downto 0);
          b : in  STD_LOGIC_VECTOR(3 downto 0);
                                c : out  STD_LOGIC );
end a1;
architecture Behavioral of a1 is
begin
process(s,b)
begin
case s is
when "00"=> c<=b(0);
when "01"=> c<=b(1);
when "10"=> c<=b(2);
when "11"=> c<=b(3);
when others=> c<='X';
end case;
end process;
end Behavioral;
```

Data Flow Model:

Output:



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