Institute of Engineering & Management
Department of Computer Science & Engineering
Computer Architecture Laboratory for 2nd year 4th semester 2018
Code: CS 493

Date: 24/02/2018

WEEK-4

Assignment-1: Conversion from Binary to Grey number & Grey to Binary using Xilinx ISE.

Objective: Convert 4bit binary to grey

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

i. Make VHDL with required port specification.
ii. Calculate the value c for both data flow and behavioural model using if and else statement with required condition.
iii. Make test bench waveform and check for the given inputs.

Truth Table:

BINARY	GREY		BINARY	GREY
0000	0000		0010	0011
0001	0001		1010	1111
1111	1000		0111	0100
1011	1110		0100	0110

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Behavioural Model:

Data flow Model:

Code:

Behavioural Model Code:

```
entity abcd is
  Port ( b : in STD_LOGIC_VECTOR (3 downto 0);
         g : out  STD_LOGIC_VECTOR (3 downto 0));
end abcd;
architecture Behavioral of abcd is

begin process(b)
Begin
g(3)<=b(3);
for i in 2 downto 0 loop
if b(i)=b(i+1) then
g(i)<='0';
```

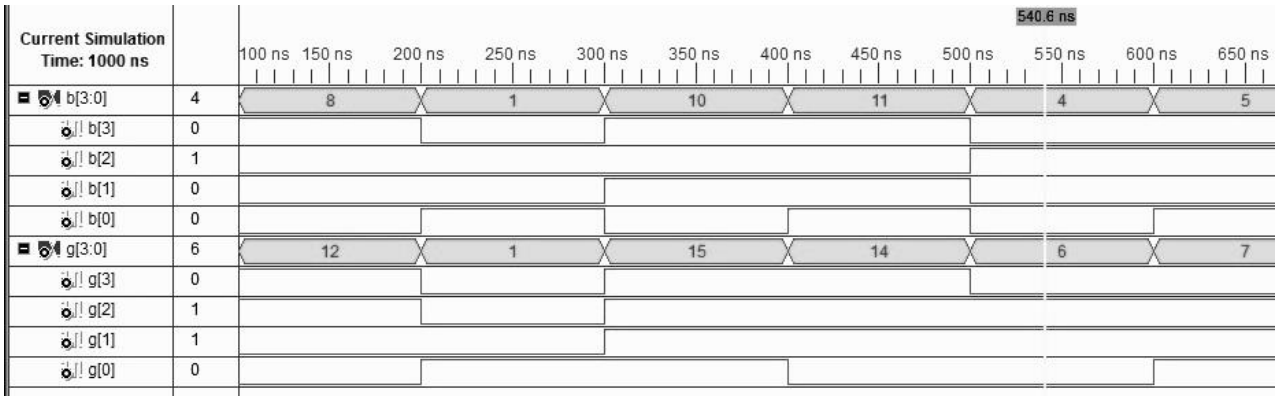
```
else
g(i)<='1';
end if;
end loop;
end process;
end Behavioral;
```

Data Flow Model Code:

```
entity abcd is
   Port ( g : in  STD_LOGIC_VECTOR (3 downto 0);
          b : out  STD_LOGIC_VECTOR (3 downto 0));
end abcd;
architecture Behavioral of abcd is

begin process(b)
begin
g(3)<=b(3);
g(2)<=b(3) xor b(2);
g(1)<=b(2) xor b(1);
g(0)<=b(1) xor b(0);
end process;
end Behavioral;
```

Output:



Objective: Convert 4 - bit grey to binary

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

i. Make VHDL with required port specification.
ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
iii. Make test bench waveform and check for the given inputs.

Truth Table:

GREY	BINARY		GREY	BINARY
0000	0000		0011	0010
0001	0001		1111	1010
1000	1111		0100	0111
1110	1011		0110	0100

Data Flow Model:

Behavioural Model:

Code:

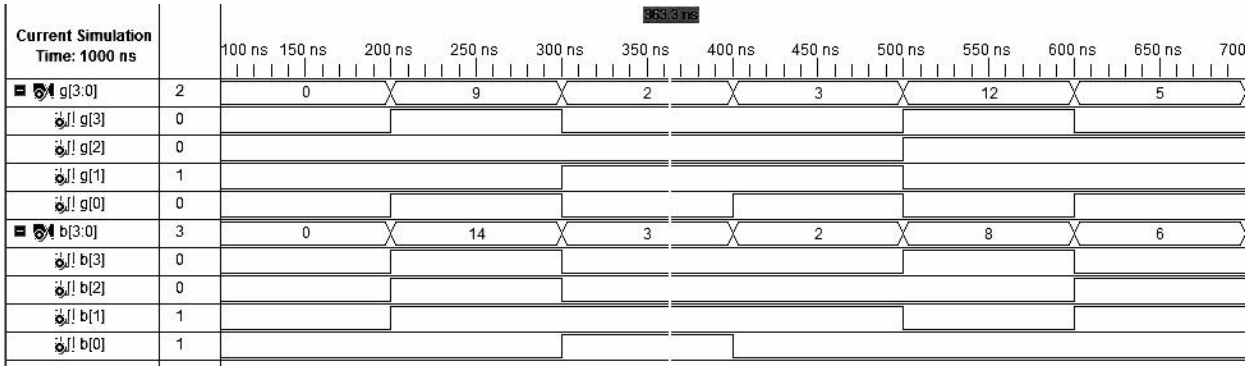
Behavioural Model Code:

```
entity abcd is
  Port ( g : in  STD_LOGIC_VECTOR (3 downto 0);
         b : inout  STD_LOGIC_VECTOR (3 downto 0));
end abcd;
architecture Behavioral of abcd is
begin process(g,b)
begin
b(3)<=g(3);
for i in 2 downto 0 loop
if g(i)=b(i+1) then
b(i)<='0';
else
b(i)<='1';
end if;
end loop;
end process;
end Behavioral;
```

Data Flow Model Code:

```
entity abcd is
  Port ( g : in  STD_LOGIC_VECTOR (3 downto 0);
         b : out  STD_LOGIC_VECTOR (3 downto 0));
end abcd;
architecture Behavioral of abcd is
begin process(g)
begin
b(3)<=g(3);
b(2)<=g(3) xor g(2);
b(1)<=g(3) xor g(2) xor g(1);
b(0)<=g(3) xor g(2) xor g(1) xor g(0);
end process;
end Behavioral;
```

Output:



Assignment-2: Implementation of 4:2 encoder using Xilinx ISE.

Objective: Implement a 4:2 encoder with behavioural code.

Software used:

Property Name	Value
Device family	Spartan 3
Device	XC3S50
Package	PQ208
Speed	-5
Top-level source type	HDL
Synthesis Tool	XST(VHDL/Verilog)
Simulator	ISE Simulator
Preferred Language	VHDL

Theory:

i. Make VHDL with required port specification.
ii. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
iii. Make test bench waveform and check for the given inputs.

Truth Table:

Input	Output
0001	00
0010	01
0100	10
1000	11

Behavioural Model:

Behavioural Model Code:

```
entity a1 is
  Port ( a : in  STD_LOGIC_VECTOR (3 downto 0);
         b : out  STD_LOGIC_VECTOR(1 downto 0));
end a1;
architecture Behavioral of a1 is

begin
process(a)
begin
if a(3)='1' then
b<="11";
elsif a(2)='1' then
b<="10";
elsif a(1)='1' then
b<="01";
elsif a(0)='1' then
b<="00";
end if;
end process;
end Behavioral;
```

Output: