

# Adhitha Dias

## Academic Statement of Purpose for University of California Irvine

---

I have come to the understanding that the humanity's future is mostly dependent upon the knowledge creation process happening through research work, however insignificant it may seem at first. Computer architecture is in the heart of all the modern technologies that have made human life incredibly easier. Modern computer architectures are vital to provide underlying hardware specification to support emerging fields like AI and IoT. Intriguing problems related but not limited to machine learning (ML) accelerators, near memory processing, branch prediction, hardware vulnerabilities, hardware security and big data handling (specifically IoT related), and memory optimization need to be addressed with new and improved architectures. Against this backdrop, I intend to pursue a PhD in Electrical and Computer Engineering specializing in Computer Architecture and I am highly motivated in contributing towards the field through fundamental research.

Based on my past academic achievements, I am convinced that I am capable of succeeding in graduate studies. I was ranked 1<sup>st</sup> in G.C.E. Advanced Level (University Entrance) Examination in the country out of 32,000+ students with a Z-score of 2.9485, marking the highest Z-score for the year. My fascination towards the technological innovations in electronics and computing substantiated my decision to join the Department of Electronic and Telecommunication Engineering of University of Moratuwa: the premier technological university in the country. I graduated with an overall GPA of 4.05/4.20 and placed 4<sup>th</sup> in the most sought-after department which accommodates top 100 students per year.

In my second year, I developed two processor implementations based on Complex Instruction Set Architecture (CISC) and Reduced Set Instruction Set Architecture (RISC). At the beginning my goal was only to design processors to down-sample images with different gaussian kernels applied. However, later I added general-purpose instructions to the control unit and developed the project to the extent of writing my own assembler to translate instructions written in assembly language to their machine code for generalization. The design was implemented in field programmable gate arrays (FPGA) with Verilog HDL. I designed the processors even before we were introduced to the module Fundamentals of Computer Architecture and Design because of the passion I had towards computer architecture.

Furthermore, we have developed an SoC with a custom hardware accelerated CRC checksum engine in an FPGA development board as part of a competition held, where our team was able to win the competition. Initially we implemented the hardware accelerator using a byte-wise table lookup algorithm. Since it was not fast enough, I independently implemented Galois field multiplication and accumulation (GFMAC) algorithm for parallel block computation to achieve maximum speed and complete checksum calculation at the earliest possible time. On a different note, I completed a group project by myself, to implement a System Bus Design architecture in Verilog according to AMBA 2.0 specified AHB type during the final year as part of Advanced Digital Systems module.

My first engagement in research during the 3<sup>rd</sup> year internship at LiveLabs Urban Lifestyle Innovation Platform of School of Information Systems of Singapore Management University under Professor Jie Xiong taught me many lessons about research. I relished every moment of the research culture and the freedom it offered. I was inspired by the Ph.D. students with whom I had worked with. I researched to find a solution to the problem of localizing a mobile device using a distributed system of wi-fi APs as opposed to localizing using an array of antennas using angle of arrival; this kind of research has not been completed successfully by anyone at the time. Wireless Open Access Research Platform (WARP) software defined radio devices were used in this research where hardware level signal processing was done using FPGA. I used different FPGA images with FPGA mezzanine cards and daughter boards for hardware extensions. I built two mathematical models based on Multiple Signal Classification Algorithm (MUSIC) and Space Alternating Generalizing Algorithm (SAGE) and tested

out in Matlab based simulation environment and actual environments using hardware platforms. Although in theory mathematical models gave promising results in high signal-to-noise (SNR) regime and lesser occluded environments, the models failed in low SNR and environments with complex multipath propagations. On a separate note, during the internship period, I also worked with professor Archan Misra and Professor Youngki Lee on identifying the important checkpoints from a recorded video stream from a smart glass using image processing and sensor-fusion.

For my senior year thesis project, I worked with two supervisors on using deep learning and augmented reality (AR) to train a set of robots to complete a construction task based on recorded sequence/set of actions taken by humans. I lead the group of my peers to accomplish this challenging research project requiring interdisciplinary knowledge – ML, machine vision, AR, robotics, and networking. Our paper titled “Deep Learning of Augmented Reality based Human Interactions for Automating a Robot Team” has been recently accepted to International Conference on Control, Automation and Robotics (ICCAR 2020).

The University of California Irvine’s Electrical and Computer Engineering PhD program resonates with my enthusiasm in computer architecture research. While I am willing to explore a variety of research by the faculty, work of Prof. Nader Bagherzadeh in network-on-chip architectures, Prof. Jean-Luc Gaudiot in low power microprocessor design, parallel and distributed processing research especially appeals to me. I am also particularly interested in the work carried out by Prof. Aparna Chandramowlishwaran related to high-performance computing and algorithm-architecture co-design research, and also Prof. Fadi Kurdahi related to power optimization and VLSI design research.

In conclusion, I believe that I have the right set of skills, motivation and above all, a passion for research in computer architecture which would make me a good fit for your Ph.D. program. Moreover, to be associated with such an esteemed institution would be a great advantage for me to serve the body of science and humanity. My future aspiration is to pursue a career in research and be part of the knowledge creation process, ideally in an industry research group that performs impactful research.