



# STM32 CubeMX

## 1. Description

### 1.1. Project

Project Name	poe
Board Name	custom
Generated with:	STM32CubeMX 6.16.1
Date	01/18/2026

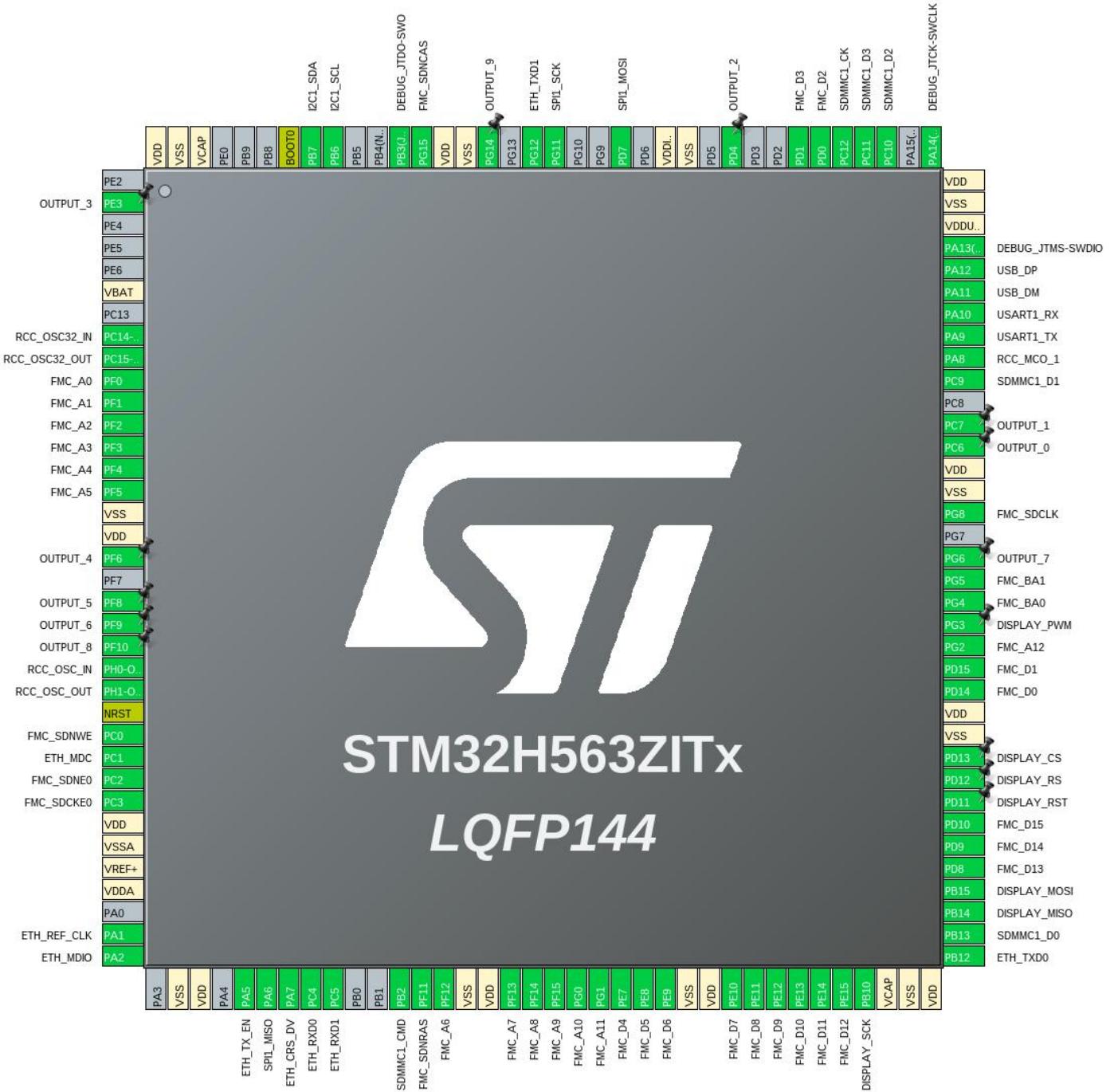
### 1.2. MCU

MCU Series	STM32H5
MCU Line	STM32H563/H573
MCU name	STM32H563ZITx
MCU Package	LQFP144
MCU Pin number	144

### 1.3. Core(s) information

Core(s)	ARM Cortex-M33
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## **2. Pinout Configuration**



### 3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
2	PE3 *	I/O	GPIO_Output	OUTPUT_3
6	VBAT	Power		
8	PC14- OSC32_IN(OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15- OSC32_OUT(OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
12	PF2	I/O	FMC_A2	
13	PF3	I/O	FMC_A3	
14	PF4	I/O	FMC_A4	
15	PF5	I/O	FMC_A5	
16	VSS	Power		
17	VDD	Power		
18	PF6 *	I/O	GPIO_Output	OUTPUT_4
20	PF8 *	I/O	GPIO_Output	OUTPUT_5
21	PF9 *	I/O	GPIO_Output	OUTPUT_6
22	PF10 *	I/O	GPIO_Output	OUTPUT_8
23	PH0-OSC_IN(PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT(PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	FMC_SDNWE	
27	PC1	I/O	ETH_MDC	
28	PC2	I/O	FMC_SDNE0	
29	PC3	I/O	FMC_SDCKE0	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
38	VSS	Power		
39	VDD	Power		
41	PA5	I/O	ETH_TX_EN	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	ETH_CRS_DV	

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Configuration Report

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Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	
48	PB2	I/O	SDMMC1_CMD	
49	PF11	I/O	FMC_SDNRAS	
50	PF12	I/O	FMC_A6	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FMC_A7	
54	PF14	I/O	FMC_A8	
55	PF15	I/O	FMC_A9	
56	PG0	I/O	FMC_A10	
57	PG1	I/O	FMC_A11	
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	
66	PE13	I/O	FMC_D10	
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
69	PB10	I/O	SPI2_SCK	DISPLAY_SCK
70	VCAP	Power		
71	VSS	Power		
72	VDD	Power		
73	PB12	I/O	ETH_TXD0	
74	PB13	I/O	SDMMC1_D0	
75	PB14	I/O	SPI2_MISO	DISPLAY_MISO
76	PB15	I/O	SPI2_MOSI	DISPLAY_MOSI
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
80	PD11 *	I/O	GPIO_Output	DISPLAY_RST
81	PD12 *	I/O	GPIO_Output	DISPLAY_RS
82	PD13 *	I/O	GPIO_Output	DISPLAY_CS
83	VSS	Power		
84	VDD	Power		

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Configuration Report

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Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
87	PG2	I/O	FMC_A12	
88	PG3 *	I/O	GPIO_Output	DISPLAY_PWM
89	PG4	I/O	FMC_BA0	
90	PG5	I/O	FMC_BA1	
91	PG6 *	I/O	GPIO_Output	OUTPUT_7
93	PG8	I/O	FMC_SDCLK	
94	VSS	Power		
95	VDD	Power		
96	PC6 *	I/O	GPIO_Output	OUTPUT_0
97	PC7 *	I/O	GPIO_Output	OUTPUT_1
99	PC9	I/O	SDMMC1_D1	
100	PA8	I/O	RCC_MCO_1	
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
103	PA11	I/O	USB_DM	
104	PA12	I/O	USB_DP	
105	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
106	VDDUSB	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
111	PC10	I/O	SDMMC1_D2	
112	PC11	I/O	SDMMC1_D3	
113	PC12	I/O	SDMMC1_CK	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
118	PD4 *	I/O	GPIO_Output	OUTPUT_2
120	VSS	Power		
121	VDDIO2	Power		
123	PD7	I/O	SPI1_MOSI	
126	PG11	I/O	SPI1_SCK	
127	PG12	I/O	ETH_TXD1	
129	PG14 *	I/O	GPIO_Output	OUTPUT_9
130	VSS	Power		
131	VDD	Power		
132	PG15	I/O	FMC_SDNCAS	
133	PB3(JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	

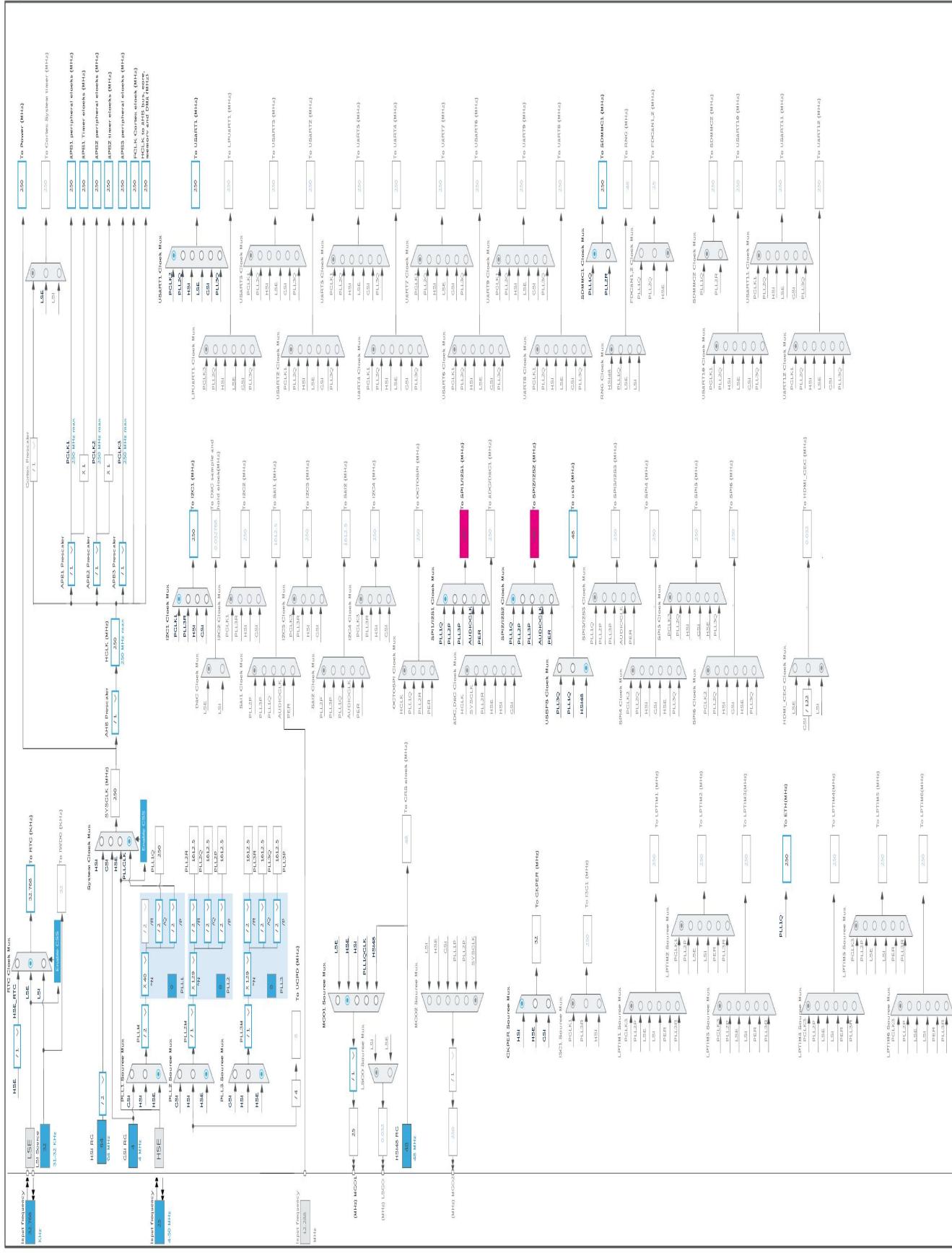
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Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
136	PB6	I/O	I2C1_SCL	
137	PB7	I/O	I2C1_SDA	
138	BOOT0	Boot		
142	VCAP	Power		
143	VSS	Power		
144	VDD	Power		

\* The pin is affected with an I/O function

## **4. Clock Tree Configuration**



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32H5
Line	STM32H563/H573
MCU	STM32H563ZITx
Datasheet	DS00000_Rev0

### 1.2. Parameter Selection

Temperature	25
Vdd	3.0

### 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

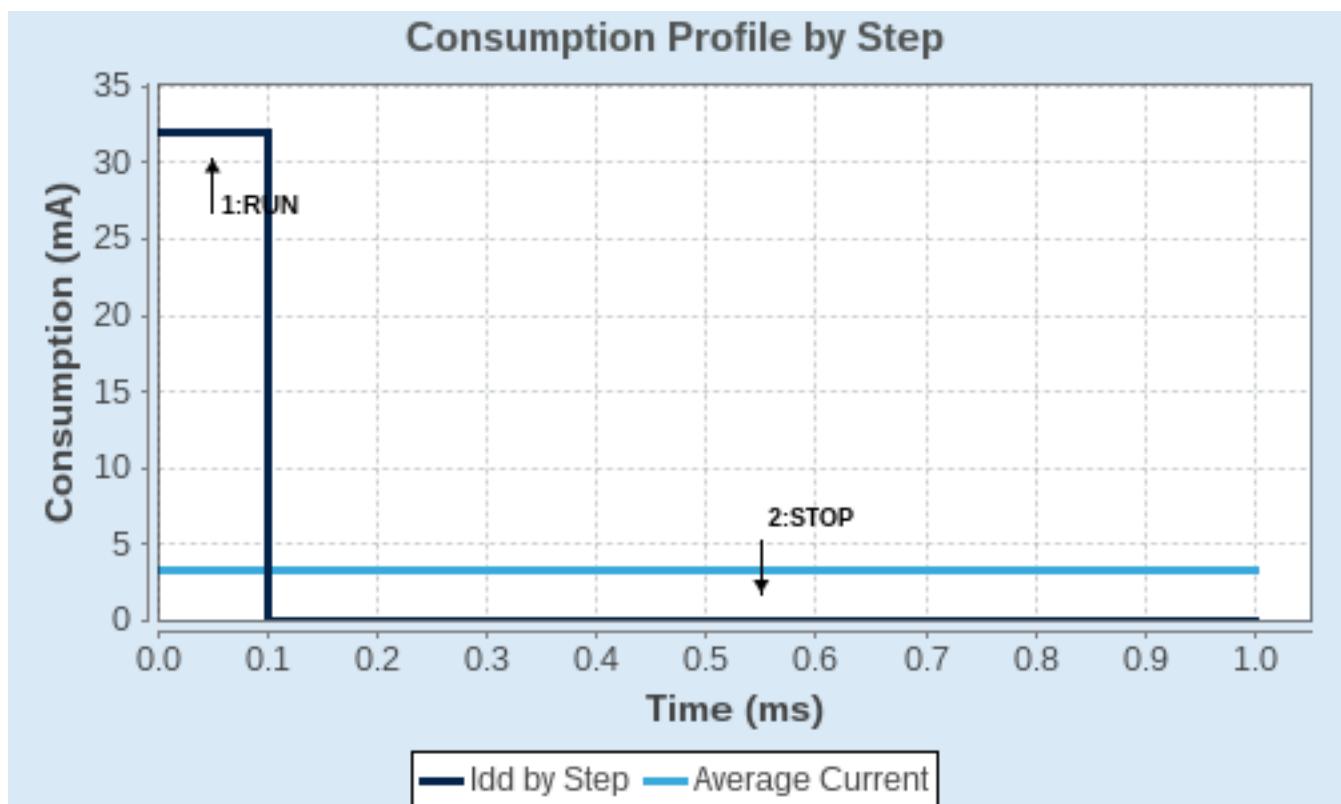
## 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	VOS0: Scale0	SVOS5: System-Scale5/SMPS
<b>Fetch Type</b>	FLASH_ON/Cache2Ways_A LL RAM RETENTION	Flash-PwrDwn PwrDwnStop OFF
<b>CPU Frequency</b>	250 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL	ALL_CLOCKS OFF
<b>Clock Source Frequency</b>	8 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	32 mA	51.5 µA
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	535.0	0.0
<b>T<sub>a</sub> Max</b>	120.78	124.99
<b>Category</b>	In DS Table	In DS Table

## 1.5. Results

Sequence Time	1 ms	Average Current	3.25 mA
Battery Life	1 month, 13 days, 4 hours	Average DMIPS	535.0 DMIPS

## 1.6. Chart



## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	poe
Project Folder	/home/rancune/devel_hw/RAS_hw.git/cubeMX
Toolchain / IDE	EWARM V9.20
Firmware Package Name and Version	STM32Cube FW_H5 V1.5.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c./h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DCACHE1_Init	DCACHE1
4	MX_ETH_Init	ETH
5	MX_FMC_Init	FMC
6	MX_I2C1_Init	I2C1
7	MX_ICACHE_Init	ICACHE
8	MX_RTC_Init	RTC
9	MX_SDMMC1_SD_Init	SDMMC1
10	MX_SPI1_Init	SPI1
11	MX_USART1_UART_Init	USART1

poe Project  
Configuration Report

Rank	Function Name	Peripheral Instance Name
12	MX_FileX_Init	FILEX
13	MX_SPI2_Init	SPI2
14	MX_USB_PCD_Init	USB

### **3. Peripherals and Middlewares Configuration**

#### **3.1. BOOTPATH**

**mode:** Activated

#### **3.2. DCACHE1**

**mode:** Activated

##### 3.2.1. Parameter Settings:

**Basic Parameters:**

DCACHE Read Burst Type	DCACHE READ BURST WRAP
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#### **3.3. DEBUG**

**Debug:** Trace Asynchronous Sw

#### **3.4. ETH**

**Mode:** RMII

##### 3.4.1. Parameter Settings:

**General : Ethernet Configuration:**

Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
Rx Descriptor Length	4
Rx Buffers Length	1524

#### **3.5. FMC**

**SDRAM 1**

**Clock and chip enable: SDCKE0+SDNE0**

**Internal bank number: 4 banks**

**Address: 13 bits**

**Data: 16 bits**

##### 3.5.1. SDRAM 1:

**SDRAM control:**

Bank	SDRAM bank 1
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Number of column address bits	8 bits
Number of row address bits	13 bits
CAS latency	1 memory clock cycle
Write protection	Disabled
SDRAM common clock	Disabled
SDRAM common burst read	Disabled
SDRAM common read pipe delay	0 HCLK clock cycle

#### **SDRAM timing in memory clock cycles:**

Load mode register to active delay	16
Exit self-refresh delay	16
Self-refresh time	16
SDRAM common row cycle delay	16
Write recovery time	16
SDRAM common row precharge delay	16
Row to column delay	16

### **3.6. I2C1**

#### **I2C: I2C**

##### 3.6.1. Parameter Settings:

#### **Timing configuration:**

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	<b>0x60808CD3 *</b>

#### **Slave Features:**

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

### **3.7. ICACHE**

#### **mode: Memory address remap**

### 3.7.1. Parameter Settings:

#### **Region 0:**

Region Disable

#### **Region 1:**

Region Disable

#### **Region 2:**

Region Disable

#### **Region 3:**

Region Disable

## **3.8. MEMORYMAP**

**mode: Activated**

## **3.9. PWR**

**mode: Power saving mode**

**mode: Privilege attributes**

### 3.9.1. PWR Privilege :

#### **Privilege PWR:**

PWR Privilege Disable

## **3.10. RCC**

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

**mode: Master Clock Output 1**

### 3.10.1. RCC Privilege :

#### **Privilege RCC:**

Privilege of RCC Non-Secure Items Disable

### 3.10.2. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3

Flash Latency(WS) 5 WS (6 CPU cycle)

Flash Programming Delay 2

**RCC Parameters:**

HSI Calibration Value 64

CSI Calibration Value 32

HSE Startup Timeout Value (ms) 100

LSE Startup Timeout Value (ms) 5000

LSE Drive Capability LSE oscillator low drive capability

TIM Prescaler Selection Disabled

**Power Parameters:**

Power Regulator Voltage Scale Power Regulator Voltage Scale 0

### 3.11. RTC

**mode: Activate Clock Source**

3.11.1. Parameter Settings:

**General:**

Hour Format Hourformat 24

Asynchronous Predivider value 127

Synchronous Predivider value 255

Bin Mode Free running BCD calendar mode

3.11.2. RTC Privilege:

**Privilege RTC:**

RTC full privilege Disable

**Backup register:**

Start zone 1 RTC\_BKP\_DR0

Start Zone 2 RTC\_BKP\_DR0

start zone 3 RTC\_BKP\_DR0

**Privilege Backup register :**

Backup Register PrivZone Non-privilege

**Privilege RTC Feature:**

RTC Initialisation Non-Privilege

RTC Alarm A Non-Privilege

RTC Alarm B Non-Privilege

RTC Calibration Non-Privilege

RTC TimeStamp Non-Privilege

RTC WakeUpTimer Non-Privilege

### 3.12. SDMMC1

**Mode: SD 4 bits Wide bus**

#### 3.12.1. Parameter Settings:

##### **SDMMC parameters:**

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	0
Is external transceiver present ?	no

### 3.13. SPI1

**Mode: Full-Duplex Master**

#### 3.13.1. Parameter Settings:

##### **Basic Parameters:**

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

##### **Clock Parameters:**

Prescaler (for Baud Rate)	2
Baud Rate	<b>125.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

##### **CRC Parameters:**

CRC Calculation	Disabled
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##### **Advanced Parameters:**

NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

Ready Master Management	Internal
Ready Signal Polarity	High

### 3.14. SPI2

#### Mode: Full-Duplex Master

##### 3.14.1. Parameter Settings:

###### **Basic Parameters:**

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

###### **Clock Parameters:**

Prescaler (for Baud Rate)	2
Baud Rate	<b>125.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

###### **CRC Parameters:**

CRC Calculation	Disabled
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###### **Advanced Parameters:**

NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled
Ready Master Management	Internal
Ready Signal Polarity	High

### 3.15. SYS

#### Timebase Source: TIM6

### 3.16. USART1

#### Mode: Asynchronous

### 3.16.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### **Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

#### **Advanced Features:**

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

## **3.17. USB**

### **Mode: Device\_Only**

### 3.17.1. Parameter Settings:

#### **Basic Parameters:**

Speed	Full Speed 12MBit/s
Physical interface	Internal Phy
Signal start of frame	Disabled

#### **Power Parameters:**

Low Power	Disabled
Link Power Management	Disabled
Battery Charging	Disabled

#### **EndPoint Parameters:**

Bulk double buffer	Disabled
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Iso single buffer	Disabled
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### 3.18. FILEX

**mode: FileX Core**

**mode: Internal RAM interface**

**mode: SD interface**

#### 3.18.1. FileX:

##### **Core:**

FX_EXFAT_MAX_CACHE_SIZE	512
FXFAULT_TOLERANT_CACHE_SIZE	1024
FX_FAULT_TOLERANT_CACHE_SIZE_NB_SIZE	10
FX_EXFAT_MAX_CACHE_SIZE_NB_BIT	9
FX_DISABLE_DIRECT_DATA_READ_CACHE_FILL	Disabled
FX_DISABLE_ERROR_CHECKING	Disabled
FX_DONT_UPDATE_OPEN_FILES	Disabled
FX_DRIVER_USE_64BIT_LBA	Disabled
FX_ENABLE_EXFAT	Disabled
FX_ENABLE_FAULT_TOLERANT	Disabled
FX_FAT_MAP_SIZE	128
FX_FAULT_TOLERANT	Disabled
FX_FAULT_TOLERANT_BOOT_INDEX	116
FX_FAULT_TOLERANT_DATA	Disabled
FX_MAX_FAT_CACHE	16
FX_MAX_LAST_NAME_LEN	256
FX_MAX_LONG_NAME_LEN	256
FX_MAX_SECTOR_CACHE	256
FX_MEDIA_DISABLE_SEARCH_CACHE	Disabled
FX_MEDIA_STATISTICS_DISABLE	Disabled
FX_RENAME_PATH_INHERIT	Disabled
FX_SINGLE_OPEN_LEGACY	Disabled
FX_UPDATE_RATE_IN_SECONDS	10
FX_UPDATE_RATE_IN_TICKS	1000
MAX_FAT_CACHE_NB_BIT	4
MAX_SECTOR_CACHE_NB_BIT	8
FX_DISABLE_CACHE	Disabled
FX_DISABLE_FILE_CLOSE	Disabled
FX_DISABLE_FAST_OPEN	Disabled
FX_DISABLE_FORCE_MEMORY_OPERATION	Disabled
FX_DISABLE_BUILD_OPTIONS	Disabled

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Configuration Report

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FX_DISABLE_ONE_LINE_FUNCTION	Disabled
FX_DISABLE_FAT_ENTRY_REFRESH	Disabled
FX_DISABLE_CONSECUTIVE_DETECT	Disabled
FX_SINGLE_THREAD	Disabled
FX_NO_LOCAL_PATH	Disabled
FX_NO_TIMER	Disabled

**Version:**

FileX version	6.4.0
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**Memory Configuration:**

FileX memory pool size	1024
FileX MemPool Name	fx_app_byte_pool

**FileX Core Init:**

FileX Generate Init Code	true
FileX Application Thread Entry Name	fx_app_thread_entry
FileX Application Thread Priority	10
FileX Application Thread Stack Size.	512

**FileX Drivers:**

Link SRAM Driver	true
Format SRAM Media	true
Link SD Driver	true
Format SD Media	false

**SRAM Disk:**

SRAM Disk Address ranges	SRAM3_BASE_NS (0x20050000UL)
SRAM Disk Address	<b>0x20050000 *</b>
SRAM Disk Size	8192

**SD Driver:**

SD instance	SDMMC1
FX Driver Initializes the SD IP	<b>true *</b>
Glue Function Implementation	HAL DMA API
Transfer Completion Mechanism	ThreadX Semaphore

### 3.19. THREADX

**mode: Core**

3.19.1. ThreadX:

**Core:**

TX_MINIMUM_STACK	200
TX_THREAD_USER_EXTENSION	
TX_DISABLE_STACK_FILLING	Disabled

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Configuration Report

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TX_ENABLE_STACK_CHECKING	Disabled
TX_DISABLE_PREEMPTION_THRESHOLD	Enabled
TX_DISABLE_REDUNDANT_CLEARING	Disabled
TX_DISABLE_NOTIFY_CALLBACKS	Enabled
TX_INLINE_THREAD_RESUME_SUSPEND	Disabled
TX_NOT_INTERRUPTABLE	Disabled
TX_MAX_PRIORITIES	32
TX_TIMER_TICKS_PER_SECOND	100
TX_NO_FILEX_POINTER	Disabled
Enable BASEPRI support	Disabled
TX_DISABLE_ERROR_CHECKING	Disabled

**Timer:**

TX_TIMER_PROCESS_IN_ISR	Disabled
TX.REACTIVATE_INLINE	Disabled
TX_TIMER_THREAD_STACK_SIZE	1024
TX_TIMER_THREAD_PRIORITY	0

**Version:**

ThreadX version	6.4.0
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**ThreadX App Init:**

Generate App Init Code	false
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**Memory Configuration:**

ThreadX memory pool size	1024
Memory Pool Allocation	Use Static Allocation
ThreadX MemPool Name	tx_app_byte_pool

\* User modified value

## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PB3(JTDO/T-RACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA5	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG12	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	High	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC2	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

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Configuration Report

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FMC	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG2	FMC_A12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN(OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT(OSC32_O)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN(PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT(PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PA8	RCC_MCO_1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SDMMC1	PB2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB13	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	High	
SPI1	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	DISPLAY_SCK

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	DISPLAY_MISO
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	DISPLAY_MOSI
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB	PA11	USB_DM	n/a	n/a	n/a	
	PA12	USB_DP	n/a	n/a	n/a	
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT_3
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT_4
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT_5
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT_6
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT_8
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISPLAY_RST
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISPLAY_RS
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISPLAY_CS
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISPLAY_PWM
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT_7
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT_0
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT_1
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT_2
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OUTPUT_9

## 4.2. GPDMA1

## 4.3. GPDMA2

## 4.4. LINKEDLIST

## 4.5. NVIC configuration

### 4.5.1. NVIC

Interrupt Table	Enable	Preenemption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	14	0
TIM6 global interrupt	true	15	0
SDMMC1 global interrupt	true	2	0
Flash non-secure global interrupt		unused	
RCC non-secure global interrupt		unused	
I2C1 Event interrupt		unused	
I2C1 Error interrupt		unused	
SPI1 global interrupt		unused	
SPI2 global interrupt		unused	
USART1 global interrupt		unused	
USB FS global interrupt		unused	
FMC global interrupt		unused	
FPU global interrupt		unused	
Instruction cache global interrupt		unused	
Data cache global interrupt		unused	
Ethernet global interrupt		unused	
Ethernet Wakeup global interrupt		unused	

### 4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false

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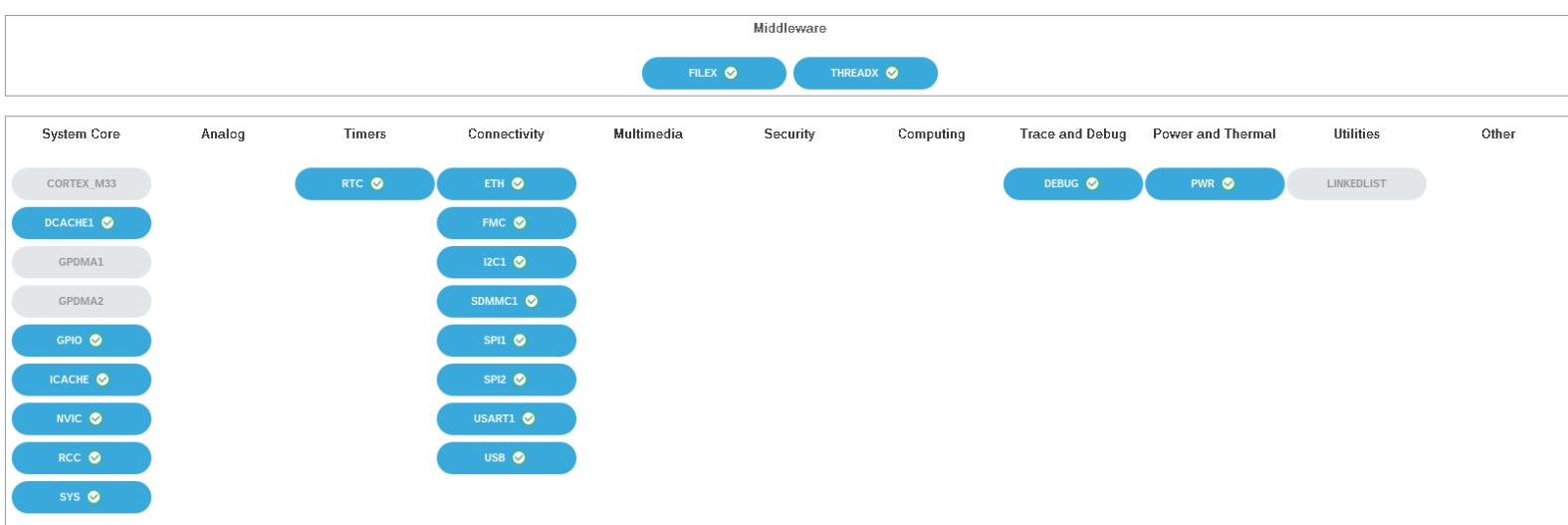
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System tick timer	false	false	true
TIM6 global interrupt	false	true	true
SDMMC1 global interrupt	false	true	true

\* User modified value

## 5. System Views

### 5.1. Category view

#### 5.1.1. Current



## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32h5-bsdl.zip">https://www.st.com/resource/en/bsdl_model/stm32h5-bsdl.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32h5-ibis.zip">https://www.st.com/resource/en/ibis_model/stm32h5-ibis.zip</a>
System View	<a href="https://www.st.com/resource/en/svd/stm32h5-svd.zip">https://www.st.com/resource/en/svd/stm32h5-svd.zip</a>
Description	
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf</a>
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Security Bulletin	<a href="https://www.st.com/resource/en/technical_note/tn1474-security-bulletin-tn1474stpsirt-information-on-softwarebased--microarchitectural-timing-sidechannel-attacks-on-mcus-with-trustzone-for--armv8m-">https://www.st.com/resource/en/technical_note/tn1474-security-bulletin-tn1474stpsirt-information-on-softwarebased--microarchitectural-timing-sidechannel-attacks-on-mcus-with-trustzone-for--armv8m-</a>

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