

**section** *DisBufferSpec* **parents** *circus\_toolkit*

$maxbuff : \mathbb{N}_1$ $maxring : \mathbb{N}_1$	$maxring = maxbuff - 1$
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*RingIndex* == 1 .. *maxring*

**channel** *input, output* :  $\mathbb{N}$   
**channel** *read, write* :  $(RingIndex) \times \mathbb{N}$   
**channel** *rd, wrt* :  $\mathbb{N}$   
**channel** *rd\_i, wrt\_i* :  $(RingIndex) \times \mathbb{N}$

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process Controller  $\hat{=}$  begin
  state ControllerState == [
    size :  $0 \dots \text{maxbuff}$ ;
    ringsize :  $0 \dots \text{maxring}$ ;
    cache :  $\mathbb{N}$ ;
    top, bot : RingIndex |
    ringsize mod maxring = (top - bot) mod maxring  $\wedge$ 
    ringsize =  $\max \{0, \text{size} - 1\}$  ]
  ControllerInit == [ (ControllerState)' |
    top' = 1  $\wedge$  bot' = 1  $\wedge$  size' = 0 ]
  CacheInput == [  $\Delta \text{ControllerState}$ ; x? :  $\mathbb{N}$  |
    size = 0  $\wedge$  size' = 1  $\wedge$ 
    cache' = x?  $\wedge$  bot' = bot  $\wedge$  top' = top ]
  StoreInputController == [  $\Delta \text{ControllerState}$  |
    0 < size  $\wedge$  size < maxbuff  $\wedge$  size' = size + 1  $\wedge$ 
    cache' = cache  $\wedge$  bot' = bot  $\wedge$  top' = (top mod maxring) + 1 ]
  InputController  $\hat{=}$  (size < maxbuff)  $\&$  input?x  $\longrightarrow$ 
    ((size = 0)  $\&$  (CacheInput))  $\square$ 
    (size > 0)  $\&$  write.top!x  $\longrightarrow$  (StoreInputController)
  NoNewCache == [  $\Delta \text{ControllerState}$  |
    size = 1  $\wedge$  size' = 0  $\wedge$ 
    cache' = cache  $\wedge$  bot' = bot  $\wedge$  top' = top ]
  StoreNewCacheController == [  $\Delta \text{ControllerState}$ ; x? :  $\mathbb{N}$  |
    size > 1  $\wedge$  size' = size - 1  $\wedge$ 
    cache' = x?  $\wedge$  bot' = (bot mod maxring) + 1  $\wedge$ 
    top' = top ]
  OutputController  $\hat{=}$  (size > 0)  $\&$  output!(cache)  $\longrightarrow$ 
    ((size > 1)  $\&$  read.bot?x  $\longrightarrow$  (StoreNewCacheController))  $\square$ 
    (size = 1)  $\&$  (NoNewCache)
  • (ControllerInit) ; ( $\mu X$  • (InputController  $\square$  OutputController) ; X)
end

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process RingCell  $\hat{=}$  begin
  state CellState == [ v :  $\mathbb{N}$  | true ]
  CellWrite == [  $\Delta \text{CellState}$ ; x? :  $\mathbb{N}$  | v' = x? ]
  Read  $\hat{=}$  rd!v  $\longrightarrow$  Skip
  Write  $\hat{=}$  wrt?x  $\longrightarrow$  (CellWrite)
  • ( $\mu X$  • (Read  $\square$  Write) ; X)
end

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process IRCell  $\hat{=}$  (i : RingIndex  $\odot$  RingCell)[rdi, wrti := read, write]

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**process**  $Ring \hat{=} ( \parallel i : RingIndex \bullet IRCell[i] )$

**process**  $Buffer \hat{=} ( Controller \parallel \{ read, write \} Ring ) \setminus \{ read, write \}$