Curriculum Vitae

Personal Information

Name: Zecheng Li   Gender: Male

Nationality: China   Date of birth: 1999. 11.22

Email: li.zecheng.t2@dc.tohoku.ac.jp   Tel: +81 070-9119-5102

Education

Bachelor of Engineering

Beijing Normal University, Zhuhai, China   2018.09 - 2022.06

Major: Measurement Control Technology and Instruments (3.2/4, Rank 15%)

Supervisor: Yi Zhao Yi Zhao – IEEE Xplore Author Profile

Master of Science

Tohoku University, Sendai, Japan (Current, 3.2/4)   2022.10 - 2024.09

Major: Computer Architecture

Supervisor: Hiroaki Kobayashi Hiroaki KOBAYASHI | Tohoku University, Sendai | Tohokudai | Research profile (researchgate.net)

Research Projects

- Design of DDS and Oscilloscope System Based on FPGA
  Provincial level of the innovation project of university students

- Smart cache system for Disaggregated Memory System
  Master Thesis

Publication

- Memory Page Prefetching for Disaggregated Memory Systems. Zecheng Li, Masayuki Sato, Kazuhiko Komatsu, and Hiroaki Kobayashi (2023)
Multidisciplinary Seminar/Multidisciplinary Seminar Preprint 4.pdf at main • Randolph7/Multidisciplinary Seminar (github.com)

Internship

- Zhuhai Atomic Technology Co., Ltd.   2021.04 - 2021.08
  Internship at the integrated circuit department
  Understand the placement and routing algorithm, verilog simulation, the current development of tsv-based-3 dIC.

- Allwinner Technology Co., Ltd.   2021.09 - 2022.06
  Internship as the Embedded Software Engineer.
  Develop Pedestrian Detection System Based on Allwinner D1-RISC-V Processor, Designed a compact development board, ported the NanoDet model, and broadcast detection results of pedestrain to other devices via BLE.

- Guangdong Institute of intelligent technology and technology.   2022.09 - 2023.02
  Supervisor:
  Li-Rong Zheng https://gdiist.cn/research/team_detail/6
  Yuxiang Huan https://gdiist.cn/research/team_detail/13

  Brain-like Computing Research Group, FPGA & Software Intern.
  Porting and FPGA Verification of RISC-V Processor CVA6: Modified CVA6
  processor for FPGA booting, completed SoC trimming, and verified booting on
  FPGA. Migrating the MPI standard to the bare-metal muiltcore NoC system.

Awards and Prizes

- Professional Excellence Scholarship   2019. 10
                                                                2020. 10 & 2021. 10

- National Inspirational Scholarship

- Second prize of the National Software and Information Technology Professional
Talent   Competition   Electronic   Contest   MCU   Design   and   Development
                                                                         2020. 10
- Third prize of the National   Software and Information Technology Professional
Talent Competition Electronic Contest MCU Design and Development   2021.04

- First prize of the English speech contest BNUZ   2018. 11 & 2019.

Others

Languages: Chinese&Cantonese(native), English (fluent), Japanese(beginner)
Programming language: C/C++, Verilog HDL, Python
Programming software: ChampSim, gem5,Visual Studio Code,Vivado,Keil
Experimental equipment : Oscilloscope, Modelsim Simulation, DDS