

MOSFET

StrongIRFET™ 2 Power-Transistor, 30 V

Features

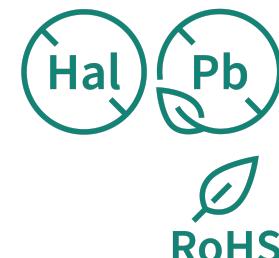
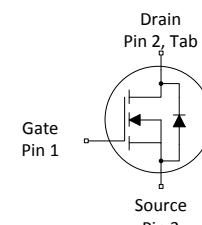
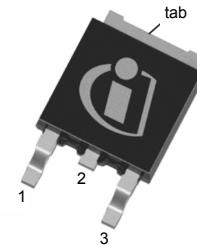
- Optimized for a wide range of applications
- N-channel, logic level
- 100% avalanche tested
- 175°C rated
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	4.7	mΩ
I_D	71	A
Q_{oss}	17	nC
$Q_G(0V..4.5V)$	10	nC



Type/Ordering Code	Package	Marking	Related Links
IPD047N03LF2S	PG-T0252-3	047N03F2	-

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1 Maximum ratings

at $T_A=25\text{ }^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	71 55 19	A	$V_{GS}=10\text{ V}, T_C=25\text{ }^\circ\text{C}$ $V_{GS}=10\text{ V}, T_C=100\text{ }^\circ\text{C}$ $V_{GS}=10\text{ V}, T_A=25\text{ }^\circ\text{C}, R_{THJA}=50\text{ }^\circ\text{C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	284	A	$T_A=25\text{ }^\circ\text{C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	54 107	mJ	$I_D=40\text{ A}, R_{GS}=25\Omega$ $I_D=20\text{ A}, R_{GS}=25\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	65 3	W	$T_C=25\text{ }^\circ\text{C}$ $T_A=25\text{ }^\circ\text{C}, R_{THJA}=50\text{ }^\circ\text{C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.3	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}	-	-	50	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	75	°C/W	-

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	30	-	-	V	$V_{\text{GS}}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{\text{GS}(\text{th})}$	1.35	1.85	2.35	V	$V_{\text{DS}}=V_{\text{GS}}$, $I_D=30\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{\text{DS}}=30\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=25^\circ\text{C}$ $V_{\text{DS}}=30\text{ V}$, $V_{\text{GS}}=0\text{ V}$, $T_j=125^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{\text{GS}}=20\text{ V}$, $V_{\text{DS}}=0\text{ V}$
Drain-source on-state resistance	$R_{\text{DS}(\text{on})}$	-	4.1 5.1	4.7 7.3	$\text{m}\Omega$	$V_{\text{GS}}=10\text{ V}$, $I_D=40\text{ A}$ $V_{\text{GS}}=4.5\text{ V}$, $I_D=20\text{ A}$
Gate resistance	R_G	-	1.9	-	Ω	-
Transconductance ⁶⁾	g_{fs}	45	-	-	S	$ V_{\text{DS}} \geq 2 I_D R_{\text{DS}(\text{on})\text{max}}$, $I_D=40\text{ A}$

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1400	-	pF	$V_{\text{GS}}=0\text{ V}$, $V_{\text{DS}}=15\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	290	-	pF	$V_{\text{GS}}=0\text{ V}$, $V_{\text{DS}}=15\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	80	-	pF	$V_{\text{GS}}=0\text{ V}$, $V_{\text{DS}}=15\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{\text{d}(\text{on})}$	-	11	-	ns	$V_{\text{DD}}=15\text{ V}$, $V_{\text{GS}}=4.5\text{ V}$, $I_D=40\text{ A}$, $R_{\text{G,ext}}=1.6\text{ }\Omega$
Rise time	t_r	-	10	-	ns	$V_{\text{DD}}=15\text{ V}$, $V_{\text{GS}}=4.5\text{ V}$, $I_D=40\text{ A}$, $R_{\text{G,ext}}=1.6\text{ }\Omega$
Turn-off delay time	$t_{\text{d}(\text{off})}$	-	10	-	ns	$V_{\text{DD}}=15\text{ V}$, $V_{\text{GS}}=4.5\text{ V}$, $I_D=40\text{ A}$, $R_{\text{G,ext}}=1.6\text{ }\Omega$
Fall time	t_f	-	6.4	-	ns	$V_{\text{DD}}=15\text{ V}$, $V_{\text{GS}}=4.5\text{ V}$, $I_D=40\text{ A}$, $R_{\text{G,ext}}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics⁷⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	4.9	-	nC	$V_{\text{DD}}=15\text{ V}$, $I_D=40\text{ A}$, $V_{\text{GS}}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{\text{g}(\text{th})}$	-	2.6	-	nC	$V_{\text{DD}}=15\text{ V}$, $I_D=40\text{ A}$, $V_{\text{GS}}=0\text{ to }4.5\text{ V}$
Gate to drain charge	Q_{gd}	-	3.3	-	nC	$V_{\text{DD}}=15\text{ V}$, $I_D=40\text{ A}$, $V_{\text{GS}}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	5.6	-	nC	$V_{\text{DD}}=15\text{ V}$, $I_D=40\text{ A}$, $V_{\text{GS}}=0\text{ to }4.5\text{ V}$
Gate charge total ⁸⁾	Q_g	-	10	15	nC	$V_{\text{DD}}=15\text{ V}$, $I_D=40\text{ A}$, $V_{\text{GS}}=0\text{ to }4.5\text{ V}$

Table 6 Gate charge characteristics⁷⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate plateau voltage	V_{plateau}	-	3.5	-	V	$V_{\text{DD}}=15 \text{ V}$, $I_{\text{D}}=40 \text{ A}$, $V_{\text{GS}}=0 \text{ to } 4.5 \text{ V}$
Gate charge total ⁸⁾	Q_g	-	21	32	nC	$V_{\text{DD}}=15 \text{ V}$, $I_{\text{D}}=40 \text{ A}$, $V_{\text{GS}}=0 \text{ to } 10 \text{ V}$
Gate charge total, sync. FET	$Q_{g(\text{sync})}$	-	8.9	-	nC	$V_{\text{DS}}=0.1 \text{ V}$, $V_{\text{GS}}=0 \text{ to } 4.5 \text{ V}$
Output charge	Q_{oss}	-	17	-	nC	$V_{\text{DS}}=15 \text{ V}$, $V_{\text{GS}}=0 \text{ V}$

⁷⁾ See "Gate charge waveforms" for parameter definition⁸⁾ Defined by design. Not subject to production test.**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	55	A	$T_c=25 \text{ }^\circ\text{C}$
Diode pulse current	$I_{S,\text{pulse}}$	-	-	284	A	$T_c=25 \text{ }^\circ\text{C}$
Diode forward voltage	V_{SD}	-	0.87	1.0	V	$V_{\text{GS}}=0 \text{ V}$, $I_F=40 \text{ A}$, $T_j=25 \text{ }^\circ\text{C}$
Reverse recovery time	t_{rr}	-	15	-	ns	$V_R=15 \text{ V}$, $I_F=40 \text{ A}$, $di_F/dt=500 \text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	34	-	nC	$V_R=15 \text{ V}$, $I_F=40 \text{ A}$, $di_F/dt=500 \text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

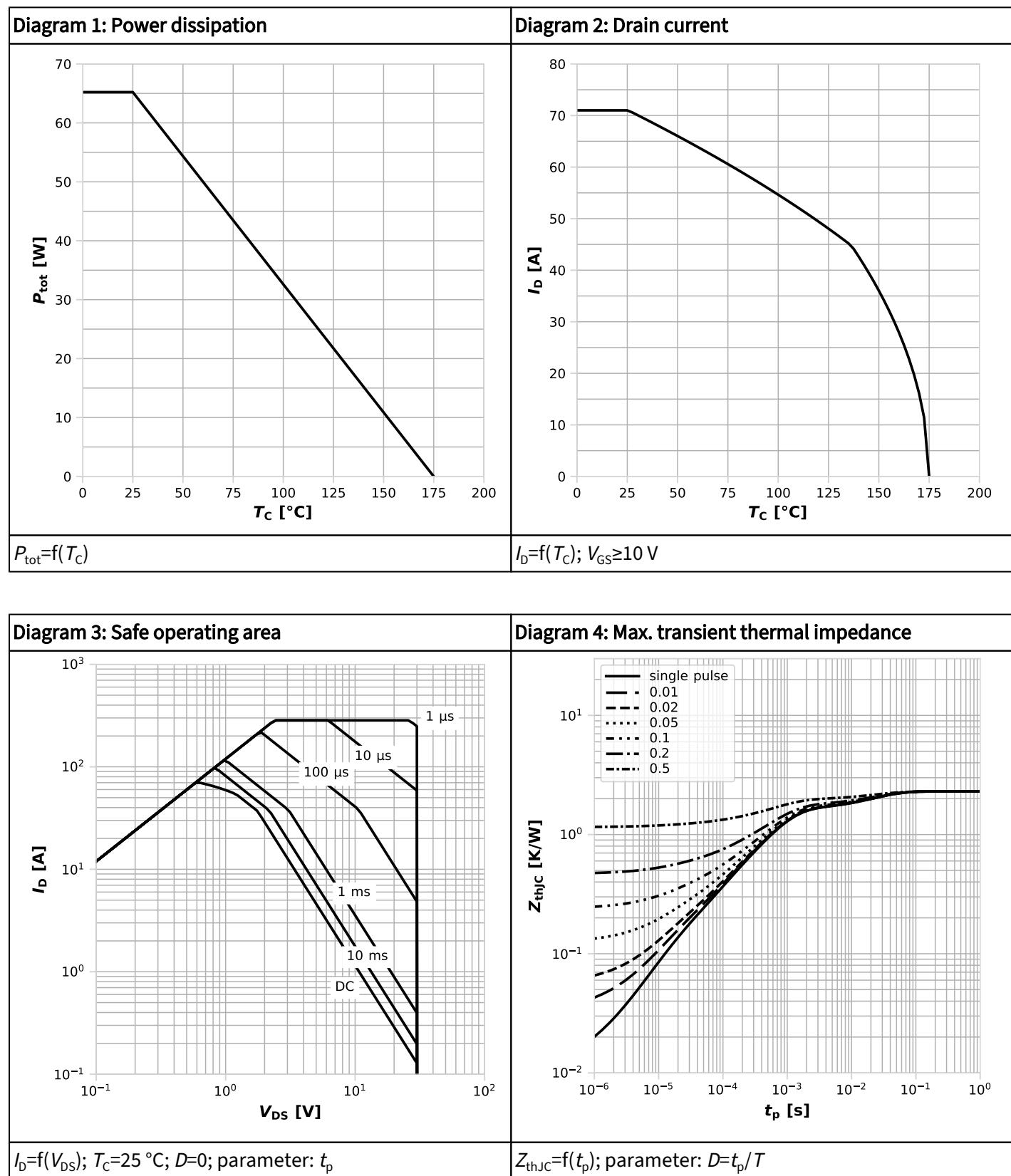


Diagram 5: Typ. output characteristics

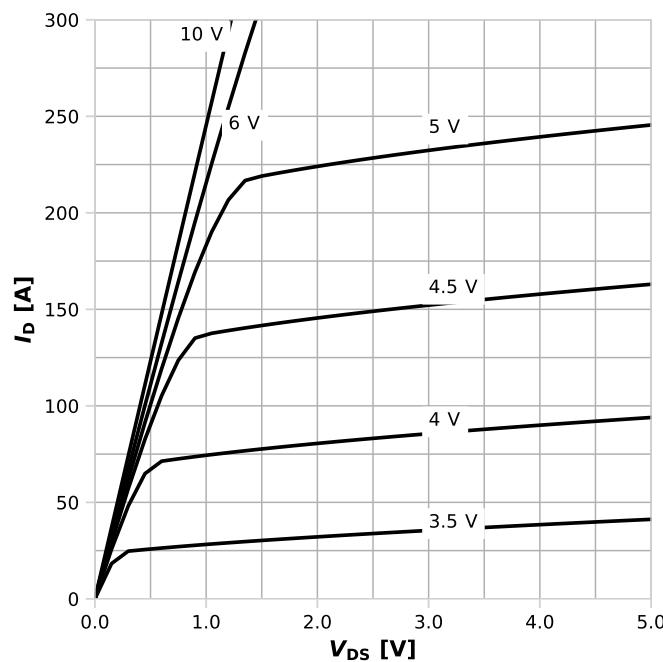

 $I_D=f(V_{DS})$, $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance

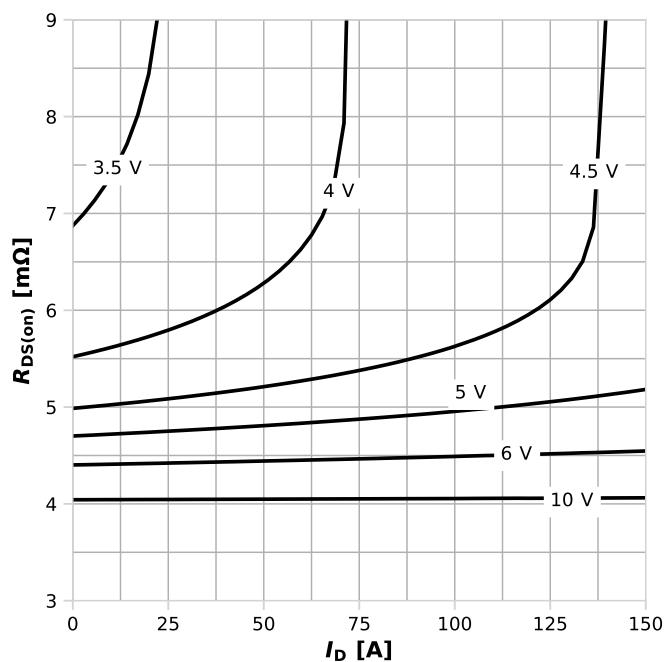

 $R_{DS(on)}=f(I_D)$, $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics

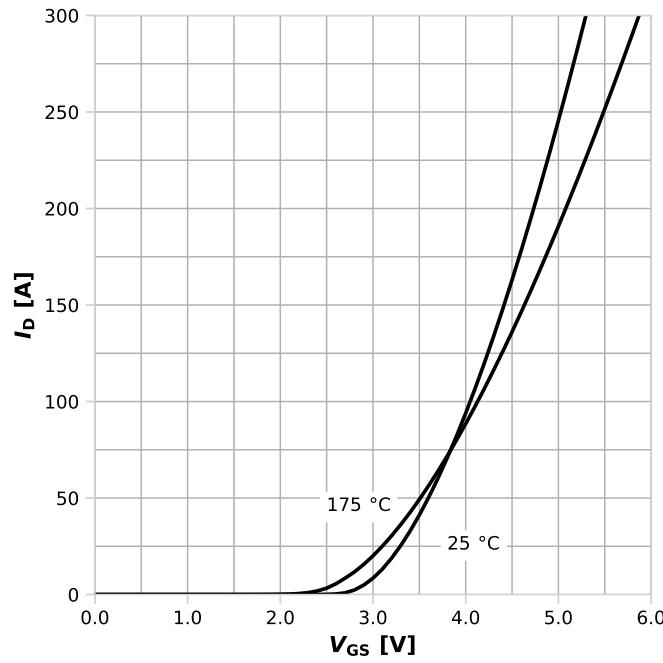

 $I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance

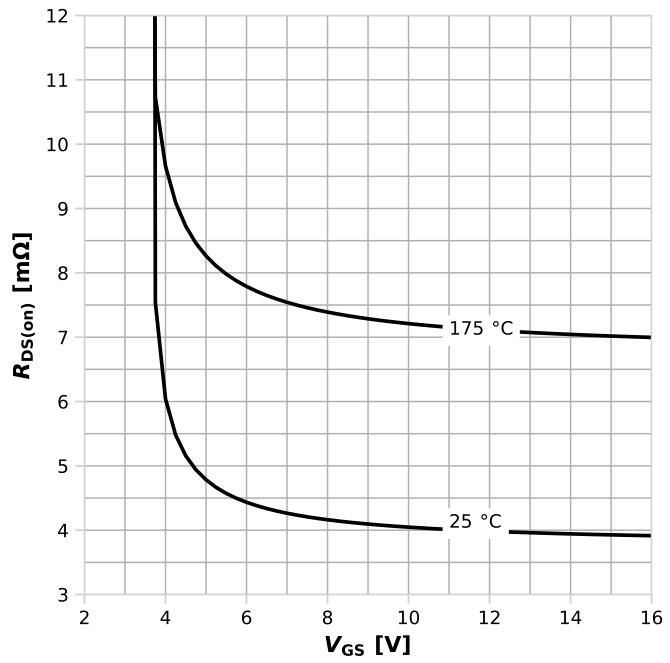

 $R_{DS(on)}=f(V_{GS})$, $I_D=40\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance

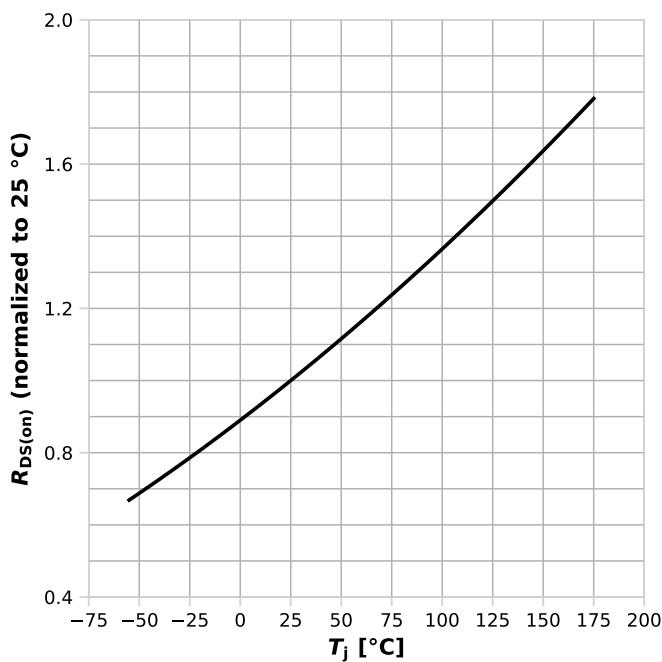

 $R_{DS(on)} = f(T_j), I_D = 40 \text{ A}, V_{GS} = 10 \text{ V}$

Diagram 10: Typ. gate threshold voltage

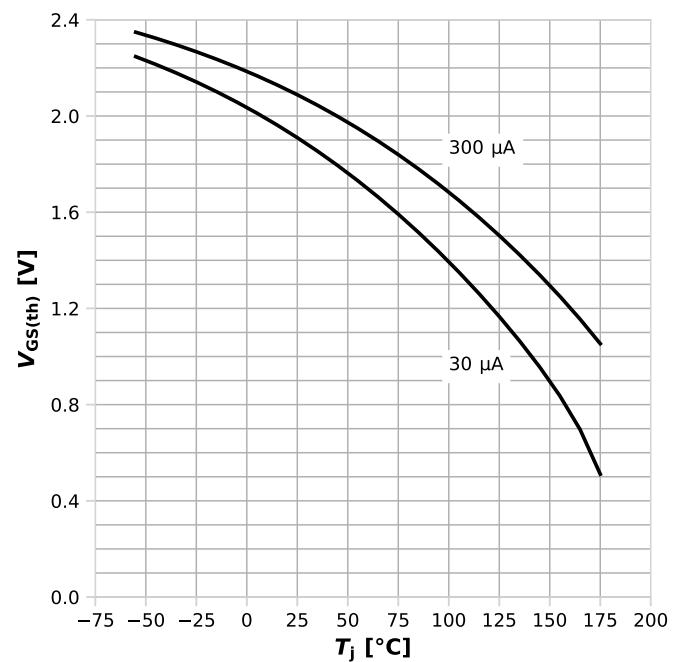

 $V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$

Diagram 11: Typ. capacitances

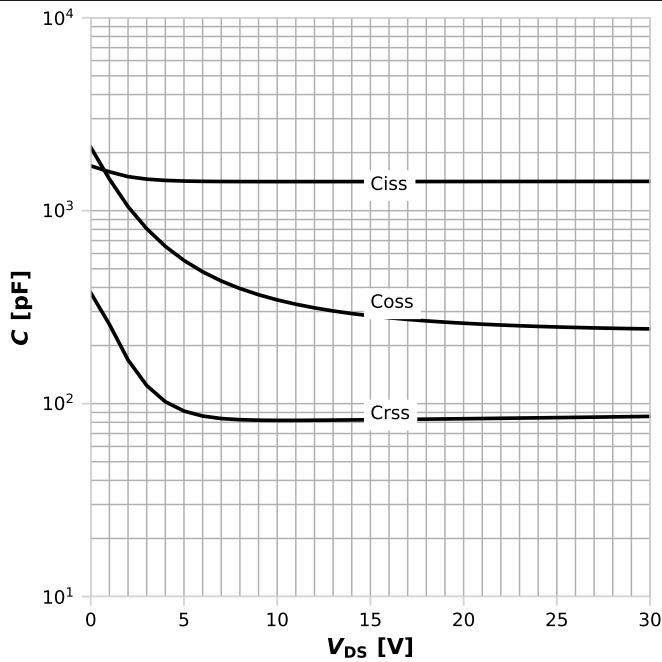

 $C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Diagram 12: Forward characteristics of reverse diode

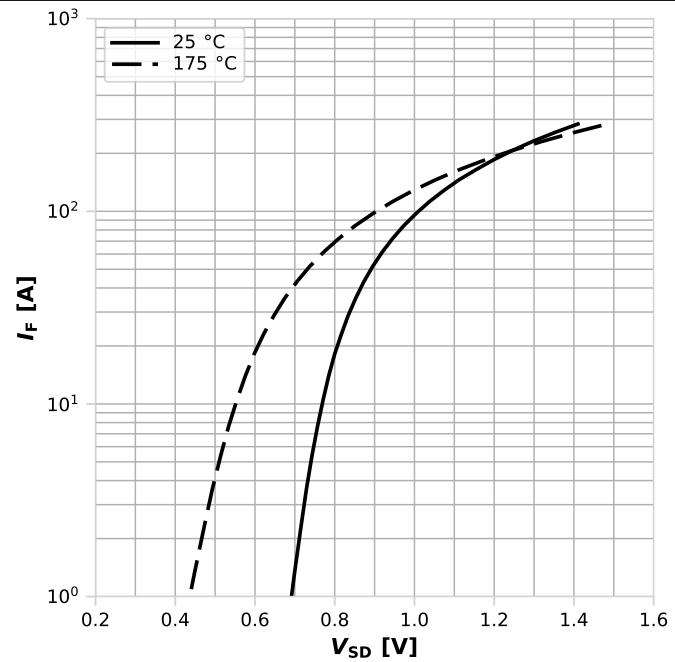
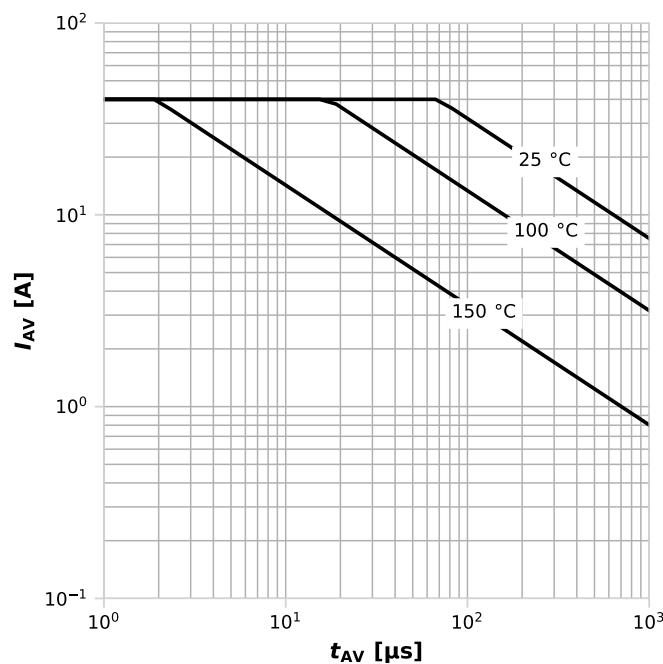
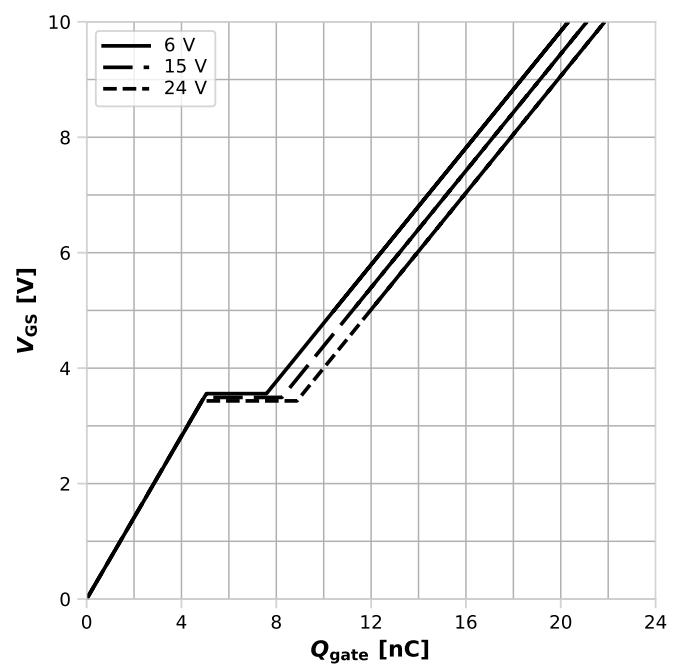

 $I_F = f(V_{SD}); \text{ parameter: } T_j$

Diagram 13: Avalanche characteristics



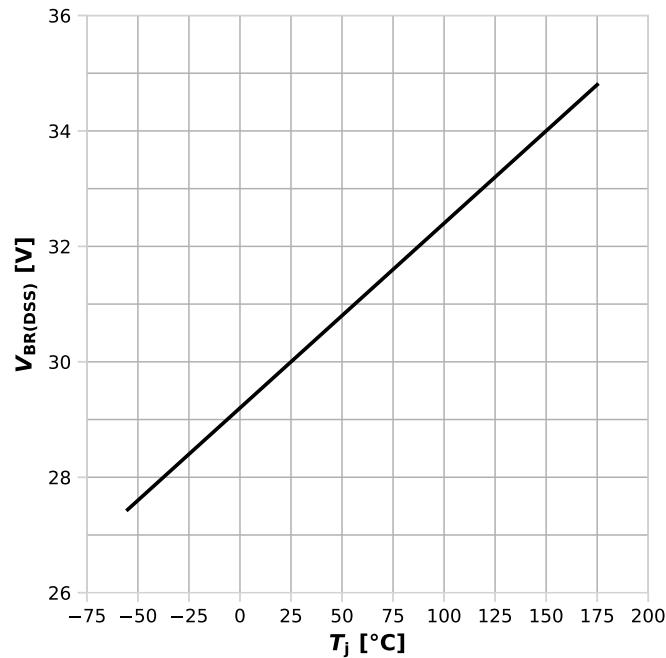
$I_{AS}=f(t_{AV})$; $R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



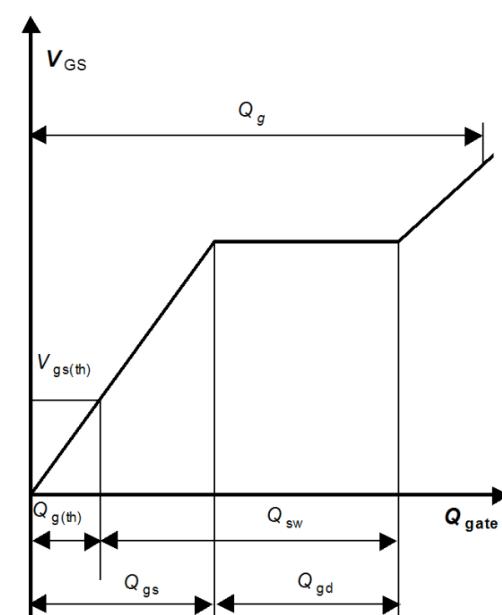
$V_{GS}=f(Q_{gate})$, $I_D=40$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



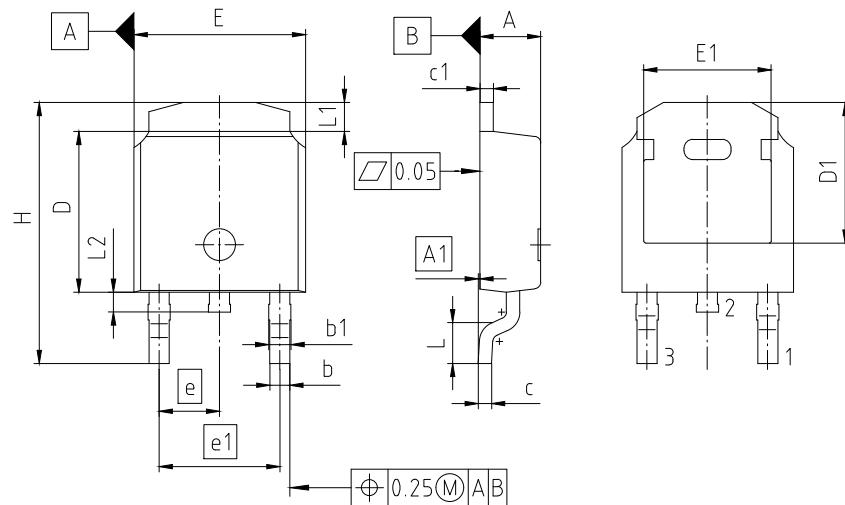
$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Gate charge waveforms



-

5 Package Outlines



PACKAGE - GROUP NUMBER: PG-T0252-3-U01		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.39
A1	0.00	0.13
b	0.64	0.89
b1	0.76	1.14
c	0.46	0.61
c1	0.40	0.89
D	5.97	6.22
D1	5.21	---
E	6.35	6.73
E1	4.32	---
e	2.29	
e1	4.58	
N	3	
H	9.40	10.41
L	1.40	1.78
L1	0.89	1.27
L2	0.50	1.02

Figure 1 Outline PG-T0252-3, dimensions in mm

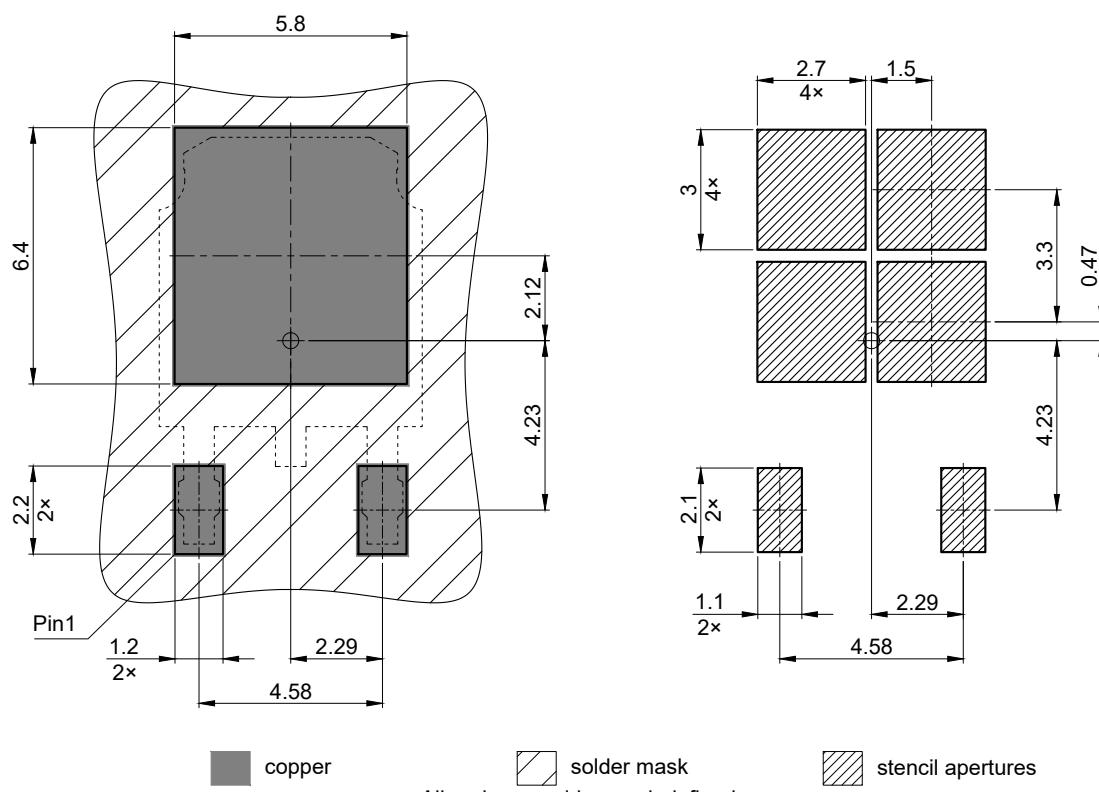


Figure 2 Footprint Drawing PG-T0252-3, dimensions in mm

Revision History

IPD047N03LF2S

Revision 2024-09-20, Rev. 1.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2024-09-20	Release of final

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