5.1 Input/Output (I/O) Interface

1) With reference to the computer system diagram (Figure 1) in the case study notes,

(a) What are the type (input, output or bi-directional) of processor pins you would connect each of the module's data signal to?

Table 1a

No.	Module	Type (Input, Output or Bidirectional)
i.	Buttons	
ii.	Wifi	
iii.	Touch Screen Controller	
iv.	System Memory	
v.	Display	

(b) Given the following interface requirement, select the appropriate module from the device information list in the case study notes to connect to the processor.

Table 1b

No.	Module	Interface Type
i.	Wifi	SPI
ii.	Touch Screen Controller	UART
iii.	System Memory	Parallel Bus

(c) For each of the interface shown in **Table 1b**, is the data transfer serial or parallel?

(d) Describe the difference between synchronous and asynchronous interface. Are the interfaces shown in **Table 1b** asynchronous or synchronous? Explain.

(e) With reference to the SPI wifi module chosen in 1(b) above, what is the maximum speed that data can be transferred between the wifi module and the processor?

(f) With reference to the device information of the system memory you have chosen in 1(b) above, what is the maximum data transfer rate achievable between the system memory and the processor? Assuming that data on the parallel bus gets transferred on each rising edge of the data strobe.

5.2 Data Transfer

2) **Fig. 2** shows the logical waveform of an asynchronous data frame.

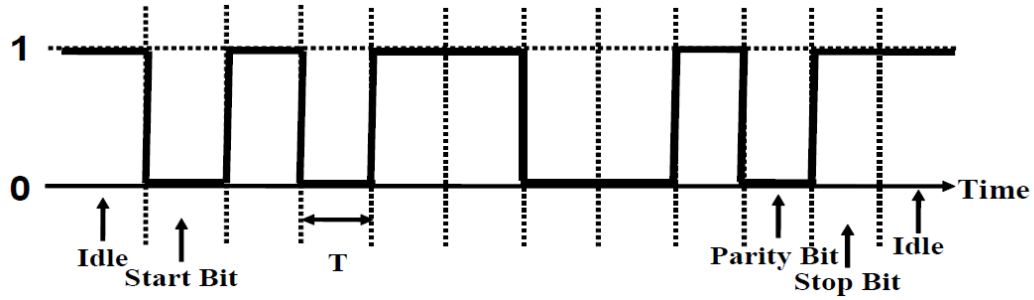

Fig. 2

Answer the following question with reference to **Fig. 2**:

(a) Specify the 7-bit ASCII character that is transmitted (LSB is transmitted first).

(b) Assume there are no errors in the transmitted waveform, state whether even or odd parity is being used.

(c) Assume two of the bits received in the character are erroneous; can the receiver detect the error? Can you extend the example to determine the limitations of parity checking?

(d) If 7-bit ASCII characters are transmitted continuously in the format shown (with no idle periods between the frames) at a baud rate of 9600, calculate the following:
   i. The value of **T** in **Fig 2**.
   ii. The data transfer rate of this serial interface in characters per second (cps).

(e) Re-compute the data transfer rate (cps) if the transmission does not use any parity bit. Compare the results with those obtained in Q3d(ii), and state your observation(s).

(f) Assume the baud rate of the transmitter is 4800, but the baud rate of the receiver is configured as 9600. Based on **Fig. 2**, determine, if any, the ASCII character(s) that will be received.

(g) Redraw the waveform in **Fig. 2** if the MAX233 line driver is used to produce a RS-232 compatible signal. You can assume the MAX233 produces signals of ±15 volts.

(Not necessary to be covered during tutorial)

3) There has been a trend of 'serialization' of interface bus standard. E.g. USB replacing Parallel Port Interface, SATA replacing IDE in HDD.
   (a) What are the advantages that Serial Bus has over Parallel Bus interface that enticed industry player to move in this direction?
   (b) What are the scenarios in which Parallel bus will still be preferred over Serial bus? What are the design considerations that need to be put in place in such cases?

4) In Q3(f) above, a wrong sampling result is observed when a wrong baud rate is used. This can actually be used to implement auto baud rate detection. Briefly describe how this can be done.