Report

Regarding the code:

We created each of the three entities in 3 sperate .vhdl files and the final top-level entity in a sperate .vhdl file as well.

The purpose of the clk_generator was to divide the frequency inputted at 50MHz to 1Hz, therefore we created a counter that counts till half of that (25MHz) and then we flip the output clock value, if it's 0 it becomes 1 and vice versa.

The purpose of the sixty_counter is to count from 0 to 59 but on two led screens, so we counted in two separate digits (a left and a right). We started each digit at 0 then we would add 1 to the right digit every rising clock edge until it reaches 9, then we'd add 1 to the left digit and return the right to 0 and so on till we reach 59. Now since the output is to be expressed in std_logic_vector, we converted the signals in which we counted for each screen from integers to std_logic_vector of 4 bits as the maximum value (9) needs 4 bits to be represented.

We implemented the pause and reset values in the sixty_counter entity, therefore before we get to counting (no matter whether the clock is at '1' or '0'), we check the values of the reset and pause button/switch. If the pause is at '1' then we pause the counting by not incrementing either digits, and if the reset is at '0' (as we assigned it to a button where if not pushed then the value is '1') then we return both screens to 0.

The purpose of the seven_seg_decoder is to take a binary number and represent it on the led screen (in 7 bits). Now since the led screens on the FPGA are active low, we put the in the places where we wanted the screen to light up '0' and '1' everywhere else.

The purpose of the final top-level entity is to connect all the 3 entities together. We first have to convert the input 50MHz clock to 1Hz using the clk_generator and use the output 1Hz as the input to the sixty_counter. Then we decode each of the output binary numbers from the sixty_counter onto each of the left and right screens using the sven_seg_decoder.

Regarding the pin assignment:

Node Name	Direction	Location	I/O Bank	VREF Group	itter Locatior	I/O Standard	Reserved	urrent Streng	Slew Rate	ifferential Pai	ict Preservati
clk_in	Input	PIN_P11	3	B3_N0	PIN_P11	2.5 V		12mA ...ault)			
left_out[6]	Output	PIN_B17	7	B7_N0	PIN_B17	2.5 V		12mA ...ault)	2 (default)		
left_out[5]	Output	PIN_A18	7	B7_N0	PIN_A18	2.5 V		12mA ...ault)	2 (default)		
left_out[4]	Output	PIN_A17	7	B7_N0	PIN_A17	2.5 V		12mA ...ault)	2 (default)		
left_out[3]	Output	PIN_B16	7	B7_N0	PIN_B16	2.5 V		12mA ...ault)	2 (default)		
left_out[2]	Output	PIN_E18	6	B6_N0	PIN_E18	2.5 V		12mA ...ault)	2 (default)		
left_out[1]	Output	PIN_D18	6	B6_N0	PIN_D18	2.5 V		12mA ...ault)	2 (default)		
left_out[0]	Output	PIN_C18	7	B7_N0	PIN_C18	2.5 V		12mA ...ault)	2 (default)		
pause	Input	PIN_C10	7	B7_N0	PIN_C10	2.5 V		12mA ...ault)			
reset	Input	PIN_A7	7	B7_N0	PIN_A7	2.5 V		12mA ...ault)			
right_out[6]	Output	PIN_C17	7	B7_N0	PIN_C17	2.5 V		12mA ...ault)	2 (default)		
right_out[5]	Output	PIN_D17	7	B7_N0	PIN_D17	2.5 V		12mA ...ault)	2 (default)		
right_out[4]	Output	PIN_E16	7	B7_N0	PIN_E16	2.5 V		12mA ...ault)	2 (default)		
right_out[3]	Output	PIN_C16	7	B7_N0	PIN_C16	2.5 V		12mA ...ault)	2 (default)		
right_out[2]	Output	PIN_C15	7	B7_N0	PIN_C15	2.5 V		12mA ...ault)	2 (default)		
right_out[1]	Output	PIN_E15	7	B7_N0	PIN_E15	2.5 V		12mA ...ault)	2 (default)		
right_out[0]	Output	PIN_C14	7	B7_N0	PIN_C14	2.5 V		12mA ...ault)	2 (default)		
<<new node>>											

We connected:

- the clk_in to the 50 MHz clock input(Bank 3B) (MAX10_CLK1_50) at PIN_P11
- the left_screen_output or left_out[n] to the Seven Segment Digit 1[n] (HEX1n) for each bit n at its corresponding PIN
- the right_screen_ouput or right_out[n] to the Seven Segment Digit 0[n] (HEX0n) for each bit n at its corresponding PIN
- the pause to Slide Switch[0] (SW0) at PIN_C10
- the reset to Push-button[1] (KEY1) at PIN_A7