

# High Level Synthesis

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September 1, 2025



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# Chapter 1

## Introduction

This report will talk about high level synthesis (HLS) desing using FPGA.

Unlike traditional hardware descirption language (VHDL, Verilog), HLS uses high level languages such as C and C++ to design product using FPGA. The advanatage is the speed of learning compared to traditional language.

introduction

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Introduction:

- *To adapt more the introduction*
- *Insert references and books*