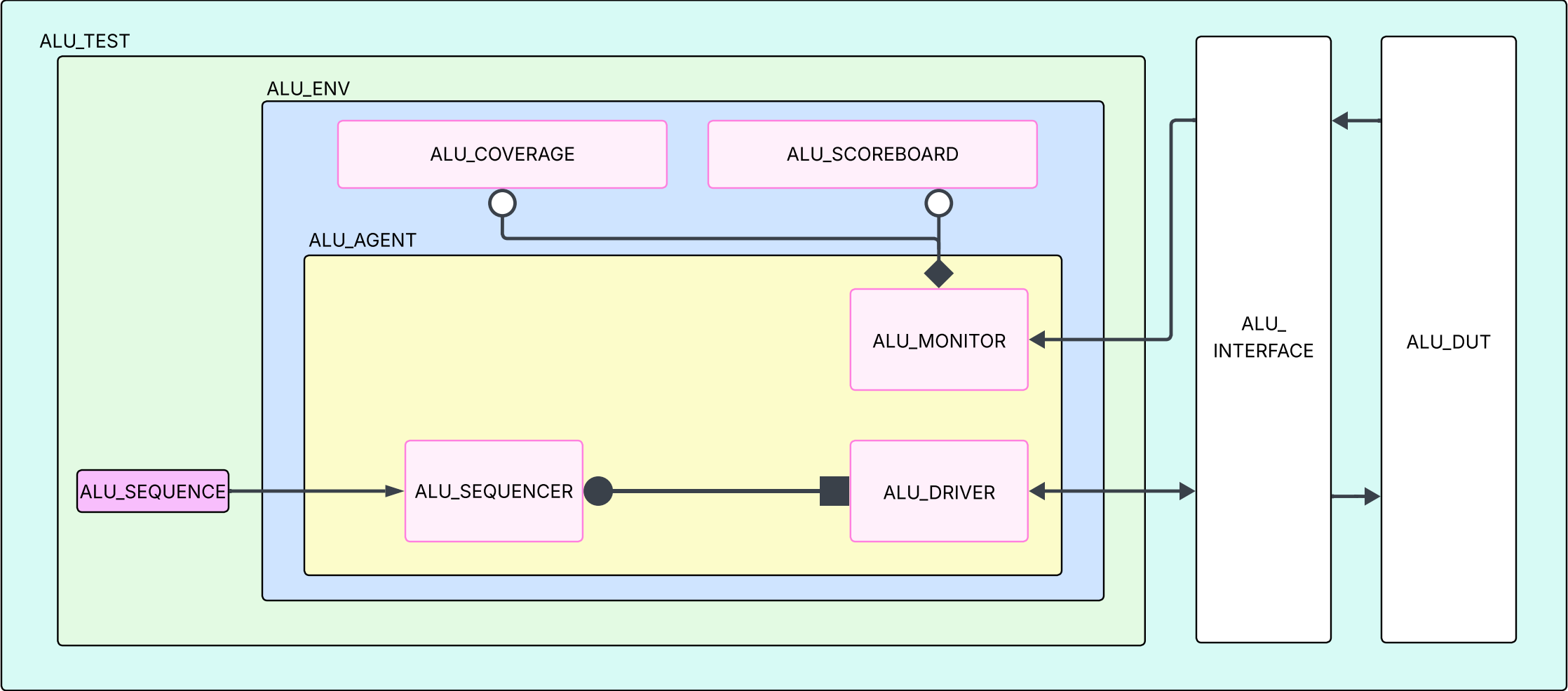


ALU\_TOP



SEQ\_ITEM\_PORT



SEQ\_ITEM\_EXPORT



UVM\_ANALYSIS\_PORT



UVM\_ANALYSIS\_EXPORT